■Bus Cycle Time

- 83.3ns (When CF=12MHz)

  Note: The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time (tCYC)

- 250ns (When CF=12MHz)

■Ports

• I/O ports	
Ports whose I/O direction can be designated in 1-bit units	28 (P10 to P17, P20 to P27, P30 to P34, P70 to P73, PWM0, PWM1, XT2)
Ports whose I/O direction can be designated in 4-bit units	8 (P00 to P07)
• USB ports	2 (UHD+, UHD-)
• Dedicated oscillator ports	2 (CF1, CF2)
• Input-only port (also used for oscillation)	1 (XT1)
• Reset pins	1 ($\overline{\text{RES}}$)
• Power supply pins	6 ($V_{SS}1$ to 3, $V_{DD}1$ to 3)

■Timers

- Timer 0: 16-bit timer/counter with 2 capture registers.
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
  - Mode 3: 16-bit counter (with two 16-bit capture registers)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  - Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from lower-order 8 bits)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (lower-order 8 bits may be used as a PWM output)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes

■SIO

- SIO0: Synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Transfer clock cycle: 4/3 to 512/3 tCYC
  3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1-bit units) (Suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)
- SIO4: Synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Transfer clock cycle: 4/3 to 1020/3 tCYC
  3) Automatic continuous data transmission (1 to 4096 bytes, specifiable in 1 byte units) (Suspension and resumption of data transmission possible in 1 byte units or in word units)
  4) Auto-start-on-falling-edge function
  5) Clock polarity selectable
  6) CRC16 calculator circuit built in

- SIO9: Synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Transfer clock cycle: 4/3 to 1020/3 tCYC
  3) Automatic continuous data transmission (1 to 4096 bytes, specifiable in 1 byte units)
     (Suspension and resumption of data transmission possible in 1 byte units or word units)
  4) Auto-start-on-falling-edge function
  5) Clock polarity selectable
  6) CRC16 calculator circuit built in

■Full Duplex UART
1) Data length: 7/8/9 bits selectable
2) Stop bits: 1 bit (2 bits in continuous transmission mode)
3) Baud rate: 16/3 to 8192/3 tCYC

■AD Converter: 8 bits × 12 channels

■PWM: Multifrequency 12-bit PWM × 2 channels

■Infrared Remote Control Receiver Circuit
1) Noise rejection function (noise filter time constant: Approx. 120µs when the 32.768kHz crystal oscillator is selected as the base clock)
2) Supports data encoding systems such as PPM (Pulse Position Modulation) and Manchester encoding.
3) X'tal HOLD mode reset function

■USB Interface (host control function)
1) Compliant with full-speed (12M bps) specifications
2) Supports 4 transfer types (control transfer, bulk transfer, interrupt transfer, and isochronous transfer).

■Audio Interface

1) Sampling frequency (fs):	32kHz, 44.1kHz, 48kHz
2) Master clock frequency (internal PLL):	12.288MHz, 16.9344MHz, 18.432MHz
3) Bit clock selectable:	48fs/64fs
4) Data bit length:	16/18/20/24 bits

5) LSB first/MSB firsts selectable
6) Left-justification/right-justification selectable

■Watchdog Timer
- Watchdog timer using external RC circuitry
- Interrupt and reset signals selectable

■Clock Output Function
1) Can output a clock with a clock rate of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 of the source oscillator clock selected as the system clock.
2) Can output the source oscillation clock for the subclock.

■Interrupts

- 40 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/UHC bus active/remote control signal receive
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H/INT6/UHC device connected/UHC disconnected/UHC resume
6	0002BH	H or L	T1L/T1H/INT7/SIO9/AIF start
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/SIO4/UART1 transmit/end of AIF
9	00043H	H or L	ADC/T6/T7/UHC-ACK/UHC-NAK/UHC error/UHC STALL
10	0004BH	H or L	Port 0/PWM0/PWM1/T4/T5/UHC-SOF/DMCOPY

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 8192 levels maximum (The stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation and PLL Circuits

• RC oscillation circuit (internal):	For system clock
• CF oscillation circuit:	For system clock
• Crystal oscillation circuit:	For system clock, time-of-day clock
• PLL circuit (internal):	For USB interface (see Fig.5)), audio interface (see Fig. 6)

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Canceled by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The PLL base clock generator, CF, RC and crystal oscillators automatically stop operation.
  2) There are four ways of resetting the HOLD mode.
     (1) Setting the reset pin to the lower level.
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an bus active interrupt source established in the USB host controll circuit
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The PLL base clock generator, CF and RC oscillator automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are six ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0
     (4) Having an interrupt source established in the base timer circuit
     (5) Having an bus active interrupt source established in the USB host controll circuit
     (6) Having an interrupt source established in the infrared remote controller receiver circuit

■Development Tools

- On-chip debugger: TCB87- type-B + LC87F1HC8A

■Flash ROM Programming Boards

Package	Programming boards
SQFP48(7×7)	W87F55256SQ

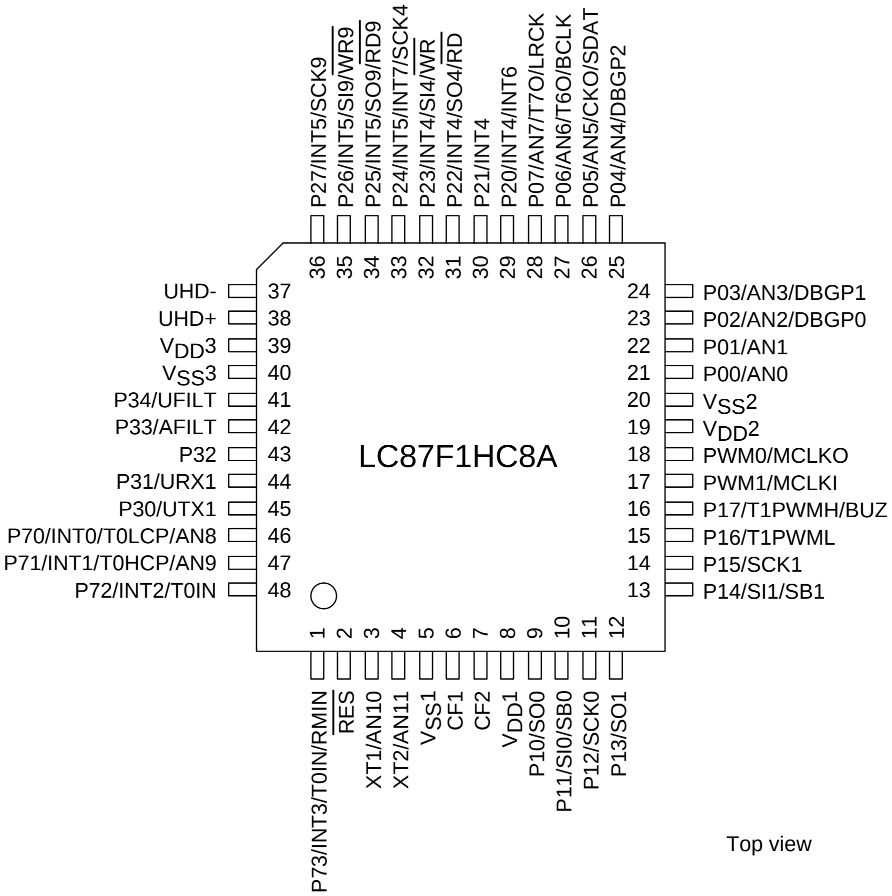
■Recommended EPROM Programmer

Maker		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single Programmer	AF9708/ AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models)	Rev 02.82 or later	LC87F1HC8A
Flash Support Group, Inc. (FSG) + Our company(Note 1)	Onboard Single/Gang Programmer	AF9101/AF9103(Main body) (FSG models)	(Note 2)	LC87F1HC8A
		SIB87(Inter Face Driver) (Our company model)		
Our company	Single/Gang Programmer	SKK/SKK TypeB (SANYO FWS)	Application Version 2.04 or later Chip Data Version 2.11 or later	LC87F1HC8
	Onboard Single/Gang Programmer	SKK-DBG TypeB (SANYO FWS)		

Note 1: With the FSG onboard programmer (AF9101/AF9103) and the serial interface driver (SIB87) provided by Our company, PC-less standalone onboard programming is possible

Note 2: Depending on programming conditions, it is necessary to use a dedicated programming device and a program. Please contact Our company or FSG if you have any questions or difficulties regarding this matter.

Pin Assignment

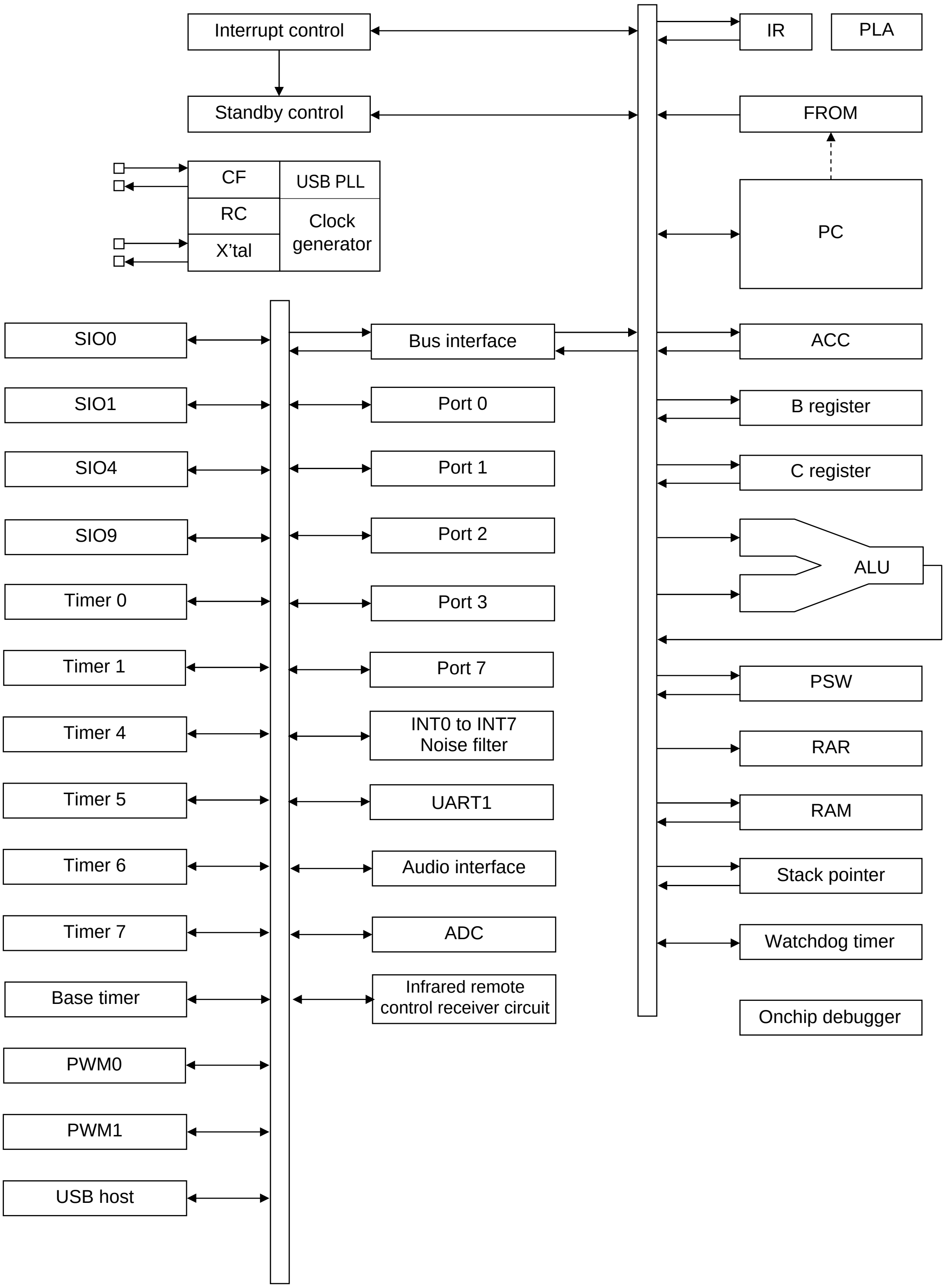


SQFP48(7×7) “Lead-/Halogen-free Type”

SQFP48	NAME
1	P73/INT3/T0IN/RMIN
2	$\overline{\text{RES}}$
3	XT1/AN10
4	XT2/AN11
5	$V_{SS}1$
6	CF1
7	CF2
8	$V_{DD}1$
9	P10/SO0
10	P11/SI0/SB0
11	P12/SCK0
12	P13/SO1
13	P14/SI1/SB1
14	P15/SCK1
15	P16/T1PWML
16	P17/T1PWMH/BUZ
17	PWM1/MCLKI
18	PWM0/MCLKO
19	$V_{DD}2$
20	$V_{SS}2$
21	P00/AN0
22	P01/AN1
23	P02/AN2/DBGP0
24	P03/AN3/DBGP1

SQFP48	NAME
25	P04/AN4/DBGP2
26	P05/AN5/CKO/SDAT
27	P06/AN6/T6O/BCLK
28	P07/AN7/T7O/LRCK
29	P20/INT4/INT6
30	P21/INT4
31	P22/INT4/SO4/$\overline{\text{RD}}$
32	P23/INT4/SI4/$\overline{\text{WR}}$
33	P24/INT5/INT7/SCK4
34	P25/INT5/SO9/$\overline{\text{RD9}}$
35	P26/INT5/SI9/$\overline{\text{WR9}}$
36	P27/INT5/SCK9
37	UHD-
38	UHD+
39	$V_{DD}3$
40	$V_{SS}3$
41	P34/UFILT
42	P33/AFILT
43	P32
44	P31/URX1
45	P30/UTX1
46	P70/INT0/T0LCP/AN8
47	P71/INT1/T0HCP/AN9
48	P72/INT2/T0IN

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$,$V_{SS}2$,
$V_{SS}3$</td><td>-</td><td>- power supply</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$</td><td>-</td><td>+ power supply</td><td>No</td></tr>
<tr><td>$V_{DD}3$</td><td>-</td><td>USB reference voltage</td><td>Yes</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O ports
• I/O specifiable in 4-bit units
• Pull-up resistors can be turned on and off in 4-bit units.
• HOLD reset input
• Port 0 interrupt input
• Pin functions
AD converter input ports: AN0 to AN7(P00 to P07)
Onchip debugger pins: DBGP0 to DBGP2(P02 to P04)
P05: System clock output/audio interface SDAT input/output
P06: Timer 6 toggle output/audio interface BCLK input/output
P07: Timer 7 toggle output/audio interface LRCK input/output</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O ports
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P10: SIO0 data output
P11: SIO0 data input/bus input/output
P12: SIO0 clock input/output
P13: SIO1 data output
P14: SIO1 data input/bus input/output
P15: SIO1 clock input/output
P16: Timer 1 PWML output
P17: Timer 1 PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P27</td><td>I/O</td><td>• 8-bit I/O ports
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P20 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input
P24 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input
P20: INT6 input/timer 0L capture 1 input
P22: SIO4 data input/output/parallel interface $\overline{RD}$ output
P23: SIO4 data input/output/parallel interface $\overline{WR}$ output
P24: SIO4 clock input/output/INT7 input/timer 0H capture 1 input
P25: SIO9 data input/output/parallel interface $\overline{RD9}$ output
P26: SIO9 data input/output/parallel interface $\overline{WR9}$ output
P27: SIO9 clock input/output
Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P34</td><td>I/O</td><td>• 5-bit I/O ports
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P30: UART1 transmit
P31: UART1 receive
P33: Audio interface PLL filter pin (see Fig. 6.)
P34: USB interface PLL filter pin (see Fig. 5.)</td><td>Yes</td></tr>
</table>

Continued on next page.

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output
P71: INT1 input/HOLD reset input/timer 0H capture input
P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/ high speed clock counter input
P73: INT3 input (input with noise filter)/timer 0 event input/timer 0H capture input/ IR remote controller receiver input
AD converter input ports: AN8(P70), AN9(P71)
Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>PWM0
PWM1</td><td>I/O</td><td>PWM0, PWM1 output port
General-purpose input port
• Pin functions
PWM0: Audio interface master clock output
PWM1: Audio interface master clock input</td><td>No</td></tr>
<tr><td>UHD-</td><td>I/O</td><td>USB data I/O pin UHD-/general-purpose I/O port</td><td>No</td></tr>
<tr><td>UHD+</td><td>I/O</td><td>USB data I/O pin UHD+/general-purpose I/O port</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>Input</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>Input</td><td>• 32.768kHz crystal oscillator input
• Pin functions
General-purpose input port
AD converter input ports: AN10
Must be connected to $V_{DD}1$ when not to be used.</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• 32.768kHz crystal oscillator output
• Pin functions
General-purpose I/O
AD converter input port: AN11
Must be set for oscillation and kept open if not to be used.</td><td>No</td></tr>
<tr><td>CF1</td><td>Input</td><td>Ceramic/crystal resonator input</td><td>No</td></tr>
<tr><td>CF2</td><td>Output</td><td>Ceramic/crystal resonator output</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

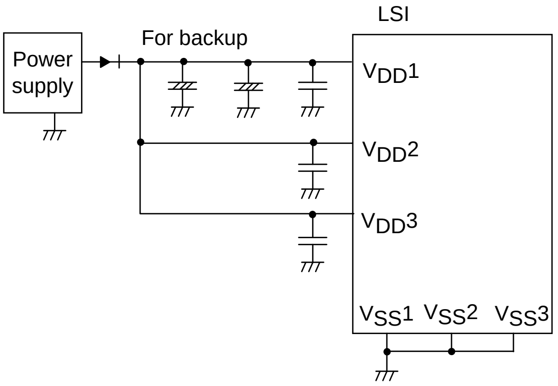
Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17 P20 to P27 P30 to P34	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
PWM0, PWM1	-	No	CMOS	No
UHD+, UHD-	-	No	CMOS	No
XT1	-	No	Input only	No
XT2	-	No	32.768kHz crystal resonator output (N channel open drain when in general-purpose output mode)	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4 bit units (P00 to 03, P04 to 07).

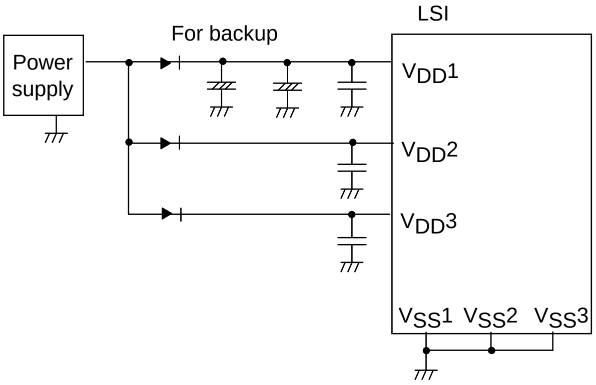
Power Pin Treatment

Connect the IC as shown below to minimize the noise input to the $V_{DD}1$ pin. and extend the backup period. Be sure to electrically short the $V_{SS}1$, $V_{SS}2$, and $V_{SS}3$ pins.

Example 1: When the microcontroller is in the backup state in the HOLD mode, the power to sustain the high level of output ports is supplied by their backup capacitors.



Example 2: The high level output at ports is not sustained and unstable in the HOLD backup mode.



USB Reference Power Option

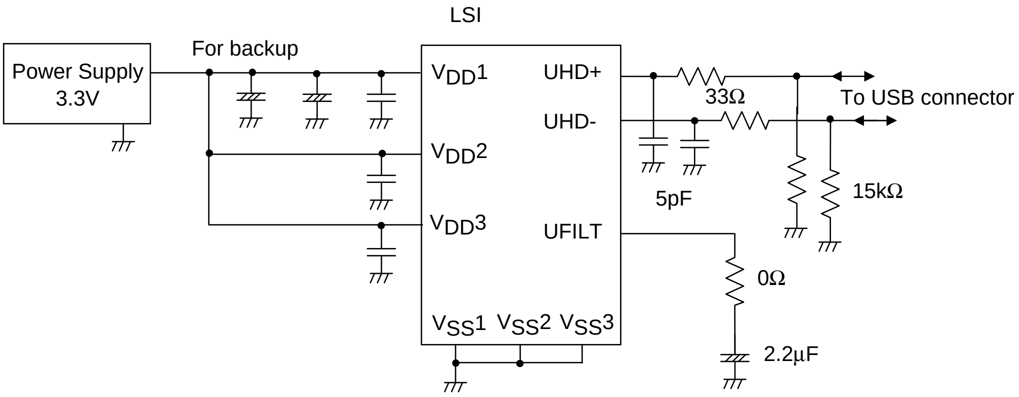
When a voltage 4.5 to 5.5V is supplied to $V_{DD}1$ and the internal USB reference voltage circuit is activated, the reference voltage for USB port output is generated. The active/inactive state of the reference voltage circuit can be switched by option select. The procedure for marking the option selection is described below.

		(1)	(2)	(3)	(4)
Option settings	USB regulator	USE	USE	USE	NONUSE
	USB regulator at HOLD mode	USE	NONUSE	NONUSE	NONUSE
	USB regulator at HALT mode	USE	NONUSE	USE	NONUSE
Reference voltage circuit state	Normal mode	active	active	active	inactive
	HOLD mode	active	inactive	inactive	inactive
	HALT mode	active	inactive	active	inactive

- When the USB reference voltage circuit is made inactive, the level of the reference voltage for USB port output is equal to $V_{DD}1$.
- Selection (2) or (3) can be used to set the reference voltage circuit inactive in HOLD or HALT mode.
- When the reference voltage circuit is activated, the current drain increases by approximately 100µA compared with when the reference voltage circuit is inactive.

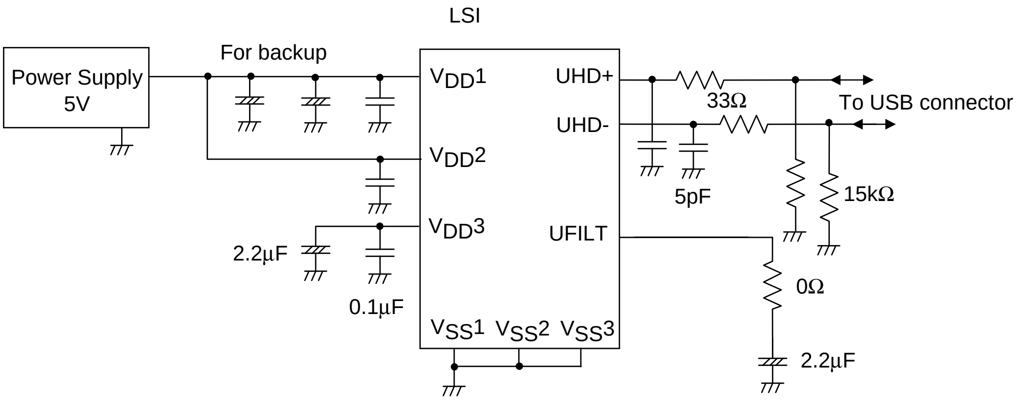
Example 1: $V_{DD}1=V_{DD}2=3.3V$

- Inactivating the reference voltage circuit (selection (4)).
- Connecting $V_{DD}3$ to $V_{DD}1$ and $V_{DD}2$.



Example 2: $V_{DD}1=V_{DD}2=5.0V$

- Activating the reference voltage circuit (selection (1)).
- Isolating $V_{DD}3$ from $V_{DD}1$ and $V_{DD}2$, and connecting capacitor between $V_{DD}3$ and V_{SS}.



Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1 = V_{DD}2 = V_{DD}3$		-0.3		+6.5	V
Input voltage		$V_I(1)$	XT1, CF1			-0.3		$V_{DD}+0.3$	
Input/output voltage		$V_{IO}(1)$	Ports 0, 1, 2, 3, 7 PWM0, PWM1 XT2			-0.3		$V_{DD}+0.3$	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2	• When CMOS output type is selected • Per 1 applicable pin		-10			mA
		IOPH(2)	PWM0, PWM1	Per 1 applicable pin		-20			
		IOPH(3)	Port 3 P71 to P73	• When CMOS output type is selected • Per 1 applicable pin		-5			
	Average output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2	• When CMOS output type is selected • Per 1 applicable pin		-7.5			
		IOMH(2)	PWM0, PWM1	Per 1 applicable pin		-15			
		IOMH(3)	Port 3 P71 to P73	• When CMOS output type is selected • Per 1 applicable pin		-3			
	Total output current	ΣIOAH(1)	Ports 0, 2	Total current of all applicable pins		-25			
		ΣIOAH(2)	Port 1 PWM0, PWM1	Total current of all applicable pins		-25			
		ΣIOAH(3)	Ports 0, 1, 2 PWM0, PWM1	Total current of all applicable pins		-45			
		ΣIOAH(4)	Port 3 P71 to P73	Total current of all applicable pins		-10			
		ΣIOAH(5)	UHD+, UHD-	Total current of all applicable pins		-25			
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2 PWM0, PWM1	Per 1 applicable pin				20	
		IOPL(2)	P00, P01	Per 1 applicable pin				30	
		IOPL(3)	Ports 3, 7 XT2	Per 1 applicable pin				10	
	Average output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2 PWM0, PWM1	Per 1 applicable pin				15	
		IOML(2)	P00, P01	Per 1 applicable pin				20	
		IOML(3)	Ports 3, 7 XT2	Per 1 applicable pin				7.5	
	Total output current	ΣIOAL(1)	Ports 0, 2	Total current of all applicable pins				45	
		ΣIOAL(2)	Port 1 PWM0, PWM1	Total current of all applicable pins				45	
		ΣIOAL(3)	Ports 0, 1, 2 PWM0, PWM1	Total current of all applicable pins				80	
		ΣIOAL(4)	Ports 3, 7 XT2	Total current of all applicable pins				15	
		ΣIOAL(5)	UHD+, UHD-	Total current of all applicable pins				25	
Allowable power Dissipation		Pd max	SQFP48(7×7)	Ta=-40 to +85°C				140	mW
Operating ambient Temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: The average output current is an average of current values measured over 100ms intervals.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	V_{DD}(1)	$V_{DD}1=V_{DD}2=V_{DD}3$	0.245µs ≤ tCYC ≤ 200µs		3.0		5.5	V
			0.490µs ≤ tCYC ≤ 200µs Except in onboard programming mode		2.7		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1=V_{DD}2=V_{DD}3$	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	V_{IH}(1)	Port 0, 1, 2, 3 P71 to P73 P70 port input/ interrupt side PWM0, PWM1		2.7 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	V_{IH}(2)	Port 70 watchdog timer side		2.7 to 5.5	$0.9V_{DD}$		V_{DD}	
	V_{IH}(3)	XT1, XT2, CF1, $\overline{RES}$		2.7 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	V_{IL}(1)	Port 1, 2, 3 P71 to P73 P70 port input/ interrupt side		4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
	V_{IL}(2)			2.7 to 4.0	V_{SS}		$0.2V_{DD}$	
	V_{IL}(3)	Port 0 PWM0, PWM1		4.0 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
	V_{IL}(4)			2.7 to 4.0	V_{SS}		$0.2V_{DD}$	
	V_{IL}(5)	Port 70 watchdog timer side		2.7 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	V_{IL}(6)	XT1, XT2, CF1, $\overline{RES}$		2.7 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	tCYC			3.0 to 5.5	0.245		200	µs
			Except for onboard programming mode	2.7 to 5.5	0.490		200	
External system clock frequency	FEXCF(1)	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty =50±5%	3.0 to 5.5	0.1		12	MHz
			• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty =50±5%	2.7 to 5.5	0.1		6	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	When 12MHz ceramic oscillation See Fig. 1.	3.0 to 5.5		12		MHz
	FmCF(2)	CF1, CF2	When 6MHz ceramic oscillation See Fig. 1.	2.7 to 5.5		6		
	FmRC		Internal RC oscillation	2.7 to 5.5	0.3	1.0	2.0	
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	2.7 to 5.5		32.768		kHz

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	I_{IH}(1)	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$ PWM0, PWM1 UHD+, UHD-	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	2.7 to 5.5			1	µA
	I_{IH}(2)	XT1, XT2	Input port configuration $V_{IN}=V_{DD}$	2.7 to 5.5			1	
	I_{IH}(3)	CF1	$V_{IN}=V_{DD}$	2.7 to 5.5			15	
Low level input current	I_{IL}(1)	Ports 0, 1, 2, 3 Port 7 $\overline{RES}$ PWM0, PWM1 UHD+, UHD-	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	2.7 to 5.5	-1			
	I_{IL}(2)	XT1, XT2	Input port configuration $V_{IN}=V_{SS}$	2.7 to 5.5	-1			
	I_{IL}(3)	CF1	$V_{IN}=V_{SS}$	2.7 to 5.5	-15			
High level output voltage	V_{OH}(1)	Ports 0, 1, 2, 3 P71 to P73	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	V_{OH}(2)		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(3)		I_{OH}=-0.2mA	2.7 to 5.5	V_{DD}-0.4			
	V_{OH}(4)	PWM0, WM1 P05 to P07 (Note 3-1)	I_{OH}=-10mA	4.5 to 5.5	V_{DD}-1.5			
	V_{OH}(5)		I_{OH}=-1.6mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(6)		I_{OH}=-1mA	2.7 to 5.5	V_{DD}-0.4			
Low level output voltage	V_{OL}(1)	P00, P01	I_{OL}=30mA	4.5 to 5.5			1.5	
	V_{OL}(2)		I_{OL}=5mA	3.0 to 5.5			0.4	
	V_{OL}(3)		I_{OL}=2.5mA	2.7 to 5.5			0.4	
	V_{OL}(4)	Ports 0, 1, 2 PWM0, PWM1 XT2	I_{OL}=10mA	4.5 to 5.5			1.5	
	V_{OL}(5)		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	V_{OL}(6)		I_{OL}=1mA	2.7 to 5.5			0.4	
	V_{OL}(7)	Ports 3, 7	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	V_{OL}(8)		I_{OL}=1mA	2.7 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3 Port 7	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.7 to 5.5	18	50	150	
Hysteresis voltage	VHYS	$\overline{RES}$ Port 1, 2, 3, 7		2.7 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	2.7 to 5.5		10		pF

Note 3-1: When the CKO system clock output function (P05) or audio interface output function (P05 to P07) is used.

Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/ Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 8.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1a)		• Continuous data transfer mode • USB, AIF, SIO4, SIO9, and DMCOPY not used at the same time. • See Fig. 8. • (Note 4-1-2)		4			
			tSCKHA(1b)		• Continuous data transfer mode • USB used at the same time. • AIF, SIO4, SIO9, and DMCOPY not used at the same time. • See Fig. 8. • (Note 4-1-2)		7			
			tSCKHA(1c)		• Continuous data transfer mode • USB, AIF, SIO4, SIO9, and DMCOPY used at the same time. • See Fig. 8. • (Note 4-1-2)		9			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• When CMOS output type is selected • See Fig. 8.	2.7 to 5.5	4/3			
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2a)		• Continuous data transfer mode • USB, AIF, SIO4, SIO9, and DMCOPY not used at the same time. • When CMOS output type is selected • See Fig. 8.		tSCKH(2) +2tCYC		tSCKH(2) + (10/3)tCYC	tCYC
			tSCKHA(2b)		• Continuous data transfer mode • USB used at the same time. • AIF, SIO4, SIO9, and DMCOPY not used at the same time. • When CMOS output type is selected. • See Fig. 8.		tSCKH(2) +2tCYC		tSCKH(2) + (19/3)tCYC	
			tSCKHA(2c)		• Continuous data transfer mode • USB, AIF, SIO4, SIO9, and DMCOPY used at the same time • When CMOS output type is selected • See Fig. 8.		tSCKH(2) +2tCYC		tSCKH(2) + (25/3)tCYC	

Note 4-1-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-1-2: In an application where the serial clock input is to be used in the continuous data transfer mode, the time from SI0RUN being set when serial clock is high to the falling edge of the first serial clock must be longer than tSCKHA.

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Parameter			Symbol	Pin/ Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial input		Data setup time	tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 8.	2.7 to 5.5	0.03			µs
		Data hold time	thDI(1)				0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transfer mode • (Note 4-1-3)	2.7 to 5.5			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)				1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)				(1/3)tCYC +0.05	

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK.
Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 8.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/ Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 8.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• When CMOS output type is selected • See Fig. 8.	2.7 to 5.5	2			
		Low level pulse width	tSCKL(4)				1/2			tSCK
		High level pulse width	tSCKH(4)				1/2			
Serial input		Data setup time	tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 8.	2.7 to 5.5	0.03			µs
		Data hold time	thDI(2)				0.03			
Serial output		Output delay time	tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 8.	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

3. SIO4 Serial I/O Characteristics (Note 4-3-1)

Parameter			Symbol	Pin/ Remarks	Conditions		Specification			
						VDD[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(5)	SCK4(P24)	See Fig. 8.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(5)				1			
		High level pulse width	tSCKH(5)				1			
			tSCKHA(5a)		• USB, SIO0 continuous transfer mode, AIF, SIO9, and DMCOPY not used at the same time. • See Fig. 8. • (Note 4-3-2)		4			
			tSCKHA(5b)		• USB used at the same time • SIO0 continuous transfer mode, AIF, SIO9, DMCOPY not used at the same time. • See Fig. 8. • (Note 4-3-2)		7			
			tSCKHA(5c)		• USB, SIO0 continuous transfer mode, SIO9, and DMCOPY used at the same time. • AIF not used at the same time. • See Fig. 8. • (Note 4-3-2)		12			
	Output clock	Frequency	tSCK(6)	SCK4(P24)	• When CMOS output type is selected. • See Fig. 8.	2.7 to 5.5	4/3			
		Low level pulse width	tSCKL(6)				1/2			tSCK
		High level pulse width (Note 4-3-3)	tSCKH(6)				1/2			
			tSCKHA(6a)		• USB, SIO0 continuous transfer mode, AIF, SIO9, and DMCOPY not used at the same time. • When CMOS output type is selected. • See Fig. 8.		tSCKH(6) + (5/3)tCYC		tSCKH(6) + (10/3)tCYC	tCYC
			tSCKHA(6b)		• USB used at the same time. • SIO0 continuous transfer mode, AIF, SIO9, and DMCOPY not used at the same time. • When CMOS output type is selected. • See Fig. 8.		tSCKH(6) + (5/3)tCYC		tSCKH(6) + (19/3)tCYC	
			tSCKHA(6c)		• USB, SIO0 continuous transfer mode, SIO9, and DMCOPY used at the same time. • AIF not used at the same time. • When CMOS output type is selected. • See Fig. 8.		tSCKH(6) + (5/3)tCYC		tSCKH(6) + (34/3)tCYC	

Note 4-3-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-3-2: In an application where the serial clock input is to be used in the continuous data transfer mode, the period from the time SI4RUN is set with the serial clock set high to the falling edge of the first serial clock must be longer than tSCKHA.

Note 4-3-3: When using the serial clock output, make sure that the load at the SCK4 (P24) pin meets the following conditions:
Clock rise time tSCKR < 0.037μs (see Figure 12.) at Ta=+25°C, V_{DD}=3.3V

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Parameter		Symbol	Pin/ Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Serial input	Data setup time	tsDI(3)	SO4(P22), SI4(P23)	• Must be specified with respect to falling edge of SIOCLK. • See Fig. 8	2.7 to 5.5	0.03			µs
	Data hold time	thDI(3)				0.03			
Serial output	Output delay time	tdD0(5)	SO4(P22), SI4(P23)	• Must be specified with respect to rising edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 8.	2.7 to 5.5			(1/3)tCYC +0.05	

4. SIO9 Serial I/O Characteristics (Note 4-4-1)

Parameter			Symbol	Pin/ Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(7)	SCK9(P27)	See Fig. 8.	2.7 to 5.5	2			tCYC
		Low level pulse width	tSCKL(7)				1			
		High level pulse width	tSCKH(7)				1			
			tSCKHA(7a)		• USB, SIO0 continuous transfer mode, AIF, SIO4 and DMCOPY not used at the same time. • See Fig. 8. • (Note 4-4-2)		4			
			tSCKHA(7b)		• USB used at the same time. • SIO0 continuous transfer mode, AIF, SIO4, and DMCOPY not used at the same time. • See Fig. 8. • (Note 4-4-2)		7			
			tSCKHA(7c)		• USB, SIO0 continuous transfer mode, SIO4 and DMCOPY used at the same time. • AIF not used at the same time. • See Fig. 8. • (Note 4-4-2)		15			

Note 4-4-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-4-2: In an application where the serial clock input is to be used in the continuous data transfer mode, the period from the time SI9RUN is set with the serial clock set high to the falling edge of the first serial clock must be longer than tSCKHA.

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Parameter			Symbol	Pin/ Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Output clock	Frequency	tSCK(8)	SCK9(P27)	• When CMOS output type is selected. • See Fig. 8.	2.7 to 5.5	4/3			tCYC
		Low level pulse width	tSCKL(8)				1/2			tSCK
		High level pulse width (Note 4-4-3)	tSCKH(8)				1/2			
			tSCKHA(8a)		• USB, SIO0 continuous transfer mode, AIF SIO4 DMCOPY not used at the same time. • When CMOS output type is selected. • See Fig. 8.		tSCKH(8) + (5/3)tCYC		tSCKH(8) + (10/3)tCYC	tCYC
			tSCKHA(8b)		• USB used at the same time. • SIO0 continuous transfer mode, AIF, SIO4, and DMCOPY not used at the same time. • When CMOS output type is selected • See Fig. 8.		tSCKH(8) + (5/3)tCYC		tSCKH(8) + (19/3)tCYC	
			tSCKHA(8c)		• USB, SIO0 continuous transfer mode , SIO4, and DMCOPY used at the same time. • AIF not used at the same time. • When CMOS output type is selected. • See Fig. 8.		tSCKH(8) + (5/3)tCYC		tSCKH(8) + (43/3)tCYC	
Serial input	Data setup time		tsDI(4)	SO9(P25), SI9(P26)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 8.	2.7 to 5.5	0.03			μs
	Data hold time		thDI(4)				0.03			
Serial output	Output delay time		tdDO(6)	SO9(P25), SI9(P26)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode • See Fig. 8.	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-4-3: When using the serial clock output, make sure that the load at the SCK9 (P27) pin meets the following conditions:
Clock rise time tSCKR < 0.037μs (see Figure 12.) at Ta=+25°C, V_{DD}=3.3V

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tP1H(1) tP1L(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27), INT6(P20), INT7(P24)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.7 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are nabled.	2.7 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.7 to 5.5	256			
	tPIL(5)	RMIN(P73)	Recognized by the infrared remote control receiver circuit as a signal	2.7 to 5.5	4			RMCK (Note 5-1)
	tPIL(6)	$\overline{RES}$	Resetting is enabled.	2.7 to 5.5	200			µs

Note 5-1: Represents the period of the reference clock (1 tCYC to 128 tCYC or the source frequency of the subclock) for the infrared remote control receiver circuit.

AD Converter Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN7(P07), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	15.68 (tCYC= 0.490µs)		97.92 (tCYC= 3.06µs)	µs
				3.0 to 5.5	23.52 (tCYC= 0.735µs)		97.92 (tCYC= 3.06µs)	
			AD conversion time=64×tCYC (when ADCR2=1) (Note 6-2)	4.5 to 5.5	18.82 (tCYC= 0. 294µs)		97.92 (tCYC= 1.53µs)	
				3.0 to 5.5	47.04 (tCYC= 0.735µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy.

Note 6-2: The conversion time refers to the period from the time when an instruction for starting a conversion process is issued to the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1$ $=V_{DD}2$ $=V_{DD}3$	• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation stopped • Internal RC oscillation stopped • USB circuit stopped • 1/1 frequency division ratio	4.5 to 5.5		9.8	24	mA
	IDDOP(2)			3.0 to 3.6		5.7	14	
	IDDOP(3)		• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation mode active • Internal RC oscillation stopped • USB circuit active • 1/1 frequency division ratio	4.5 to 5.5		15	35	
	IDDOP(4)			3.0 to 3.6		7.7	20	
	IDDOP(5)		• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 6MHz side • Internal RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		6.7	16	
	IDDOP(6)			3.0 to 3.6		3.9	9.0	
	IDDOP(7)			2.7 to 3.0		3.2	7.3	
	IDDOP(8)		• FmCF=0Hz(oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation. • 1/2 frequency division ratio	4.5 to 5.5		0.72	3.4	
	IDDOP(9)			3.0 to 3.6		0.41	1.9	
	IDDOP(10)			2.7 to 3.0		0.35	1.5	
	IDDOP(11)		• FmCF=0Hz(oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to crystal oscillation. (32.768kHz) • Internal RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		45	184	µA
	IDDOP(12)			3.0 to 3.6		18	65	
	IDDOP(13)			2.7 to 3.0		14	47	
HALT mode consumption current (Note7-1)	IDDHALT(1)		• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation stopped • Internal RC oscillation stopped • USB circuit stopped • 1/1 frequency division ratio	4.5 to 5.5		4.9	12	mA
	IDDHALT(2)			3.0 to 3.6		2.7	6.4	
	IDDHALT(3)		• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal PLL oscillation mode active • Internal RC oscillation stopped • USB circuit active • 1/1 frequency division ratio	4.5 to 5.5		9.5	23	
	IDDHALT(4)			3.0 to 3.6		4.7	12	
	IDDHALT(5)		• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 6MHz side • Internal RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		3.0	7.3	
	IDDHALT(6)			3.0 to 3.6		1.6	3.8	
	IDDHALT(7)			2.7 to 3.0		1.3	2.9	
	IDDHALT(8)		• HALT mode • FmCF=0Hz(oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation. • 1/2 frequency division ratio	4.5 to 5.5		0.41	2.0	
	IDDHALT(9)			3.0 to 3.6		0.20	0.95	
	IDDHALT(10)			2.7 to 3.0		0.17	0.70	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(11)	$V_{DD}1$ $=V_{DD}2$ $=V_{DD}3$	• HALT mode • FmCF=0MHz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to crystal oscillation. (32.768kHz) • Internal RC oscillation stopped • 1/2 frequency division ratio	4.5 to 5.5		31	132	µA
	IDDHALT(12)			3.0 to 3.6		9.1	39	
	IDDHALT(13)			2.7 to 3.0		6.3	27	
HOLD mode consumption current	IDDHOLD(1)	$V_{DD}1$	• HOLD mode • CF1=V_{DD} or open (External clock mode)	4.5 to 5.5		0.14	39	
	IDDHOLD(2)			3.0 to 3.6		0.04	19	
	IDDHOLD(3)			2.7 to 3.0		0.04	17	
Timer HOLD mode consumption current	IDDHOLD(4)		• Timer HOLD mode • CF1=V_{DD} or open (External clock mode) • FsX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		25	115	
	IDDHOLD(5)			3.0 to 3.6		6.0	32	
	IDDHOLD(6)			2.7 to 3.0		3.7	20	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

USB Characteristics and Timing at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Conditions	Specification			
			min	typ	max	unit
High level output	$V_{OH(USB)}$	• 15kΩ±5% to GND	2.8		3.6	V
Low level output	$V_{OL(USB)}$	• 1.5kΩ±5% to 3.6V	0.0		0.3	V
Output signal crossover voltage	V_{CRS}		1.3		2.0	V
Differential input sensitivity	V_{DI}	• $\|(UHD+)-(UHD-)\|$	0.2			V
Differential input common mode range	V_{CM}		0.8		2.5	V
High level input	$V_{IH(USB)}$		2.0			V
Low level input	$V_{IL(USB)}$				0.8	V
USB data rise time	t_R	• R_S=33Ω, C_L=50pF	4		20	ns
USB data fall time	t_F	• R_S=33Ω, C_L=50pF	4		20	ns

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Excluding power dissipation in the microcontroller block	3.0 to 5.5		5	10	mA
Programming time	tFW(1)		• Erase operation	3.0 to 5.5		20	30	ms
	tFW(2)		• Write operation			40	60	µs

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 shows the characteristics of a oscillation circuit when USB host function is not used.

If USB host function is to be used, it is absolutely recommended to use an oscillator that satisfies the precision and stability according to the USB standards.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant			Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rd1 [Ω]		typ [ms]	max [ms]	
6MHz	MURATA	CSTCR6M00GH5L**-R0	(39)	(39)	1k	2.7 to 5.5	0.1	0.5	C1 and C2 integrated SMD type
8MHz	MURATA	CSTCE8M00GH5L**-R0	(33)	(33)	470	3.0 to 5.5	0.1	0.5	
10MHz	MURATA	CSTCE10M0GH5L**-R0	(33)	(33)	330	3.0 to 5.5	0.1	0.5	
12MHz	MURATA	CSTCE12M0GH5L**-R0	(33)	(33)	330	3.0 to 5.5	0.1	0.5	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in the following cases (see Figure 4):

- Till the oscillation gets stabilized after V_{DD} goes above the operating voltage lower limit.
- Till the oscillation gets stabilized after the instruction for starting the main clock oscillation circuit is executed
- Till the oscillation gets stabilized after the HOLD mode is reset.
- Till the oscillation gets stabilized after the X'tal HOLD mode is reset with CFSTOP (OCR register, bit 0) set to 0

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	OPEN	560k	2.7 to 5.5	1.1	3.0	Applicable CL value=12.5pF SMD type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in the following cases (see Figure 4):

- Till the oscillation gets stabilized after the instruction for starting the subclock oscillation circuit is executed
- Till the oscillation gets stabilized after the HOLD mode is reset with EXTOSC (OCR register, bit 6) set to 1

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

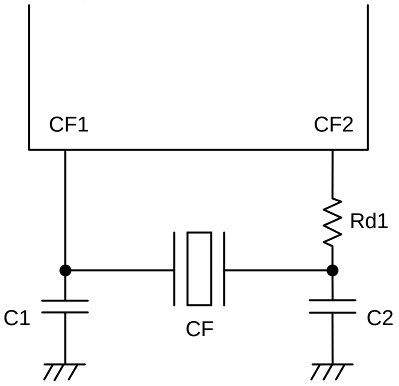


Figure 1 CF Oscillator Circuit

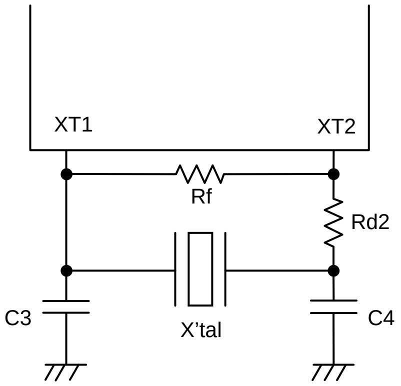


Figure 2 Crystal Oscillator Circuit

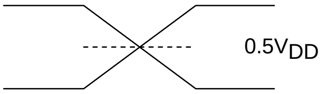
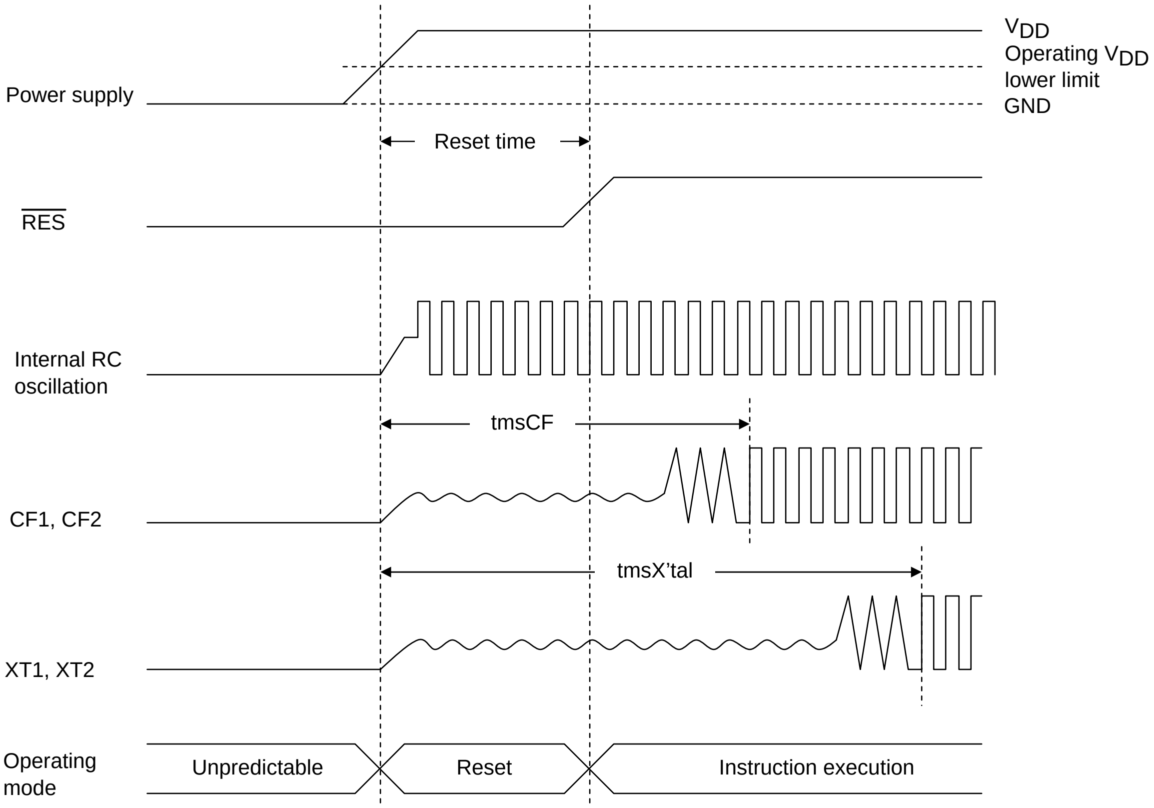
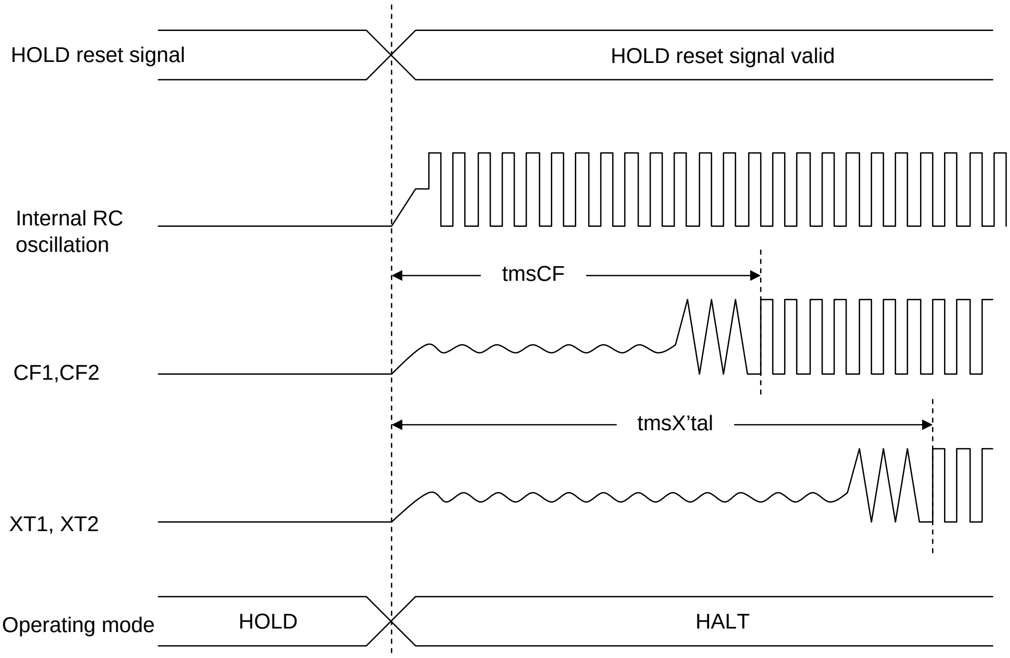


Figure 3 AC Timing Measurement Point

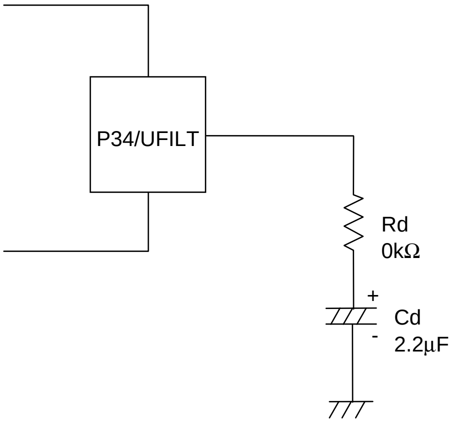


Reset Time and Oscillation Stabilization Time



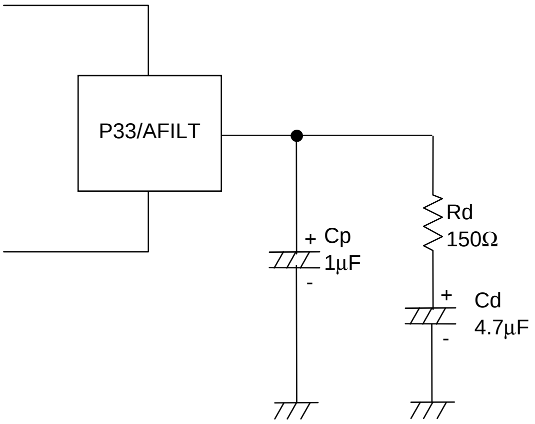
HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time



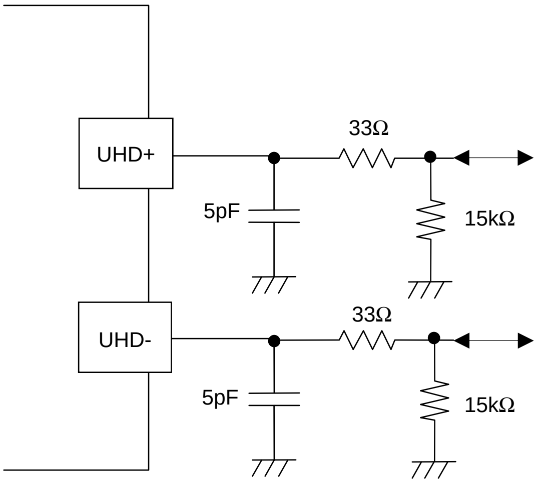
When using the internal PLL circuit to generate the 48MHz clock for USB , it is necessary to connect a filter circuit such to the P34/UFILT pin such as that shown in the left Fig.

Figure 5 External Filter Circuit for the Internal USB-dedicated PLL Circuit



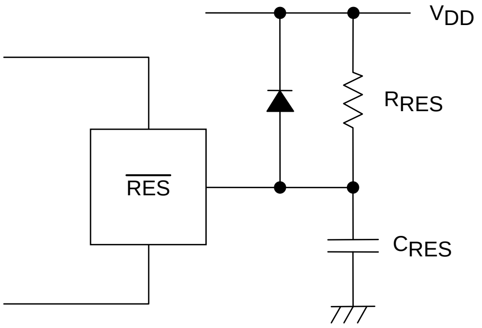
To generate the master clock for the audio interface using the internal PLL circuit, it is necessary to connect a filter circuit to the P33/AFILT pin that is shown in the left Fig.

Figure 6 External Filter Circuit for Audio Interface (Used with Internal PLL Circuit)



It’s necessary to adjust the Circuit Constant of the USB Port Peripheral Circuit for each mounting board.

Figure 7 USB Port Peripheral Circuit



Note:
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200μs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 8 Reset Circuit

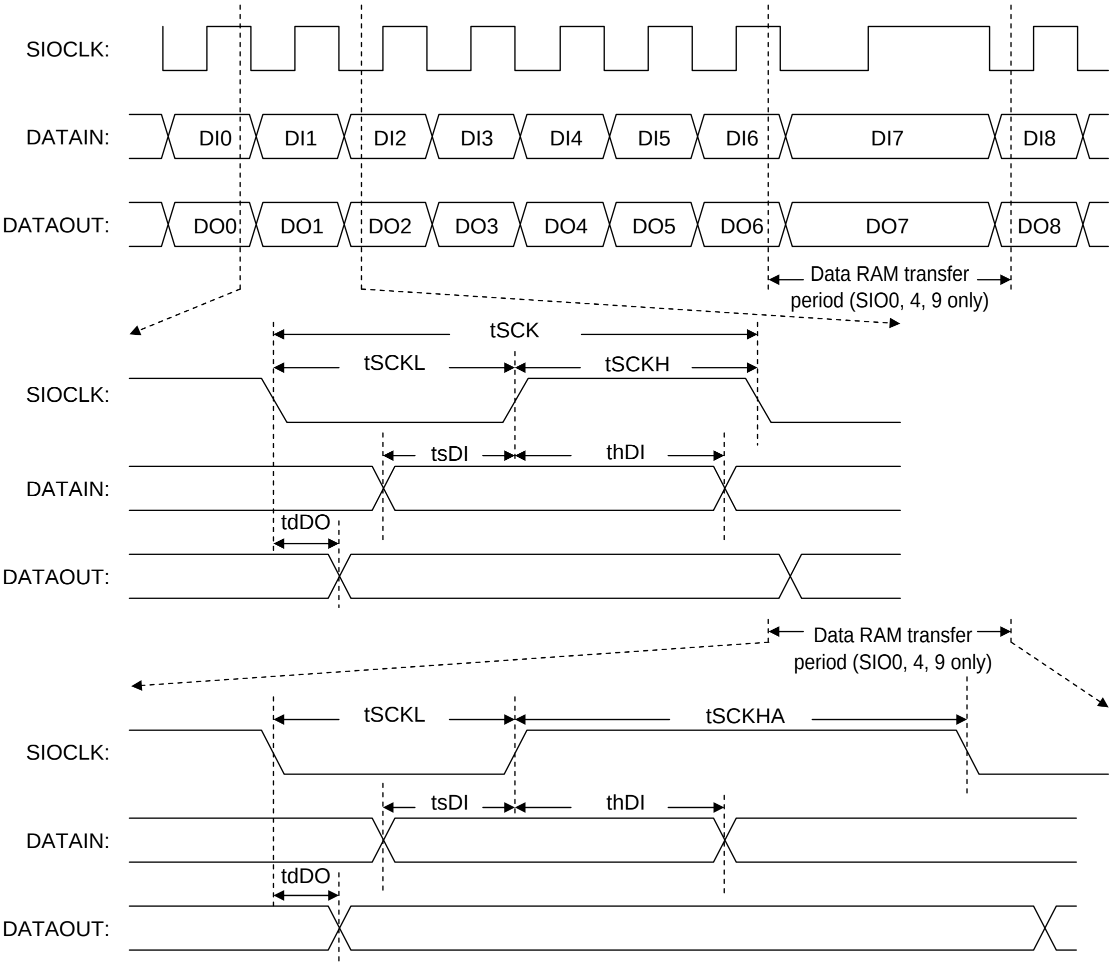


Figure 9 Serial Input/Output Waveform

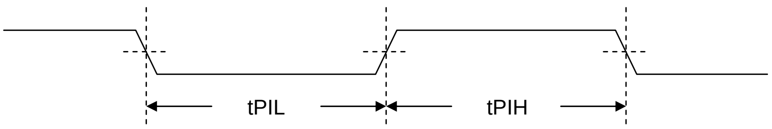


Figure 10 Pulse Input Timing Signal Waveform

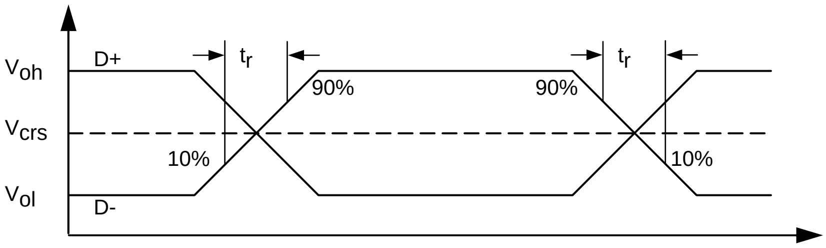
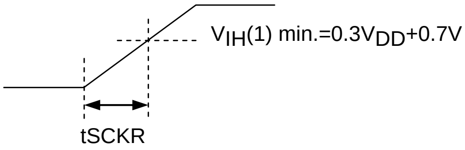


Figure 11 USB Data Signal Timing and Voltage Level



tSCKR:
Defined as the time period from the time the state of the output starts changing till the time it reaches the minimum value of $V_{IH}(1)$.

Figure 12 Serial Clock Output Timing Signal Waveform

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