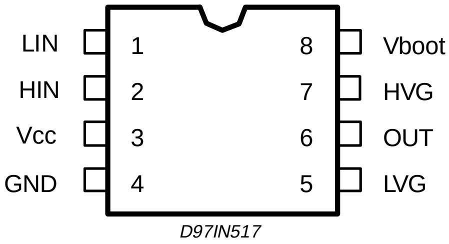
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vout	Output Voltage	-3 to Vboot - 18	V
Vcc	Supply Voltage	- 0.3 to +18	V
Vboot	Floating Supply Voltage	- 1 to 618	V
Vhvg	Upper Gate Output Voltage	- 1 to Vboot	V
Vlvg	Lower Gate Output Voltage	-0.3 to Vcc +0.3	V
Vi	Logic Input Voltage	-0.3 to Vcc +0.3	V
dVout/dt	Allowed Output Slew Rate	50	V/ns
Ptot	Total Power Dissipation (Tj = 85 °C)	750	mW
Tj	Junction Temperature	150	°C
Ts	Storage Temperature	-50 to 150	°C

Note: ESD immunity for pins 6, 7 and 8 is guaranteed up to 900V (Human Body Model)

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	SO8	Minidip	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction to Ambient	150	100	°C/W

PIN DESCRIPTION

N.	Name	Type	Function
1	LIN	I	Lower Driver Logic Input
2	HIN	I	Upper Driver Logic Input
3	Vcc	I	Low Voltage Power Supply
4	GND		Ground
5	LVG (*)	O	Low Side Driver Output
6	VOUT	O	Upper Driver Floating Reference
7	HVG (*)	O	High Side Driver Output
8	Vboot		Bootstrap Supply Voltage

(*) The circuit guarantees 0.3V maximum on the pin (@ I_{sink} = 10mA). This allows to omit the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vout	6	Output Voltage		Note 1		580	V
Vboot-Vout	8	Floating Supply Voltage		Note 1		17	V
fsw		Switching Frequency	HVG,LVG load CL = 1nF			400	kHz
Vcc	2	Supply Voltage				17	V
T_j		Junction Temperature		-45		125	°C

Note 1: If the condition Vboot - Vout < 18V is guaranteed, Vout can range from -3 to 580V.

ELECTRICAL CHARACTERISTICS
AC Operation (Vcc = 15V; Tj = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ton	1 vs 5	High/Low Side Driver Turn-On Propagation Delay	Vout = 0V		110		ns
toff	2 vs 7	High/Low Side Driver Turn-Off Propagation Delay	Vout = 600V		105		ns
tr	7,5	Rise Time	CL = 1000pF		50		ns
tf	7,5	Fall Time	CL = 1000pF		30		ns

DC OPERATION (Vcc = 15V; Tj = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Low Supply Voltage Section							
Vcc	3	Supply Voltage				17	V
Vccth1		Vcc UV Turn On Threshold		9.1	9.6	10.1	V
Vccth2		Vcc UV Turn Off Threshold		7.9	8.3	8.8	V
Vcchys		Vcc UV Hysteresis			1.3		V
Iqccu		Undervoltage Quiescent Supply Current	Vcc ≤ 9V		150	220	µA
Iqcc		Quiescent Current	Vcc = 15V		250	320	µA
R_{dson}		Bootstrap Driver on Resistance (*)	Vcc ≥ 12.5V		125		Ω
Bootstrapped supply Voltage Section							
VBS	8	Bootstrap Supply Voltage				17	V
VBSth1		VBS UV Turn On Threshold		8.5	9.5	10.5	V
VBSth2		VBS UV Turn Off Threshold		7.2	8.2	9.2	V
VBShys		VBS UV Hysteresis			1.3		V
IQBS		VBS Quiescent Current	HVG ON			200	µA
ILK		High Voltage Leakage Current	VS = VB = 600V			10	µA
High/Low Side Driver							
Iso	5,7	Source Short Circuit Current	VIN = Vih (tp < 10µs)	300	400		mA
Isi		Sink Short Circuit Current	VIN = Vil (tp < 10µs)	450	650		mA
Logic Inputs							
Vil	2,3	Low Level Logic Threshold Voltage				1.5	V
Vih		High Level Logic Threshold Voltage		3.6			V
Iih		High Level Logic Input Current	VIN = 15V		50	70	µA
Iil		Low Level Logic Input Current	VIN = 0V			1	µA

(*) R_{DSON} is tested in the following way: $R_{DSON} = \frac{(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})}{I_1(V_{CC},V_{CBOOT1}) - I_2(V_{CC},V_{CBOOT2})}$

where I_1 is pin 8 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$.

Figure 1. Input/Output Timing Diagram

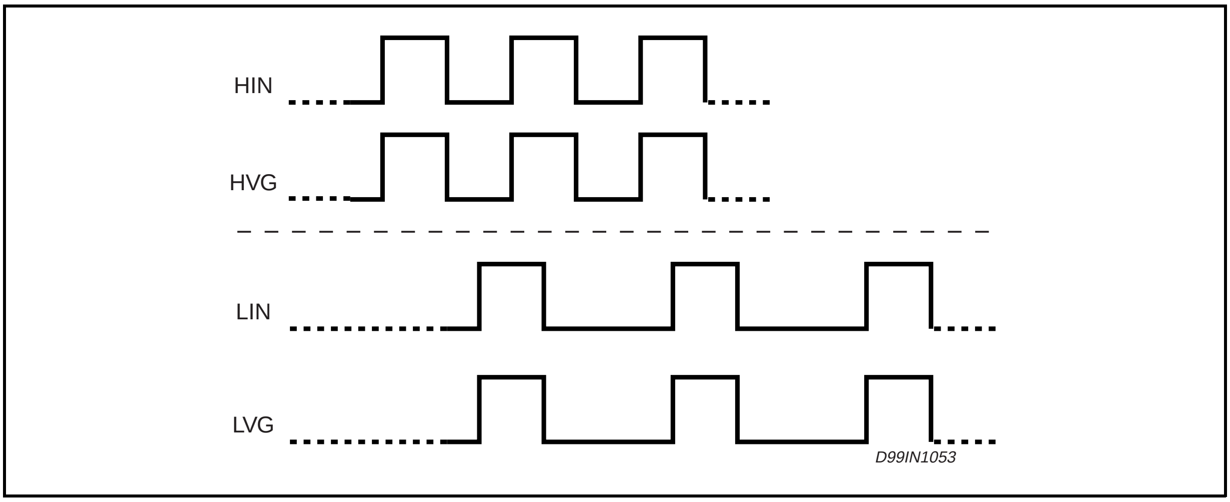


Figure 2. Typical Rise and Fall Times vs. Load Capacitance

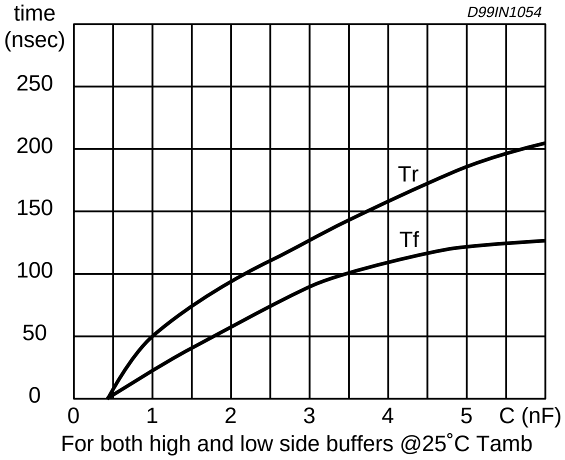
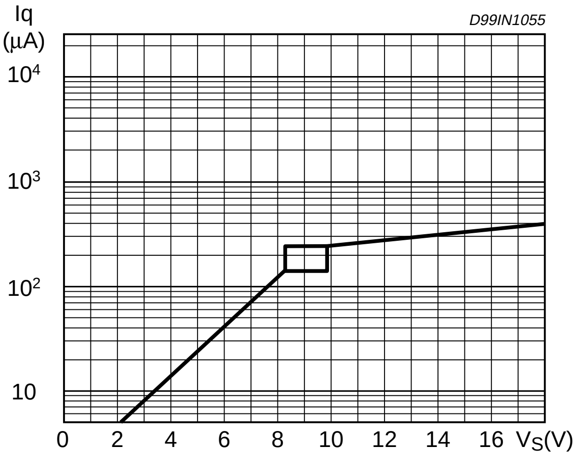


Figure 3. Quiescent Current vs. Supply Voltage



BOOTSTRAP DRIVER

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (fig. 4a). In the L6385 a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in fig. 4b

An internal charge pump (fig. 4b) provides the DMOS driving voltage .

The diode connected in series to the DMOS has been added to avoid undesirable turn on of it.

CBOOT selection and charging:

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge :

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss .

It has to be:

$$C_{BOOT} >>> C_{EXT}$$

e.g.: if Q_{gate} is 30nC and V_{gate} is 10V, C_{EXT} is 3nF. With C_{BOOT} = 100nF the drop would be 300mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage losses.

e.g.: HVG steady state consumption is lower than 200µA, so if HVG T_{ON} is 5ms, C_{BOOT} has to supply 1µC to C_{EXT}. This charge on a 1µF capacitor means a voltage drop of 1V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has great leakage current). This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSON} (typical value: 125 Ohm). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{drop} = I_{charge}R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}}R_{dson}$$

where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1V, if the T_{charge} is 5µs. In fact:

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 4. Bootstrap Driver.

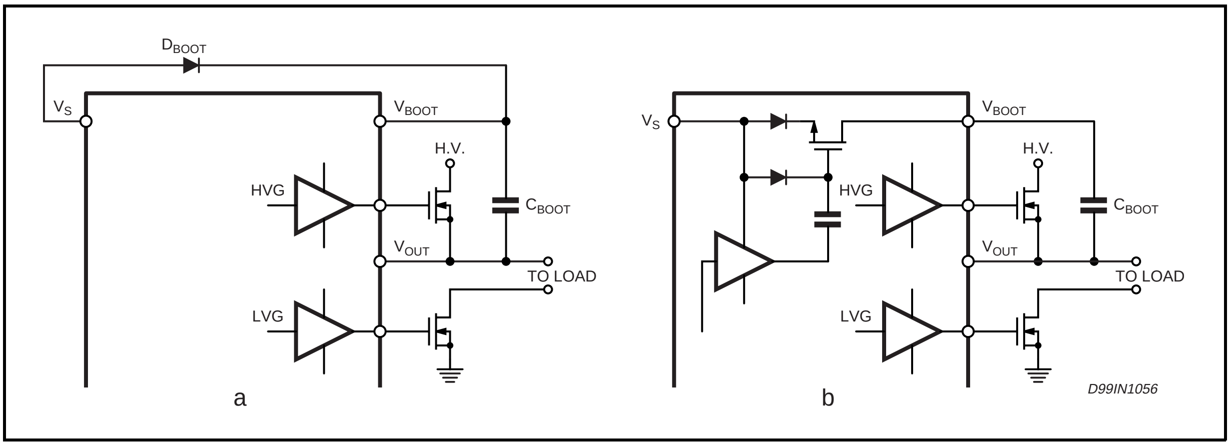


Figure 5. Turn On Time vs. Temperature

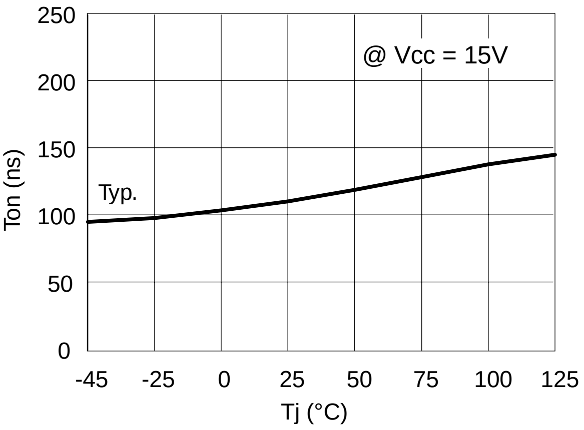


Figure 6. Turn Off Time vs. Temperature

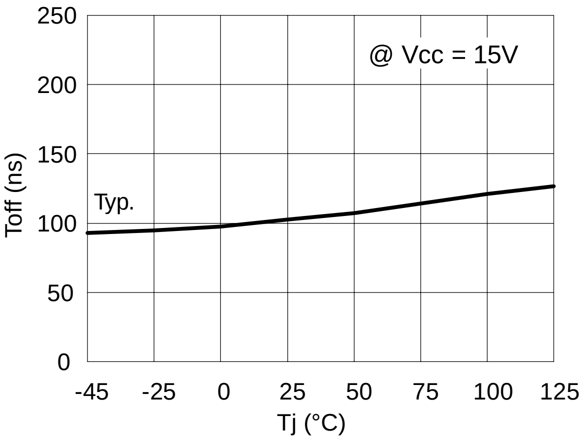


Figure 7. V_{BOOT} UV Turn On Threshold vs. Temperature

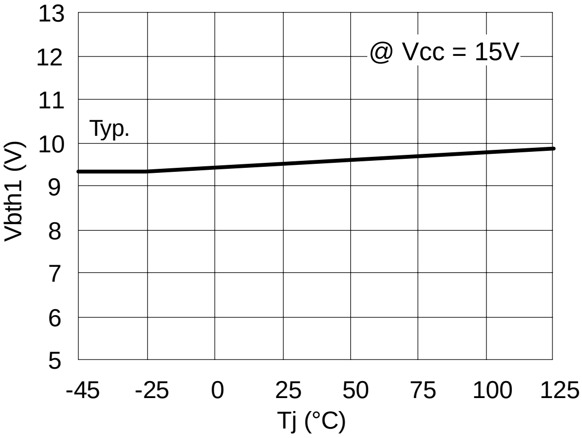


Figure 10. Vcc UV Turn Off Threshold vs. Temperature

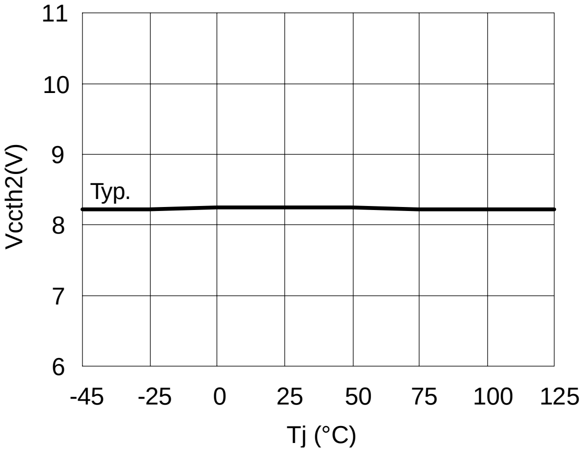


Figure 8. V_{BOOT} UV Turn Off Threshold vs. Temperature

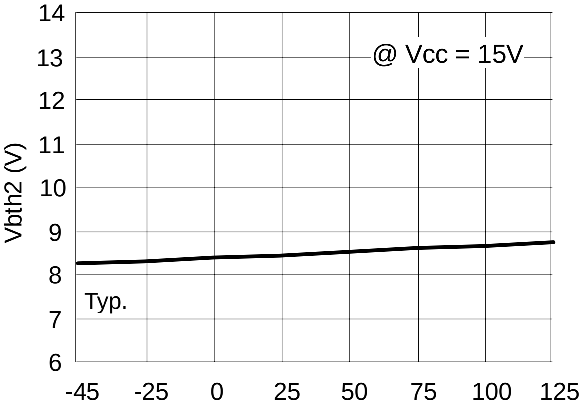


Figure 11. Output Source Current vs. Temperature

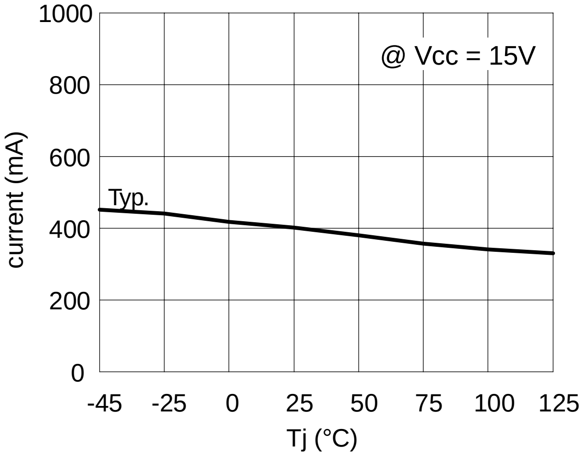


Figure 9. Vcc UV Turn On Threshold vs. Temperature

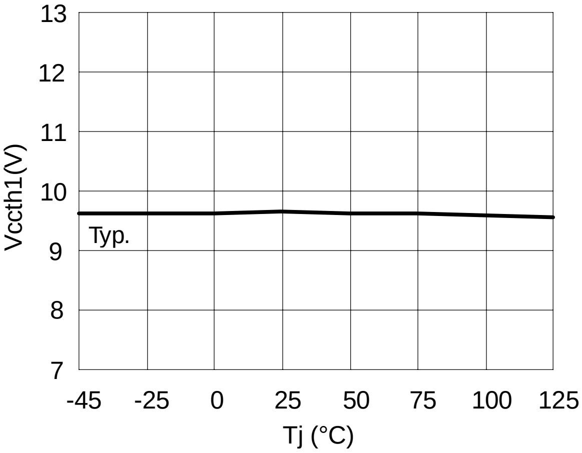
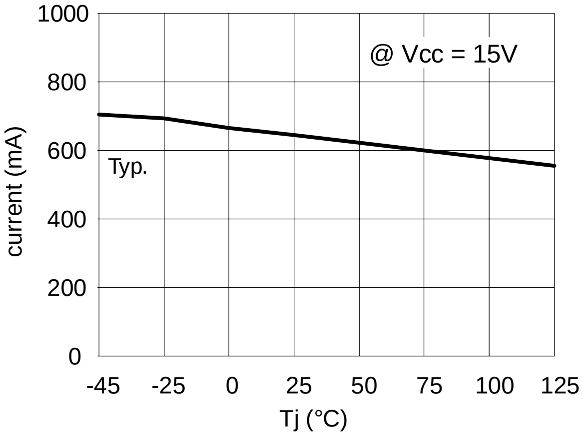
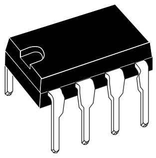


Figure 12. Output Sink Current vs. Temperature

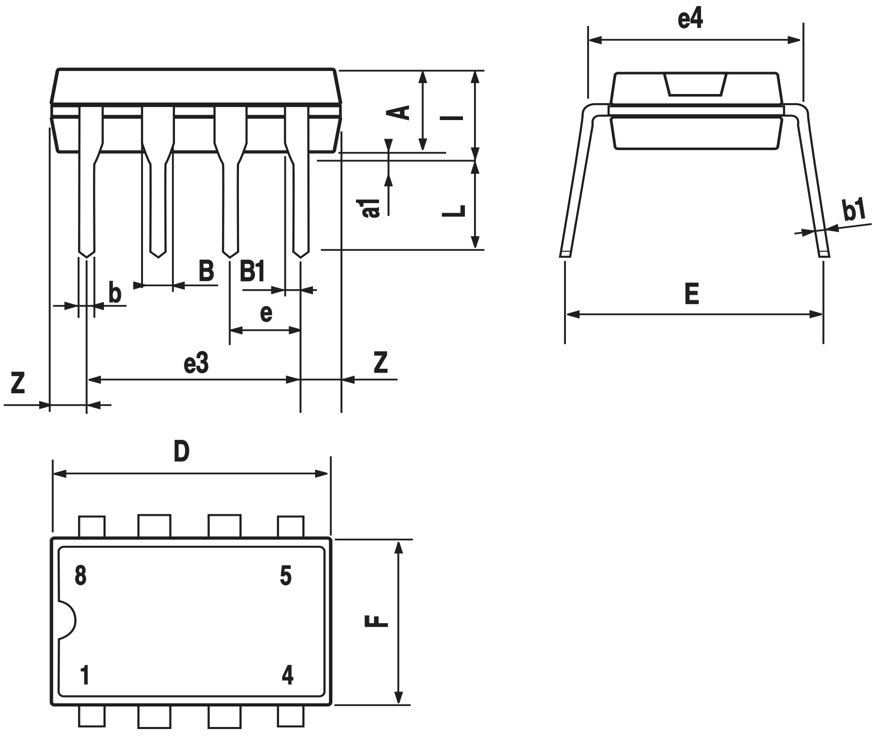


OUTLINE AND MECHANICAL DATA



Minidip

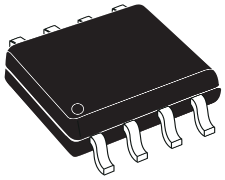
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060



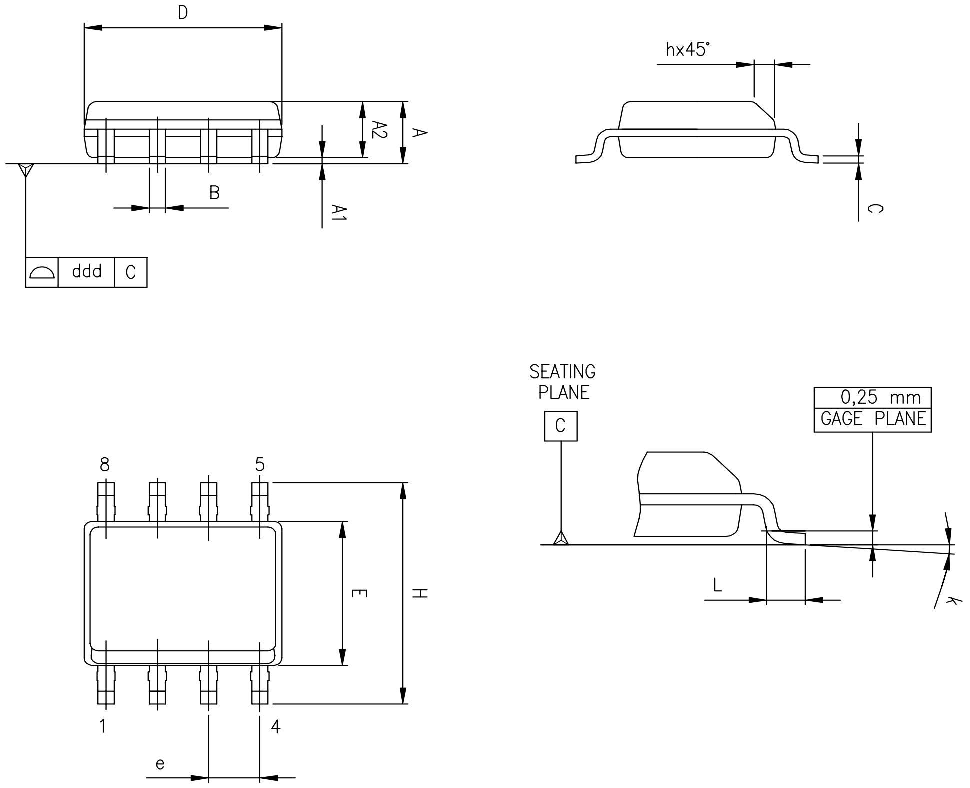
DIM.	mm			inch		
	MIN.	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

Note: (1) Dimensions D does not include mold flash, protrusions or gate burrs.
Mold flash, potrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

OUTLINE AND MECHANICAL DATA



SO-8



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