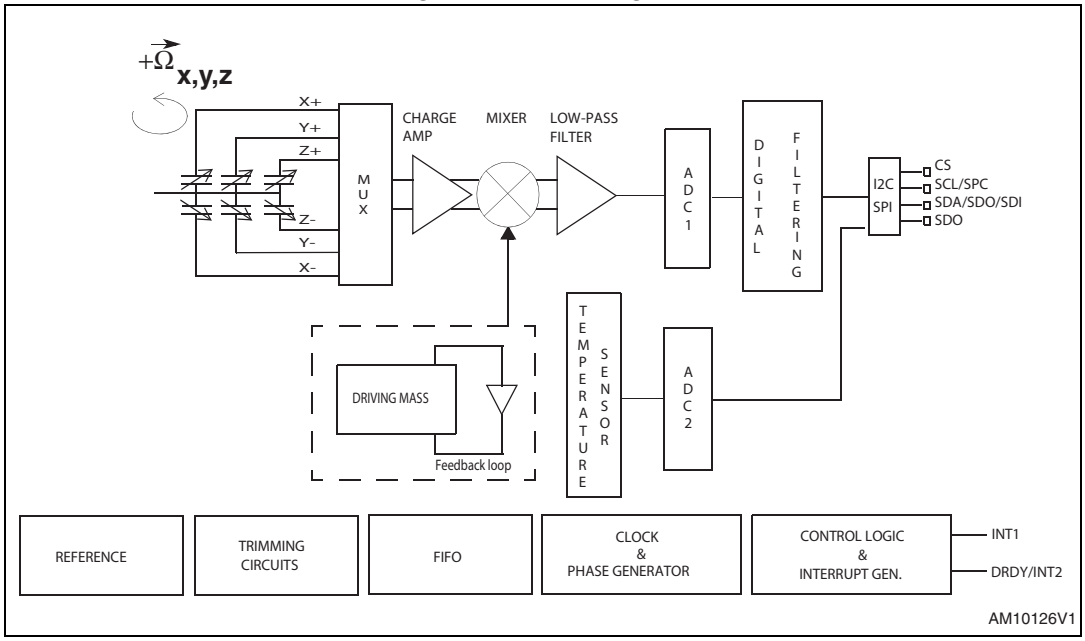
# Contents

# List of tables

# List of figures

# 1 Block diagram and pin description

**Figure 1. Block diagram**




*Note: The vibration of the structure is maintained by drive circuitry in a feedback loop. The sensing signal is filtered and appears as a digital signal at the output.*

## 1.1 Pin description

**Figure 2. Pin connection**

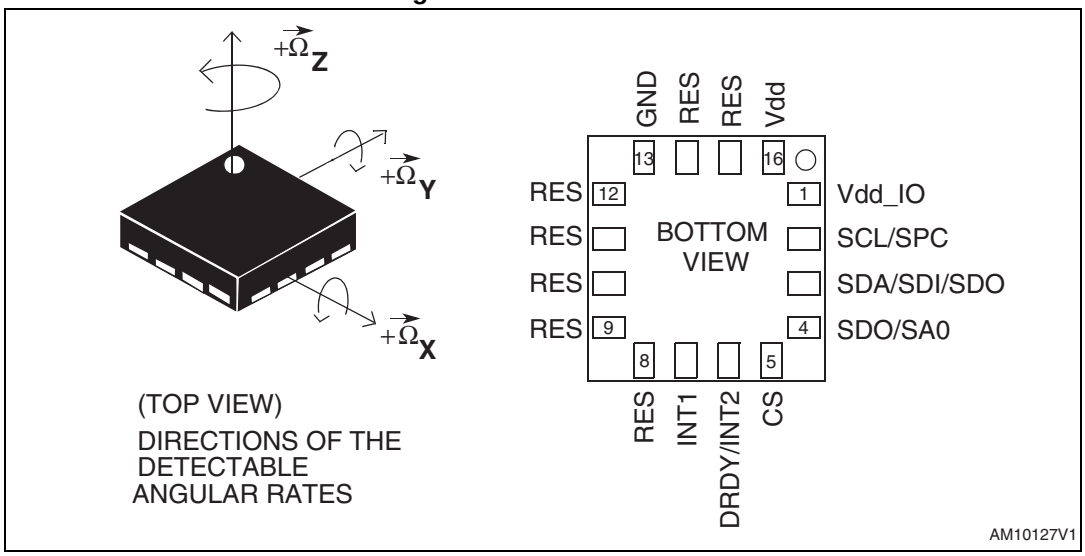


**Table 2. Pin description**

**Table 3.**

| Pin# | Name | Function |
|---|---|---|
| 1 | Vdd_IO(1) | Power supply for I/O pins |
| 2 | SCL<br>SPC | $I^2C$ serial clock (SCL)<br>SPI serial port clock (SPC) |
| 3 | SDA<br>SDI<br>SDO | $I^2C$ serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| 4 | SDO<br>SA0 | SPI serial data output (SDO)<br>$I^2C$ less significant bit of the device address (SA0) |
| 5 | CS | $I^2C$/SPI mode selection (1: SPI idle mode / $I^2C$ communication enabled; 0: SPI communication mode / $I^2C$ disabled) |
| 6 | DRDY/INT2 | Data ready/FIFO interrupt (Watermark/Overrun/Empty) |
| 7 | INT1 | Programmable interrupt |
| 8 | Reserved | Connect to GND |
| 9 | Reserved | Connect to GND |
| 10 | Reserved | Connect to GND |
| 11 | Reserved | Connect to GND |
| 12 | Reserved | Connect to GND |
| 13 | GND | 0 V supply |
| 14 | Reserved | Connect to GND with ceramic capacitor(2) |
| 15 | Reserved | Connect to Vdd |
| 16 | Vdd(3) | Power supply |

1. 100 nF filter capacitor recommended.
2. 1 nF min value must be guaranteed under 11 V bias condition.
3. 100 nF plus 10 $\mu$F capacitors recommended.

# 2 Mechanical and electrical specifications

## 2.1 Mechanical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted.

**Table 4. Mechanical characteristics(1)**

| Symbol | Parameter | Test condition | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|
| FS | Measurement range | User-selectable | | ±250 | | dps |
| | | | | ±500 | | |
| | | | | ±2000 | | |
| So | Sensitivity | FS = 250 dps | | 8.75 | | mdps/digit |
| | | FS = 500 dps | | 17.50 | | |
| | | FS = 2000 dps | | 70 | | |
| SoDr | Sensitivity change vs. temperature | From -40 °C to +85 °C | | ±2 | | % |
| DVoff | Digital zero-rate level | FS = 250 dps | | ±10 | | dps |
| | | FS = 500 dps | | ±15 | | |
| | | FS = 2000 dps | | ±75 | | |
| OffDr | Zero-rate level change vs. temperature | FS = 250 dps | | ±0.03 | | dps/°C |
| | | FS = 2000 dps | | ±0.04 | | dps/°C |
| NL | Non linearity | Best fit straight line | | 0.2 | | % FS |
| Rn | Rate noise density | | | 0.03 | | dps/(√Hz) |
| ODR | Digital output data rate | | | 95/190/ 380/760 | | Hz |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. The product is factory calibrated at 3.0 V. The operational power supply range is specified in *Table 5*.
2. Typical specifications are not guaranteed.

## 2.2 Electrical characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted.

**Table 5. Electrical characteristics (1)**

| Symbol | Parameter | Test condition | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|
| Vdd | Supply voltage | | 2.4 | 3.0 | 3.6 | V |
| Vdd_IO | I/O pins supply voltage(3) | | 1.71 | | Vdd+0.1 | V |
| Idd | Supply current | | | 6.1 | | mA |
| IddSL | Supply current in sleep mode(4) | Selectable by digital interface | | 2 | | mA |
| IddPdn | Supply current in power-down mode | Selectable by digital interface | | 5 | | µA |
| VIH | Digital high level input voltage | | 0.8*Vdd_IO | | | V |
| VIL | Digital low level input voltage | | | | 0.2*Vdd_IO | V |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses; in this condition the measurement chain is powered off.
4. Sleep mode introduces a faster turn-on time relative to power-down mode.

## 2.3 Temperature sensor characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted.

**Table 6. Electrical characteristics (1)**

| Symbol | Parameter | Test condition | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|
| TSDr | Temperature sensor output change vs. temperature | - | | -1 | | °C/digit |
| TODR | Temperature refresh rate | | | 1 | | Hz |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.

## 2.4 Communication interface characteristics

### 2.4.1 SPI - serial peripheral interface

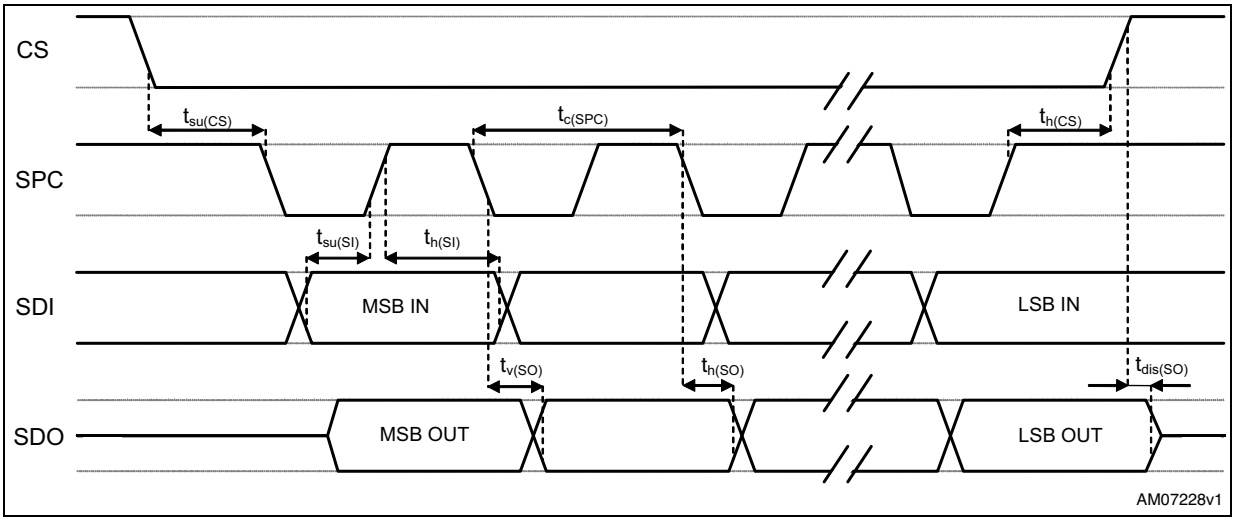
Subject to general operating conditions for Vdd and $T_{op}$.

**Table 7. SPI slave timing values**

| Symbol | Parameter | Value(1) | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| tc(SPC) | SPI clock cycle | 100 | | ns |
| fc(SPC) | SPI clock frequency | | 10 | MHz |
| tsu(CS) | CS setup time | 5 | | ns |
| th(CS) | CS hold time | 8 | | |
| tsu(SI) | SDI input setup time | 5 | | |
| th(SI) | SDI input hold time | 15 | | |
| tv(SO) | SDO valid output time | | 50 | |
| th(SO) | SDO output hold time | 6 | | |
| tdis(SO) | SDO output disable time | | 50 | |

1. Values are guaranteed at a 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results; not tested in production.

**Figure 3. SPI slave timing diagram (a)**




a. Measurement points are at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output port.

### 2.4.2 I²C - Inter IC control interface

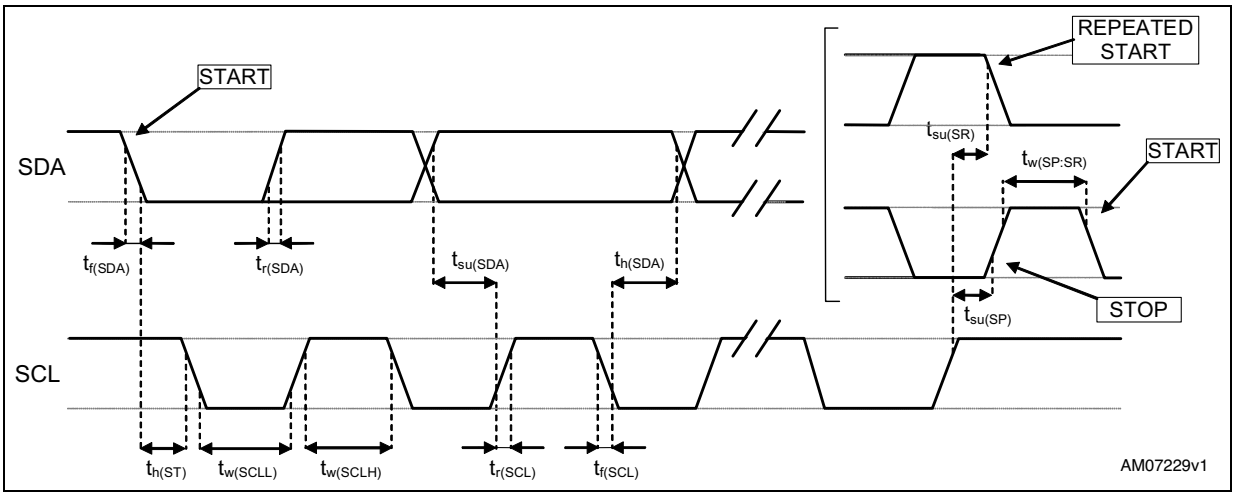
Subject to general operating conditions for Vdd and $T_{op}$.

**Table 8. I²C slave timing values (TBC)**

| Symbol | Parameter | I²C standard mode(1) | | I²C fast mode (1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{(SCL)}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | μs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | 3.45 | 0 | 0.9 | μs |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | 20 + 0.1$C_b$ (2) | 300 | ns |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | | 300 | 20 + 0.1$C_b$ (2) | 300 | |
| $t_{h(ST)}$ | START condition hold time | 4 | | 0.6 | | μs |
| $t_{su(SR)}$ | Repeated START condition setup time | 4.7 | | 0.6 | | |
| $t_{su(SP)}$ | STOP condition setup time | 4 | | 0.6 | | |
| $t_{w(SP:SR)}$ | Bus free time between STOP and START condition | 4.7 | | 1.3 | | |

1. Data based on standard I²C protocol requirement; not tested in production.
2. Cb = total capacitance of one bus line, in pF.

**Figure 4. I²C slave timing diagram (b)**




b. Measurement points are at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

## 2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 9. Absolute maximum ratings**

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| Vdd | Supply voltage | -0.3 to 4.8 | V |
| $T_{STG}$ | Storage temperature range | -40 to +125 | °C |
| Sg | Acceleration g for 0.1 ms | 10,000 | g |
| ESD | Electrostatic discharge protection | 2 (HBM) | kV |
| | | 1.5 (CDM) | kV |
| | | 200 (MM) | V |
| Vin | Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0) | -0.3 to Vdd_IO +0.3 | V |

*Note: Supply voltage on any pin should never exceed 4.8 V*

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part

This is an ESD sensitive device, improper handling can cause permanent damage to the part

## 2.6 Terminology

### 2.6.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counter-clockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

### 2.6.2 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

## 2.7 Soldering information

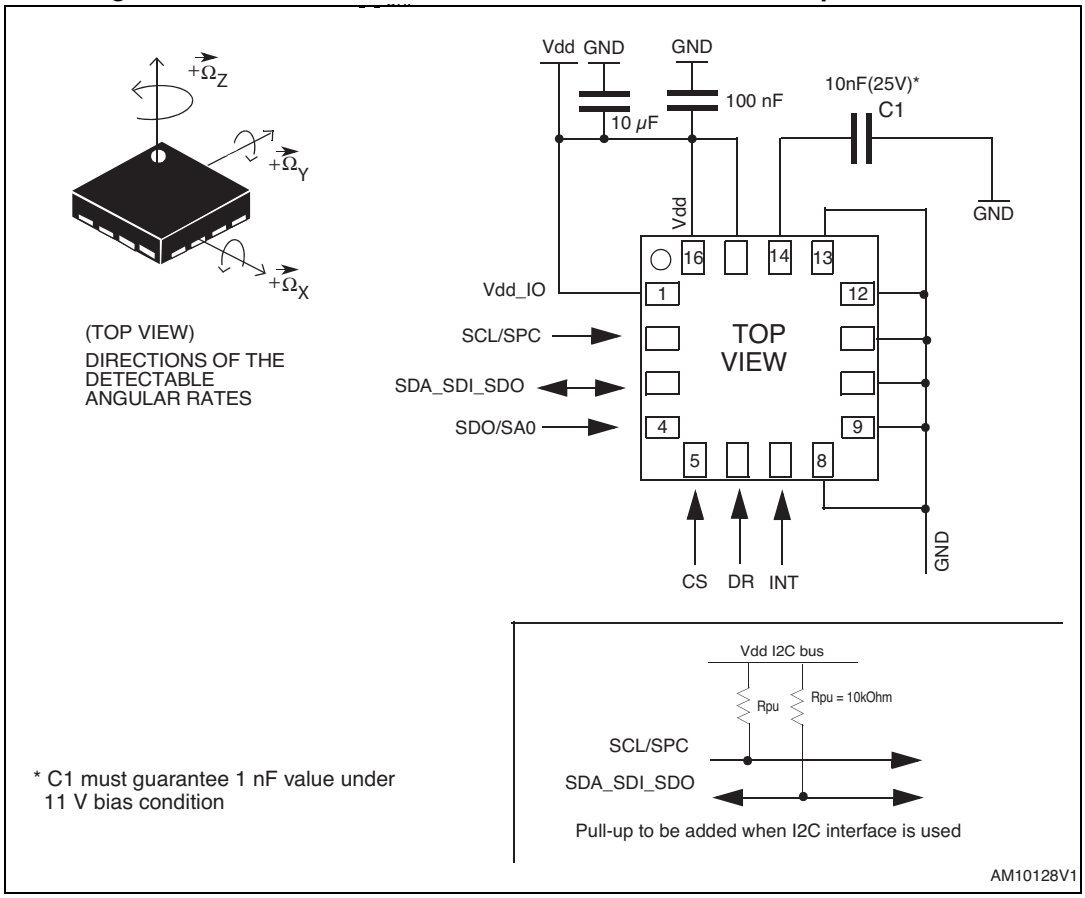
The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

# 3 Application hints

**Figure 5. L3GD20 electrical connections and external component values**



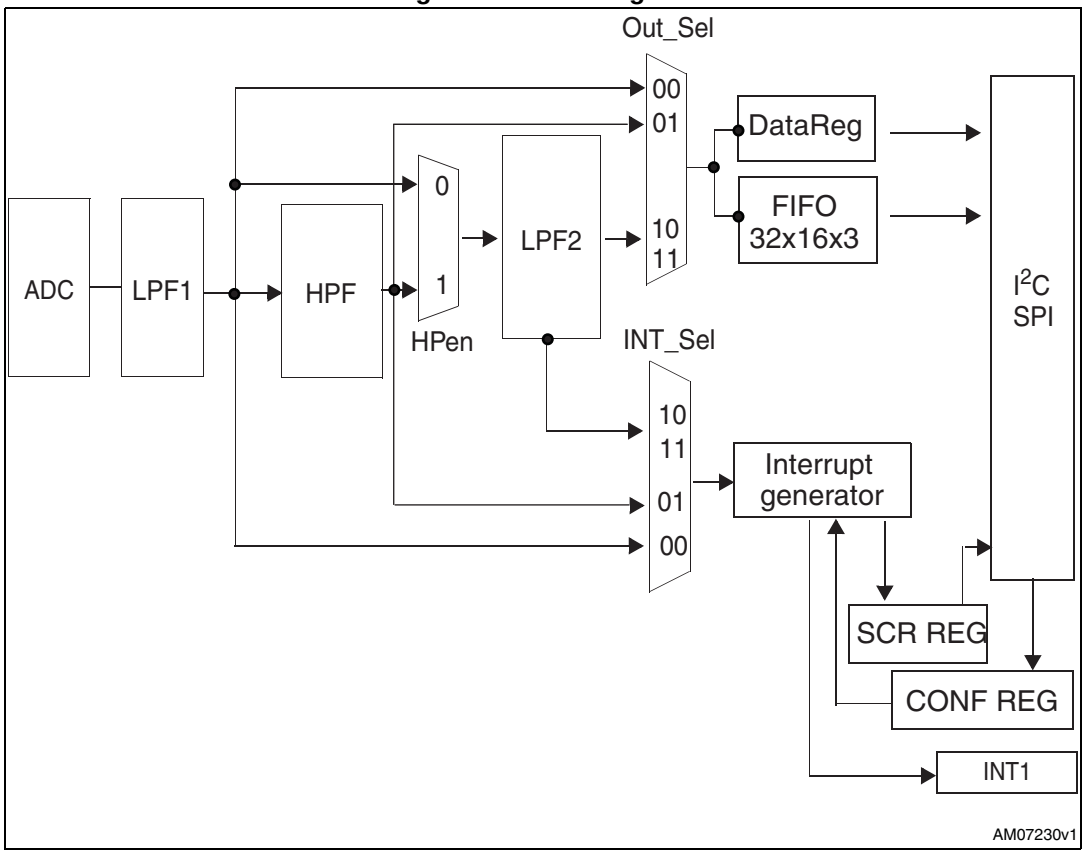

Power supply decoupling capacitors (100 nF + 10 µF) should be placed as near as possible to the device (common design practice).

If Vdd and Vdd_IO are not connected together, 100 nF and 10 µF decoupling capacitors must be placed between Vdd and common ground, and 100 nF between Vdd_IO and common ground. Capacitors should be placed as near as possible to the device (common design practice).

# 4 Digital main blocks

## 4.1 Block diagram

**Figure 6. Block diagram**



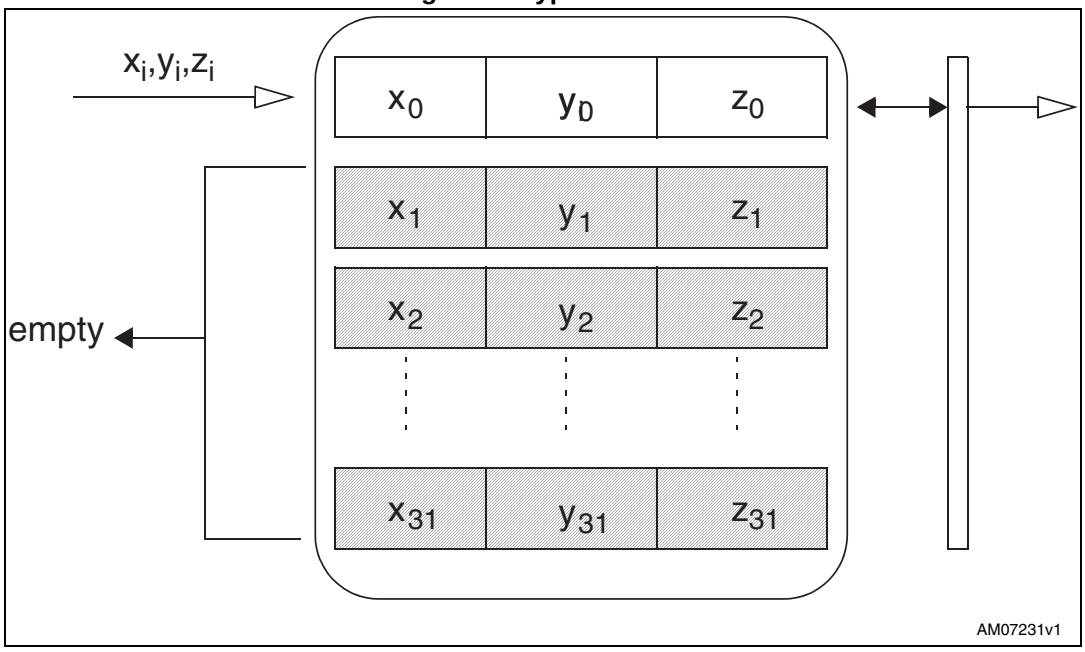

## 4.2 FIFO

The L3GD20 embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in the FIFO_CTRL_REG (2Eh). Programmable Watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL_REG3 (22h) and event detection information is available in FIFO_SRC_REG (2Fh). Watermark level can be configured to WTM4:0 in FIFO_CTRL_REG (2Eh).

### 4.2.1 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in *Figure 7* below, for each channel only the first address is used. The remaining FIFO slots are empty. When new data is available, the old data is overwritten.

**Figure 7. Bypass mode**

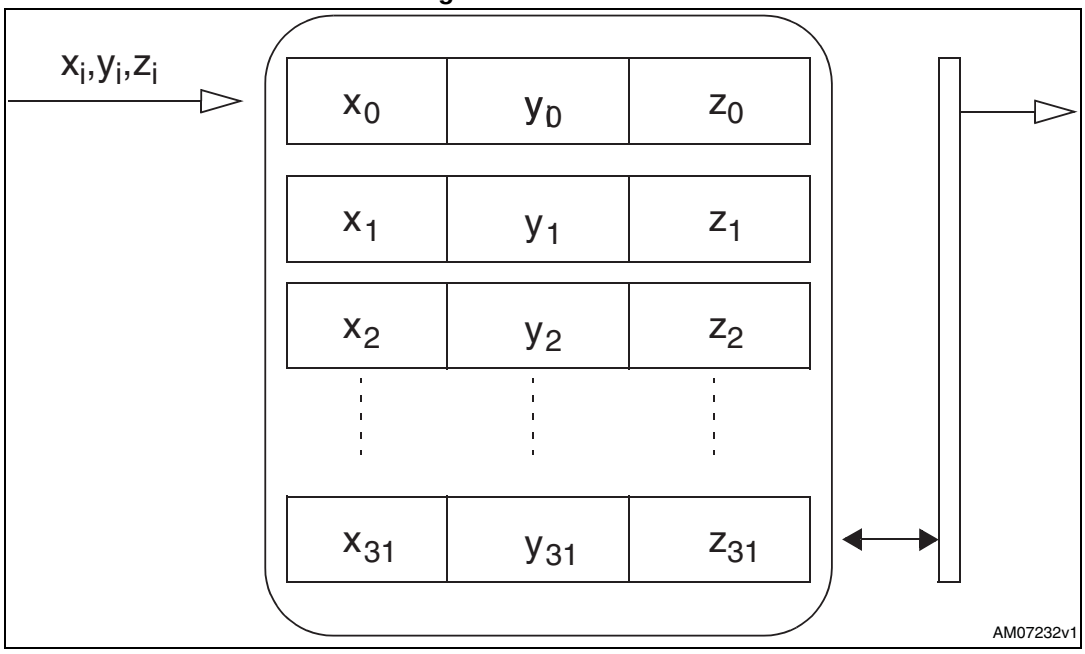



### 4.2.2 FIFO mode

In FIFO mode, data from the yaw, pitch and roll channels is stored in the FIFO. A watermark interrupt can be enabled (I2_WMK bit into CTRL_REG3 (22h)) in order to be raised when the FIFO is filled to the level specified in the WTM 4:0 bits of FIFO_CTRL_REG (2Eh). The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, the FIFO_CTRL_REG (2Eh) must be written back to Bypass mode.

FIFO mode is represented in *Figure 8: FIFO mode*.

Figure 8. FIFO mode

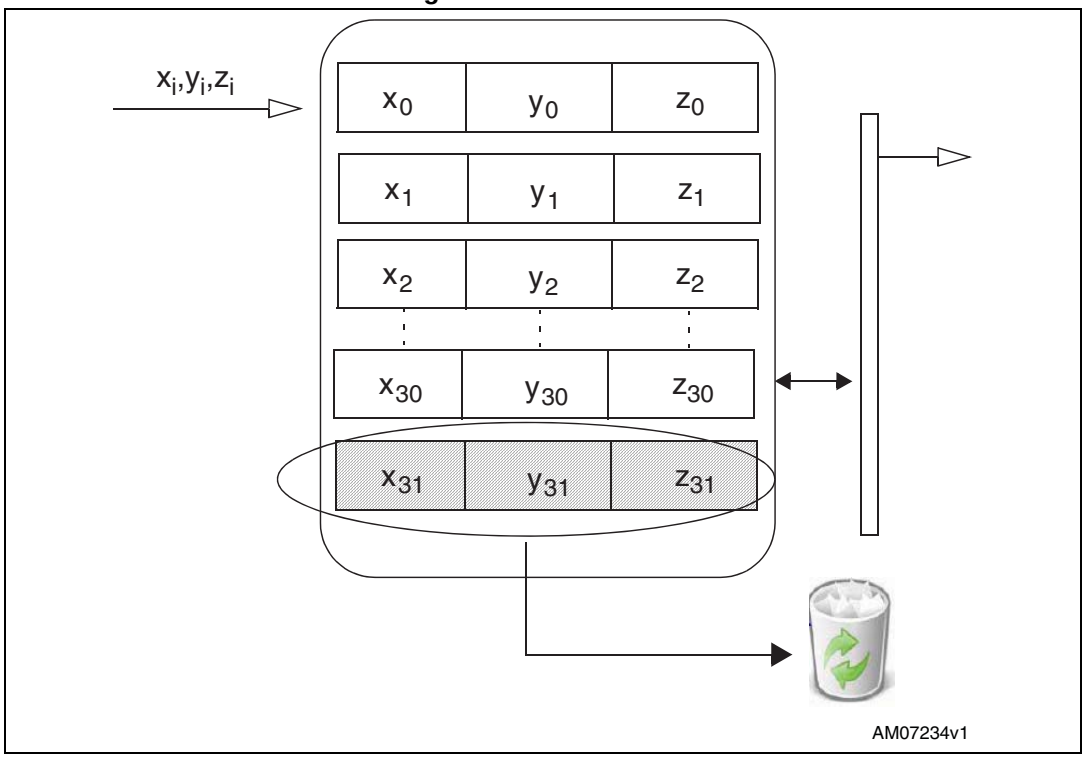



### 4.2.3 Stream mode

In Stream mode, data from yaw, pitch and roll measurement are stored in the FIFO. A watermark interrupt can be enabled and set as in the FIFO mode.The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL_REG3 (22h).

Stream mode is represented in *Figure 9: Stream mode*.

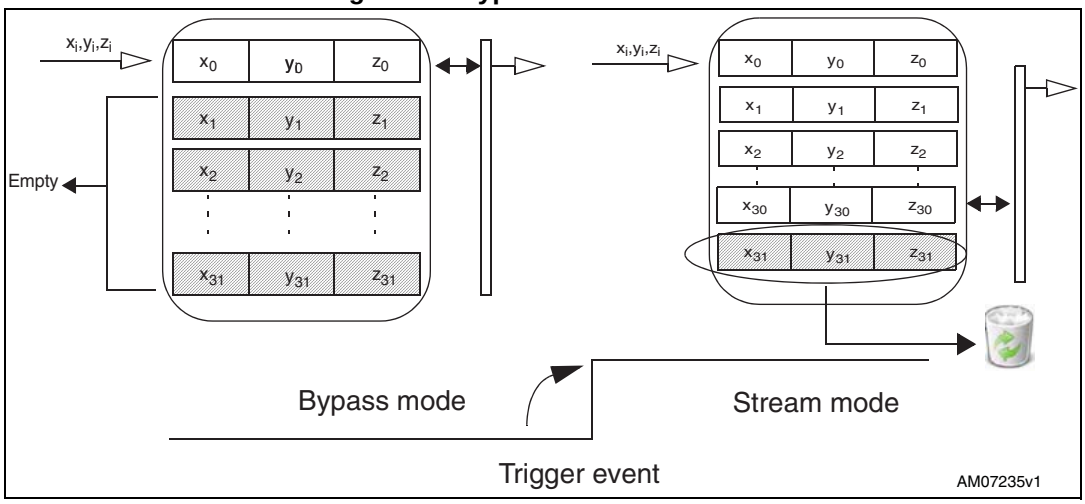
**Figure 9. Stream mode**



### 4.2.4 Bypass-to-stream mode

In Bypass-to-stream mode, the FIFO begins operating in Bypass mode and once a trigger event occurs (related to INT1_CFG (30h) register events), the FIFO starts operating in Stream mode. Refer to *Figure 10* below.

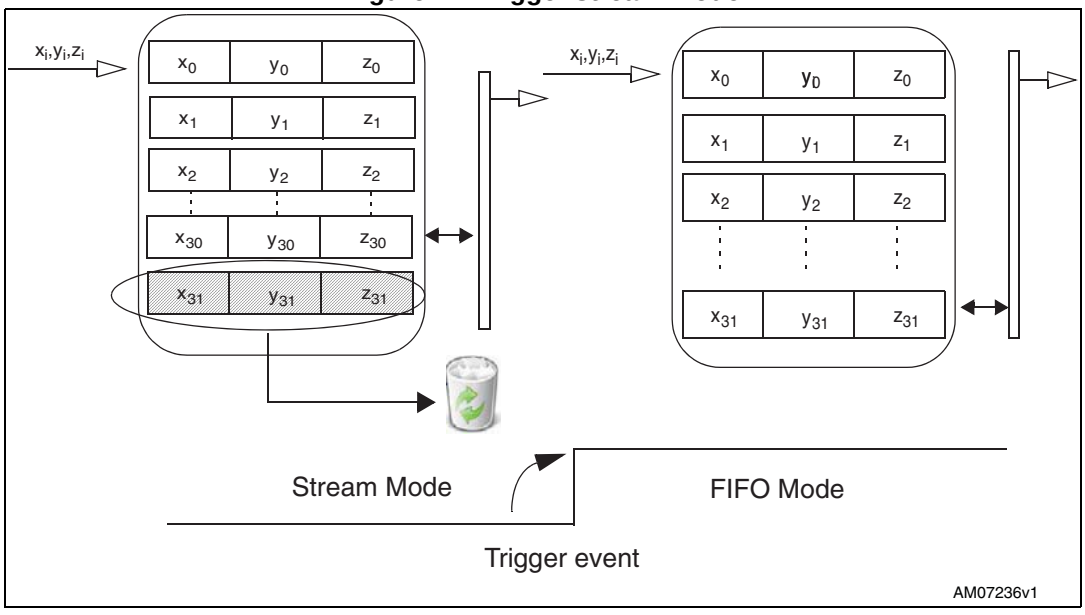
**Figure 10. Bypass-to-stream mode**




### 4.2.5 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from yaw, pitch and roll measurement is stored in the FIFO. A watermark interrupt can be enabled on pin DRDY/INT2 by setting the I2_WTM bit in CTRL_REG3 (22h) in order to be raised when the FIFO is filled to the level specified in the WTM4:0 bits of FIFO_CTRL_REG (2Eh). The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Once a trigger event occurs (related to INT1_CFG (30h) register events), the FIFO starts operating in FIFO mode. Refer to *Figure 11* below.

**Figure 11. Trigger stream mode**



### 4.2.6 Retrieve data from FIFO

FIFO data is read through OUT_X (Addr reg 28h,29h), OUT_Y (Addr reg 2Ah,2Bh) and OUT_Z (Addr reg 2Ch,2Dh). When the FIFO is in Stream, Trigger or FIFO mode, a read operation of the OUT_X, OUT_Y or OUT_Z registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest pitch, roll and yaw data is placed in the OUT_X, OUT_Y and OUT_Z registers and both single read and read_burst (X,Y & Z with auto-incrementing address) operations can be used. When data included in OUT_Z_H (2Dh) is read, the system restarts to read information from addr OUT_X_L (28h).

# 5 Digital interfaces

The registers embedded in the L3GD20 may be accessed through both the $I^2C$ and SPI serial interfaces. The latter may be SW-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the $I^2C$ interface, the CS line must be tied high (i.e connected to Vdd_IO).

**Table 10. Serial interface pin description**

| Pin name | Pin description |
|---|---|
| CS | $I^2C$/SPI mode selection (1: SPI idle mode / $I^2C$ communication enabled; 0: SPI communication mode / $I^2C$ disabled) |
| SCL/SPC | $I^2C$ serial clock (SCL)<br>SPI serial port clock (SPC) |
| SDA/SDI/SDO | $I^2C$ serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| SDO | SPI serial data output (SDO)<br>$I^2C$ less significant bit of the device address |

## 5.1 $I^2C$ serial interface

The L3GD20 $I^2C$ is a bus slave. The $I^2C$ is employed to write data into registers whose content can also be read back.

The relevant $I^2C$ terminology is given in the table below.

**Table 11. $I^2C$ terminology**

| Term | Description |
|---|---|
| Transmitter | The device which sends data to the bus |
| Receiver | The device which receives data from the bus |
| Master | The device which initiates a transfer, generates clock signals and terminates a transfer |
| Slave | The device addressed by the master |

There are two signals associated with the $I^2C$ bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both lines are high.

The $I^2C$ interface is compliant with fast mode (400 kHz) $I^2C$ standards as well as with normal mode.

### 5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave ADdress (SAD) associated with the L3GD20 is 110101xb. The **SDO** pin can be used to modify the less significant bit of the device address. If the SDO pin is connected to voltage supply, LSb is '1' (address 1101011b). Otherwise, if the SDO pin is connected to ground, the LSb value is '0' (address 1101010b). This solution allows to connect and address two different gyroscopes to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obligated to generate an acknowledge after each byte of data received.

The I²C embedded in the L3GD20 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted: the 7 LSb represent the actual register address while the MSb enables address auto-increment. If the MSb of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 12* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

**Table 12. SAD+read/write patterns**

| Command | SAD[6:1] | SAD[0] = SDO | R/W | SAD+R/W |
|---|---|---|---|---|
| Read | 110101 | 0 | 1 | 11010101 (D5) |
| Write | 110101 | 0 | 0 | 11010100 (D4) |
| Read | 110101 | 1 | 1 | 11010111 (D7) |
| Write | 110101 | 1 | 0 | 11010110 (D6) |

**Table 13. Transfer when master is writing one byte to slave**

| Master | ST | SAD + W | | SUB | | DATA | | SP |
|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | SAK | |

**Table 14. Transfer when master is writing multiple bytes to slave**

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | DATA | | DATA | | SP |
| Slave | | | SAK | | SAK | | SAK | | SAK | |

**Table 15. Transfer when master is receiving (reading) one byte of data from slave**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | SR | SAD + R | | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | |

**Table 16. Transfer when master is receiving (reading) multiple bytes of data from slave**

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD+W | | SUB | | SR | SAD+R | | | MAK | | MAK | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | DATA | | DATA | | |

Data is transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes sent per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL, LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to ‘1’ while SUB(6-0) represents the address of the first register to be read.

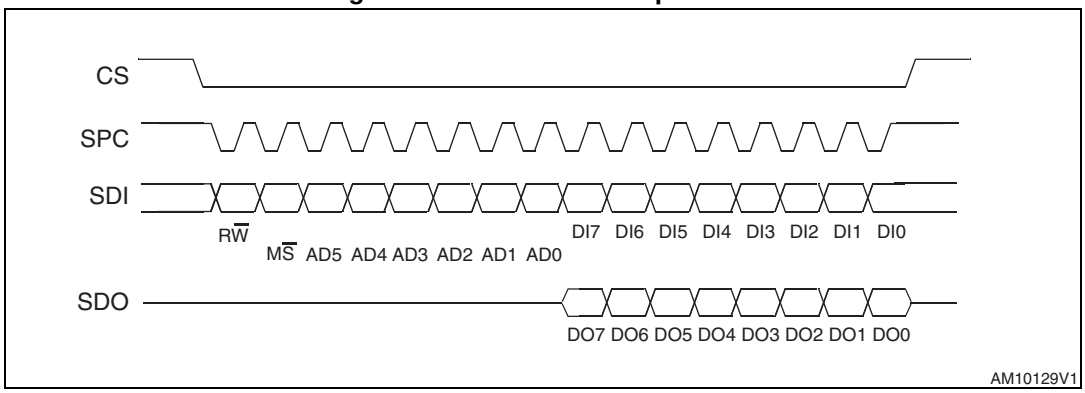
In the communication format presented, MAK is Master Acknowledge and NMAK is No Master Acknowledge.

## 5.2 SPI bus interface

The SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

**Figure 12. Read and write protocol**




**CS** is the Serial Port Enable and is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

***bit 0***: R$\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

***bit 1***: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address will be auto-incremented in multiple read/write commands.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

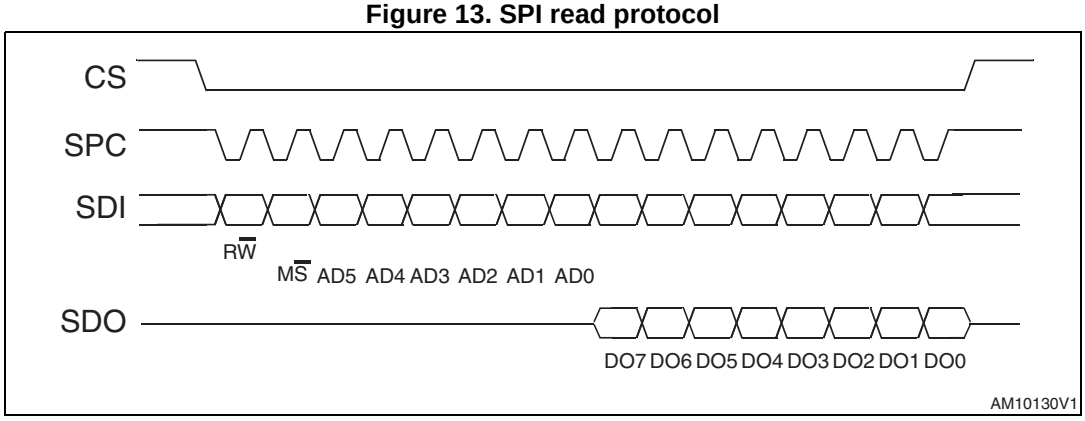
***bit 8-15***: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods will be added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

### 5.2.1 SPI read

**Figure 13. SPI read protocol**




The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

***bit 0***: READ bit. The value is 1.

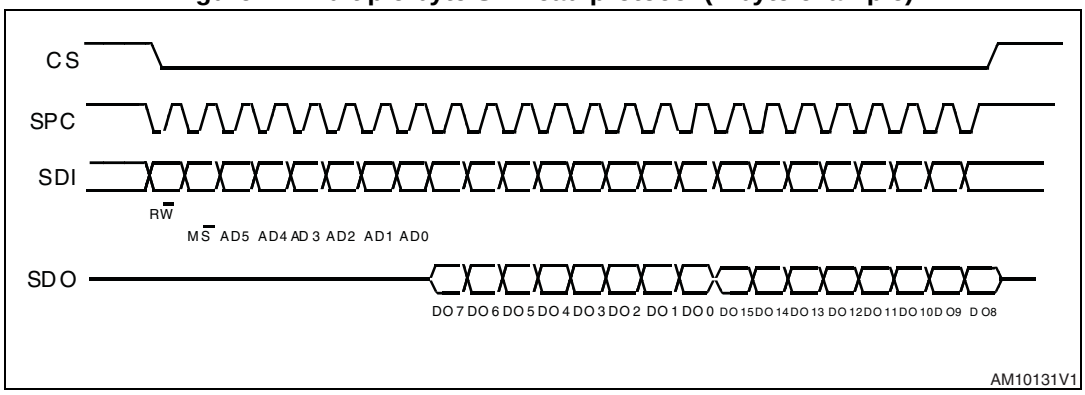
***bit 1***: MS bit. When 0 do not increment address; when 1 increment address in multiple reading.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

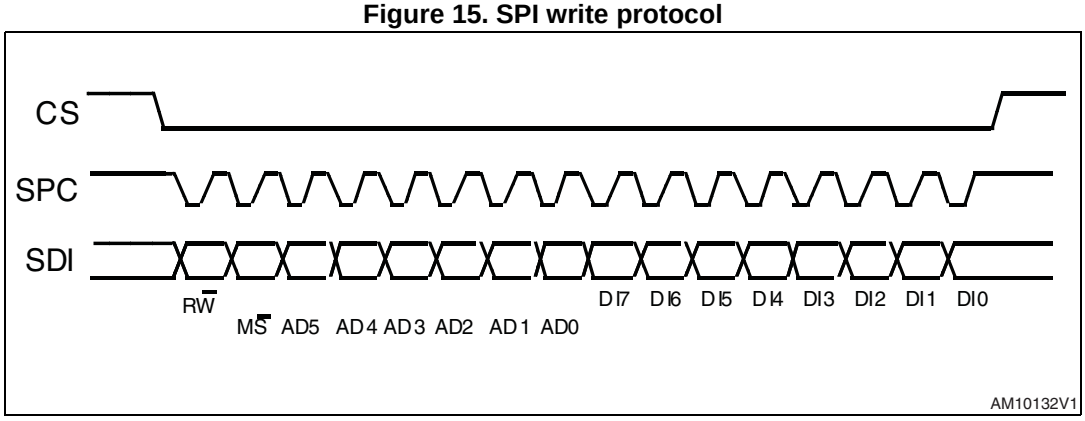
***bit 16-...*** : data DO(...-8). Further data in multiple byte reading.

**Figure 14. Multiple byte SPI read protocol (2-byte example)**



### 5.2.2 SPI write

**Figure 15. SPI write protocol**




The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

***bit 0***: WRITE bit. The value is 0.

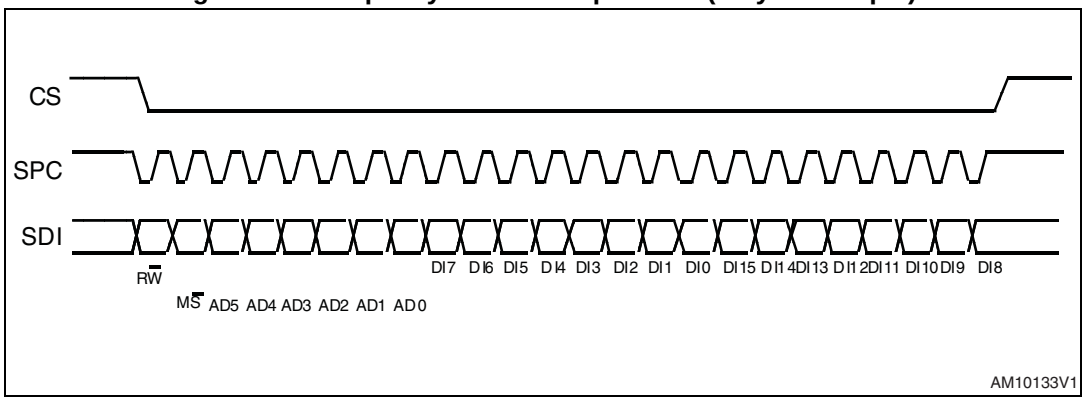
***bit 1***: $\overline{MS}$ bit. When 0, do not increment address; when 1, increment address in multiple writing.

***bit 2 -7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

***bit 16-...*** : data DI(...-8). Further data in multiple byte writing.

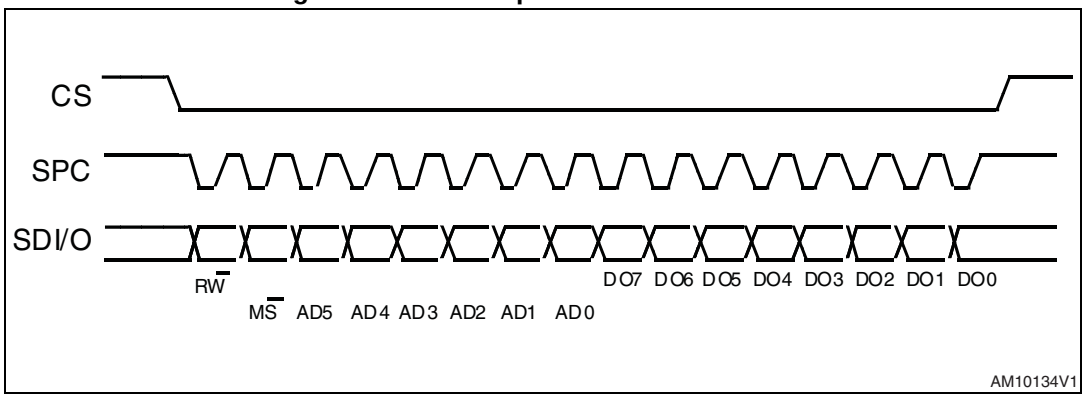
**Figure 16. Multiple byte SPI write protocol (2-byte example)**




### 5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the bit SIM (SPI serial interface mode selection) to ‘1’ in CTRL_REG2.

**Figure 17. SPI read protocol in 3-wire mode**




The SPI Read command is performed with 16 clock pulses:

***bit 0***: READ bit. The value is 1.

***bit 1***: $\overline{MS}$ bit. When 0, do not increment address; when 1, increment address in multiple reading.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wire mode.

# 6 Output register mapping

The table below provides a listing of the 8-bit registers embedded in the device, and the related addresses:

**Table 17. Register address map**

| Name | Type | Register address | | Default |
|---|---|---|---|---|
| | | Hex | Binary | |
| Reserved | - | 00-0E | - | - |
| WHO_AM_I | r | 0F | 000 1111 | 11010100 |
| Reserved | - | 10-1F | - | - |
| CTRL_REG1 | rw | 20 | 010 0000 | 00000111 |
| CTRL_REG2 | rw | 21 | 010 0001 | 00000000 |
| CTRL_REG3 | rw | 22 | 010 0010 | 00000000 |
| CTRL_REG4 | rw | 23 | 010 0011 | 00000000 |
| CTRL_REG5 | rw | 24 | 010 0100 | 00000000 |
| REFERENCE | rw | 25 | 010 0101 | 00000000 |
| OUT_TEMP | r | 26 | 010 0110 | output |
| STATUS_REG | r | 27 | 010 0111 | output |
| OUT_X_L | r | 28 | 010 1000 | output |
| OUT_X_H | r | 29 | 010 1001 | output |
| OUT_Y_L | r | 2A | 010 1010 | output |
| OUT_Y_H | r | 2B | 010 1011 | output |
| OUT_Z_L | r | 2C | 010 1100 | output |
| OUT_Z_H | r | 2D | 010 1101 | output |
| FIFO_CTRL_REG | rw | 2E | 010 1110 | 00000000 |
| FIFO_SRC_REG | r | 2F | 010 1111 | output |
| INT1_CFG | rw | 30 | 011 0000 | 00000000 |
| INT1_SRC | r | 31 | 011 0001 | output |
| INT1_TSH_XH | rw | 32 | 011 0010 | 00000000 |
| INT1_TSH_XL | rw | 33 | 011 0011 | 00000000 |
| INT1_TSH_YH | rw | 34 | 011 0100 | 00000000 |
| INT1_TSH_YL | rw | 35 | 011 0101 | 00000000 |
| INT1_TSH_ZH | rw | 36 | 011 0110 | 00000000 |
| INT1_TSH_ZL | rw | 37 | 011 0111 | 00000000 |
| INT1_DURATION | rw | 38 | 011 1000 | 00000000 |

Registers marked as *Reserved* must not be changed. Writing to these registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

# 7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

## 7.1 WHO_AM_I (0Fh)

**Table 18. WHO_AM_I register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |

Device identification register.

## 7.2 CTRL_REG1 (20h)

**Table 19. CTRL_REG1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DR1 | DR0 | BW1 | BW0 | PD | Zen | Xen | Yen |

**Table 20. CTRL_REG1 description**

| | |
|---|---|
| DR1-DR0 | Output data rate selection. Refer to *Table 21* |
| BW1-BW0 | Bandwidth selection. Refer to *Table 21* |
| PD | Power-down mode enable. Default value: 0<br>(0: power-down mode, 1: normal mode or sleep mode) |
| Zen | Z axis enable. Default value: 1<br>(0: Z axis disabled; 1: Z axis enabled) |
| Yen | Y axis enable. Default value: 1<br>(0: Y axis disabled; 1: Y axis enabled) |
| Xen | X axis enable. Default value: 1<br>(0: X axis disabled; 1: X axis enabled) |

**DR<1:0>** is used for ODR selection. **BW <1:0>** is used for Bandwidth selection.

In the *Table 21* all frequencies resulting in combinations of DR / BW bits are reported.

**Table 21. DR and BW configuration setting**

| DR <1:0> | BW <1:0> | ODR [Hz] | Cut-Off |
|---|---|---|---|
| 00 | 00 | 95 | 12.5 |
| 00 | 01 | 95 | 25 |
| 00 | 10 | 95 | 25 |

Table 21. DR and BW configuration setting (continued)

| DR <1:0> | BW <1:0> | ODR [Hz] | Cut-Off |
|---|---|---|---|
| 00 | 11 | 95 | 25 |
| 01 | 00 | 190 | 12.5 |
| 01 | 01 | 190 | 25 |
| 01 | 10 | 190 | 50 |
| 01 | 11 | 190 | 70 |
| 10 | 00 | 380 | 20 |
| 10 | 01 | 380 | 25 |
| 10 | 10 | 380 | 50 |
| 10 | 11 | 380 | 100 |
| 11 | 00 | 760 | 30 |
| 11 | 01 | 760 | 35 |
| 11 | 10 | 760 | 50 |
| 11 | 11 | 760 | 100 |

A combination of **PD, Zen, Yen, Xen** is used to set device to different modes (power-down / normal / sleep mode) in accordance with *Table 22* below.

Table 22. Power mode selection configuration

| Mode | PD | Zen | Yen | Xen |
|---|---|---|---|---|
| Power-down | 0 | - | - | - |
| Sleep | 1 | 0 | 0 | 0 |
| Normal | 1 | - | - | - |

## 7.3 CTRL_REG2 (21h)

Table 23. CTRL_REG2 register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0(1) | 0(1) | HPM1 | HPM0 | HPCF3 | HPCF2 | HPCF1 | HPCF0 |

1. These bits must be set to ‘0’ to ensure proper operation of the device

Table 24. CTRL_REG2 description

| | |
|---|---|
| HPM1-HPM0 | High-pass filter mode selection. Default value: 00<br>Refer to *Table 25* |
| HPCF3-HPCF0 | High-pass filter cutoff frequency selection<br>Refer to *Table 26* |

Table 25. High-pass filter mode configuration

| HPM1 | HPM0 | High-pass filter mode |
|---|---|---|
| 0 | 0 | Normal mode (reset reading HP_RESET_FILTER) |
| 0 | 1 | Reference signal for filtering |
| 1 | 0 | Normal mode |
| 1 | 1 | Autoreset on interrupt event |

Table 26. High-pass filter cut off frequency configuration [Hz]

| HPCF3-0 | ODR=95 Hz | ODR=190 Hz | ODR=380 Hz | ODR=760 Hz |
|---|---|---|---|---|
| 0000 | 7.2 | 13.5 | 27 | 51.4 |
| 0001 | 3.5 | 7.2 | 13.5 | 27 |
| 0010 | 1.8 | 3.5 | 7.2 | 13.5 |
| 0011 | 0.9 | 1.8 | 3.5 | 7.2 |
| 0100 | 0.45 | 0.9 | 1.8 | 3.5 |
| 0101 | 0.18 | 0.45 | 0.9 | 1.8 |
| 0110 | 0.09 | 0.18 | 0.45 | 0.9 |
| 0111 | 0.045 | 0.09 | 0.18 | 0.45 |
| 1000 | 0.018 | 0.045 | 0.09 | 0.18 |
| 1001 | 0.009 | 0.018 | 0.045 | 0.09 |

## 7.4 CTRL_REG3 (22h)

Table 27. CTRL_REG1 register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| I1_Int1 | I1_Boot | H_Lactive | PP_OD | I2_DRDY | I2_WTM | I2_ORun | I2_Empty |

Table 28. CTRL_REG3 description

| | |
|---|---|
| I1_Int1 | Interrupt enable on INT1 pin. Default value 0. (0: disable; 1: enable) |
| I1_Boot | Boot status available on INT1. Default value 0. (0: disable; 1: enable) |
| H_Lactive | Interrupt active configuration on INT1. Default value 0. (0: high; 1:low) |
| PP_OD | Push-pull / Open drain. Default value: 0. (0: push- pull; 1: open drain) |
| I2_DRDY | Date-ready on DRDY/INT2. Default value 0. (0: disable; 1: enable) |
| I2_WTM | FIFO watermark interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable) |
| I2_ORun | FIFO overrun interrupt on DRDY/INT2 Default value: 0. (0: disable; 1: enable) |
| I2_Empty | FIFO empty interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable) |

## 7.5 CTRL_REG4 (23h)

**Table 29. CTRL_REG4 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BDU | BLE | FS1 | FS0 | - | 0(1) | 0(1) | SIM |

1. This value must not be changed.

**Table 30. CTRL_REG4 description**

| | |
|---|---|
| BDU | Block data update. Default value: 0<br>(0: continuos update; 1: output registers not updated until MSb and LSb reading) |
| BLE | Big/little endian data selection. Default value 0.<br>(0: Data LSb @ lower address; 1: Data MSb @ lower address) |
| FS1-FS0 | Full scale selection. Default value: 00<br>(00: 250 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps) |
| SIM | SPI serial interface mode selection. Default value: 0<br>(0: 4-wire interface; 1: 3-wire interface). |

## 7.6 CTRL_REG5 (24h)

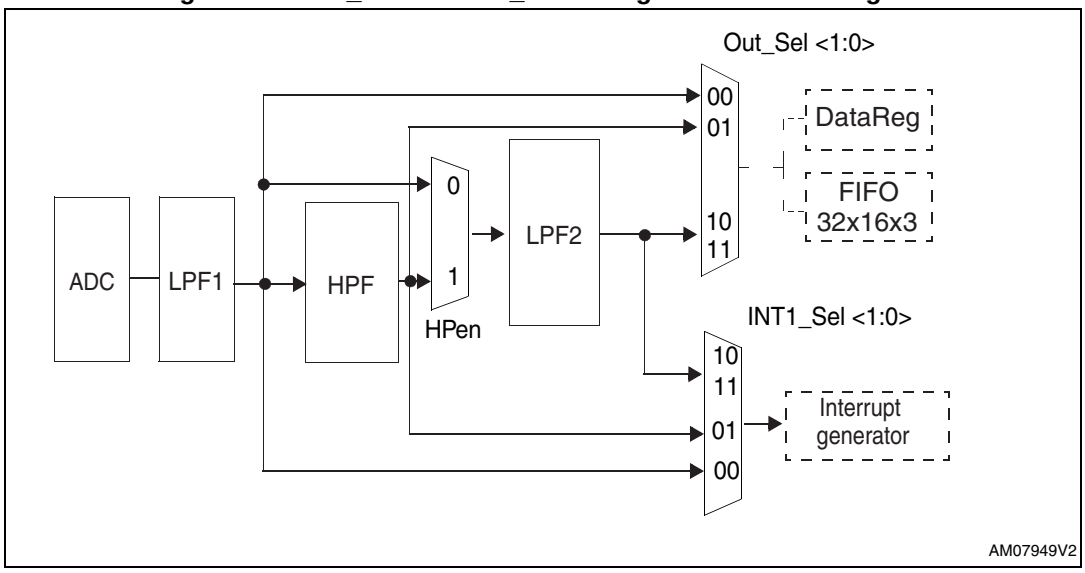
**Table 31. CTRL_REG5 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BOOT | FIFO_EN | -- | HPen | INT1_Sel1 | INT1_Sel0 | Out_Sel1 | Out_Sel0 |

**Table 32. CTRL_REG5 description**

| | |
|---|---|
| BOOT | Reboot memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content) |
| FIFO_EN | FIFO enable. Default value: 0<br>(0: FIFO disable; 1: FIFO Enable) |
| HPen | High-pass filter enable. Default value: 0<br>(0: HPF disabled; 1: HPF enabled See Figure 20) |
| INT1_Sel1-INT1_-Sel0 | INT1 selection configuration. Default value: 0<br>(See *Figure 20*) |
| Out_Sel1-Out_-Sel1 | Out selection configuration. Default value: 0<br>(See *Figure 20*) |

Figure 18. INT1_Sel and Out_Sel configuration block diagram




## 7.7 REFERENCE/DATACAPTURE (25h)

Table 33. REFERENCE register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Ref7 | Ref6 | Ref5 | Ref4 | Ref3 | Ref2 | Ref1 | Ref0 |

Table 34. REFERENCE register description

| | |
|---|---|
| Ref 7-Ref0 | Reference value for interrupt generation. Default value: 0 |

## 7.8 OUT_TEMP (26h)

Table 35. OUT_TEMP register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Temp7 | Temp6 | Temp5 | Temp4 | Temp3 | Temp2 | Temp1 | Temp0 |

Table 36. OUT_TEMP register description

| | |
|---|---|
| Temp7-Temp0 | Temperature data |

Temperature data (1LSB/deg - 8-bit resolution). The value is expressed as two's complement.

## 7.9 STATUS_REG (27h)

**Table 37. STATUS_REG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ZYXOR | ZOR | YOR | XOR | ZYXDA | ZDA | YDA | XDA |

**Table 38. STATUS_REG description**

| | |
|---|---|
| ZYXOR | X, Y, Z -axis data overrun. Default value: 0<br>(0: no overrun has occurred; 1: new data has overwritten the previous data before it was read) |
| ZOR | Z axis data overrun. Default value: 0<br>(0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data) |
| YOR | Y axis data overrun. Default value: 0<br>(0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data) |
| XOR | X axis data overrun. Default value: 0<br>(0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data) |
| ZYXDA | X, Y, Z -axis new data available. Default value: 0<br>(0: a new set of data is not yet available; 1: a new set of data is available) |
| ZDA | Z axis new data available. Default value: 0<br>(0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available) |
| YDA | Y axis new data available. Default value: 0<br>(0: new data for the Y-axis is not yet available;1: new data for the Y-axis is available) |
| XDA | X axis new data available. Default value: 0<br>(0: new data for the X-axis is not yet available; 1: new data for the X-axis is available) |

## 7.10 OUT_X_L (28h), OUT_X_H (29h)

X-axis angular rate data. The value is expressed as two’s complement.

## 7.11 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis angular rate data. The value is expressed as two’s complement.

## 7.12 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis angular rate data. The value is expressed as two’s complement.

## 7.13 FIFO_CTRL_REG (2Eh)

**Table 39. REFERENCE register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FM2 | FM1 | FM0 | WTM4 | WTM3 | WTM2 | WTM1 | WTM0 |

Table 40. REFERENCE register description

| | |
|---|---|
| FM2-FM0 | FIFO mode selection. Default value: 00 (see *Table 41*) |
| WTM4-WTM0 | FIFO threshold. Watermark level setting |

Table 41. FIFO mode configuration

| FM2 | FM1 | FM0 | FIFO mode |
|---|---|---|---|
| 0 | 0 | 0 | Bypass mode |
| 0 | 0 | 1 | FIFO mode |
| 0 | 1 | 0 | Stream mode |
| 0 | 1 | 1 | Stream-to-FIFO mode |
| 1 | 0 | 0 | Bypass-to-Stream mode |

## 7.14 FIFO_SRC_REG (2Fh)

Table 42. FIFO_SRC register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| WTM | OVRN | EMPTY | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 |

Table 43. FIFO_SRC register description

| | |
|---|---|
| WTM | Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal or higher than WTM level) |
| OVRN | Overrun bit status.<br>(0: FIFO is not completely filled; 1:FIFO is completely filled) |
| EMPTY | FIFO empty bit.<br>(0: FIFO not empty; 1: FIFO empty) |
| FSS4-FSS1 | FIFO stored data level |

## 7.15 INT1_CFG (30h)

Table 44. INT1_CFG register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AND/OR | LIR | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |

Table 45. INT1_CFG description

| | |
|---|---|
| AND/OR | AND/OR combination of interrupt events. Default value: 0<br>(0: OR combination of interrupt events 1: AND combination of interrupt events |
| LIR | Latch interrupt request. Default value: 0<br>(0: interrupt request not latched; 1: interrupt request latched)<br>Cleared by reading INT1_SRC reg. |
| ZHIE | Enable interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold) |
| ZLIE | Enable interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold) |
| YHIE | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold) |
| YLIE | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold) |
| XHIE | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold) |
| XLIE | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold) |

## 7.16 INT1_SRC (31h)

Interrupt source register. Read only register.

Table 46. INT1_SRC register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | IA | ZH | ZL | YH | YL | XH | XL |

Table 47. INT1_SRC description

| | |
|---|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred) |
| ZL | Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred) |
| YH | Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred) |
| YL | Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred) |
| XH | X high. Default value: 0 (0: no interrupt, 1: X High event has occurred) |
| XL | X low. Default value: 0 (0: no interrupt, 1: X Low event has occurred) |

Reading at this address clears INT1_SRC IA bit (and eventually the interrupt signal on the INT1 pin) and allows the refresh of data in the INT1_SRC register if the latched option was chosen.

## 7.17 INT1_THS_XH (32h)

**Table 48. INT1_THS_XH register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| - | THSX14 | THSX13 | THSX12 | THSX11 | THSX10 | THSX9 | THSX8 |

**Table 49. INT1_THS_XH description**

| | |
|---|---|
| THSX14 - THSX9 | Interrupt threshold. Default value: 0000 0000 |

## 7.18 INT1_THS_XL (33h)

**Table 50. INT1_THS_XL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| THSX7 | THSX6 | THSX5 | THSX4 | THSX3 | THSX2 | THSX1 | THSX0 |

**Table 51. INT1_THS_XL description**

| | |
|---|---|
| THSX7 - THSX0 | Interrupt threshold. Default value: 0000 0000 |

## 7.19 INT1_THS_YH (34h)

**Table 52. INT1_THS_YH register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| - | THSY14 | THSY13 | THSY12 | THSY11 | THSY10 | THSY9 | THSY8 |

**Table 53. INT1_THS_YH description**

| | |
|---|---|
| THSY14 - THSY9 | Interrupt threshold. Default value: 0000 0000 |

## 7.20 INT1_THS_YL (35h)

**Table 54. INT1_THS_YL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| THSY7 | THSY6 | THSY5 | THSY4 | THSY3 | THSY2 | THSY1 | THSY0 |

**Table 55. INT1_THS_YL description**

| | |
|---|---|
| THSY7 - THSY0 | Interrupt threshold. Default value: 0000 0000 |

## 7.21 INT1_THS_ZH (36h)

**Table 56. INT1_THS_ZH register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| - | THSZ14 | THSZ13 | THSZ12 | THSZ11 | THSZ10 | THSZ9 | THSZ8 |

**Table 57. INT1_THS_ZH description**

| | |
|---|---|
| THSZ14 - THSZ9 | Interrupt threshold. Default value: 0000 0000 |

## 7.22 INT1_THS_ZL (37h)

**Table 58. INT1_THS_ZL register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| THSZ7 | THSZ6 | THSZ5 | THSZ4 | THSZ3 | THSZ2 | THSZ1 | THSZ0 |

**Table 59. INT1_THS_ZL description**

| | |
|---|---|
| THSZ7 - THSZ0 | Interrupt threshold. Default value: 0000 0000 |

## 7.23 INT1_DURATION (38h)

**Table 60. INT1_DURATION register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| WAIT | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 61. INT1_DURATION description**

| | |
|---|---|
| WAIT | WAIT enable. Default value: 0 (0: disable; 1: enable) |
| D6 - D0 | Duration value. Default value: 000 0000 |

The **D6 - D0** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT** bit has the following definitions:

Wait = ‘0’: the interrupt falls immediately if the signal crosses the selected threshold

Wait = ‘1’: if the signal crosses the selected threshold, the interrupt falls only after the duration has counted the number of samples at the selected data rate, written into the duration counter register.

Figure 19. Wait disabled

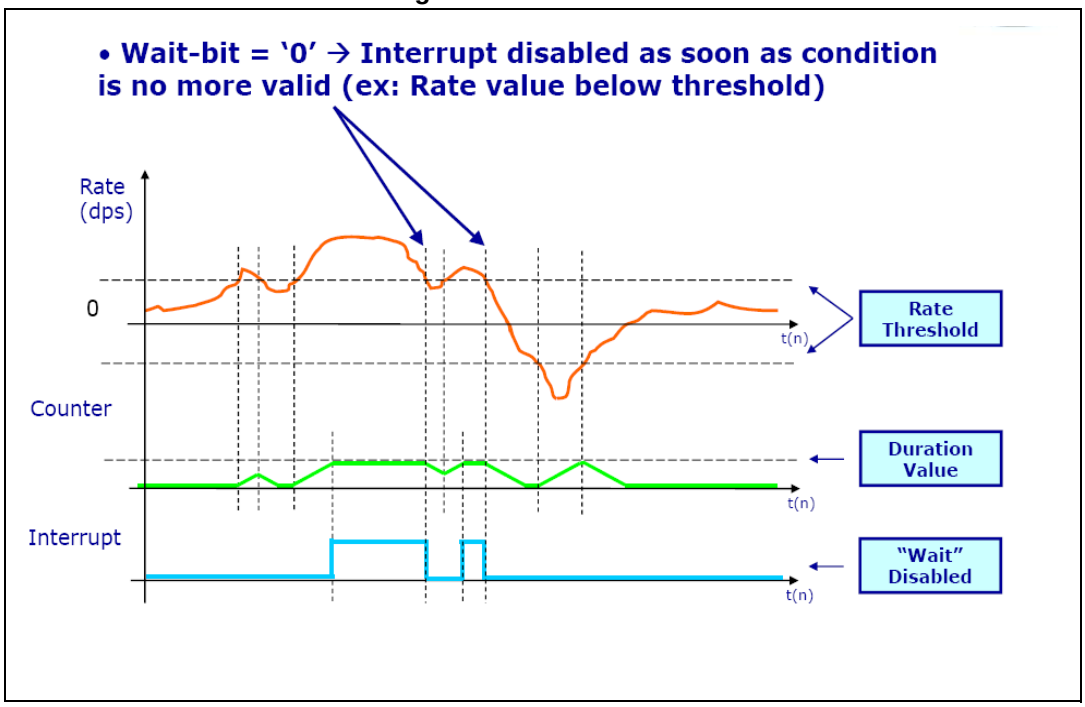
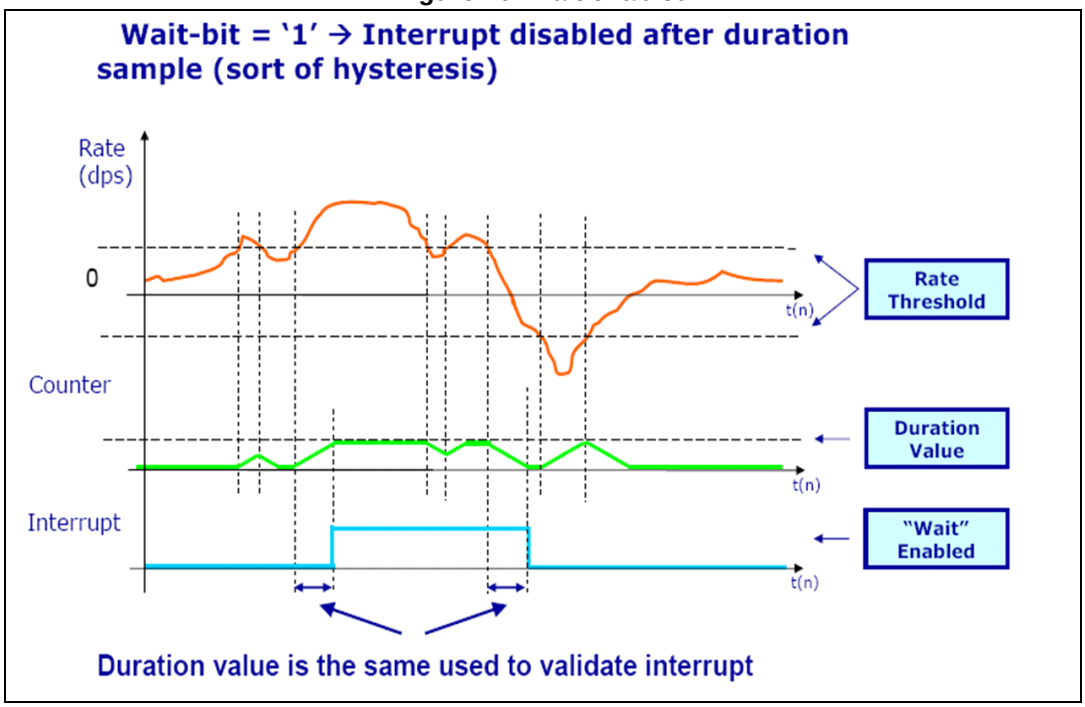



Figure 20. Wait enabled



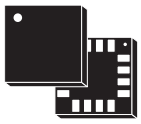
# 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

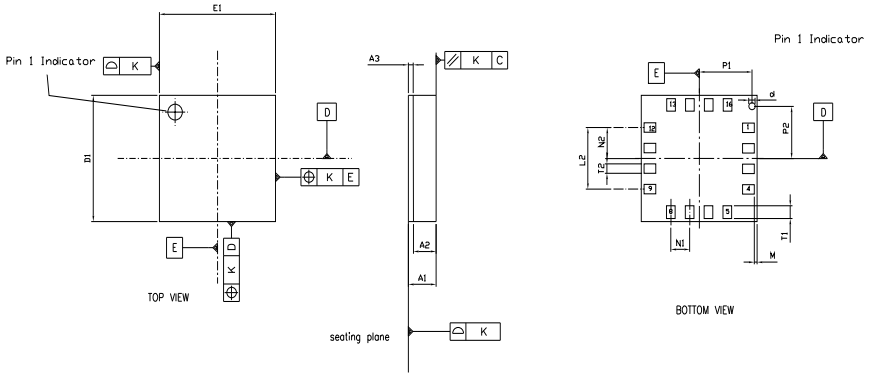
**Figure 21. LGA-16: mechanical data and package dimensions**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | mm | | | inch | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A1 | | | 1.000 | | | 0.0394 |
| A2 | | 0.785 | | | 0.0309 | |
| A3 | | 0.200 | | | 0.0079 | |
| d | | 0.300 | | | 0.0118 | |
| D1 | 3.850 | 4.000 | 4.150 | 0.1516 | 0.1575 | 0.1634 |
| E1 | 3.850 | 4.000 | 4.150 | 0.1516 | 0.1575 | 0.1634 |
| L2 | | 1.950 | | | 0.0768 | |
| M | | 0.100 | | | 0.0039 | |
| N1 | | 0.650 | | | 0.0256 | |
| N2 | | 0.975 | | | 0.0384 | |
| P1 | | 1.750 | | | 0.0689 | |
| P2 | | 1.525 | | | 0.0600 | |
| T1 | | 0.400 | | | 0.0157 | |
| T2 | | 0.300 | | | 0.0118 | |
| k | | 0.050 | | | 0.0020 | |

**Outline and mechanical data**



**LGA-16 (4x4x1mm)**
**Land Grid Array Package**



# 9 Revision history

Table 62. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 18-Aug-2011 | 1 | Initial release. |
| 27-Feb-2013 | 2 | Updated *Table 12: SAD+read/write patterns* and *Table 23: CTRL_REG2 register*. |

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