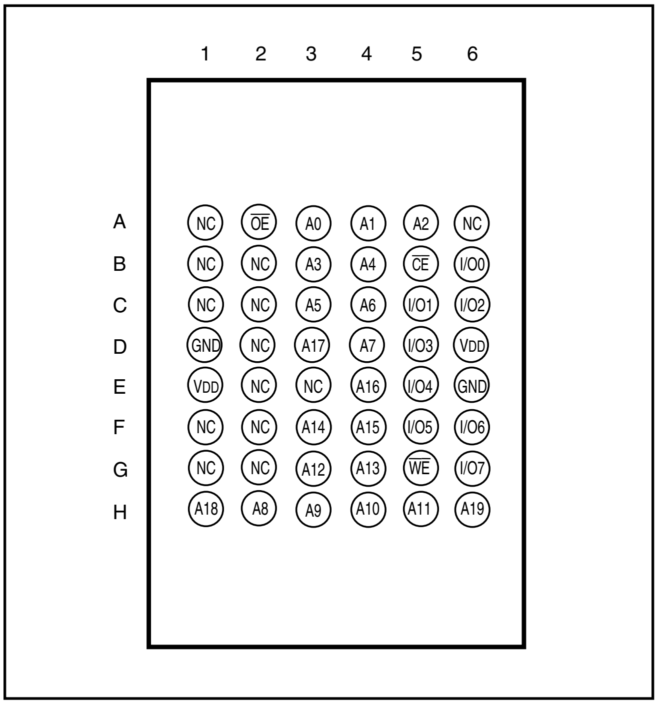
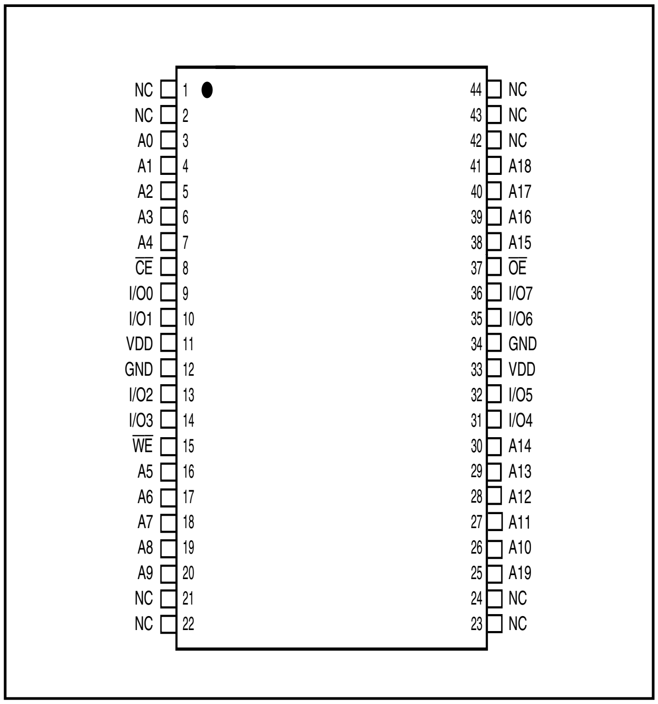
PIN CONFIGURATION

48-pin Mini BGA (M) (9mm x 11mm)



44-pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A19	Address Inputs
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{WE}}$	Write Enable Input
I/O0-I/O7	Data Input / Output
VDD	Power
GND	Ground
NC	No Connection

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{DD} + 0.5	V
V_{DD}	V_{DD} Relates to GND	–0.3 to 4.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

OPERATING RANGE (V_{DD}) (IS61WV10248ALL)

Range	Ambient Temperature	V_{DD} (20 ns)
Commercial	0°C to +70°C	1.65V-2.2V
Industrial	–40°C to +85°C	1.65V-2.2V
Automotive	–40°C to +125°C	1.65V-2.2V

OPERATING RANGE (V_{DD}) (IS61WV10248BLL)(1)

Range	Ambient Temperature	V_{DD} (8 ns)	V_{DD} (10 ns)
Commercial	0°C to +70°C	3.3V ± 5%	2.4V-3.6V
Industrial	–40°C to +85°C	3.3V ± 5%	2.4V-3.6V

Note:

1. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

OPERATING RANGE (V_{DD}) (IS64WV10248BLL)

Range	Ambient Temperature	V_{DD} (10 ns)
Automotive	–40°C to +125°C	2.4V-3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage(1)		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:

1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width ≤ 2 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width ≤ 2 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	1.8	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage(1)		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:

1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width ≤ 2 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width ≤ 2 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.65V-2.2V

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{DD} + 0.2	V
V_{IL}(1)	Input LOW Voltage		1.65-2.2V	–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Note:

1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width ≤ 2 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width ≤ 2 ns). Not 100% tested.

AC TEST CONDITIONS (HIGH SPEED)

Parameter	Unit (2.4V-3.6V)	Unit (3.3V ± 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to V_{DD}-0.3V	0.4V to V_{DD}-0.3V	0.4V to V_{DD}-0.2V
Input Rise and Fall Times	1.5ns	1.5ns	1.5ns
Input and Output Timing and Reference Level (V_{Ref})	V_{DD}/2	V_{DD}/2 + 0.05	V_{DD}/2
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2

AC TEST LOADS

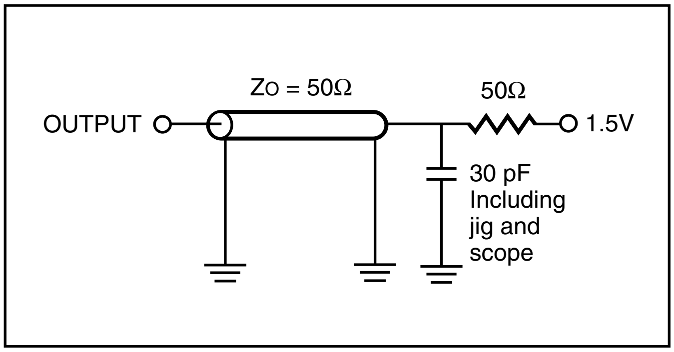


Figure 1.

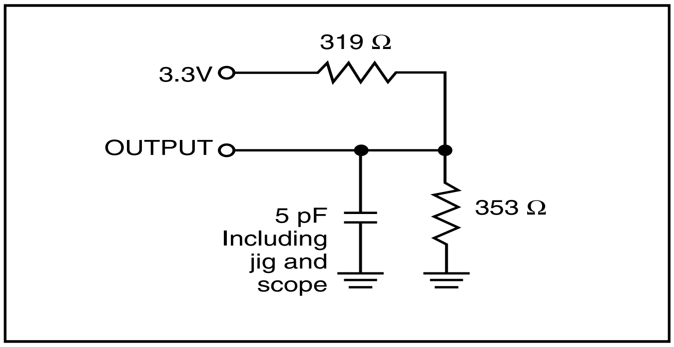


Figure 2.

POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 Min.	-8 Max.	-10 Min.	-10 Max.	-20 Min.	-20 Max.	Unit
I_{CC}	V_{DD} Dynamic Operating	V_{DD} = Max.,	Com.	—	110	—	95	—	90	mA
	Supply Current	I_{OUT} = 0 mA, f = f_{MAX}	Ind.	—	120	—	100	—	100	
			Auto.	—	—	—	140	—	140	
			typ.(2)			60				
$I_{CC}1$	Operating	V_{DD} = Max.,	Com.	—	30	—	30	—	30	mA
	Supply Current	I_{OUT} = 0 mA, f = 0	Ind.	—	35	—	35	—	35	
			Auto.	—	—	—	60	—	70	
I_{SB1}	TTL Standby Current	V_{DD} = Max.,	Com.	—	30	—	30	—	30	mA
	(TTL Inputs)	V_{IN} = V_{IH} or V_{IL}	Ind.	—	35	—	35	—	35	
		$\overline{CE} \geq V_{IH}$, f = 0	Auto.	—	—	—	70	—	70	
I_{SB2}	CMOS Standby	V_{DD} = Max.,	Com.	—	20	—	20	—	15	mA
	Current (CMOS Inputs)	$\overline{CE} \geq V_{DD} - 0.2V$,	Ind.	—	25	—	25	—	20	
		$V_{IN} \geq V_{DD} - 0.2V$, or	Auto.	—	—	—	70	—	70	
		$V_{IN} \leq 0.2V$, f = 0	typ.(2)			4				

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS(1) (Over Operating Range)

		-8		-10		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{RC}	Read Cycle Time	8	—	10	—	ns
t_{AA}	Address Access Time	—	8	—	10	ns
t_{OHA}	Output Hold Time	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5.5	—	6.5	ns
t_{HZOE}(2)	$\overline{OE}$ to High-Z Output	—	3	—	4	ns
t_{LZOE}(2)	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZCE}(2	$\overline{CE}$ to High-Z Output	0	3	0	4	ns
t_{LZCE}(2)	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t_{PU}	Power Up Time	0	—	0	—	ns
t_{PD}	Power Down Time	—	8	—	10	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

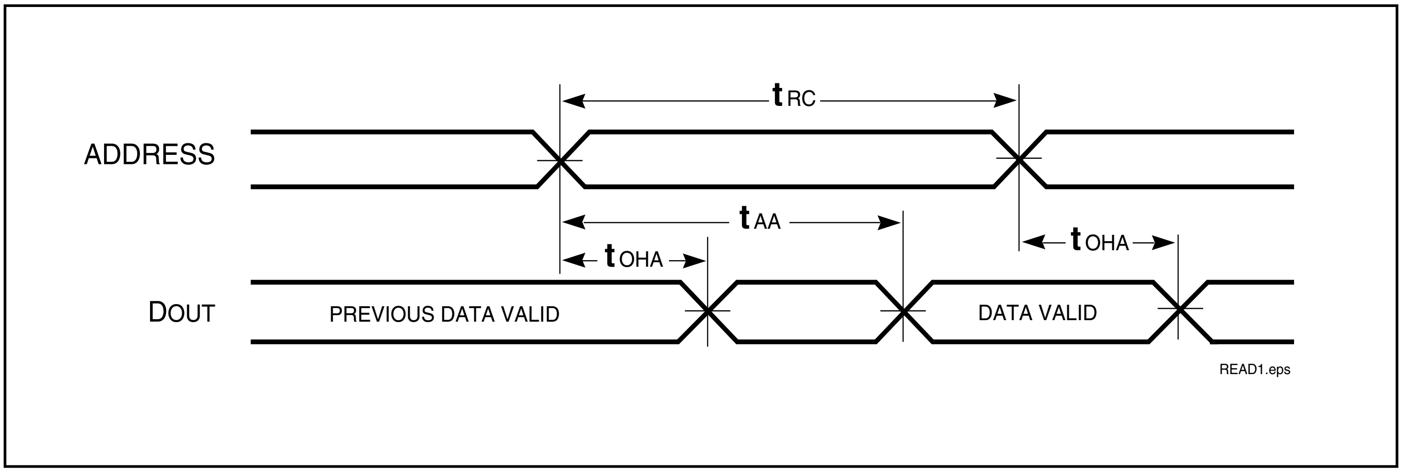
READ CYCLE SWITCHING CHARACTERISTICS(1) (Over Operating Range)

		-20 ns		
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
t_{RC}	Read Cycle Time	20	—	ns
t_{AA}	Address Access Time	—	20	ns
t_{OHA}	Output Hold Time	2.5	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	20	ns
t_{DOE}	$\overline{OE}$ Access Time	—	8	ns
t_{HZOE}(2)	$\overline{OE}$ to High-Z Output	0	8	ns
t_{LZOE}(2)	$\overline{OE}$ to Low-Z Output	0	—	ns
t_{HZCE}(2	$\overline{CE}$ to High-Z Output	0	8	ns
t_{LZCE}(2)	$\overline{CE}$ to Low-Z Output	3	—	ns
t_{PU}	Power Up Time	0	—	ns
t_{PD}	Power Down Time	—	20	ns

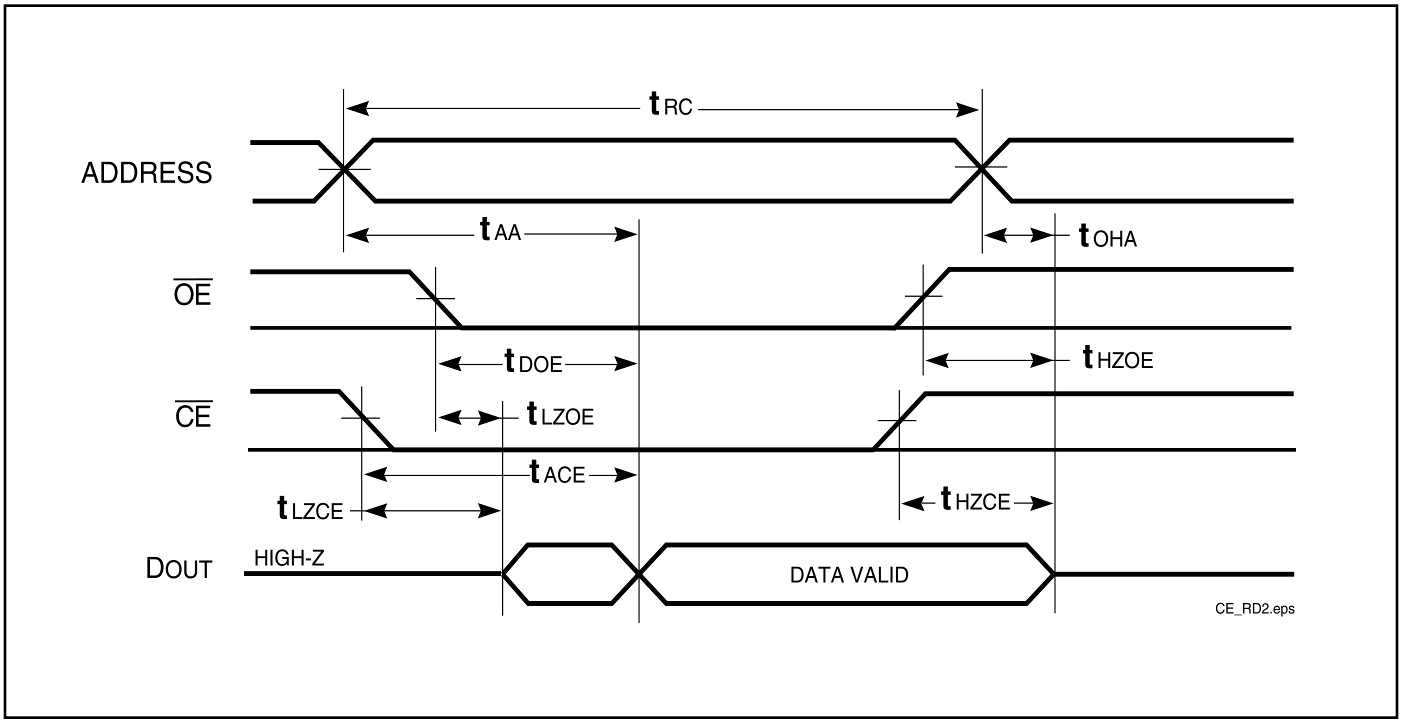
Notes:
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{\text{CE}}$ = $\overline{\text{OE}}$ = V_{IL})



READ CYCLE NO. 2[1,3] ($\overline{\text{CE}}$ and $\overline{\text{OE}}$ Controlled)



Notes:

1. $\overline{\text{WE}}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{\text{CE}}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

		-8		-10		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{WC}	Write Cycle Time	8	—	10	—	ns
t_{SCE}	$\overline{CE}$ to Write End	6.5	—	8	—	ns
t_{AW}	Address Setup Time to Write End	6.5	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	6.5	—	8	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	8.0	—	10	—	ns
t_{SD}	Data Setup to Write End	5	—	6	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}(2)	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	ns
t_{LZWE}(2)	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

WRITE CYCLE SWITCHING CHARACTERISTICS(1,2) (Over Operating Range)

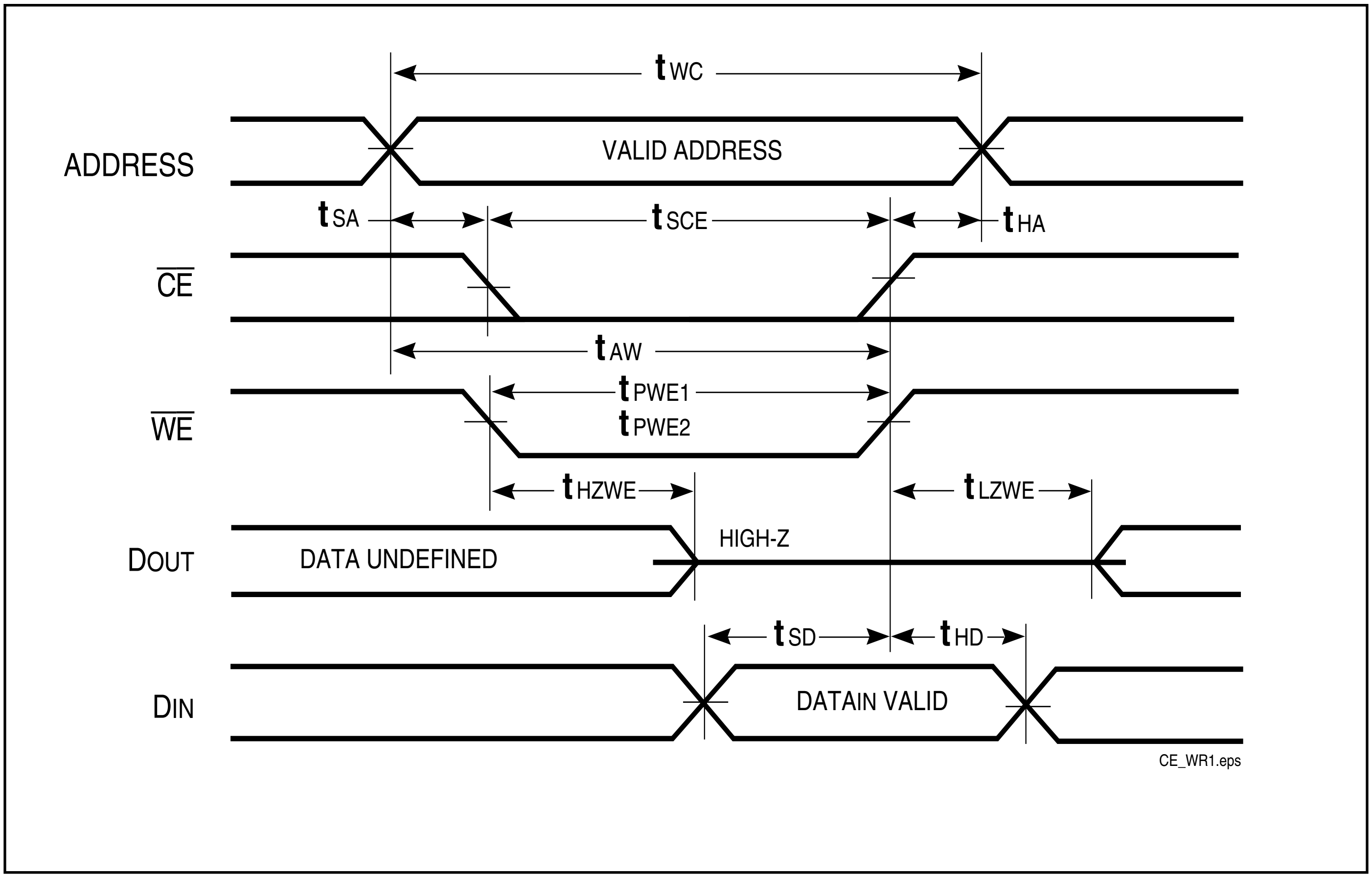
		-20 ns		
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
t_{WC}	Write Cycle Time	20	—	ns
t_{SCE}	$\overline{CE}$ to Write End	12	—	ns
t_{AW}	Address Setup Time to Write End	12	—	ns
t_{HA}	Address Hold from Write End	0	—	ns
t_{SA}	Address Setup Time	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	12	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	17	—	ns
t_{SD}	Data Setup to Write End	9	—	ns
t_{HD}	Data Hold from Write End	0	—	ns
t_{HZWE}(3)	$\overline{WE}$ LOW to High-Z Output	—	9	ns
t_{LZWE}(3)	$\overline{WE}$ HIGH to Low-Z Output	3	—	ns

Notes:

1. Test conditions assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

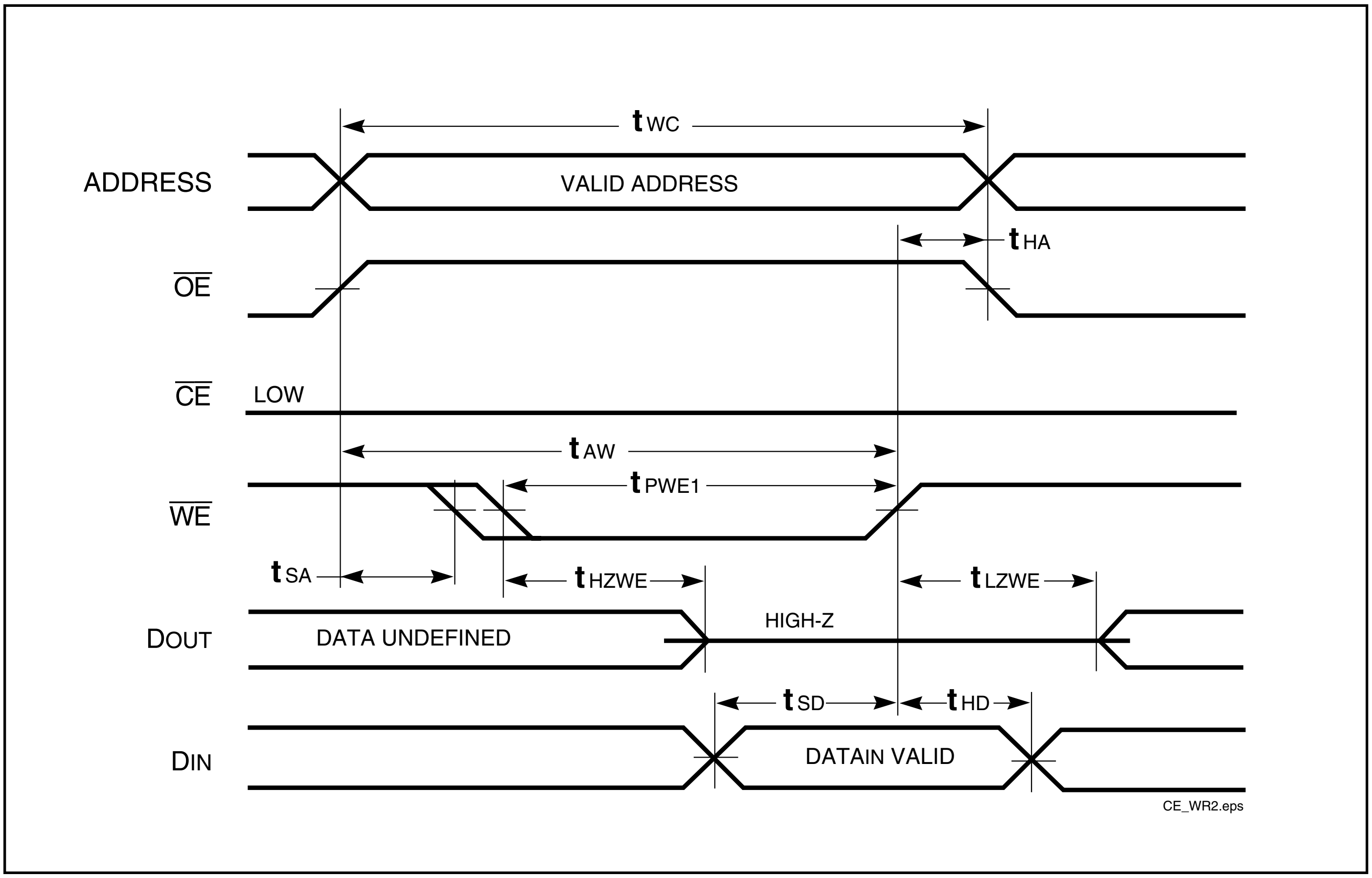
AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)



AC WAVEFORMS

WRITE CYCLE NO. 2[(1,2)] ($\overline{\text{WE}}$ Controlled: $\overline{\text{OE}}$ is HIGH During Write Cycle)

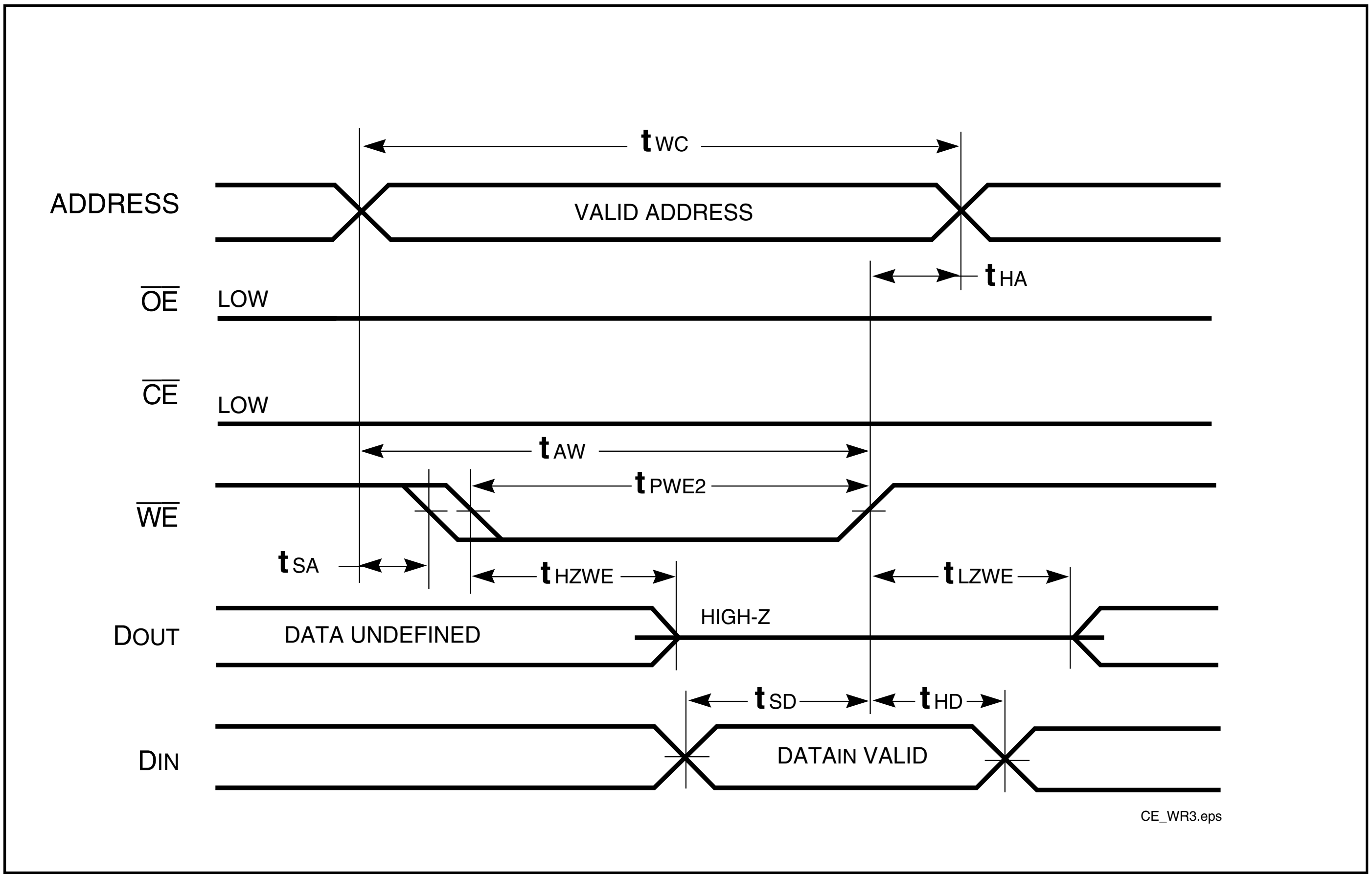


Notes:

1. The internal write time is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{\text{OE}}$ > V_{IH}.

AC WAVEFORMS

WRITE CYCLE NO. 3 ($\overline{\text{WE}}$ Controlled: $\overline{\text{OE}}$ is LOW During Write Cycle)



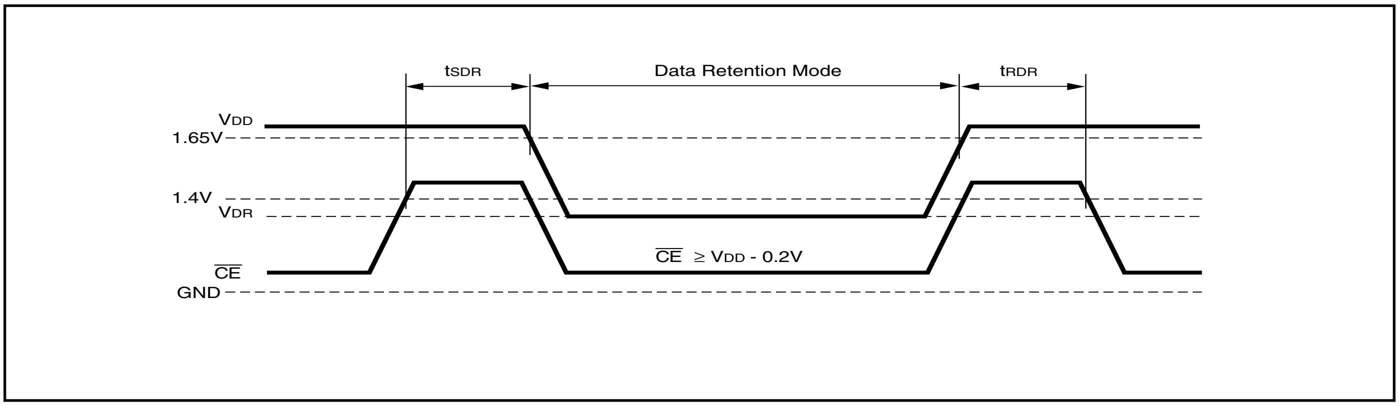
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$	Ind.	—	25	mA
			Auto.	—	70	
			typ.(1)		4	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

Note:

1. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION

Industrial Range: -40°C to +85°C
Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10 (8[1])	IS61WV10248BLL-10MI	48 mini BGA (9mm x 11mm)
	IS61WV10248BLL-10MLI	48 mini BGA (9mm x 11mm), Lead-free
	IS61WV10248BLL-10TI	TSOP (Type II)
	IS61WV10248BLL-10TLI	TSOP (Type II), Lead-free

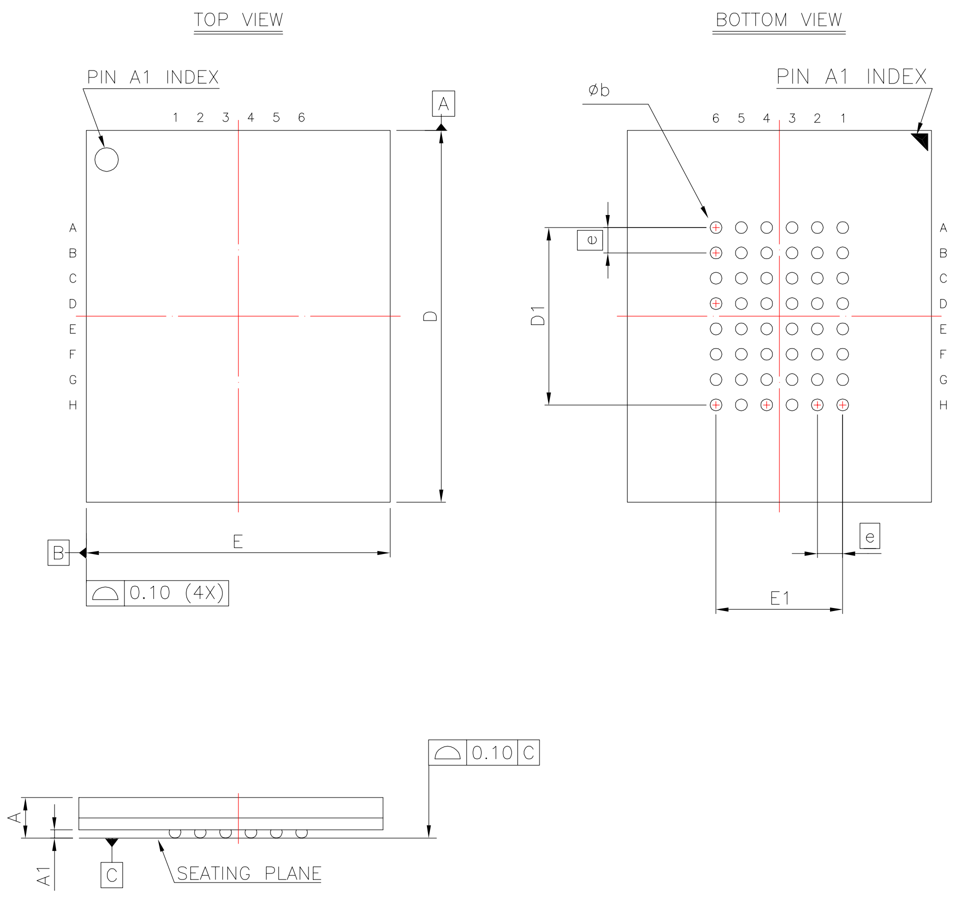
Note:
1. Speed = 8ns for V_{DD} = 3.3V ± 5%. Speed = 10ns for V_{DD} = 2.4V to 3.3V.

Industrial Range: -40°C to +85°C
Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
20	IS61WV10248ALL-20MI	48 mini BGA (9mm x 11mm)
	IS61WV10248ALL-20MLI	48 mini BGA (9mm x 11mm), Lead-free
	IS61WV10248ALL-20TI	TSOP (Type II)

Automotive Range: -40°C to +125°C
Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10	IS64WV10248BLL-10MA3	48 mini BGA (9mm x 11mm)
	IS64WV10248BLL-10TA3	TSOP (Type II)
	IS64WV10248BLL-10CTLA3	TSOP (Type II), Lead-free, Copper Leadframe

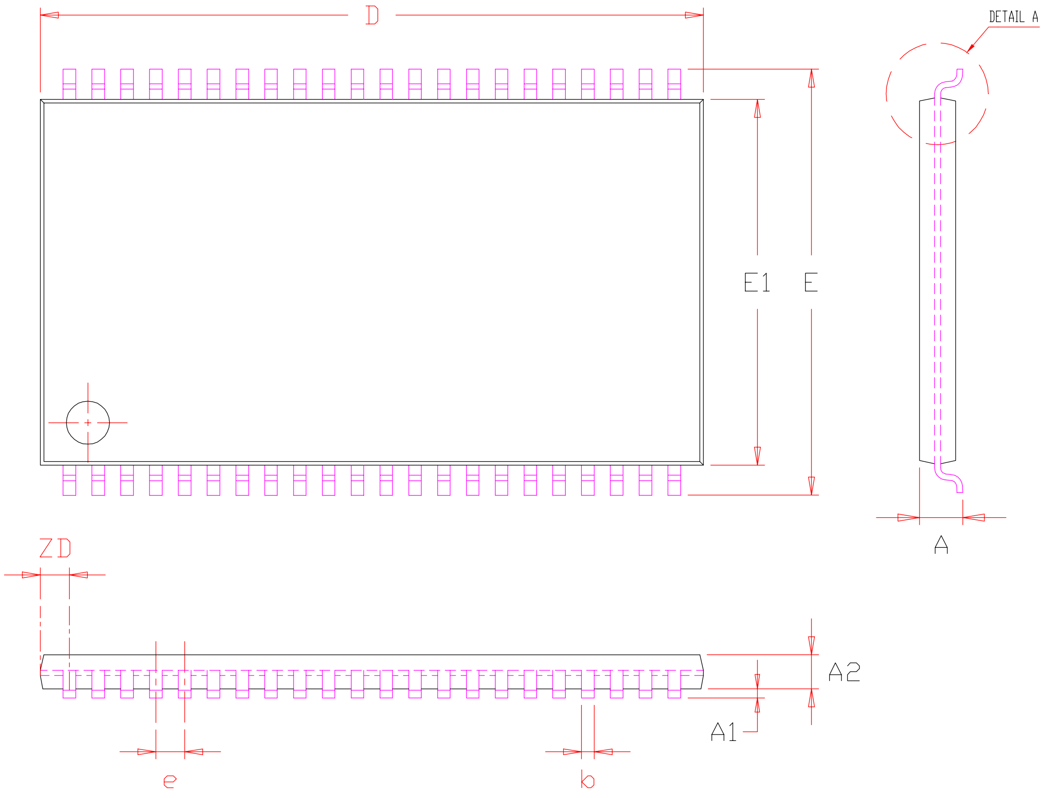


SYM.	DIMENSION (mm)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
b	0.30	0.35	0.40	0.012	0.014	0.016
D	10.90	11.00	11.10	0.429	0.433	0.437
D1	5.25 BSC			0.207 BSC		
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC			0.030 BSC		

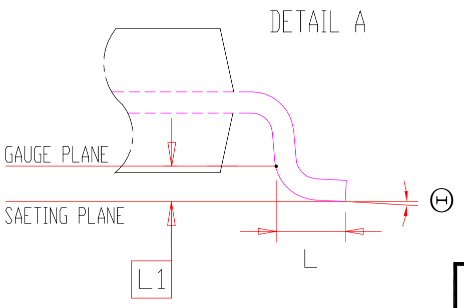
NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

	TITLE	48L 9x11mm TF-BGA Package Outline	REV.	B	DATE	08/21/2008



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	—	0.69	0.016	—	0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
Θ	0	—	8°	0	—	8°



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

	TITLE	44L 400mil TSOP-2 Package Outline	REV.	F	DATE	06/04/2008