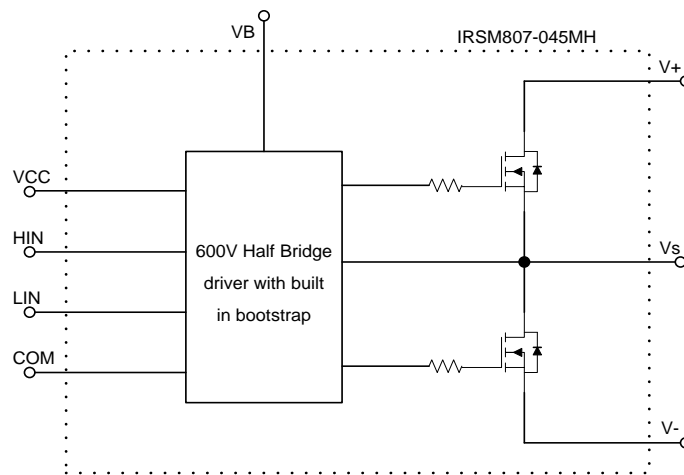


Internal Electrical Schematic



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the module may occur. These are not tested at manufacturing. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The thermal resistance rating is measured under board mounted and still air conditions.

Symbol	Description	Min	Max	Unit
BV_{DSS}	FREDFET Blocking Voltage	---	500	V
I_O @ $T_C=25^\circ\text{C}$	DC Output Current	---	4	A
I_{OP}	Pulsed Output Current (Note 1)	---	35	
P_d	Maximum Power Dissipation per FREDFET @ $T_C=25^\circ\text{C}$	---	50	W
V_{ISO}	Isolation Voltage (1min) (Note 2)	---	1500	V_{RMS}
T_J	Operating Junction Temperature	-40	150	$^\circ\text{C}$
T_L	Lead Temperature (Soldering, 30 seconds)	---	260	$^\circ\text{C}$
T_S	Storage Temperature	-40	150	$^\circ\text{C}$
$V_{S1,2,3}$	High Side Floating Supply Offset Voltage	$V_{B1,2,3} - 20$	$V_{B1,2,3} + 0.3$	V
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	500	V
V_{CC}	Low Side and Logic Supply voltage	-0.3	20	V
V_{IN}	Input Voltage of LIN, HIN	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V

Note 1: Pulse Width = 100 μs , $T_C=25^\circ\text{C}$, Duty=1%.

Note 2: Characterized, not tested at manufacturing.

Recommended Operating Conditions

Symbol	Description	Min	Max	Unit
V^+	Positive DC Bus Input Voltage	---	400	V
$V_{S1,2,3}$	High Side Floating Supply Offset Voltage	(Note 3)	400	V
$V_{B1,2,3}$	High Side Floating Supply Voltage	V_S+12	V_S+20	V
V_{CC}	Low Side and Logic Supply Voltage	12	16.5	V
V_{IN}	Logic Input Voltage	COM	V_{CC}	V
F_p	PWM Carrier Frequency	---	20	kHz

The Input/Output logic diagram is shown in Figure 1. For proper operation the module should be used within the recommended conditions. All voltages are absolute referenced to COM. The V_S offset is tested with all supplies biased at 15V differential.

Note 3: Logic operational for V_S from COM-8V to COM+500V. Logic state held for V_S from COM-8V to COM- V_{BS} .

Static Electrical Characteristics

$(V_{CC}-COM) = (V_B-V_S) = 15V$. $T_A = 25^\circ C$ unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels. The V_{CCUV} parameters are referenced to V_{SS} . The V_{BSUV} parameters are referenced to V_S .

Symbol	Description	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	---	---	V	$T_J=25^\circ C$, $I_{LK}=250\mu A$
I_{LKH}	Leakage Current of High Side FET		10		μA	$T_J=25^\circ C$, $V_{DS}=500V$
I_{LKL}	Leakage Current of Low Side FET Plus Gate Drive IC		15		μA	$T_J=25^\circ C$, $V_{DS}=500V$
$R_{DS(ON)}$	Drain to Source ON Resistance	---	1.5	1.7	Ω	$T_J=25^\circ C$, $V_{CC}=10V$, $I_d = 2A$
		---	3	---		$T_J=150^\circ C$, $V_{CC}=10V$, $I_d = 2A$ (Note 4)
V_{SD}	Diode Forward Voltage	---	0.85	---	V	$T_J=25^\circ C$, $I_d = 2A$
$V_{HIN/LIN}$	Logic "1" input voltage for HIN and LIN	2.2	---	---	V	
$V_{HIN/LIN}$	Logic "0" input voltage for HIN and LIN	---	---	0.8	V	
V_{CCUV+} , V_{BSUV+}	V_{CC} and V_{BS} Supply Under-Voltage, Positive Going Threshold	8	8.9	9.8	V	
V_{CCUV-} , V_{BSUV-}	V_{CC} and V_{BS} supply Under-Voltage, Negative Going Threshold	6.9	7.7	8.5	V	
V_{CCUVH} , V_{BSUVH}	V_{CC} and V_{BS} Supply Under-Voltage Lock-Out Hysteresis	---	0.7	---	V	
I_{QBS}	Quiescent V_{BS} Supply Current $V_{IN}=0V$	---	45	70	μA	
I_{QCC}	Quiescent V_{CC} Supply Current $V_{IN}=0V$	---	1100	3000	μA	
I_{IN+}	Input Bias Current $V_{IN}=4V$	---	5	20	μA	
I_{IN-}	Input Bias Current $V_{IN}=0V$	---	---	2	μA	
R_{BR}	Internal Bootstrap Equivalent Resistor Value	---	200	---	Ω	$T_J=25^\circ C$

Note 4: Characterized, not tested at manufacturing

Dynamic Electrical Characteristics

$(V_{CC}-COM) = (V_B-V_S) = 15\text{ V}$. $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Description	Min	Typ	Max	Units	Conditions
T_{ON}	Input to Output Propagation Turn-On Delay Time	---	0.9	1.5	μs	$I_D=1\text{mA}$, $V^+=50\text{V}$
T_{OFF}	Input to Output Propagation Turn-Off Delay Time	---	0.9	1.5	μs	
DT	Built-in Dead Time	---	300	---	ns	
$T_{FIL,IN}$	Input Filter Time (HIN, LIN)	---	300	---	ns	

FREDFET Avalanche Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
EAS	Single Pulse Avalanche Energy (Note 5)	---	209	---	mJ	$T_J=25^\circ\text{C}$, $L=9.5\text{mH}$, $V_{DD}=150\text{V}$, $I_{AS}=6.7\text{A}$

Note 5: Characterized using TO-220 packaged device

Thermal and Mechanical Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
$R_{th(J-CT)}$	Total Thermal Resistance Junction to Case Top (Note 6)	---	25	---	$^\circ\text{C/W}$	
$R_{th(J-CB)}$	Total Thermal Resistance Junction to Case Bottom (Note 6)	---	1.55	---	$^\circ\text{C/W}$	

Note 6: Calculated

Qualification Information†

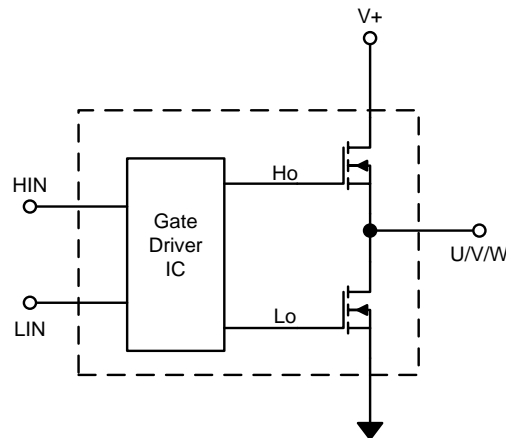
Qualification Level		Industrial ^{††}
Moisture Sensitivity Level		MSL3 ^{†††}
ESD	Machine Model	Class B
	Human Body Model	Class 1C
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Input-Output Logic Level Table



HIN	LIN	U,V,W
HI	LO	V+
LO	HI	0
HI	HI	**
LO	LO	*

* V+ if motor current is flowing into VS, 0 if current is flowing out of VS into the motor winding

** Anti Shoot-through protection active (LO, HO are switched off)

Referenced Figures

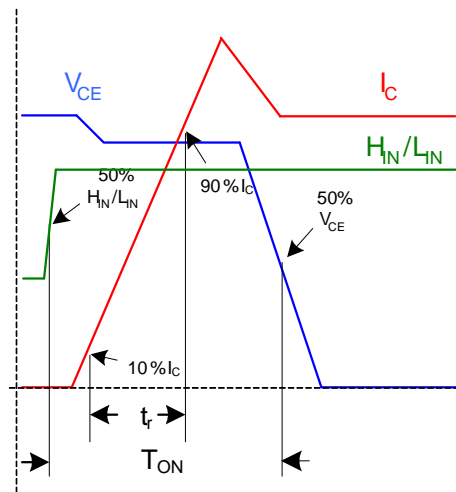


Figure 1a. Input to Output propagation turn-on delay time.

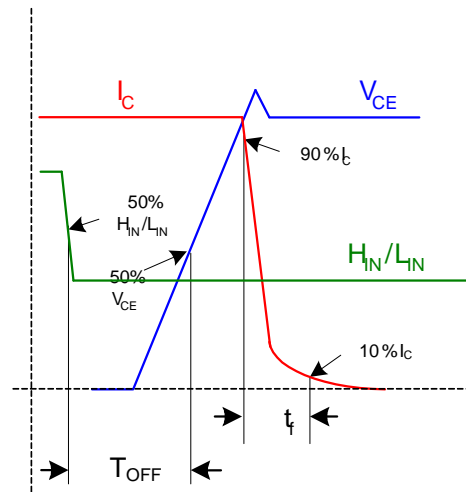


Figure 1b. Input to Output propagation turn-off delay time.

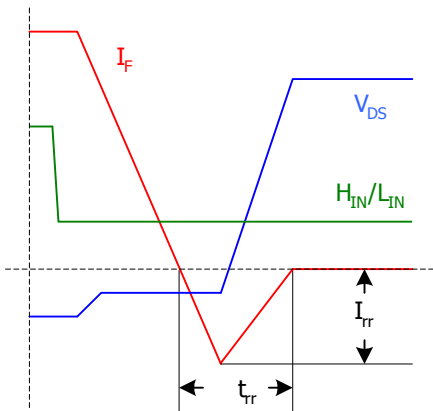
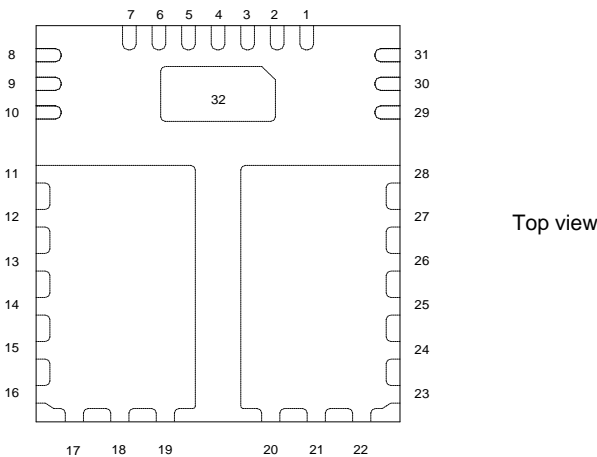


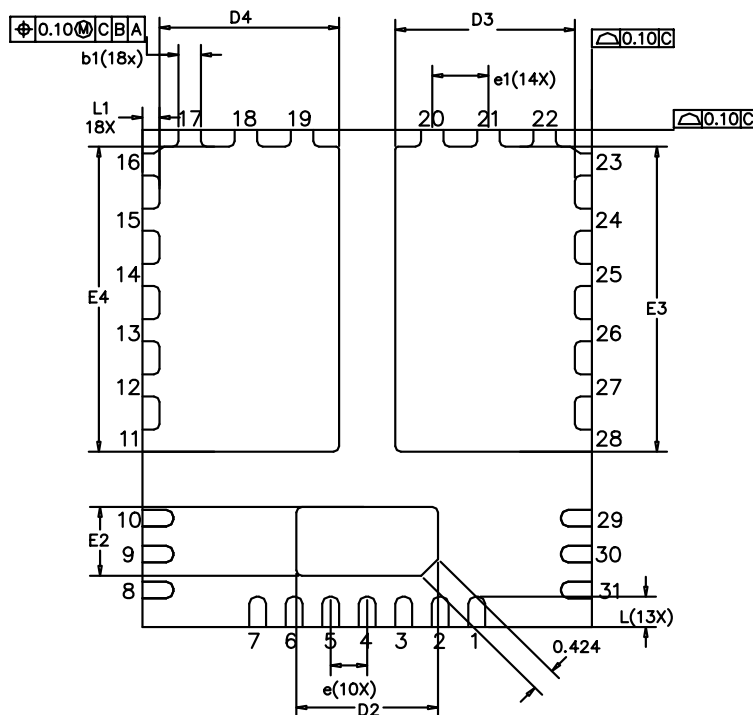
Figure 1c. Diode Reverse Recovery.

Figure 1. Switching Parameter Definitions

Module Pin-Out Description

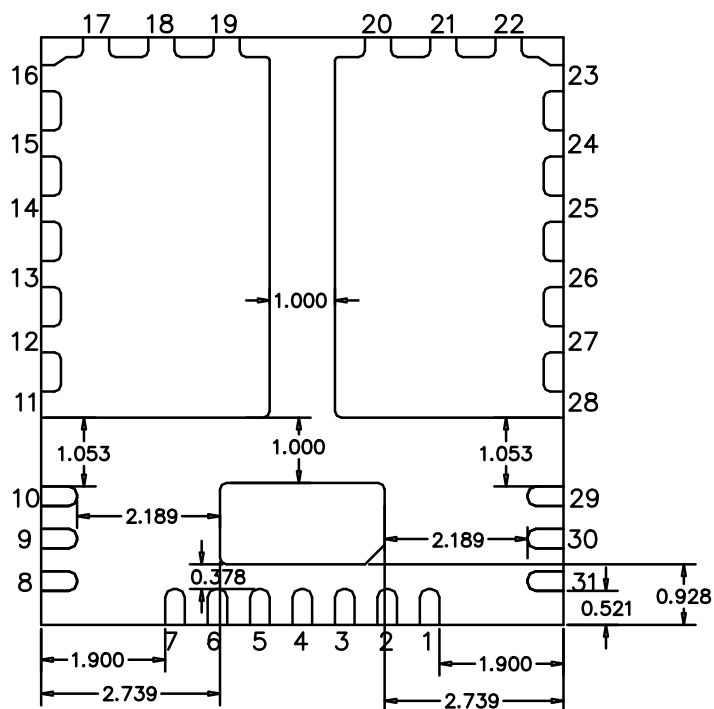
Pin	Name	Description
1, 4, 7, 32	COM	Low Side Gate Drive Return
2	VCC	15V Gate Drive Supply
3	HIN	Logic Input for High Side (Active High)
5	LIN	Logic Input for Low Side (Active High)
6	NC	Not Connected
8, 9, 10	V-	Low Side Source Connection
11 – 19	VS	Phase Output
20 – 28	V+	DC Bus
29 – 30	VS	Phase Output (-ve Bootstrap Cap Connection)
31	VB	High Side Floating Supply (+ve Bootstrap Cap Connection)
32	-	To be connected to COM



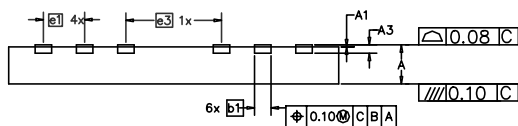
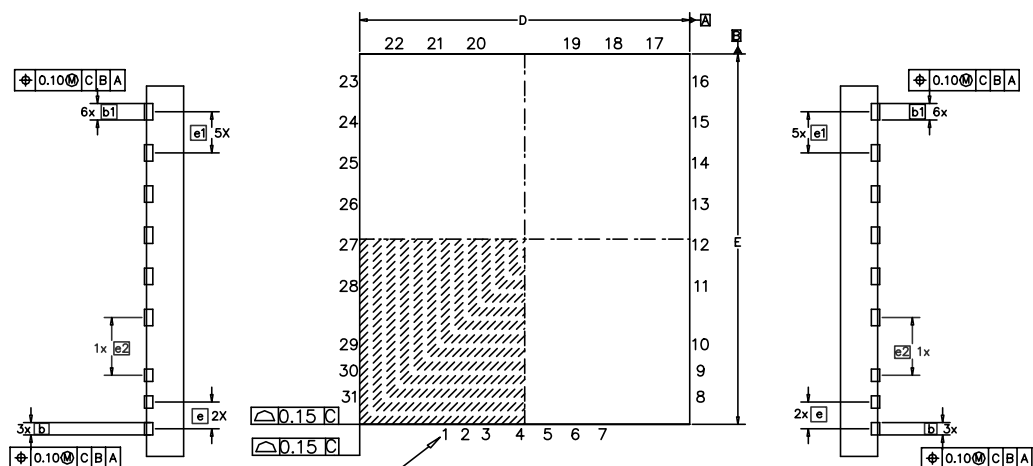
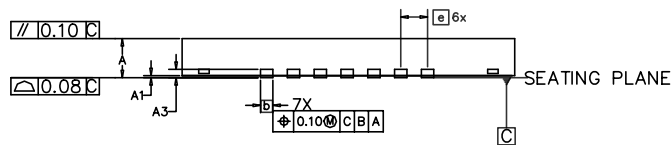
Package Outline IRSM807-045MH (Bottom View), 1 of 2


SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN.	NOM.	MAX.
A	0.800	0.900	1.000
A1	0.000		0.050
A3	0.203 REF.		
b	0.250	0.300	0.350
b1	0.350	0.400	0.450
D	7.900	8.000	8.100
E	8.900	9.000	9.100
D2	2.472	2.522	2.572
E2	1.197	1.247	1.297
D3	3.147	3.197	3.247
E3	5.472	5.522	5.572
D4	3.147	3.197	3.247
E4	5.472	5.522	5.572
e	0.650 BSC		
e1	1.000 BSC		
e2	1.403 BSC		
e3	2.318 BSC		
L	0.500	0.550	0.600
L1	0.253	0.303	0.353

Dimensions in mm

Package Outline IRSM807-045MH (Bottom View), 2 of 2


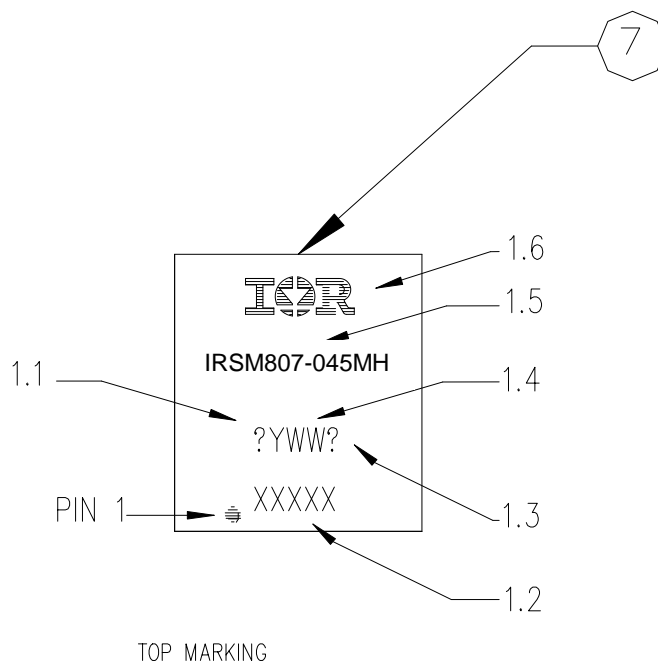
Dimensions in mm

Package Outline IRSM807-045MH (Top & Side View)
BACK SIDE VIEW

TOP VIEW

LEFT SIDE VIEW
RIGHT SIDE VIEW

FRONT SIDE VIEW

SYMBOL	DIMENSIONS IN MILLIMETER			
	MIN.	NOM.	MAX.	
A	0.800	0.900	1.000	
A1	0.000		0.050	
A3	0.203 REF.			
b	0.250	0.300	0.350	
b1	0.350	0.400	0.450	
D	7.900	8.000	8.100	
E	8.900	9.000	9.100	
D2	2.472	2.522	2.572	
E2	1.197	1.247	1.297	
D3	3.147	3.197	3.247	
E3	5.472	5.522	5.572	
D4	3.147	3.197	3.247	
E4	5.472	5.522	5.572	
e	0.650 BSC			
e1	1.000 BSC			
e2	1.403 BSC			
e3	2.318 BSC			
L	0.500	0.550	0.600	
L1	0.253	0.303	0.353	

Dimensions in mm

Top Marking



NOTES, MARKING:

- 1.1) SITE CODE: X
- 1.2) LAST 4 CHARACTER OF SPN/NANA CODE: XXXX
- 1.3) LEADFREE INDICATOR: P
- 1.4) DATE CODE: YWW
- 1.5) PART NUMBER: IRSM607-105MH
- 1.6) IR LOGO
- 1.7) MEDIUM:
 - 1.7.1) TOP: LASER
 - 1.7.2) BOTTOM: NONE

Revision History

International
 Rectifier

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TAC Fax: (310) 252-7903

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