Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are referenced to SOURCE lead. ($T_{Ambient}$ = 25°C unless otherwise specified). PCB mounting uses the standard footprint with 70 µm copper thickness.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{ds}	Maximum drain to source voltage	—	47	V	
V_{in}	Maximum input voltage	-0.3	7		
$I_{in,\ max}$	Maximum IN current	-10	+10	mA	
$I_{sd\ cont.}$	Diode max. continuous current (1)			A	
	rth=100°C/W	—	1.6		D-Pak Std footprint
	rth=5°C/W	—	18		D-Pak with Rth=5°C/W
	rth=50°C/W	—	3		D-Pak with sq. footprint
$I_{sd\ pulsed}$	Diode max. pulsed current (1)	—	18		
P_d	Maximum power dissipation(1)			W	
	rth=50°C/W	—	2.5		
	rth=100°C/W	—	1.25		
ESD1	Electrostatic discharge voltage (Human Body)	—	4	kV	C=100pF, R=1500Ω,
ESD2	Electrostatic discharge voltage (Machine Model)	—	0.5		C=200pF, R=0Ω, L=10µH
$T_{stor.}$	Max. storage temperature	-55	150	°C	
T_j max.	Max. junction temperature	-40	+150		
T_{lead}	Lead temperature (soldering, 10 seconds)	—	300		

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{th} 1	Thermal resistance with standard footprint	—	100	—	°C/W	D-PAK
R_{th} 2	Thermal resistance with 1" square footprint	—	50	—		
R_{th} 3	Thermal resistance junction to case	—	3	—		

Recommended Operating Conditions

These values are given for a quick design. For operation outside these conditions, please consult the application notes.

Symbol	Parameter	Min.	Max.	Units
$V_{ds\ (max)}$	Continuous drain to source voltage	—	35	V
V_{IH}	High level input voltage	4	6	
V_{IL}	Low level input voltage	0	0.5	
I_{ds} Tamb=85°C	Continuous drain current			A
	TAmbient = 85°C, IN = 5V, rth = 50°C/W, Tj = 125°C) 1" sq. footprint	—	3.3	
	TAmbient = 85°C, IN = 5V, rth = 100°C/W, Tj = 125°C) Std. footprint	—	2	
R_{in}	Recommended resistor in series with IN pin	0.2	5	kΩ
$T_{r\text{-}in(max)}$	Max recommended rise time for IN signal (see fig. 2)	—	1	µS
$F_{r\text{-}Isc}$ (2)	Max. frequency in short circuit condition (Vcc = 14V)	0	1	kHz

(1) Limited by junction temperature (pulsed current limited also by internal wiring)
(2) Operations at higher switching frequencies is possible. See Application. Notes.

Static Electrical Characteristics

(T_j = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{ds(on)}$	ON state resistance T_j = 25°C	20	45	60	mΩ	V_{in} = 5V, I_{ds} = 1A
$R_{ds(on)}$	ON state resistance T_j = 150°C	—	75	100		
I_{dss} @Tj=25°C	Drain to source leakage current	0	0.5	25	µA	V_{cc} = 14V, T_j = 25°C
I_{dss2} @Tj=25°C	Drain to source leakage current	0	5	50		V_{cc} = 40V, T_j = 25°C
V clamp 1	Drain to source clamp voltage 1	47	52	56	V	I_d = 20mA (see Fig.3 & 4)
V clamp 2	Drain to source clamp voltage 2	50	53	60		I_d=$I_{shutdown}$ (see Fig.3 & 4)
$V_{in\ clamp}$	IN to source clamp voltage	7	8.1	9.5		I_{in} = 1 mA
V_{th}	IN threshold voltage	1	1.6	2		I_d = 50mA, Vds = 14V
I_{in}, -on	ON state IN positive current	25	90	200	µA	V_{in} = 5V
I_{in}, -off	OFF state IN positive current	50	130	250		V_{in} = 5V over-current triggered

Switching Electrical Characteristics

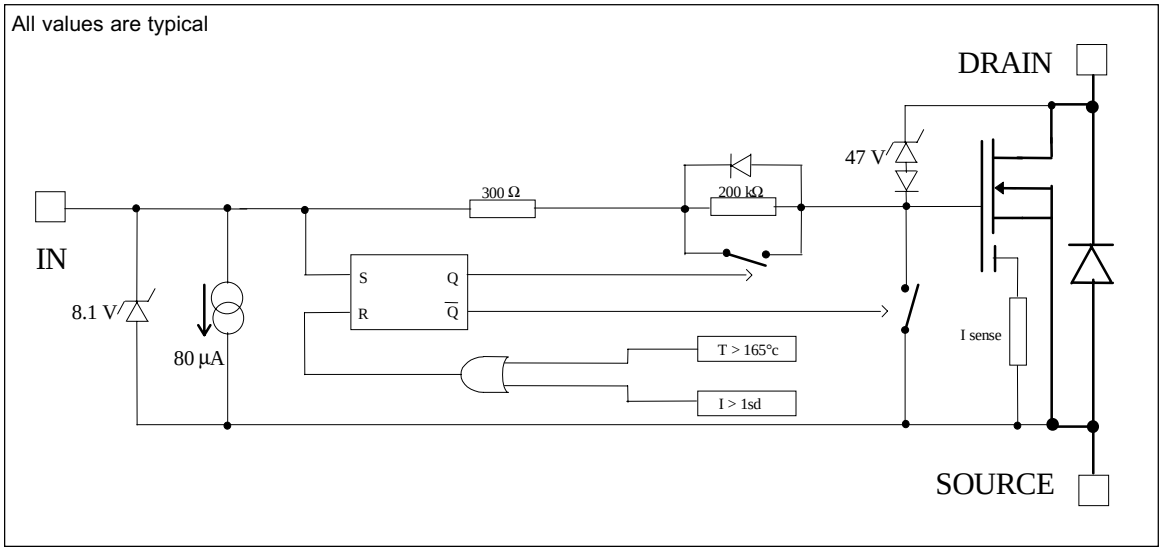
V_{cc} = 14V, Resistive Load = 5Ω , Rinput = 50Ω, 100µs pulse,T_j = 25°C, (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{on}	Turn-on delay time	0.05	0.3	0.6	µs	See figure 2
T_r	Rise time	0.4	1	2		
T_{rf}	Time to 130% final $R_{ds(on)}$	—	8	—		
T_{off}	Turn-off delay time	0.8	2	3.5		See figure 2
T_f	Fall time	0.5	1.5	2.5		
Q_{in}	Total gate charge	—	11	—	nC	V_{in} = 5V

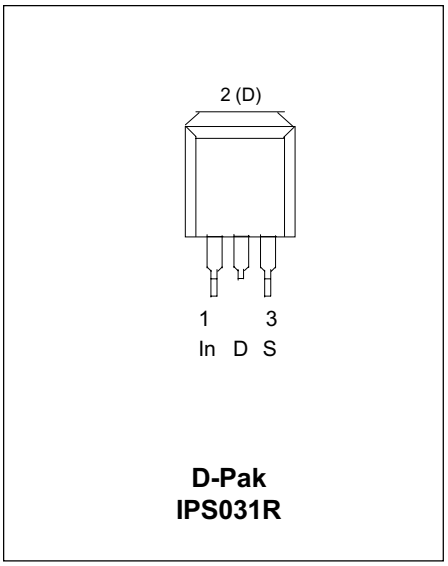
Protection Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
T_{sd}	Over temperature threshold	—	165	—	°C	See fig. 1
I_{sd}	Over current threshold	10	14	18	A	See fig. 1
V_{reset}	IN protection reset threshold	1.5	2.3	3	V	
T_{reset}	Time to reset protection	2	10	40	µs	V_{in} = 0V, Tj = 25°C
EOI_OT	Short circuit energy (see application note)	—	400	—	µJ	V_{cc} = 14V

Functional Block Diagram



Lead Assignments



D-Pak
IPS031R

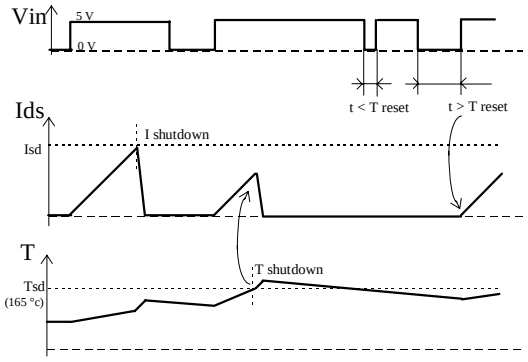


Figure 1 - Timing diagram

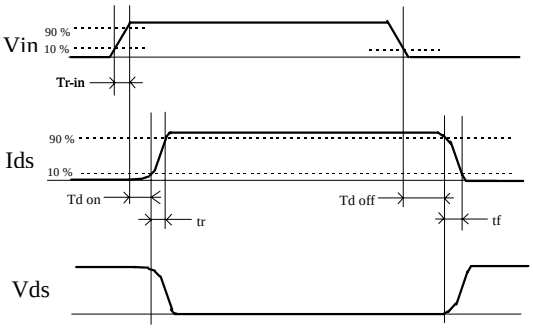


Figure 2 - IN rise time & switching time definitions

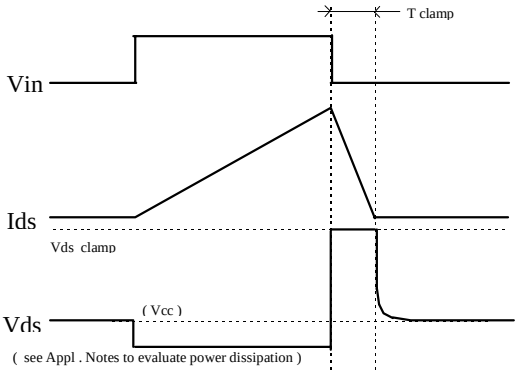


Figure 3 - Active clamp waveforms

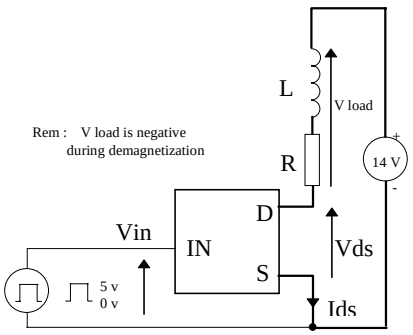


Figure 4 - Active clamp test circuit

All curves are typical values with standard footprints. Operating in the shaded area is not recommended.

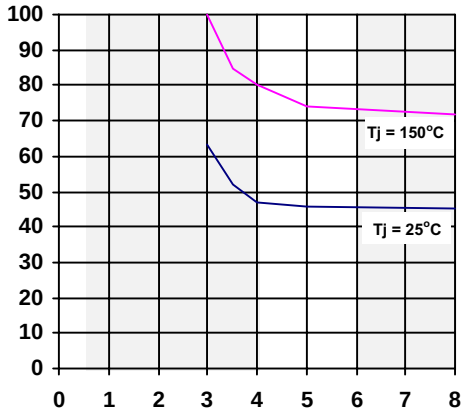


Figure 5 - Rds ON (mΩ) Vs Input Voltage (V)

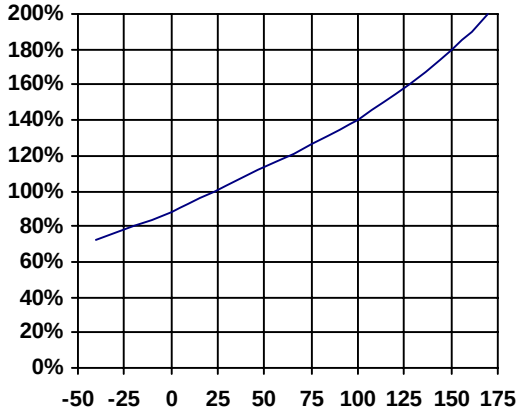


Figure 6 - Normalised Rds ON (%) Vs Tj (°C)

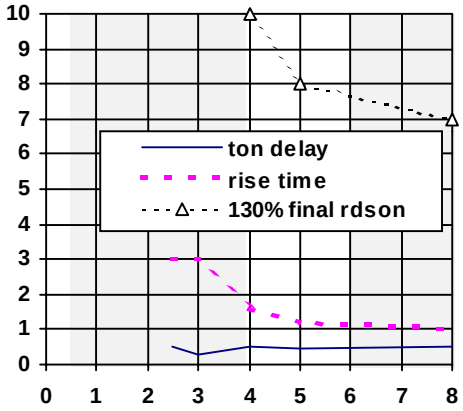


Figure 7 - Turn-ON Delay Time, Rise Time & Time to 130% final $R_{ds(on)}$ (us) Vs Input Voltage (V)

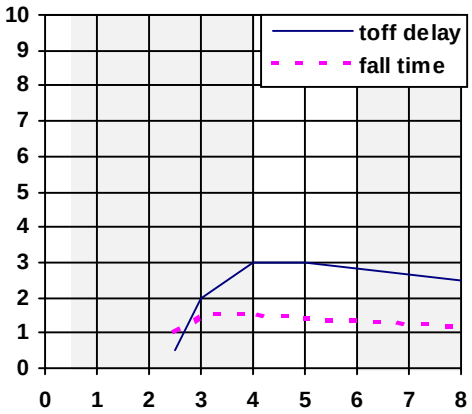


Figure 8 - Turn-OFF Delay Time & Fall Time (us) Vs Input Voltage (V)

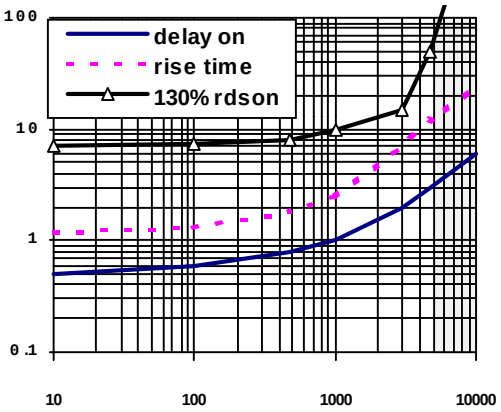


Figure 9 - Turn-ON Delay Time, Rise Time & Time to 130% final $R_{ds(on)}$ (us) Vs IN Resistor (Ω)

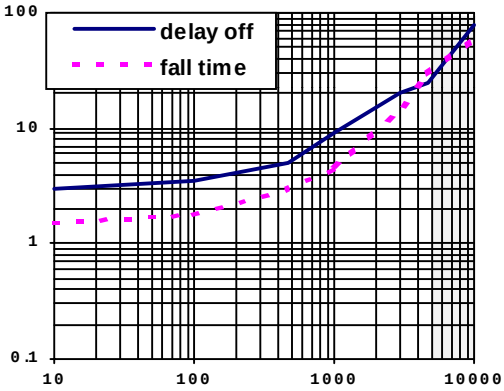


Figure 10 - Turn-OFF Delay Time & Fall Time (us) Vs IN Resistor (Ω)

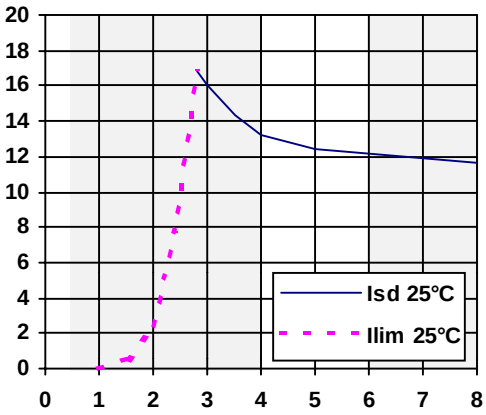


Figure 11 - Current limitation & I shutdown (A) Vs Vin (V)

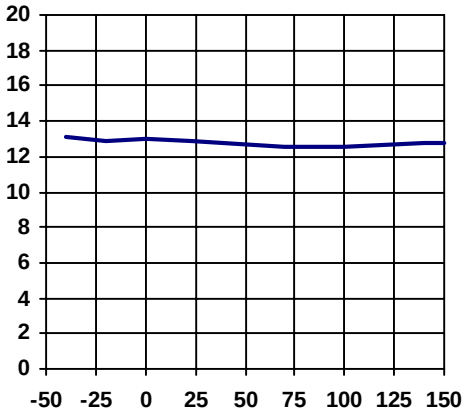


Figure 12 - I shutdown (A) Vs Temperature (°C)

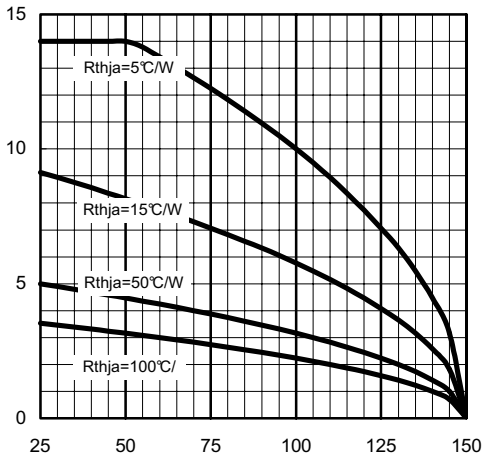


Figure 13 - Max. I load current (A) Vs Tamb (°C)
IPS031R

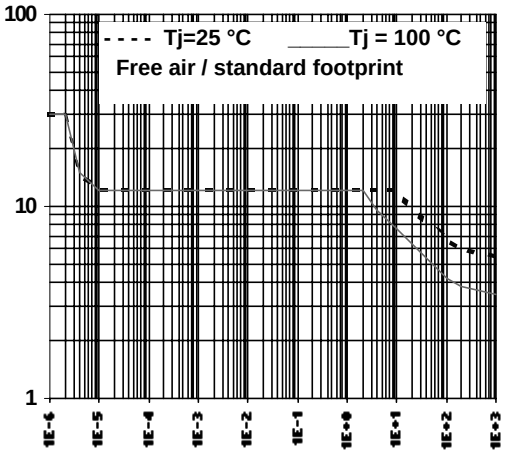


Figure 14 - Ids (A) Vs Protection Resp. Time (s)
IPS031R

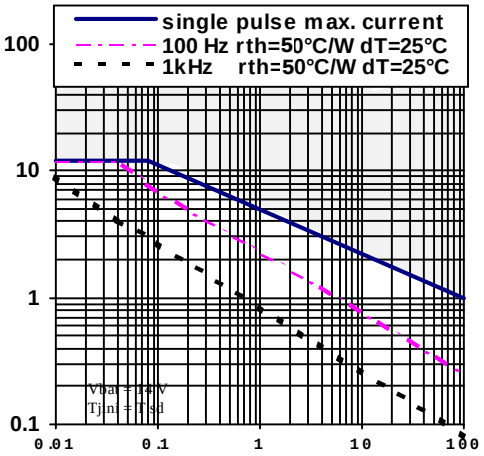


Figure 15 - Iclamp (A) Vs Inductive Load (mH)

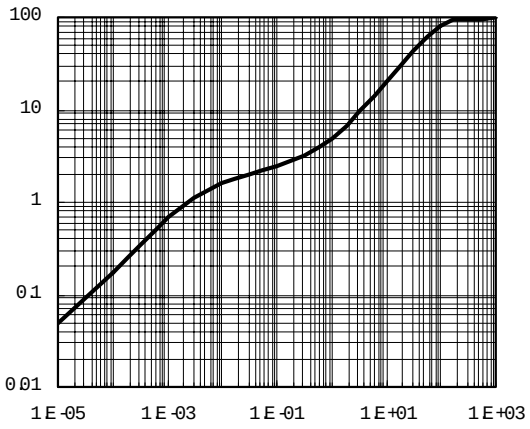


Fig.16 - Transient Thermal Impedance (°C/W)
Vs Time (s) - IPS031R

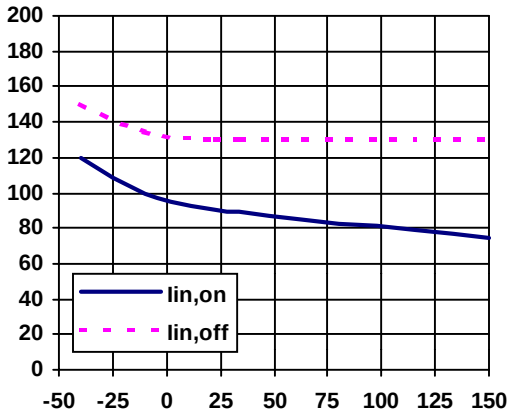


Figure 17 - Input current (µA) Vs Junction (°C)

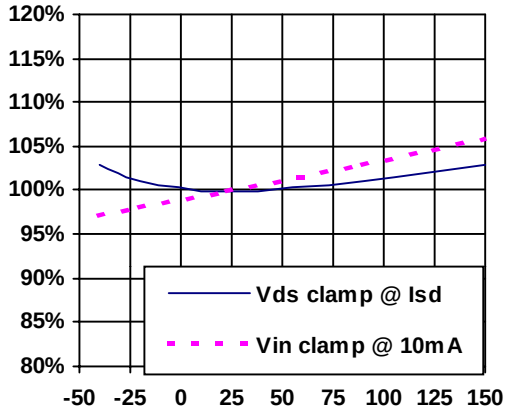


Figure 18 - Vin clamp and V clamp2 (%) Vs Tj (°C)

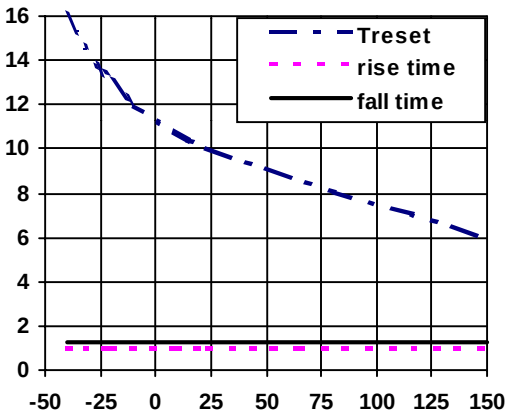
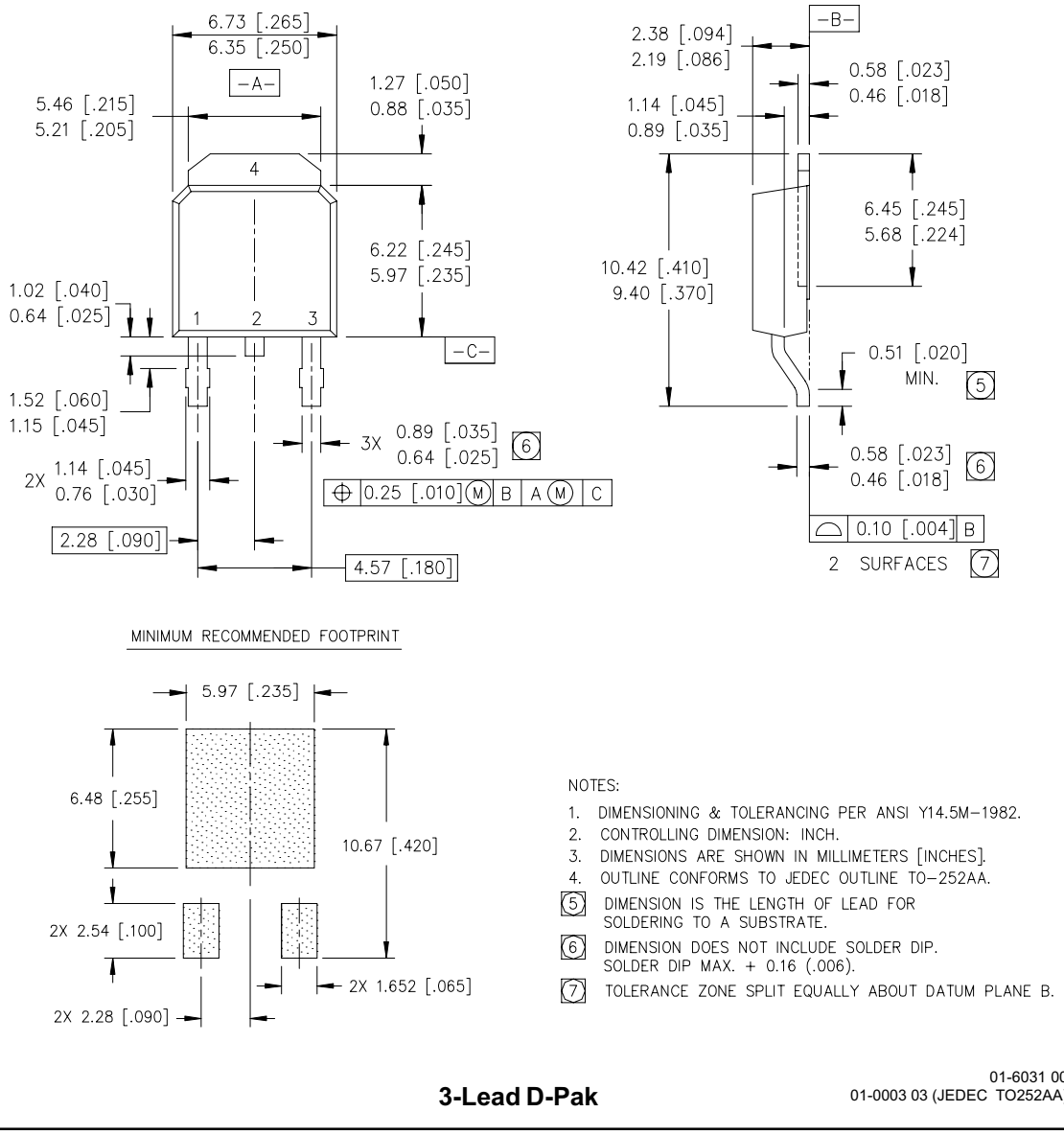


Figure 19 - Turn-on, Turn-off, and treset (µs) Vs Tj (°C)

Case Outline



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

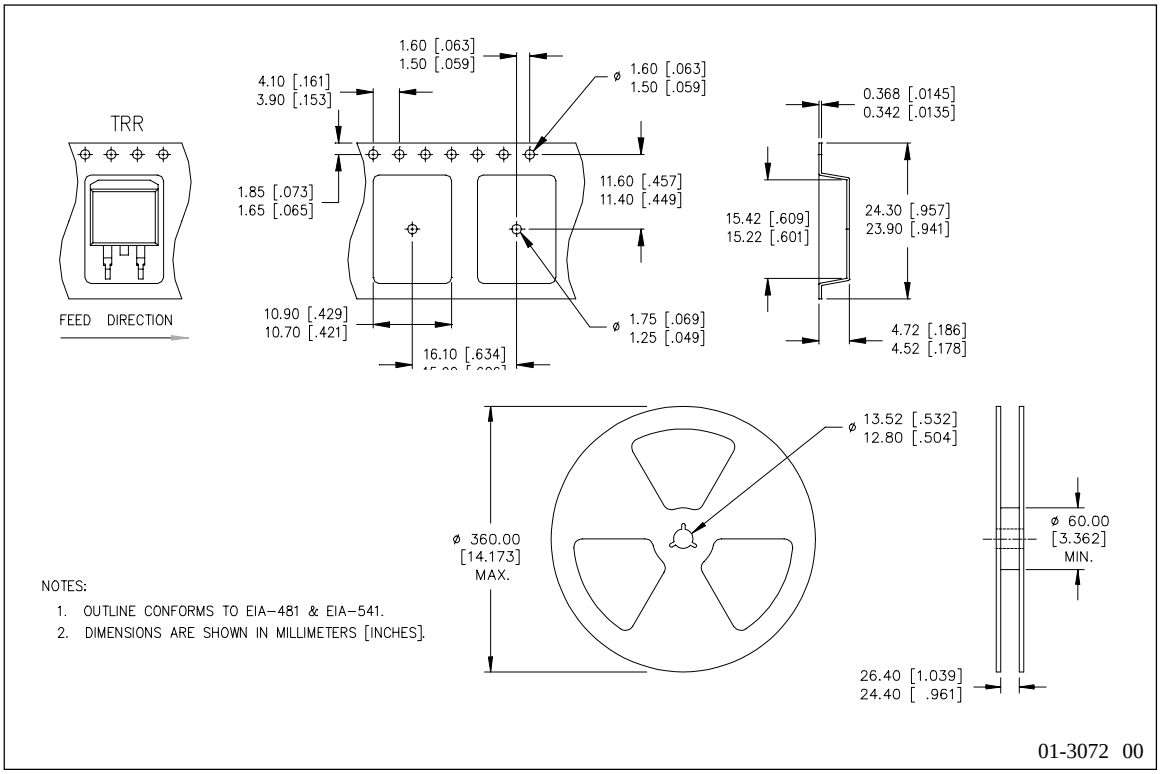
(6) DIMENSION DOES NOT INCLUDE SOLDER DIP. SOLDER DIP MAX. + 0.16 (.006).

(7) TOLERANCE ZONE SPLIT EQUALLY ABOUT DATUM PLANE B.

3-Lead D-Pak

01-6031 00
01-0003 03 (JEDEC TO252AA)

Tape & Reel - D-PAK



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

This device was designed and qualified peer automotive level (Q101)

Data and specifications subject to change without notice. 6/1/2004

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/