Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}		-	-	1.1	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}		-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm² cooling area[4]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D= 1 mA	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=80 µA	2.1	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	V_{DS}=55 V, V_{GS}=0 V, T_j=25 °C	-	-	1	µA
		V_{DS}=55 V, V_{GS}=0 V, T_j=125 °C[2]	-	1	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=51 A	-	5.8	6.8	mΩ
		V_{GS}=10 V, I_D=51 A, SMD version	-	5.5	6.5	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	7768	-	pF
Output capacitance	C_{oss}		-	1182	-	
Reverse transfer capacitance	C_{rss}		-	1128	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=27.5 V, V_{GS}=10 V, I_D=80 A, R_G=3.5 Ω	-	30	-	ns
Rise time	t_r		-	41	-	
Turn-off delay time	$t_{d(off)}$		-	34	-	
Fall time	t_f		-	33	-	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD}=11 V, I_D=80 A, V_{GS}=0 to 10 V	-	56	-	nC
Gate to drain charge	Q_{gd}		-	25	-	
Gate charge total	Q_g		-	113	170	
Gate plateau voltage	$V_{plateau}$		-	6.6	-	V
Reverse Diode[2]						
Diode continous forward current	I_S	T_C=25 °C	-	-	80	A
Diode pulse current	$I_{S,pulse}$		-	-	320	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=80 A, T_j=25 °C	0.6	0.9	1.3	V
Reverse recovery time	t_{rr}	V_R=27.5 V, I_F=I_S, di_F/dt=100 A/µs	-	55	-	ns
Reverse recovery charge	Q_{rr}		-	70	-	nC

[1] Current is limited by bondwire; with an R_{thJC} = 1.1 K/W the chip is able to carry 105 A at 25°C. For detailed information see Application Note ANPS071E

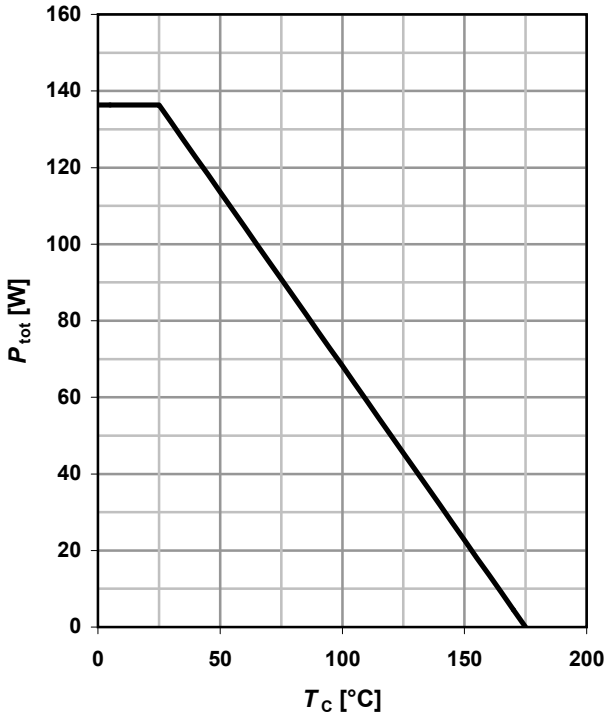
[2] Defined by design. Not subject to production test.

[3] Qualified at -5V and +20V.

[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

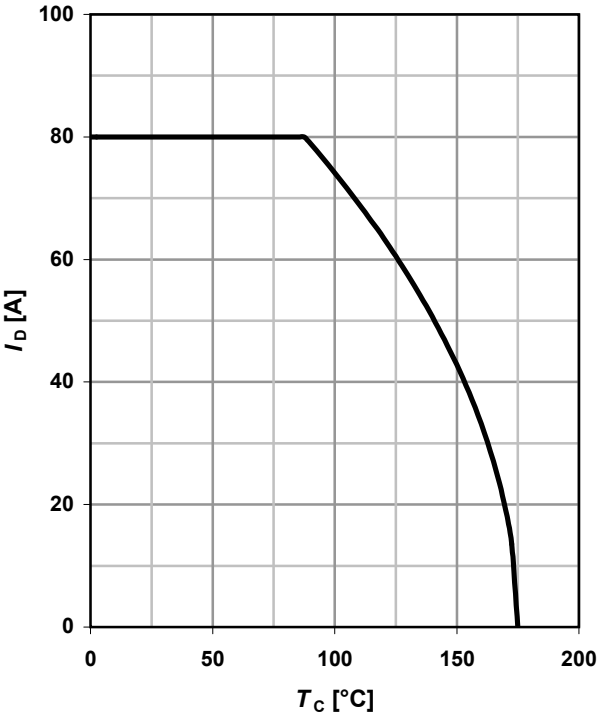
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



2 Drain current

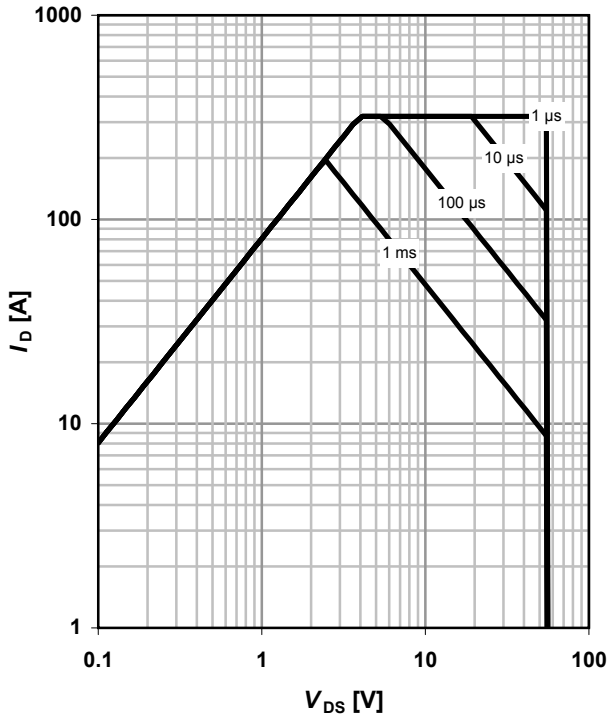
$I_D = f(T_C)$; $V_{GS} \geq 6$ V



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

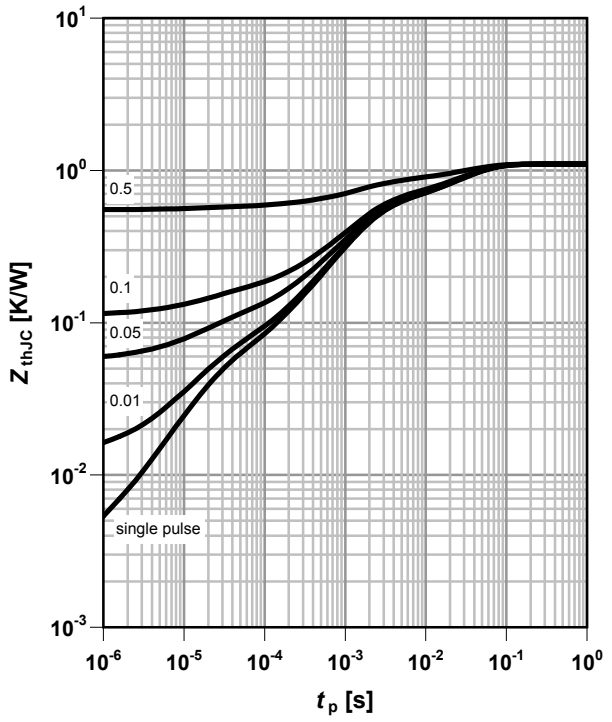
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

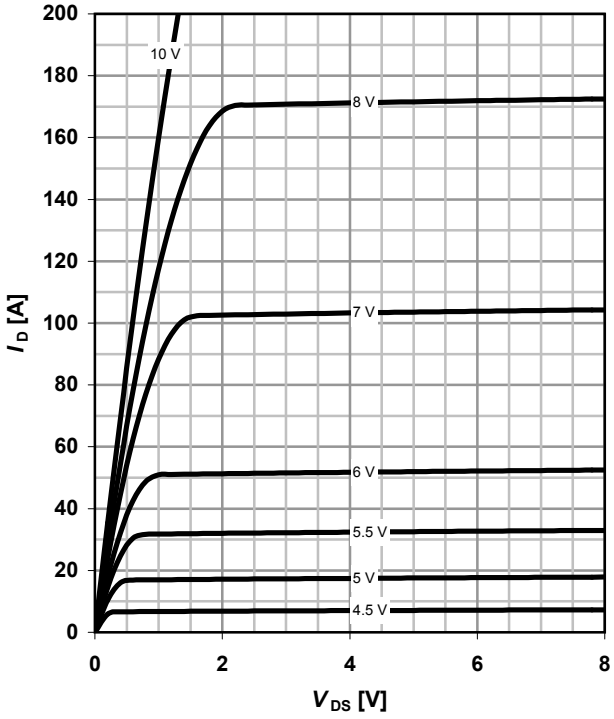
parameter: $D = t_p / T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

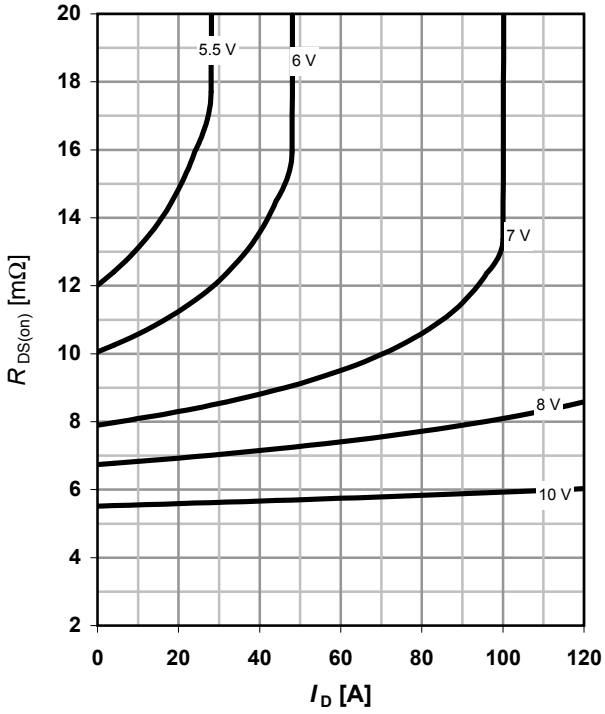
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C

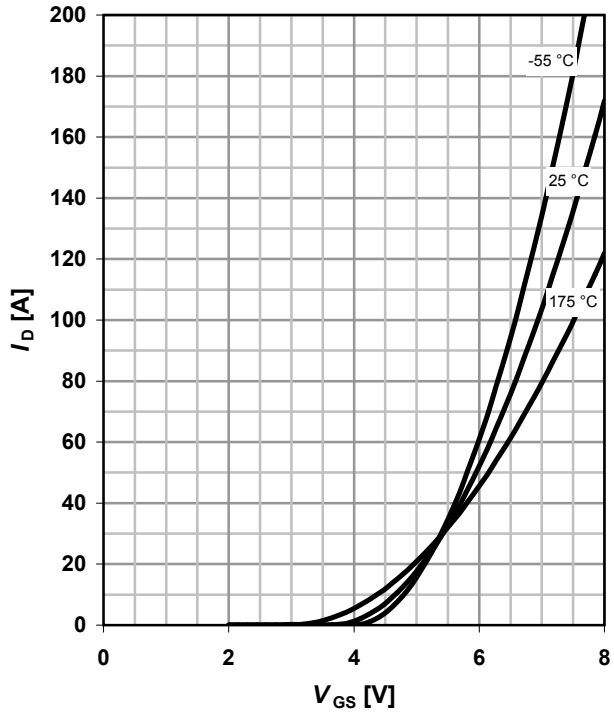
parameter: V_{GS}



7 Typ. transfer characteristics

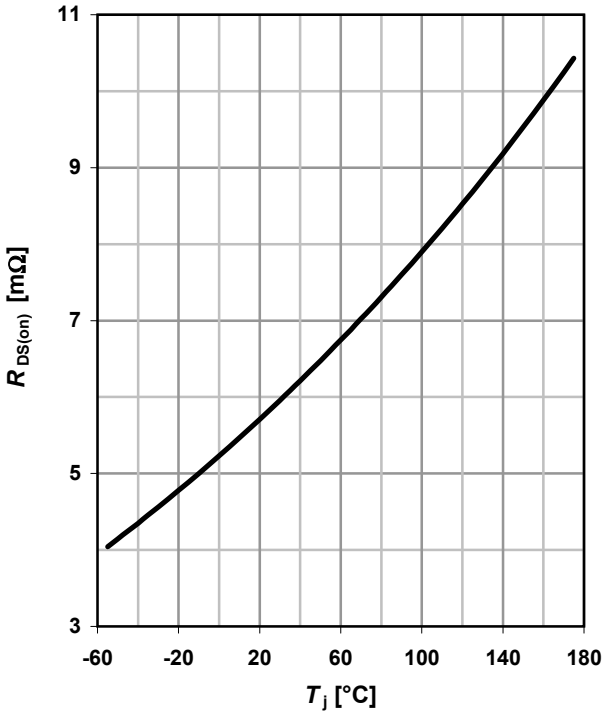
$I_D = f(V_{GS})$; $V_{DS} = 6$V

parameter: T_j



8 Typ. drain-source on-state resistance

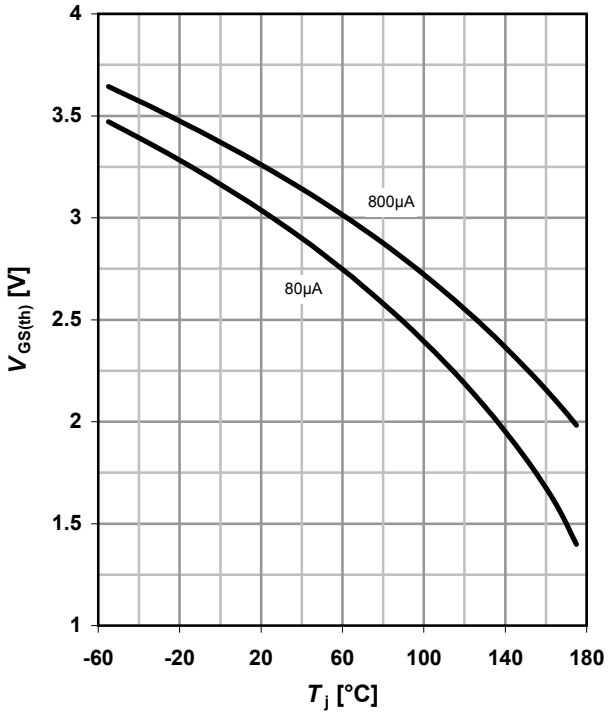
$R_{DS(on)} = f(T_j)$; $I_D = 80$ A; $V_{GS} = 10$ V



9 Typ. gate threshold voltage

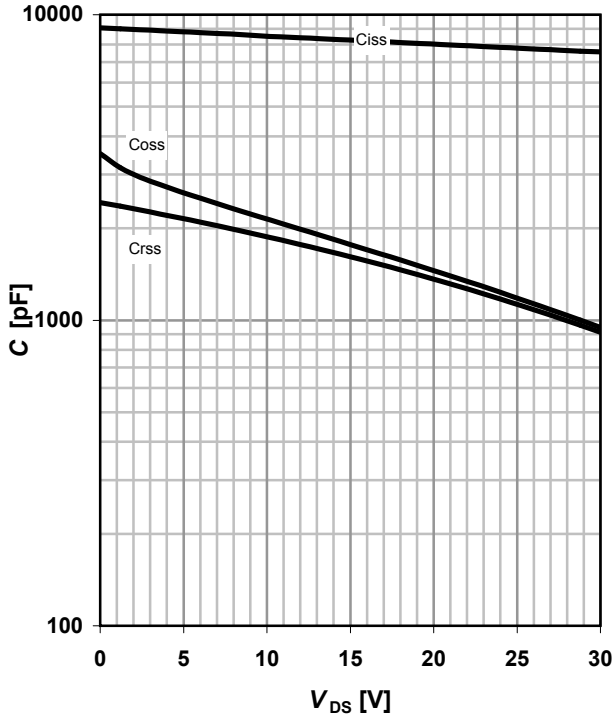
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

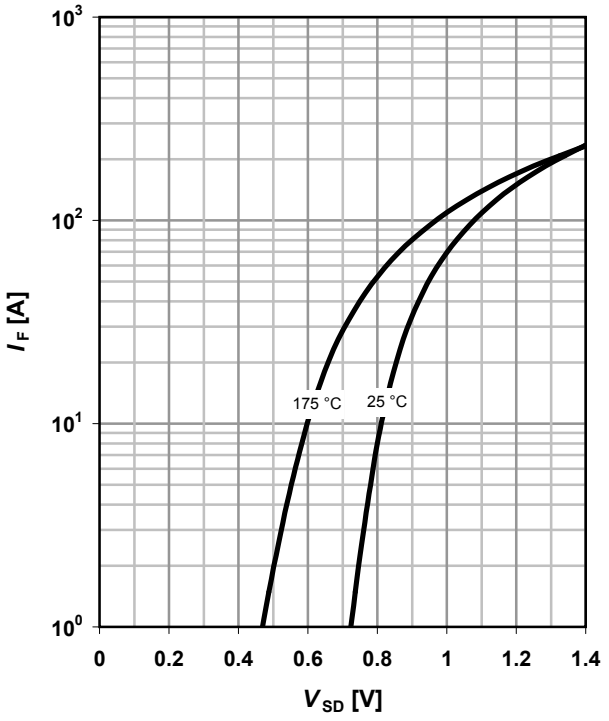
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis

IF = f(V_{SD})

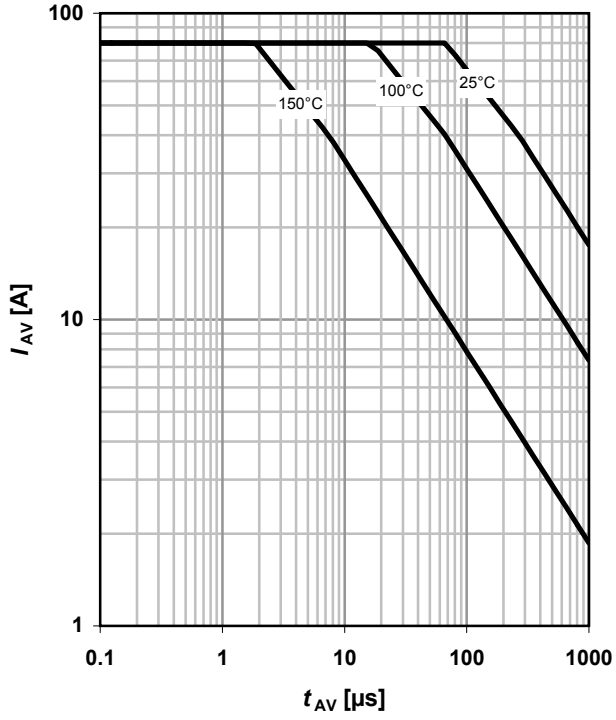
parameter: T_j



12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$

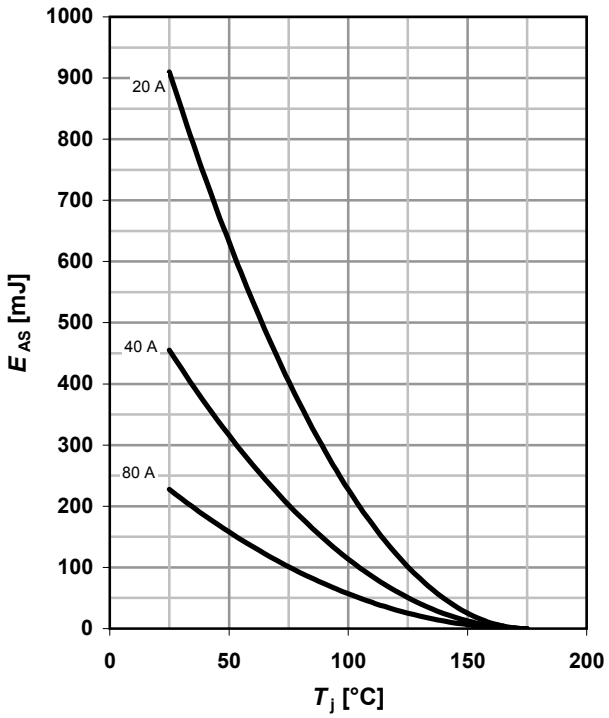
parameter: $T_{j(start)}$



13 Typical avalanche energy

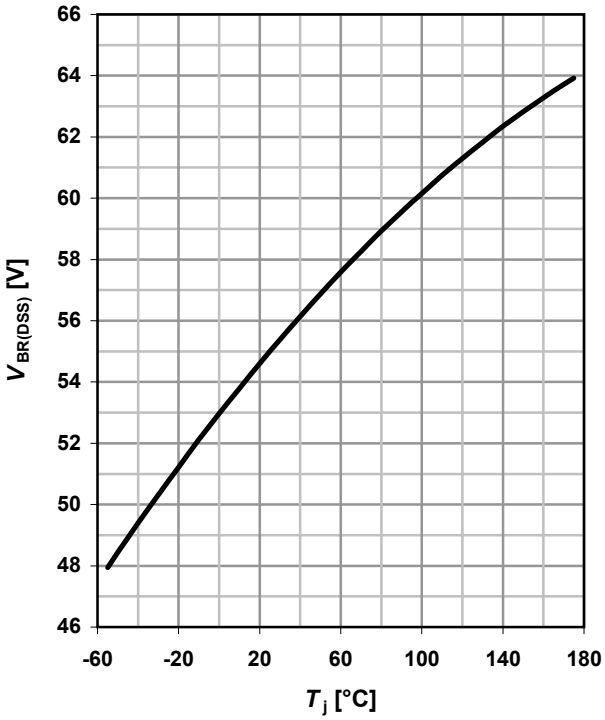
$E_{AS} = f(T_j)$

parameter: I_D



14 Typ. drain-source breakdown voltage

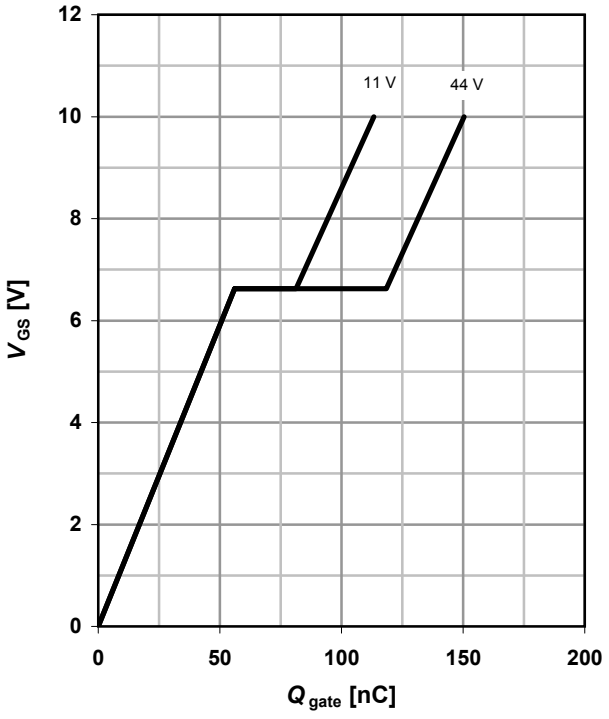
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



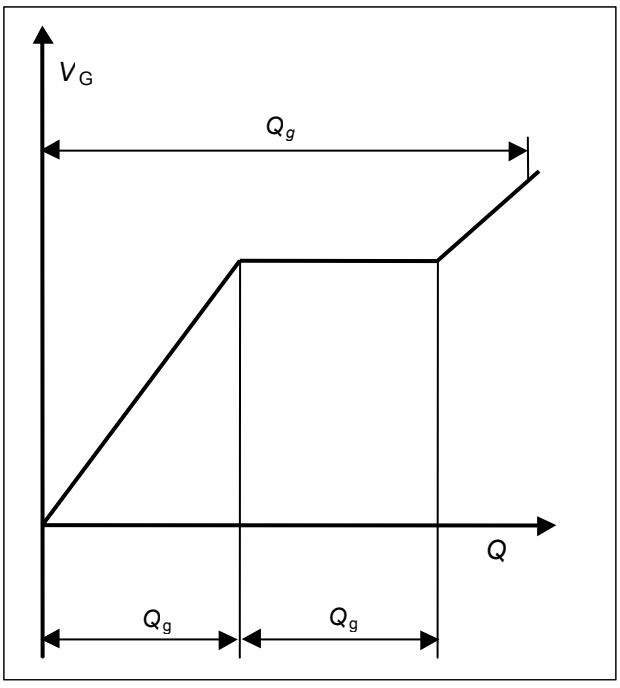
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 80$ A pulsed

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Data Sheet 2.1	15.12.2006	Removal of ordering code
Data Sheet 2.1	15.12.2006	Update of Infineon Logo
Data Sheet 2.1	15.12.2006	Implementation of avalanche current single pulse
Data Sheet 2.1	15.12.2006	Removal of ESD class
Data Sheet 2.1	15.12.2006	Update of Infineon address
Data Sheet 2.1	15.12.2006	Removal of foot note 3, avalanche diagrams
Data Sheet 2.1	15.12.2006	Update of trr and Qrr
Data Sheet 2.1	15.12.2006	Update of disclaimer
Data Sheet 2.1	15.12.2006	Implementation of RoHS and AEC logo, update of feature list
Data Sheet 1.1	07.11.2007	Update of data sheet layout
Data Sheet 1.1	07.11.2007	Adaptation of Ias
Data Sheet 1.1	07.11.2007	implementation of footnote 2 for Eas specification
Data Sheet 1.1	07.11.2007	removal of Vdg specification from data sheet