

PIN DESCRIPTIONS

SYMBOL	FUNCTION	DESCRIPTION
VREF	POWER	THE REFERENCE VOLTAGE USED TO DETERMINE THE OUTPUT VOLTAGE SWING
STROBE	INPUT	A LOGIC HIGH ON THIS INPUT PLACES THE DRIVER IN POWER DOWN MODE
SYNC	INPUT	SYNCHRONIZES DATA INPUTS
DATA (A)	INPUT	DATA INPUT TERMINAL A
CA	INPUT	CONNECTION FOR DATA (A) SLEW-RATE CAPACITOR
AOUT	OUTPUT	ARINC OUTPUT TERMINAL A
-V	POWER	-12V to -15V
GND	POWER	0.0V
+V	POWER	+12V to +15V
BOUT	OUTPUT	ARINC OUTPUT TERMINAL B
Cb	INPUT	CONNECTION FOR DATA (B) SLEW-RATE CAPACITOR
DATA (B)	INPUT	DATA INPUT TERMINAL B
CLOCK	INPUT	SYNCHRONIZES DATA INPUTS
V1	POWER	+5V ±5%

ABSOLUTE MAXIMUM RATINGS

All Voltages referenced to GND, TA = Operating Temperature Range (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	OPERATING RANGE	MAXIMUM	UNIT
Differential Voltage	VDIF	Voltage between +V and -V terminals		40	V
Supply Voltage	+V -V V1		+10.8 to +16.5 -10.8 to -16.5 +5 ±5%	+7	V V V
Voltage Reference	VREF	For ARINC 429 For Applications other than ARINC	+5 ±5% 0 to 6	6 6	V V
Input Voltage Range	VIN			≥ GND -0.3 ≤ V1 +0.3	V V
Output Short-Circuit Duration		See Note: 1			
Output Overvoltage Protection		See Note: 2			
Operating Temperature Range	TA	Extended Industrial	-55 to +125 -40 to +85		°C °C
Storage Temperature Range	TSTG	Ceramic & Plastic	-65 to +150		°C
Lead Temperature		Soldering, 10 seconds		+275	°C
Junction Temperature	TJ			+175	°C
Power Dissipation	PD	16-Pin Ceramic DIP 28-Pin Ceramic LCC 28-Pin Plastic PLCC 32-Pin CERQUAD	See Note: 3 See Note: 3 See Note: 3 See Note: 3	1.725 1.120 2.143 1.725	W W W W
Thermal Resistance, (Junction-to-Ambient)	ΘJA	16-Pin Ceramic DIP 28-Pin Ceramic LCC 28-Pin Plastic PLCC 32-Pin CERQUAD		86.5 133.7 70.0 86.5	°C/W °C/W °C/W °C/W

Note 1. Heatsinking may be required for Output Short Circuit at +125°C and for 100KBPS at +125°C.

Note 2. The fuses used for Output Overvoltage Protection may be blown by the presence of a voltage at either output that is greater than ±12.0V with respect to GND. (HI-8382 only)

Note 3. Derate above +25°C, 11.5mW/°C for 16-PIN DIP and 32-PIN CERQUAD, 7.5 mW/°C for 28-PIN LCC, 14.2 mW/°C for 28-PIN PLCC

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V₁ = V_{REF} = +5.0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Current +V (Operating)	ICCOP (+V)	No Load (0 - 100KBPS)			+11	mA
Supply Current -V (Operating)	ICCOP (-V)	No Load (0 - 100KBPS)	-11			mA
Supply Current V ₁ (Operating)	ICCOP (V ₁)	No Load (0 - 100KBPS)			500	μA
Supply Current V _{REF} (Operating)	ICCOP (V _{REF})	No Load (0 - 100KBPS)			500	μA
Supply Current +V (Power Down)	ICCPD (+V)	STROBE = HIGH			475	uA
Supply Current -V (Power Down)	ICCPD (-V)	STROBE = HIGH	-475			uA
Supply Current +V (During Short Circuit Test)	ISC (+V)	Short to Ground (See Note: 1)			150	mA
Supply Current -V (During Short Circuit Test)	ISC (-V)	Short to Ground (See Note: 1)	-150			mA
Output Short Circuit Current (Output High)	IOHSC	Short to Ground V _{MIN} =0 (See Note: 2)			-80	mA
Output Short Circuit Current (Output Low)	IOLSC	Short to Ground V _{MIN} =0 (See Note: 2)	+80			mA
Input Current (Input High)	I _{IH}				1.0	μA
Input Current (Input Low)	I _{IL}				-1.0	μA
Input Voltage High	V _{IH}		2.0			V
Input Voltage Low	V _{IL}				0.5	V
Output Voltage High (Output to Ground)	V _{OH}	No Load (0 -100KBPS)	+V _{REF} - .25		+V _{REF} + .25	V
Output Voltage Low (Output to Ground)	V _{OL}	No Load (0 -100KBPS)	-V _{REF} - .25		-V _{REF} + .25	V
Output Voltage Null	V _{NULL}	No Load (0-100KBPS)	-250		+250	mV
Input Capacitance	C _{IN}	See Note 1		15		pF

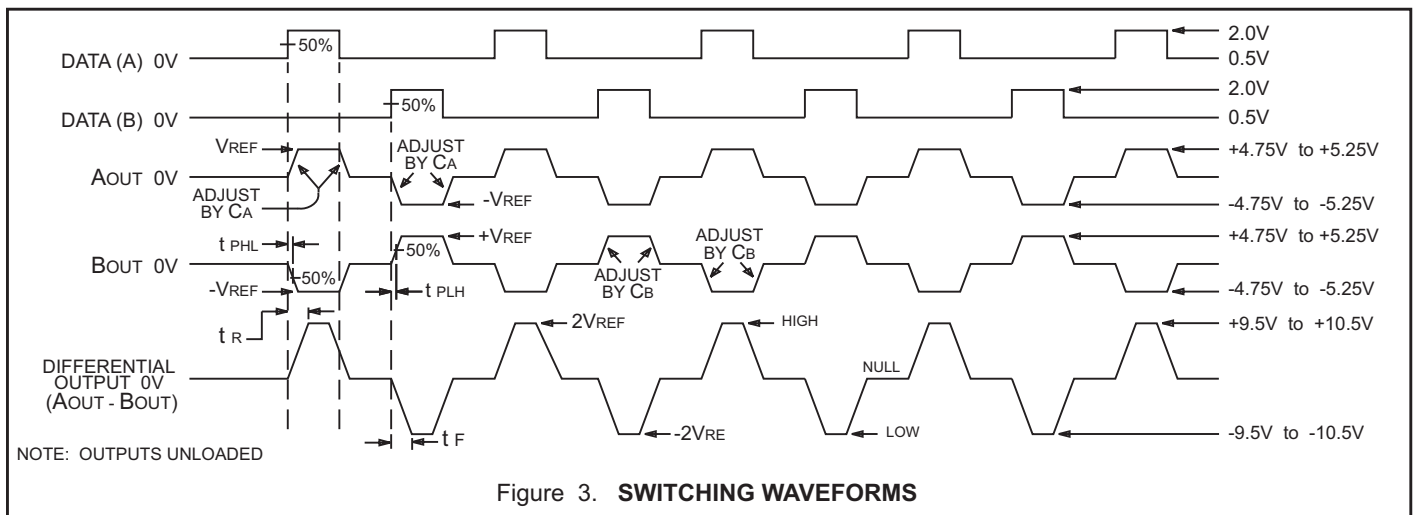
Note 1. Not tested, but characterized at initial device design and after major process and/or design change which affects this parameter.

Note 2. Interchangeability of force and sense is acceptable.

AC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V₁ = V_{REF} = +5.0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Rise Time (AOUT, BOUT)	t _R	CA = CB = 75pF See Figure 3.	1.0		2.0	μs
Fall Time (AOUT, BOUT)	t _F	CA = CB = 75pF See Figure 3.	1.0		2.0	μs
Propagation Delay Input to Output	t _{PLH}	CA = CB = 75pF See Figure 3.			3.0	μs
Propagation Delay Input to Output	t _{PHL}	CA = CB = 75pF See Figure 3.			3.0	μs



HI-8382 PACKAGE THERMAL CHARACTERISTICS

MAXIMUM ARINC LOAD ⁷

PACKAGE STYLE ¹	ARINC 429 DATA RATE	SUPPLY CURRENT (mA) ²			JUNCTION TEMP, T _j (°C)		
		T _a = 25°C	T _a = 85°C	T _a = 125°C	T _a = 25°C	T _a = 85°C	T _a = 125°C
28 Lead PLCC	Low Speed ³	17.6	17.2	17.0	48	107	142
	High Speed ⁴	25.4	24.5	24.2	56	110	150
16 Lead Ceramic SB DIP	Low Speed	17.9	17.4	17.1	41	103	145
	High Speed	25.8	24.8	24.4	47	112	147

AOUT and BOUT Shorted To Ground ^{5, 6, 7}

PACKAGE STYLE ¹	ARINC 429 DATA RATE	SUPPLY CURRENT (mA) ²			JUNCTION TEMP, T _j (°C)		
		T _a = 25°C	T _a = 85°C	T _a = 125°C	T _a = 25°C	T _a = 85°C	T _a = 125°C
28 Lead PLCC	Low Speed ³	60.1	55.7	52.4	110	157	194
	High Speed ⁴	63.1	56.3	52.3	100	150	182
16 Lead Ceramic SB DIP	Low Speed	62.1	56.2	53.0	90	145	180
	High Speed	64.0	56.2	52.2	86	144	176

Notes:

1. All data taken in still air on devices soldered to a single layer copper PCB (3" X 4.5" X .062").
2. At 100% duty cycle, 15V power supplies. For 12V power supplies multiply all tabulated values by 0.8.
3. Low Speed: Data Rate = 12.5 Kbps, Load: R = 400 Ohms, C = 30 nF.
4. High Speed: Data Rate = 100 Kbps, Load: R = 400 Ohms, C = 10 nF. Data not presented for C = 30 nF as this is considered unrealistic for high speed operation.
5. Similar results would be obtained with AOUT shorted to BOUT.
6. For applications requiring survival with continuous short circuit, operation above T_j = 175°C is not recommended.
7. Data will vary depending on air flow and the method of heat sinking employed.

ORDERING INFORMATION

HI - 838x x x - xx (Ceramic)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	NOTES
Blank	-40°C to +85°C	I	No	
T	-55°C to +125°C	T	No	
M-01	-55°C to +125°C	M	Yes	(1)
M-03	-55°C to +125°C	DSCC	Yes	(1) & (2)

PART NUMBER	PACKAGE DESCRIPTION	LEAD FINISH	NOTES
C	16 PIN CERAMIC SIDE BRAZED DIP (16C)	Gold	(3) & (1)
S	28 PIN CERAMIC LEADLESS CHIP CARRIER (28S)	Gold	(3) & (1)
U	32 PIN CERQUAD (32U) not available with 'M' flow	Tin/Lead Solder	

PART NUMBER	OUTPUT SERIES	
	RESISTANCE	FUSE
8382	37.5 Ohms	Yes
8383	13 Ohms	No

- (1) Process Flows M and DSCC always have Tin/Lead (Sn/Pb) solder lead finish.
- (2) DSCC SMD# 5962-8687901EA. Only available in "C" package with Sn/Pb solder lead finish.
- (3) Gold terminal finish is Pb-Free, RoHS compliant.

HI - 838xJ x x (Plastic)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
Blank	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION	OUTPUT SERIES	
		RESISTANCE	FUSE
8382J	28 PIN PLASTIC PLCC (28J) (1)	37.5 Ohms	Yes
8383J	28 PIN PLASTIC PLCC (28J) (1)	13 Ohms	No

(1) NOT RECOMMENDED FOR NEW DESIGNS. The newer HI-3182PJxx and HI-3183PJxx are drop-in replacements for the older HI-8382Jxx and HI-8383Jxx respectively.

HI - 838x PDx x (Plastic DIP)

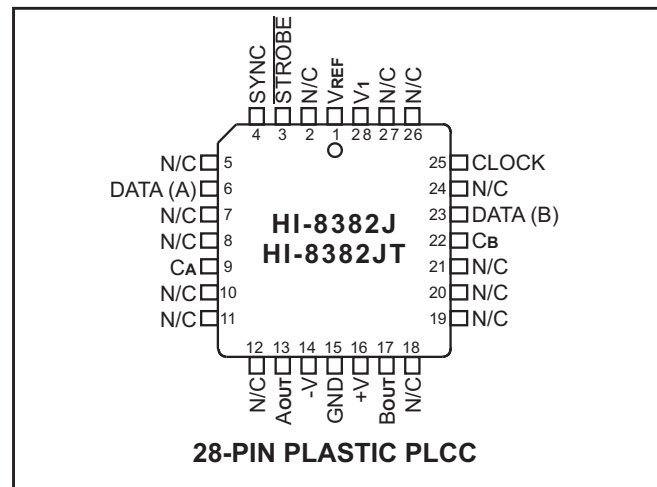
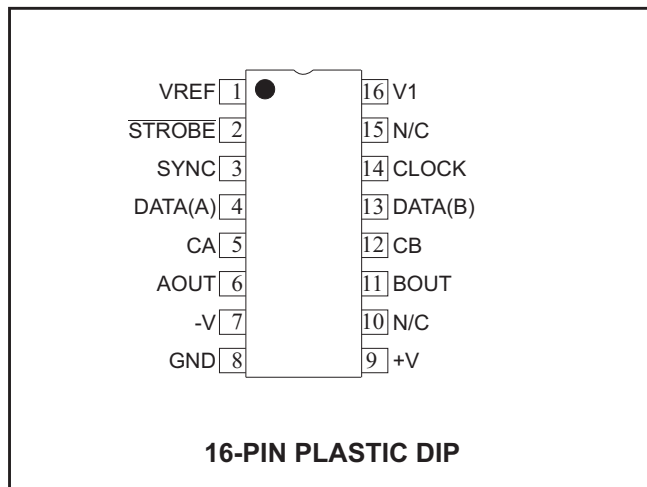
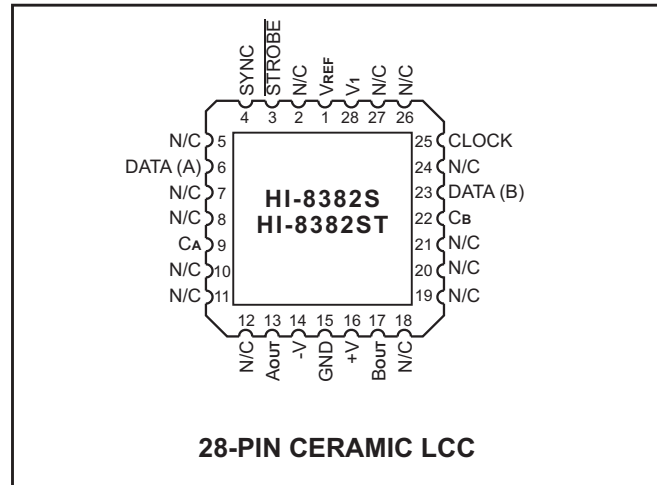
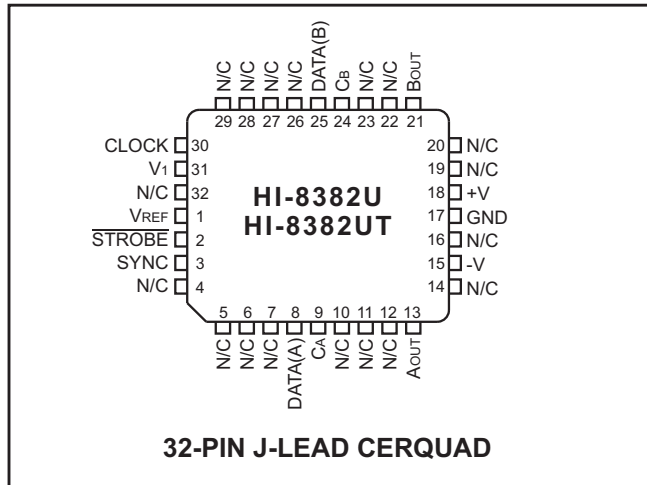
PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION	OUTPUT SERIES	
		RESISTANCE	FUSE
8382	16 PIN PLASTIC DIP	37.5 Ohms	Yes
8383	16 PIN PLASTIC DIP	13 Ohms	No

ADDITIONAL PIN CONFIGURATIONS

(See page 1 for the 16-pin Ceramic Side-Brazed DIP Package)



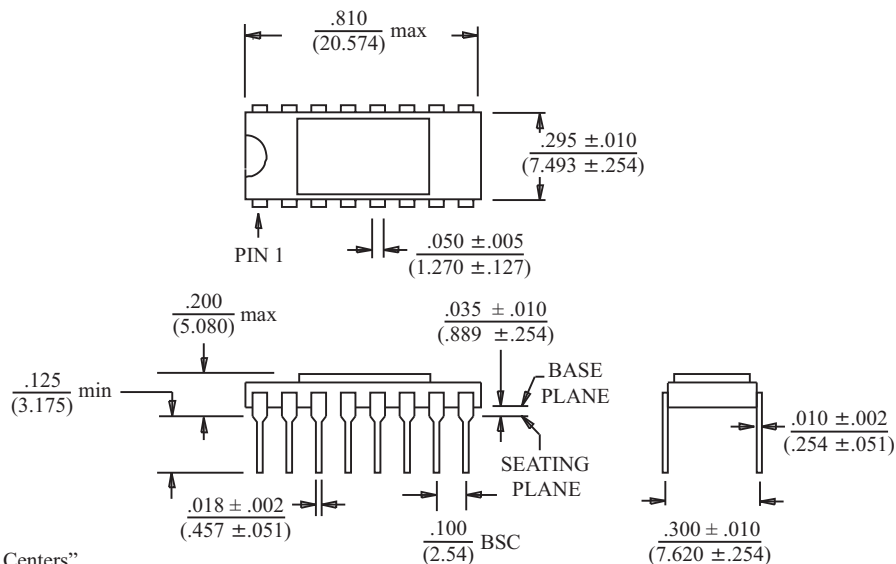
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8382	E	02/26/09	Clarified the temperature ranges, and Note (1) in the Ordering Information.
	F	09/16/11	Realigned pin names and numbers with package pin locations in Additional Pin Configuration drawings.
	G	09/10/13	Added Plastic DIP package option.

16-PIN CERAMIC SIDE-BRAZED DIP

inches (millimeters)

Package Type: 16C

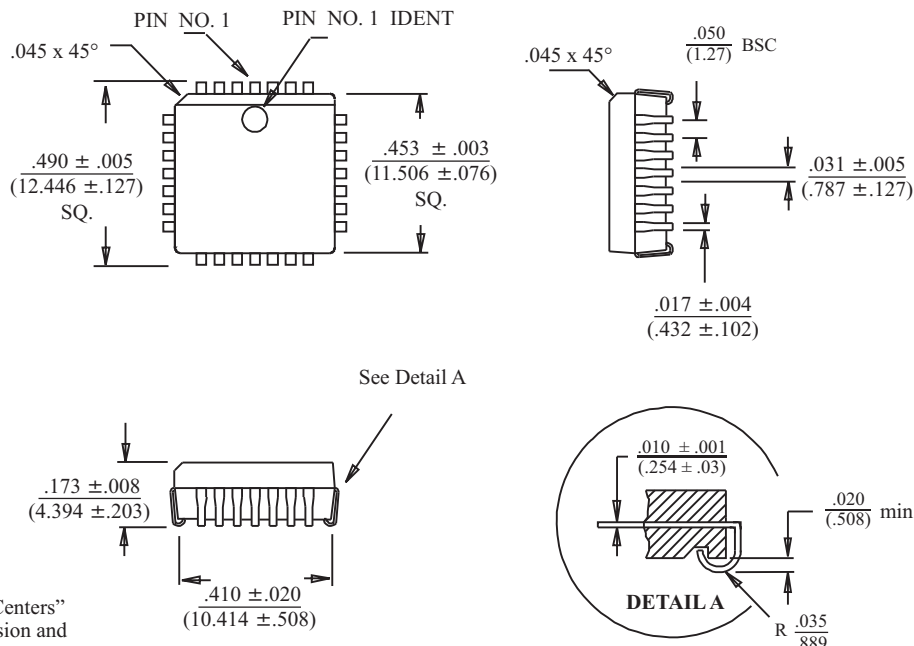


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

28-PIN PLASTIC PLCC

inches (millimeters)

Package Type: 28J

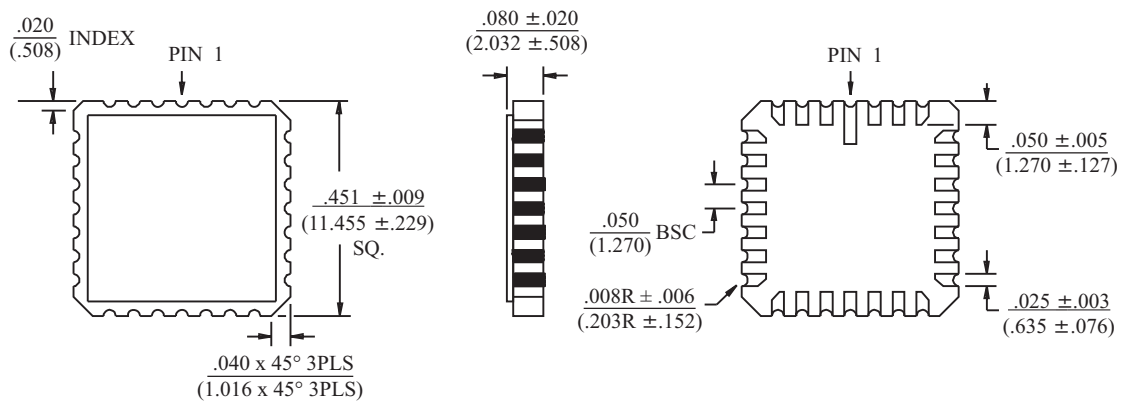


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28-PIN CERAMIC LEADLESS CHIP CARRIER

inches (millimeters)

Package Type: 28S

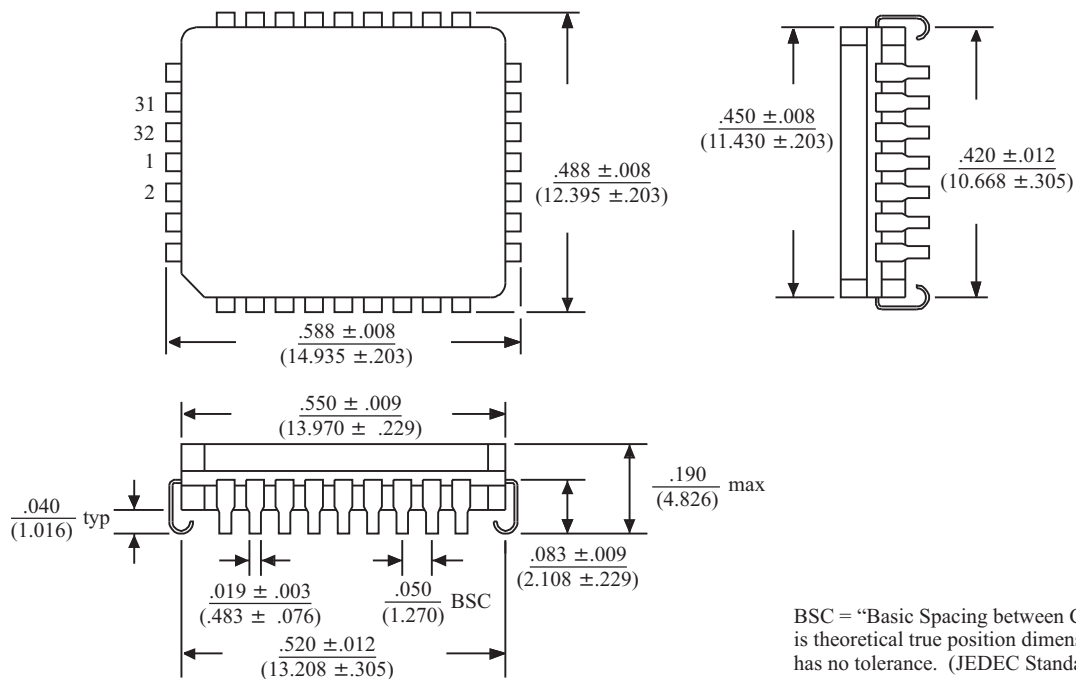


BSC = "Basic Spacing between Centers"
is theoretical true position dimension and
has no tolerance. (JEDEC Standard 95)

32-PIN J-LEAD CERQUAD

inches (millimeters)

Package Type: 32U

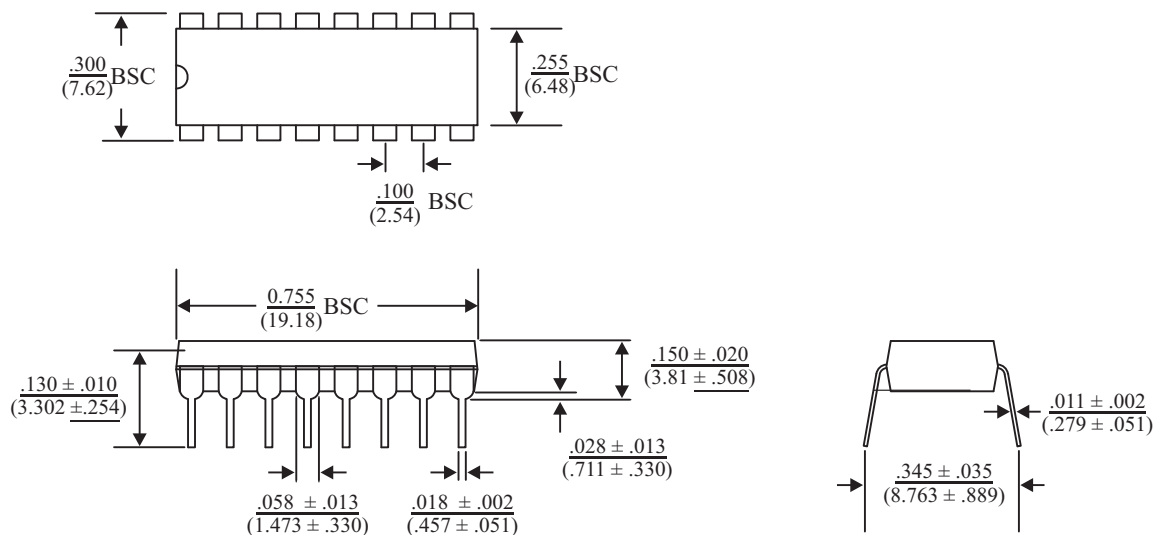


BSC = "Basic Spacing between Centers"
is theoretical true position dimension and
has no tolerance. (JEDEC Standard 95)

16-PIN PLASTIC DUAL IN-LINE PACKAGE (PDIP) (300mil Body)

inches (millimeters)

Package Type: 16PDIP



BSC = "Basic Spacing between Centers"
is theoretical true position dimension and
has no tolerance. (JEDEC Standard 95)