FUNCTIONAL DESCRIPTION

The SYNC and CLOCK inputs establish data synchronization utilizing two AND gates, one for each data input. Each logic input, including the power enable (STROBE) input, are TTL/CMOS compatible. Besides reducing chip current drain, STROBE also floats each output. However the overvoltage fuses and diodes of the HI-8382 are not switched out.

Figure 1 illustrates a typical ARINC 429 bus application. Three power supplies are necessary to operate the HI-8382; typically +15V, -15V and +5V. The chip also works with $\pm 12V$ supplies. The +5V supply can also provide a reference voltage that determines the output voltage swing. The differential output voltage swing will equal 2VREF. If a value of VREF other than +5V is needed, a separate +5V power supply is required for pin V1.

With the DATA (A) input at a logic high and DATA (B) input at a logic low, AOUT will switch to the +VREF rail and BOUT will switch to the -VREF rail (ARINC HIGH state). With both data input signals at a logic low state, the outputs will both switch to OV (ARINC NULL state).

The driver output impedance, Rout, is nominally 75 ohms. The rise and fall times of the outputs can be calibrated through the selection of two external capacitor values that are connected to the CA and CB input pins. Typical values for high-speed operation (100KBPS) are CA = CB = 75pF and for low-speed operation (12.5 to 14KBPS) CA = CB = 500pF. The driver can be externally powered down by applying a logic high to the $\overline{\text{STROBE}}$ input pin. If this feature is not being used, the pin should be tied to ground.

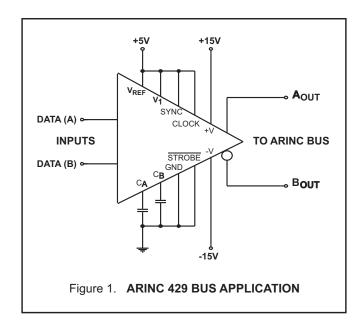
The CA and CB pins are inputs to unity gain amplifiers. Therefore they must be allowed to swing to -5V. Provision to

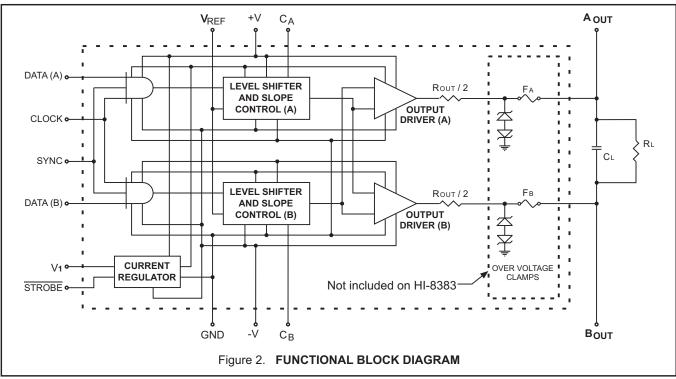
switch capacitors must be done with analog switches that allow voltages below their ground.

Both ARINC outputs of the HI-8382 are protected by internal fuses capable of sinking between 800 - 900 mA for short periods of time ($125\mu s$).

POWER SUPPLY SEQUENCING

The power supplies should be controlled to prevent large currents during supply turn-on and turn-off. The recommended sequence is +V followed by V1, always ensuring that +V is the most positive supply. The -V supply is not critical and can be asserted at any time.





PIN DESCRIPTIONS

SYMBOL	FUNCTION	DESCRIPTION
VREF	POWER	THE REFERENCE VOLTAGE USED TO DETERMINE THE OUTPUT VOLTAGE SWING
STROBE	INPUT	A LOGIC HIGH ON THIS INPUT PLACES THE DRIVER IN POWER DOWN MODE
SYNC	INPUT	SYNCHRONIZES DATA INPUTS
DATA (A)	INPUT	DATA INPUT TERMINAL A
Са	INPUT	CONNECTION FOR DATA (A) SLEW-RATE CAPACITOR
Аоит	OUTPUT	ARINC OUTPUT TERMINAL A
-V	POWER	-12V to -15V
GND	POWER	0.0V
+V	POWER	+12V to +15V
Воит	OUTPUT	ARINC OUTPUT TERMINAL B
Св	INPUT	CONNECTION FOR DATA (B) SLEW-RATE CAPACITOR
DATA (B)	INPUT	DATA INPUT TERMINAL B
CLOCK	INPUT	SYNCHRONIZES DATA INPUTS
V1	POWER	+5V ±5%

ABSOLUTE MAXIMUM RATINGS

All Voltages referenced to GND, TA = Operating Temperature Range (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	OPERATING RANGE	MAXIMUM	UNIT
Differential Voltage	VDIF	Voltage between +V and -V terminals		40	V
Supply Voltage	+V -V V1		+10.8 to +16.5 -10.8 to -16.5 +5 ±5%	+7	V V
Voltage Reference	VREF	For ARINC 429 For Applications other than ARINC	+5 ±5% 0 to 6	6 6	V
Input Voltage Range	VIN			≥ GND -0.3 ≤ V1 +0.3	V
Output Short-Circuit Duration		See Note: 1			
Output Overvoltage Protection		See Note: 2			
Operating Temperature Range	Та	Extended Industrial	-55 to +125 -40 to +85		သို့
Storage Temperature Range	Тѕтс	Ceramic & Plastic	-65 to +150		°C
Lead Temperature		Soldering, 10 seconds		+275	°C
Junction Temperature	TJ			+175	°C
Power Dissipation	PD	16-Pin Ceramic DIP See Note: 3 28-Pin Ceramic LCC See Note: 3 28-Pin Plastic PLCC See Note: 3 32-Pin CERQUAD See Note: 3		1.725 1.120 2.143 1.725	W W W
Thermal Resistance, (Junction-to-Ambient)	ØJA	16-Pin Ceramic DIP 28-Pin Ceramic LCC 28-Pin Plastic PLCC 32-Pin CERQUAD		86.5 133.7 70.0 86.5	°C/W °C/W °C/W °C/W

Heatsinking may be required for Output Short Circuit at +125°C and for 100KBPS at +125°C. Note 1.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The fuses used for Output Overvoltage Protection may be blown by the presence of a voltage at either output that is greater than ±12.0V with respect to GND. (HI-8382 only)

Derate above +25°C, 11.5mW/°C for 16-PIN DIP and 32-PIN CERQUAD, 7.5 mW/°C for 28-PIN LCC, 14.2 mW/°C for 28-PIN PLCC

DC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V1 = VREF = +5.0V, TA = Operating Temperature Range (unless otherwise specified).

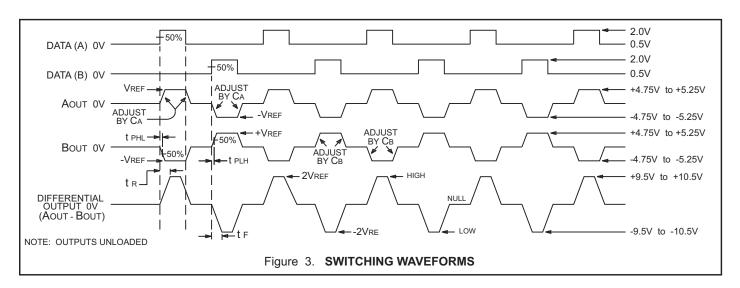
PARAMETER	SYMBOL	CONI	DITION	MIN	TYP	MAX	UNITS
Supply Current +V (Operating)	ICCOP (+V)	No Load	(0 - 100KBPS)			+11	mA
Supply Current -V (Operating)	ICCOP (-V)	No Load	(0 - 100KBPS)	-11			mA
Supply Current V1 (Operating)	ICCOP (V1)	No Load	(0 - 100KBPS)			500	μA
Supply Current VREF (Operating)	ICCOP (VREF)	No Load	(0 - 100KBPS)			500	μΑ
Supply Current +V (Power Down)	ICCPD (+V)	STROBE = HIG	Н			475	uA
Supply Current -V (Power Down)	ICCPD (-V)	STROBE = HIG	Н	-475			uA
Supply Current +V (During Short Circuit Test)	Isc (+V)	Short to Ground	(See Note: 1)			150	mA
Supply Current -V (During Short Circuit Test)	Isc (-V)	Short to Ground	(See Note: 1)	-150			mA
Output Short Circuit Current (Output High)	Ionsc	Short to Ground	VMIN=0 (See Note: 2)			-80	mA
Output Short Circuit Current (Output Low)	lolsc	Short to Ground	VMIN=0 (See Note: 2)	+80			mA
Input Current (Input High)	Iн					1.0	μΑ
Input Current (Input Low)	lıL					-1.0	μA
Input Voltage High	ViH			2.0			V
Input Voltage Low	VIL					0.5	V
Output Voltage High (Output to Ground)	Voн	No Load	(0 -100KBPS)	+VREF 25		+VREF +.25	V
Output Voltage Low (Output to Ground)	Vol	No Load	(0 -100KBPS)	-VREF 25		-VREF +.25	V
Output Voltage Null	VNULL	No Load	(0-100KBPS)	-250		+250	mV
Input Capacitance	CIN	See Note 1			15		pF

Note 1. Not tested, but characterized at initial device design and after major process and/or design change which affects this parameter.

AC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V1 = VREF = +5.0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDI	TION	MIN	TYP	MAX	UNITS
Rise Time (AOUT, BOUT)	t R	CA = CB = 75pF	See Figure 3.	1.0		2.0	μs
Fall Time (AOUT, BOUT)	t F	CA = CB = 75pF	See Figure 3.	1.0		2.0	μs
Propagtion Delay Input to Output	t PLH	CA = CB = 75pF	See Figure 3.			3.0	μs
Propagtion Delay Input to Output	t PHL	CA = CB = 75pF	See Figure 3.			3.0	μs



Note 2. Interchangeability of force and sense is acceptable.

HI-8382 PACKAGE THERMAL CHARACTERISTICS

MAXIMUM ARINC LOAD 7

PACKAGE STYLE 1	ARINC 429	SUPPLY CURRENT (mA) ²			JUNCTION TEMP, Tj (°C)		
PACKAGE STILE	DATA RATE	Ta = 25°C	Ta = 85°C	Ta = 125°C	Ta = 25°C	Ta = 85°C	Ta = 125°C
28 Lead PLCC	Low Speed ³	17.6	17.2	17.0	48	107	142
	High Speed ⁴	25.4	24.5	24.2	56	110	150
16 Lead Ceramic SB DIP	Low Speed	17.9	17.4	17.1	41	103	145
	High Speed	25.8	24.8	24.4	47	112	147

AOUT and BOUT Shorted To Ground 5, 6, 7

PACKAGE STYLE 1	ARINC 429	SUPPLY CURRENT (mA) ²			JUNCTION TEMP, Tj (°C)		
PACKAGE STILE	DATA RATE	Ta = 25°C	Ta = 85°C	Ta = 125°C	Ta = 25°C	Ta = 85°C	Ta = 125°C
001 10100	Low Speed ³	60.1	55.7	52.4	110	157	194
28 Lead PLCC	High Speed ⁴	63.1	56.3	52.3	100	150	182
46 Load Conomic CD DID	Low Speed	62.1	56.2	53.0	90	145	180
16 Lead Ceramic SB DIP	High Speed	64.0	56.2	52.2	86	144	176

Notes:

- 1. All data taken in still air on devices soldered to a single layer copper PCB (3" X 4.5" X .062").
- 2. At 100% duty cycle, 15V power supplies. For 12V power supplies multiply all tabulated values by 0.8.
- 3. Low Speed: Data Rate = 12.5 Kbps, Load: R = 400 Ohms, C = 30 nF.
- 4. High Speed: Data Rate = 100 Kbps, Load: R = 400 Ohms, C = 10 nF. Data not presented for C = 30 nF as this is considered unrealistic for high speed operation.
- 5. Similar results would be obtained with AOUT shorted to BOUT.
- 6. For applications requiring survival with continuous short circuit, operation above Tj = 175°C is not recommended.
- 7. Data will vary depending on air flow and the method of heat sinking employed.

ORDERING INFORMATION

HI - 838x x x - xx (Ceramic)

	PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	NOTES
	Blank	-40°C to +85°C	I	No	
ı	Т	-55°C to +125°C	Т	No	
ı	M-01	-55°C to +125°C	М	Yes	(1)
	M-03	-55°C to +125°C	DSCC	Yes	(1) & (2)

PART NUMBER	PACKAGE DESCRIPTION	LEAD FINISH	NOTES
С	16 PIN CERAMIC SIDE BRAZED DIP (16C)	Gold	(3) & (1)
S	28 PIN CERAMIC LEADLESS CHIP CARRIER (28S)	Gold	(3) & (1)
U	32 PIN CERQUAD (32U) not available with 'M' flow	Tin/Lead Solder	

PART	OUTPUT SERIES			
NUMBER	RESISTANCE	FUSE		
8382	37.5 Ohms	Yes		
8383	13 Ohms	No		

- (1) Process Flows M and DSCC always have Tin/Lead (Sn/Pb) solder lead finish.
- (2) DSCC SMD# 5962-8687901EA. Only available in "C" package with Sn/Pb solder lead finish.
- (3) Gold terminal finish is Pb-Free, RoHS compliant.

HI - <u>838xJ</u> <u>x</u> <u>x</u> (Plastic)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

	PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
ı	Blank	-40°C to +85°C	I	No
ı	Т	-55°C to +125°C	Т	No

PART	171111		OUTPUT SERIES			
NUMBER	DESCRIPTION	RESISTANCE	FUSE			
8382J	28 PIN PLASTIC PLCC (28J) (1)	37.5 Ohms	Yes			
8383J	28 PIN PLASTIC PLCC (28J) (1)	13 Ohms	No			

(1) NOT RECOMMENDED FOR NEW DESIGNS. The newer HI-3182PJxx and HI-3183PJxx are drop-in replacements for the older HI-8382Jxx and HI-8383Jxx respectively.

HI - 838x PDx x (Plastic DIP)

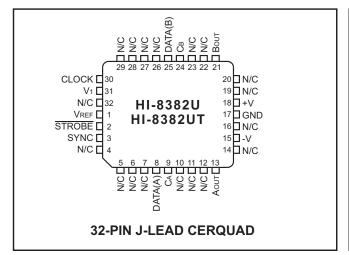
PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

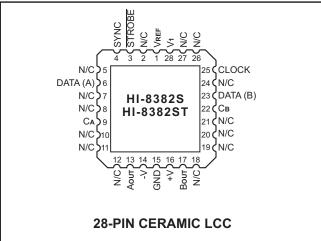
PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
Т	-55°C to +125°C	Т	No
М	-55°C to +125°C	М	Yes

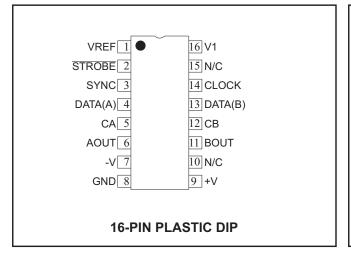
PART	PACKAGE	OUTPUT SERIES	
NUMBER	DESCRIPTION	RESISTANCE	FUSE
8382	16 PIN PLASTIC DIP	37.5 Ohms	Yes
8383	16 PIN PLASTIC DIP	13 Ohms	No

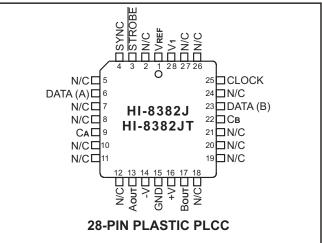
ADDITIONAL PIN CONFIGURATIONS

(See page 1 for the 16-pin Ceramic Side-Brazed DIP Package)









REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8382	Е	02/26/09	Clarified the temperature ranges, and Note (1) in the Ordering Information.
	F	09/16/11	Realigned pin names and numbers with package pin locations in Additional Pin Configuration drawings.
	G	09/10/13	Added Plastic DIP package option.

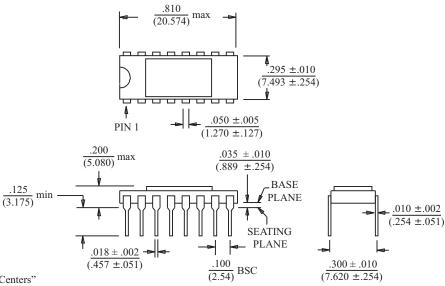


HI-8382 PACKAGE DIMENSIONS

16-PIN CERAMIC SIDE-BRAZED DIP

inches (millimeters)

Package Type: 16C

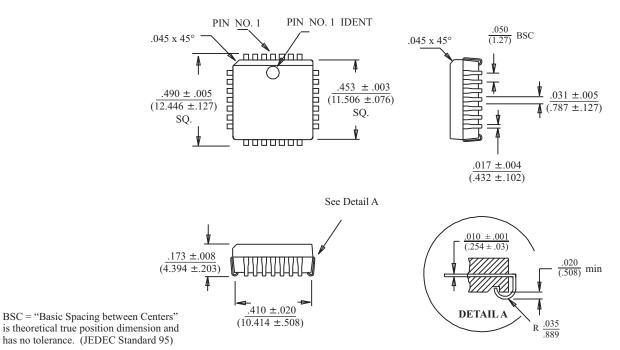


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

28-PIN PLASTIC PLCC

inches (millimeters)

Package Type: 28J



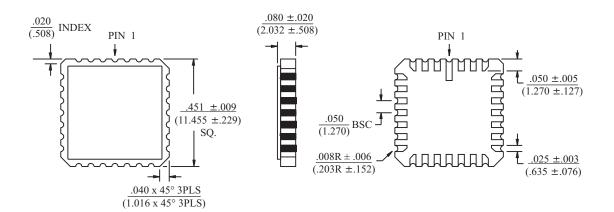


HI-8382 PACKAGE DIMENSIONS

28-PIN CERAMIC LEADLESS CHIP CARRIER

inches (millimeters)

Package Type: 28S

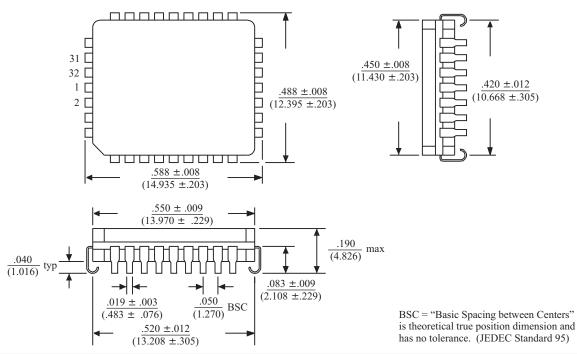


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

32-PIN J-LEAD CERQUAD

inches (millimeters)

Package Type: 32U



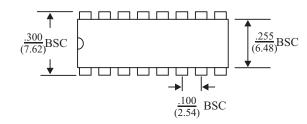


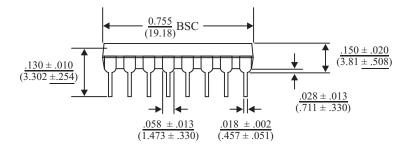
HI-8382 PACKAGE DIMENSIONS

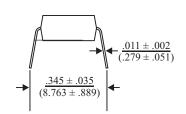
16-PIN PLASTIC DUAL IN-LINE PACKAGE (PDIP) (300mil Body)

inches (millimeters)

Package Type: 16PDIP







BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)