

# 1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32G232 devices.

**Table 1.1. Ordering Information**

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32G232F32-QFP64	32	8	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F64-QFP64	64	16	32	1.98 - 3.8	-40 - 85	TQFP64
EFM32G232F128-QFP64	128	16	32	1.98 - 3.8	-40 - 85	TQFP64

Adding the suffix 'T' to the part number (e.g. EFM32G232F32-QFP64T) denotes tray.

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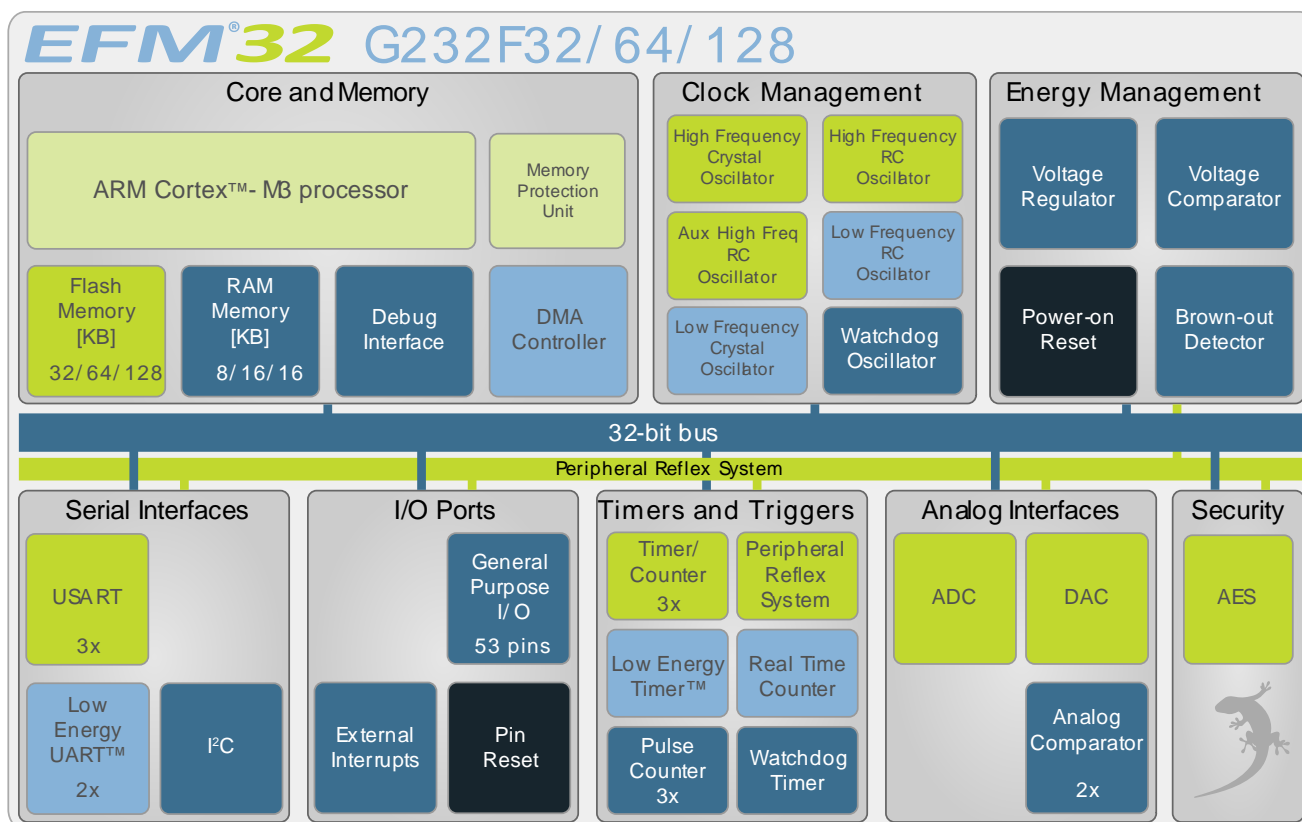
## 2 System Summary

### 2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32G microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32G232 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32G Reference Manual*.

A block diagram of the EFM32G232 is shown in Figure 2.1 (p. 3) .

**Figure 2.1. Block Diagram**



#### 2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32G Cortex-M3 Reference Manual*.

#### 2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

#### 2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32G microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided

into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

### 2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230  $\mu$ DMA controller licensed from ARM.

### 2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32G.

### 2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32G microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

### 2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32G. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

### 2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

### 2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

### 2.1.10 Inter-Integrated Circuit Interface (I2C)

The I<sup>2</sup>C module provides an interface between the MCU and a serial I<sup>2</sup>C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I<sup>2</sup>C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

### 2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, and IrDA devices.

### 2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

### 2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART<sup>™</sup>, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

### 2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

### 2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

### 2.1.16 Low Energy Timer (LETIMER)

The unique LETIMER<sup>™</sup>, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

### 2.1.17 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn\_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

### 2.1.18 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

## 2.1.19 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

## 2.1.20 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

## 2.1.21 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has one single ended output buffer connected to channel 0. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

## 2.1.22 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

## 2.1.23 General Purpose Input/Output (GPIO)

In the EFM32G232, there are 53 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

## 2.2 Configuration Summary

The features of the EFM32G232 is a subset of the feature set described in the EFM32G Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

**Table 2.1. Configuration Summary**

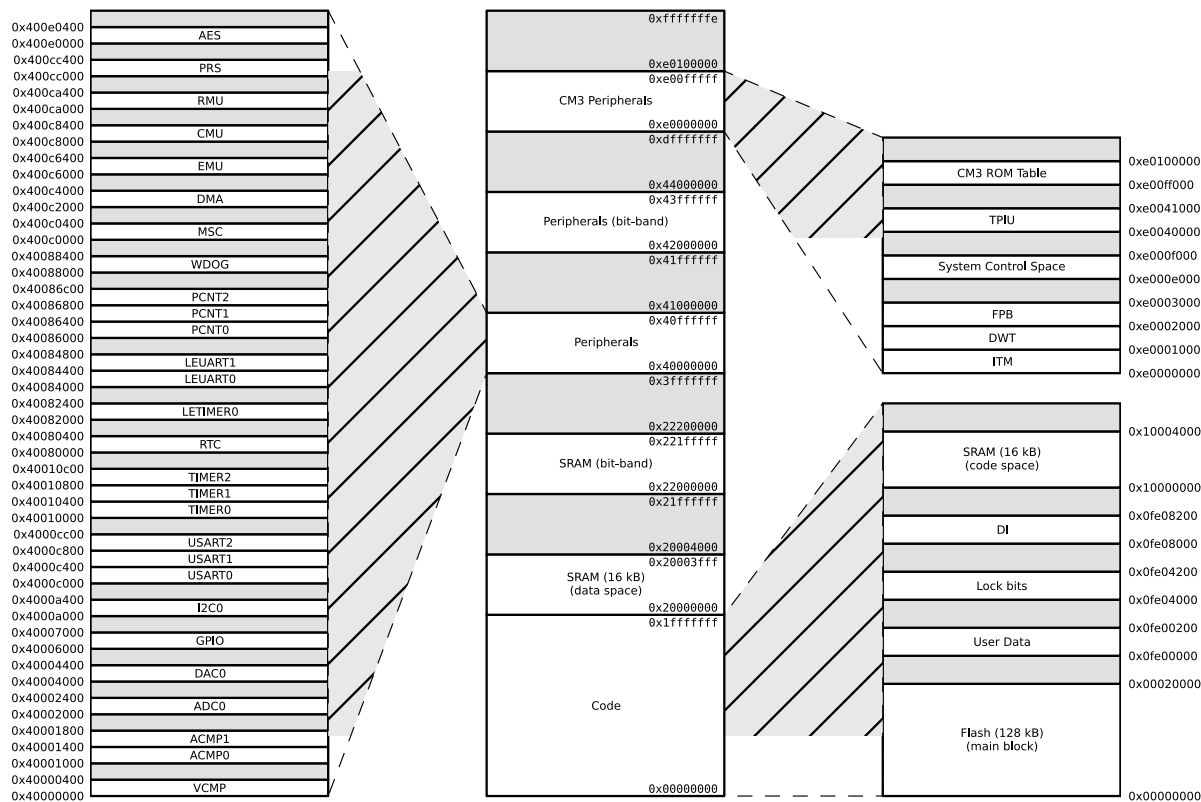
Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA

Module	Configuration	Pin Connections
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 8-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[15:8], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[0]
AES	Full configuration	NA
GPIO	53 pins	Available pins are shown in Table 4.3 (p. 53)

## 2.3 Memory Map

The *EFM32G232* memory map is shown in Figure 2.2 (p. 8), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32G232 Memory Map with largest RAM and Flash sizes



## 3 Electrical Characteristics

### 3.1 Test Conditions

#### 3.1.1 Typical Values

The typical data are based on  $T_{AMB}=25^{\circ}\text{C}$  and  $V_{DD}=3.0\text{ V}$ , as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

#### 3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

### 3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 9) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 9).

**Table 3.1. Absolute Maximum Ratings**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$T_{STG}$	Storage temperature range		-40		150 <sup>1</sup>	$^{\circ}\text{C}$
$T_S$	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	$^{\circ}\text{C}$
$V_{DDMAX}$	External main supply voltage		0		3.8	V
$V_{IOPIN}$	Voltage on any I/O pin		-0.3		$V_{DD}+0.3$	V
$I_{IOMAX}$	Current per I/O pin (sink)				100	mA
	Current per I/O pin (source)				-100	mA

<sup>1</sup>Based on programmed devices tested for 10000 hours at  $150^{\circ}\text{C}$ . Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

### 3.3 General Operating Conditions

#### 3.3.1 General Operating Conditions

**Table 3.2. General Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Unit
$T_{AMB}$	Ambient temperature range	-40		85	$^{\circ}\text{C}$
$V_{DDOP}$	Operating supply voltage	1.98		3.8	V
$f_{APB}$	Internal APB clock frequency			32	MHz
$f_{AHB}$	Internal AHB clock frequency			32	MHz



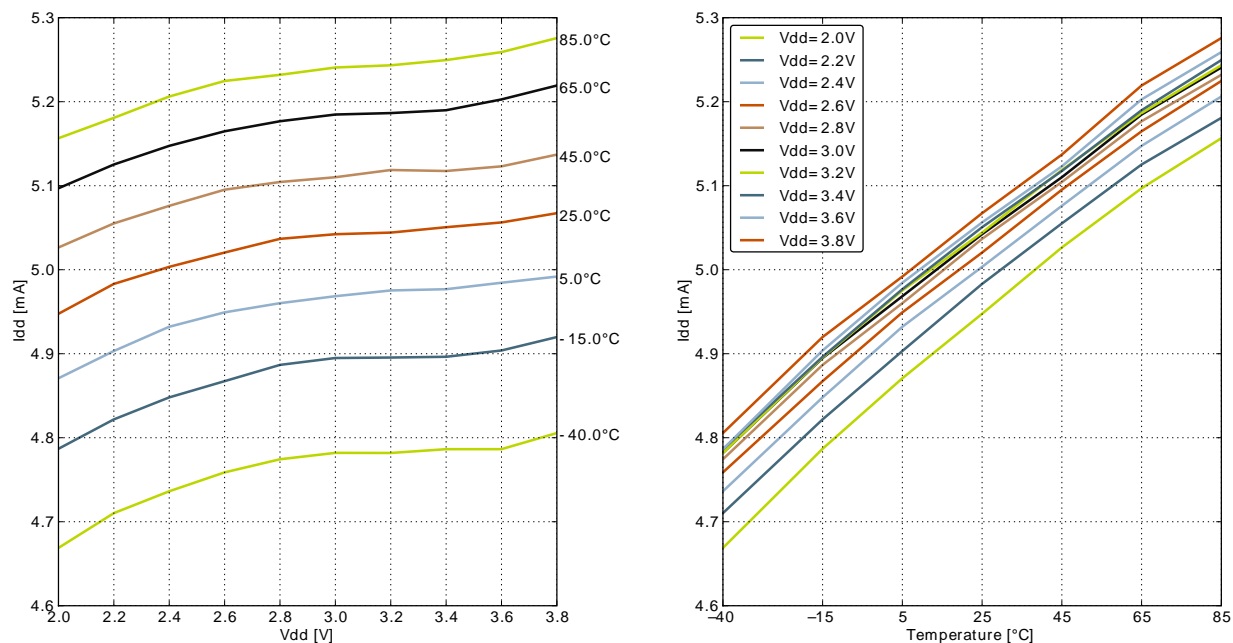
## 3.4 Current Consumption

**Table 3.3. Current Consumption**

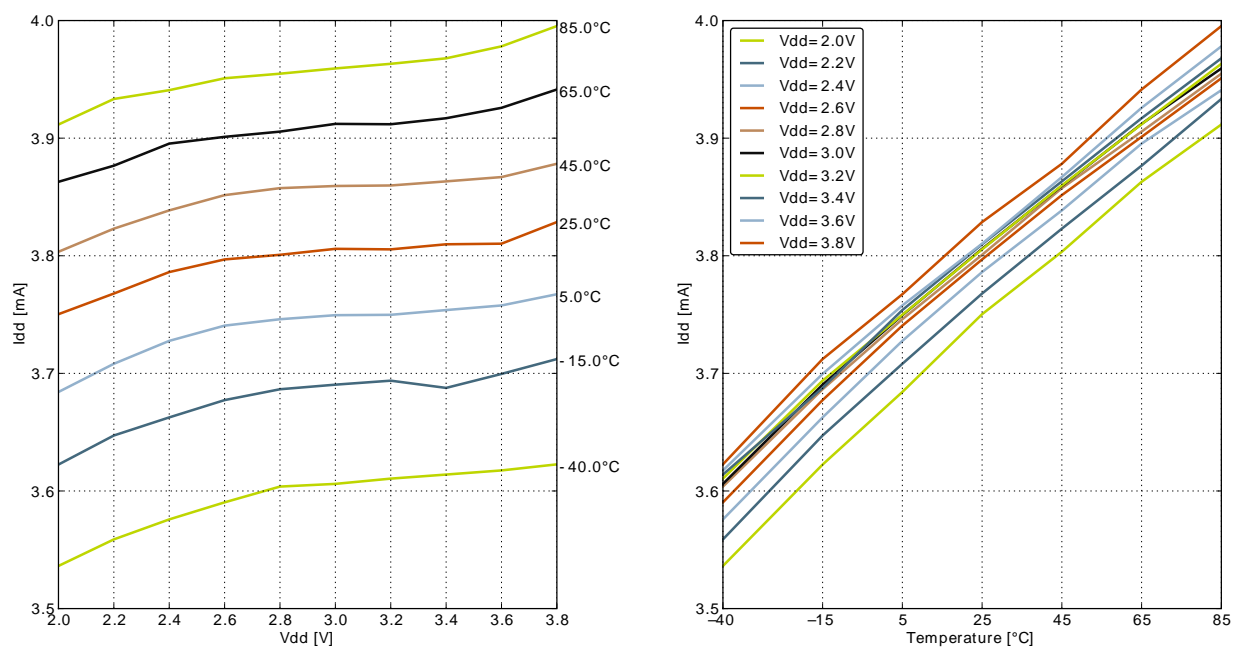
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{EM0}$	EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	32 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		180		$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		181	206	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		183	207	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		185	211	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		186	215	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		191	218	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		220		$\mu\text{A}/\text{MHz}$
$I_{EM1}$	EM1 current (Production test condition = 14 MHz)	32 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		45		$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		47	62	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		48	64	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		50	69	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		51	72	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		56	83	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$		103		$\mu\text{A}/\text{MHz}$
$I_{EM2}$	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}=3.0\text{ V}$ , $T_{AMB}=25^{\circ}\text{C}$		0.9	1.5	$\mu\text{A}$
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}=3.0\text{ V}$ , $T_{AMB}=85^{\circ}\text{C}$		3.0	6.0	$\mu\text{A}$
$I_{EM3}$	EM3 current	$V_{DD}=3.0\text{ V}$ , $T_{AMB}=25^{\circ}\text{C}$		0.59	1.0	$\mu\text{A}$
		$V_{DD}=3.0\text{ V}$ , $T_{AMB}=85^{\circ}\text{C}$		2.75	5.8	$\mu\text{A}$
$I_{EM4}$	EM4 current	$V_{DD}=3.0\text{ V}$ , $T_{AMB}=25^{\circ}\text{C}$		0.02	0.045	$\mu\text{A}$
		$V_{DD}=3.0\text{ V}$ , $T_{AMB}=85^{\circ}\text{C}$		0.25	0.7	$\mu\text{A}$

### 3.4.1 EM0 Current Consumption

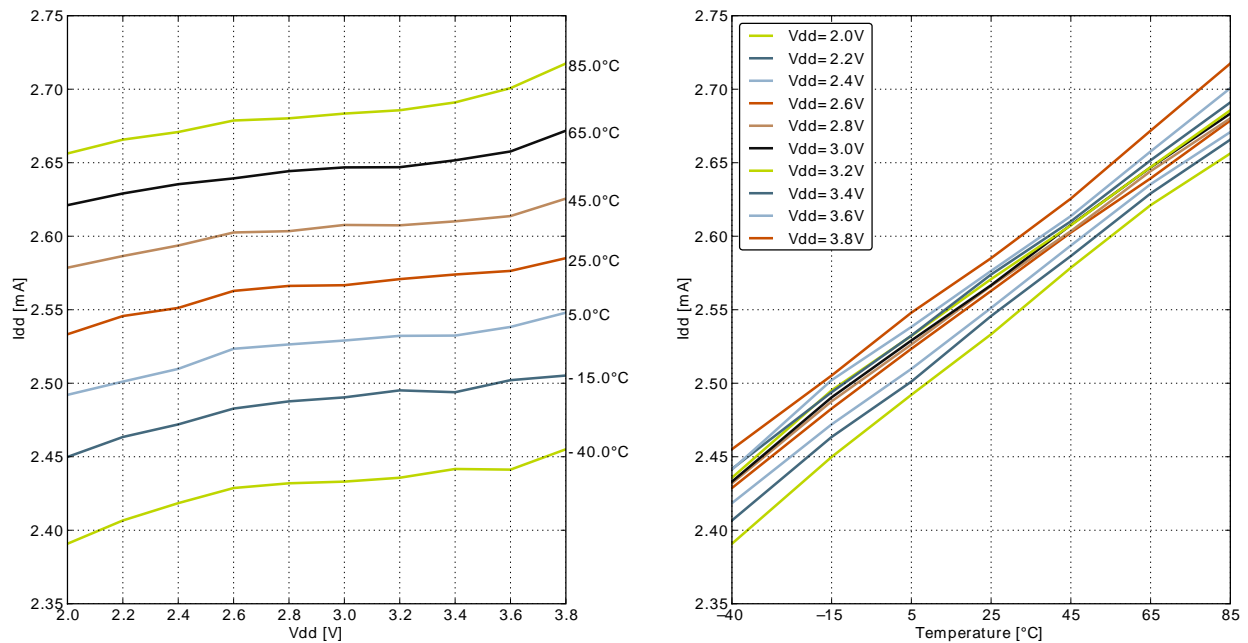
**Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 28 MHz**



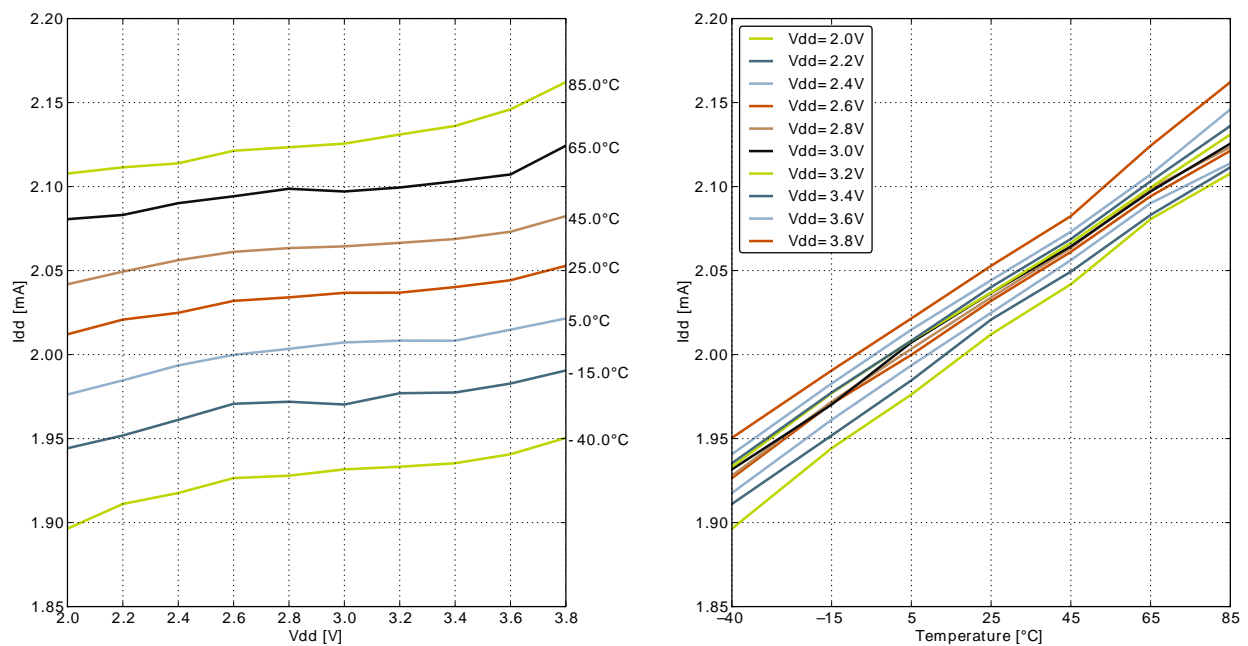
**Figure 3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz**



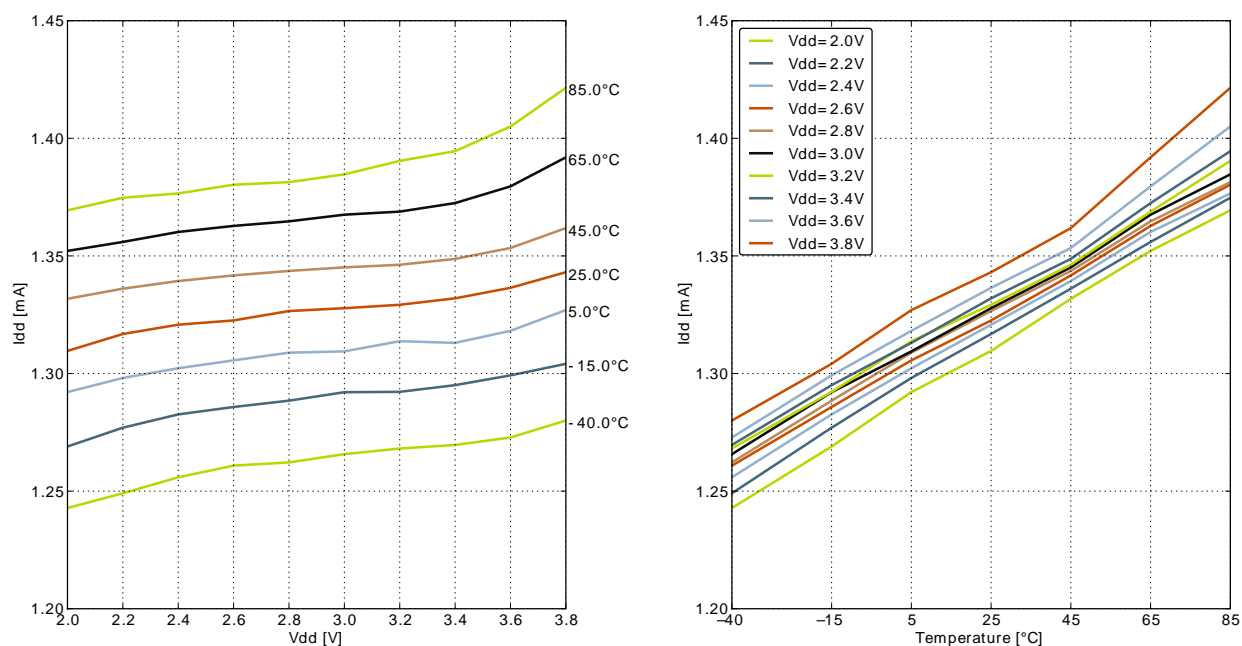
**Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz**



**Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz**

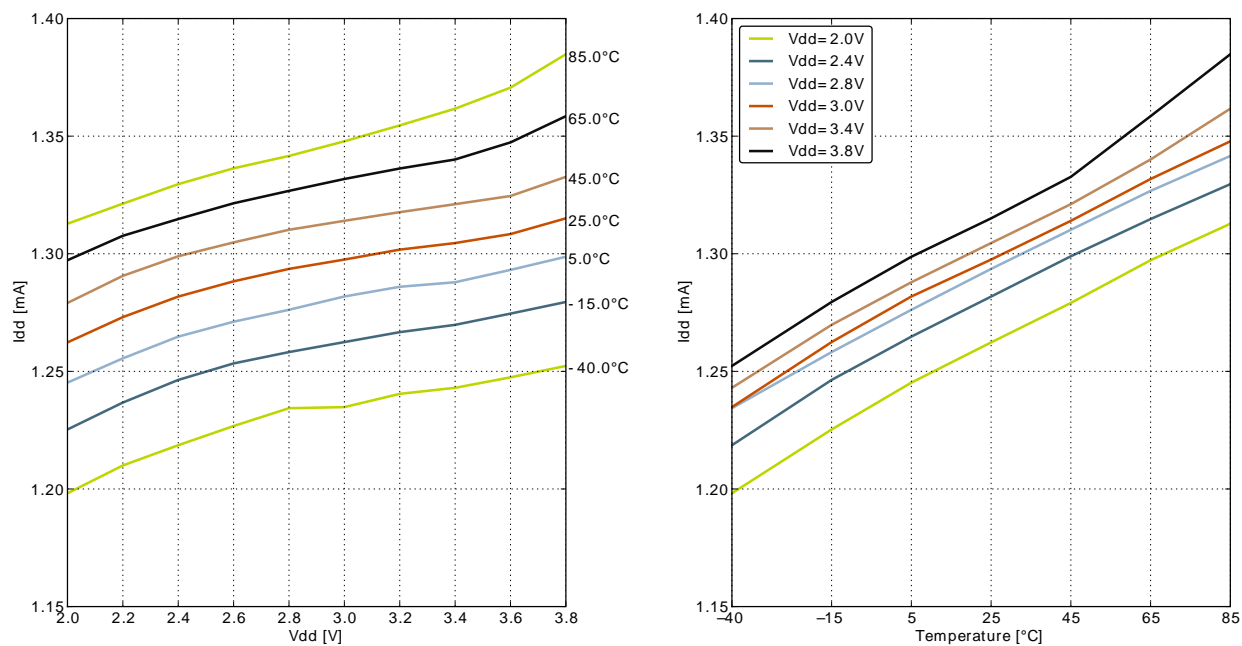


**Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 7 MHz**

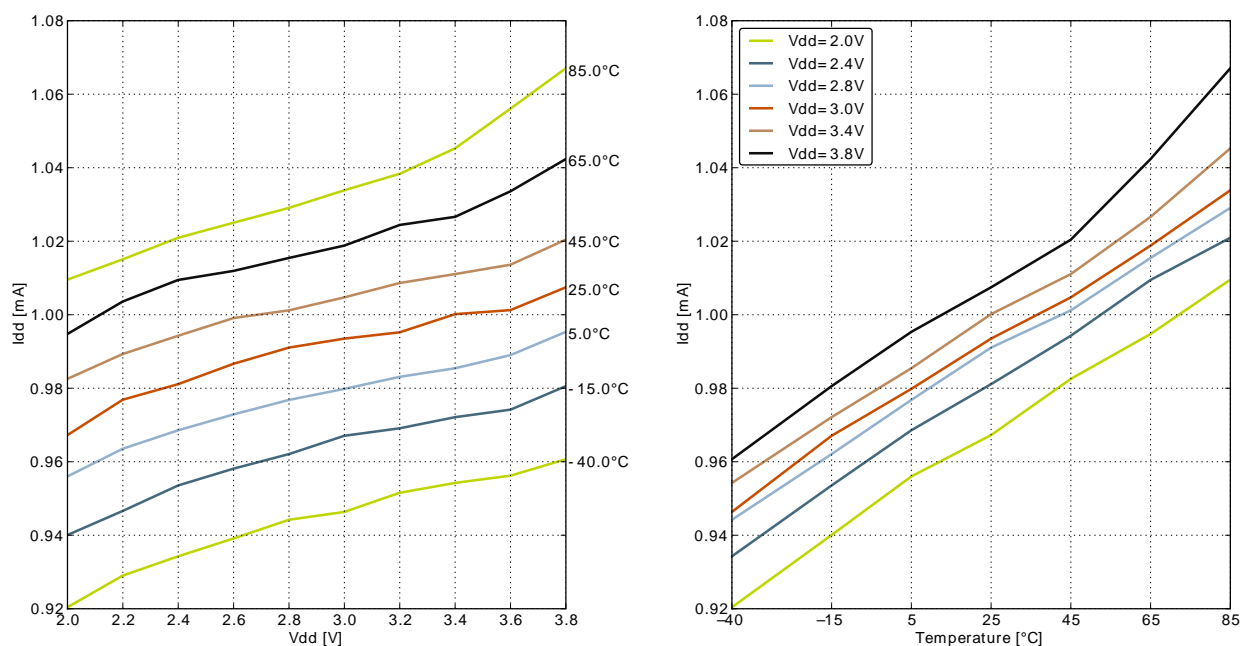


### 3.4.2 EM1 Current Consumption

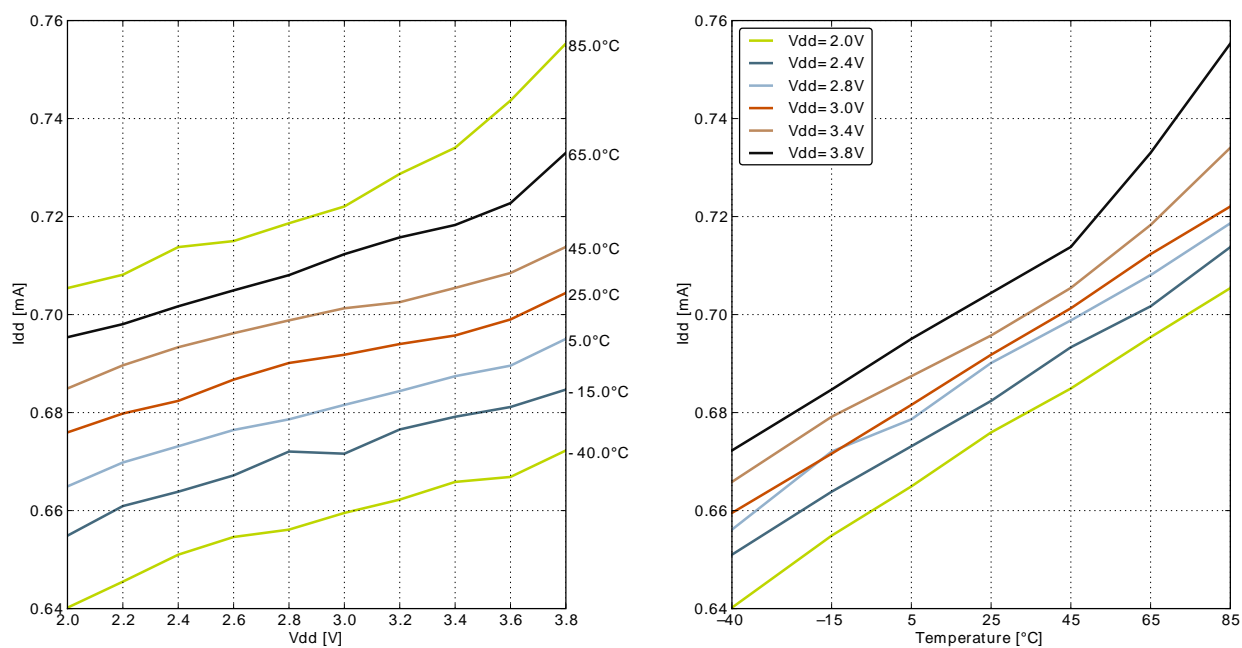
**Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 28 MHz**



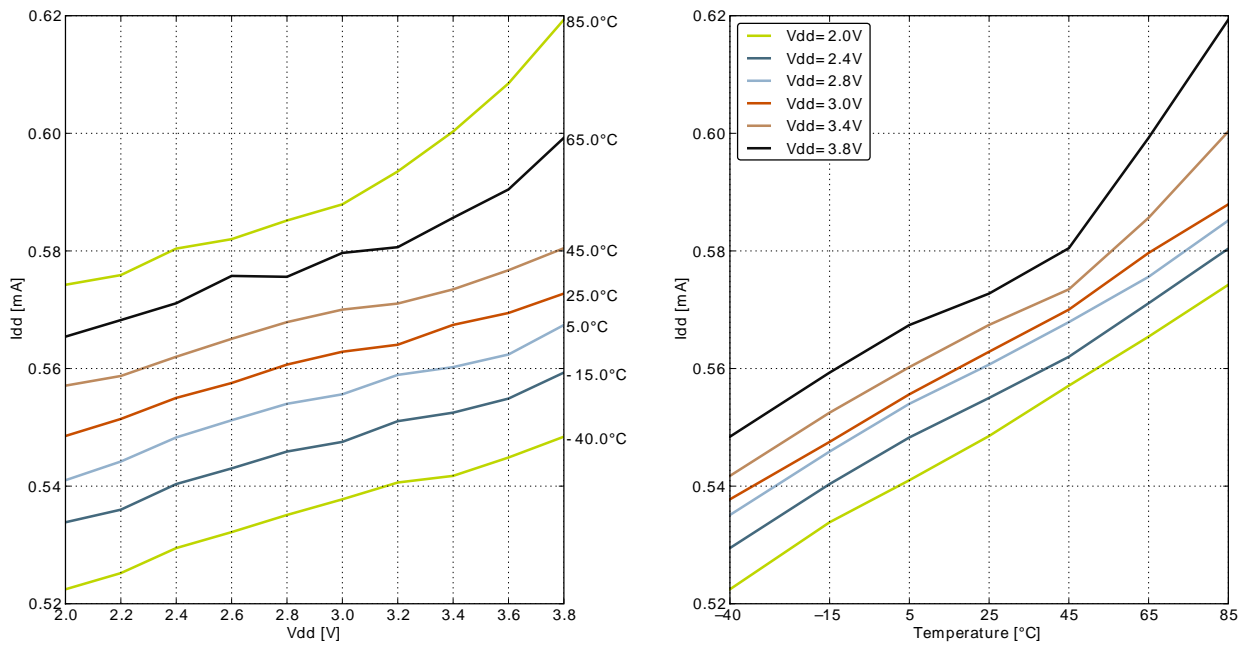
**Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz**



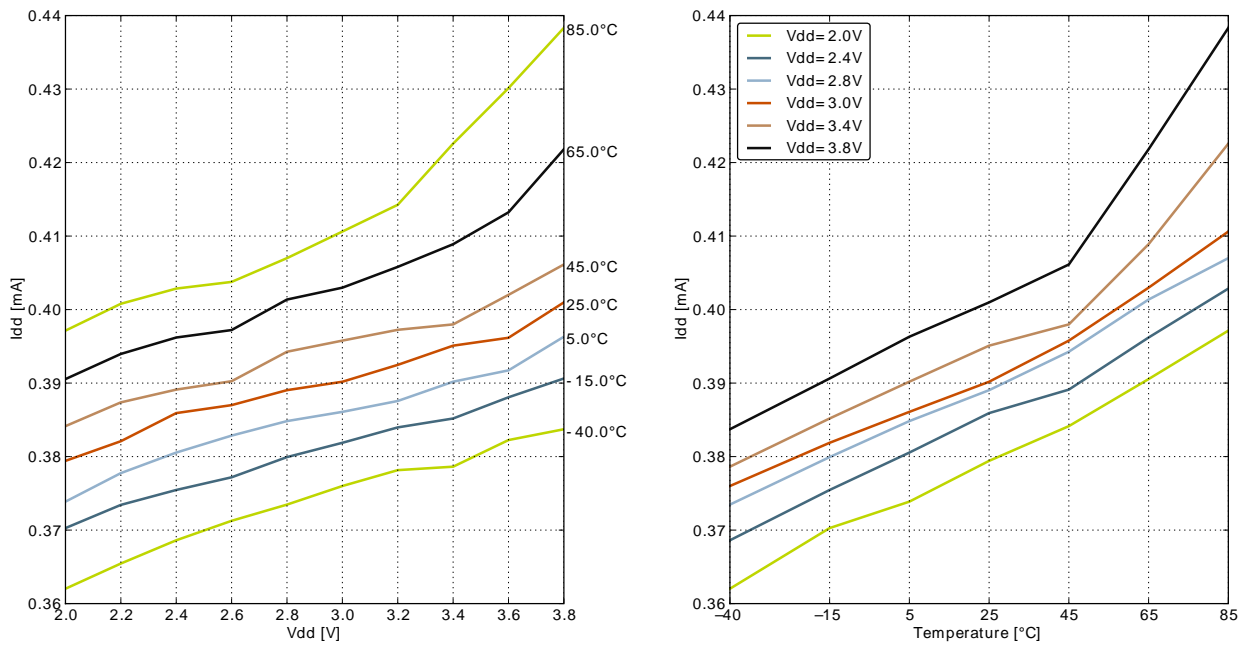
**Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz**



**Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz**

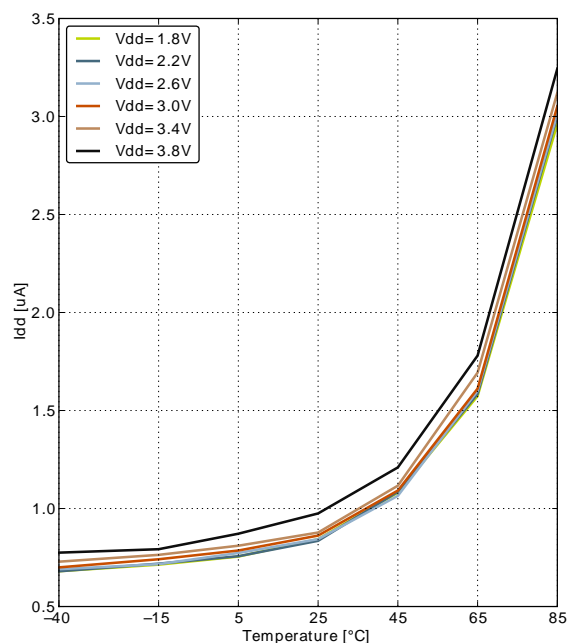
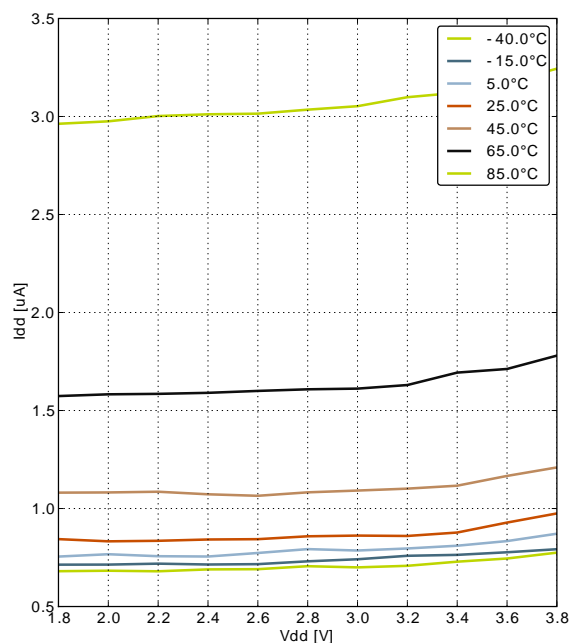


**Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 7 MHz**



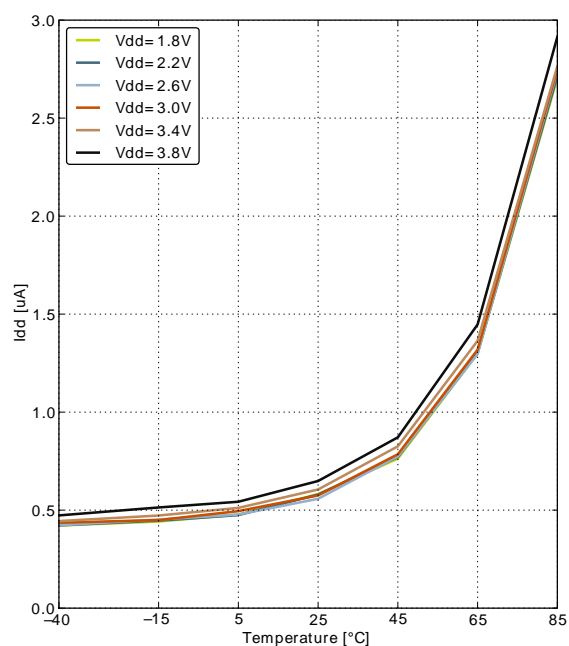
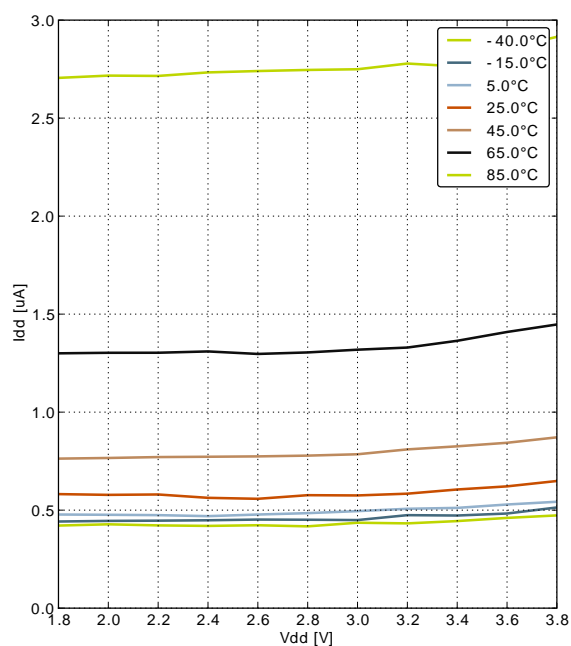
### 3.4.3 EM2 Current Consumption

Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.



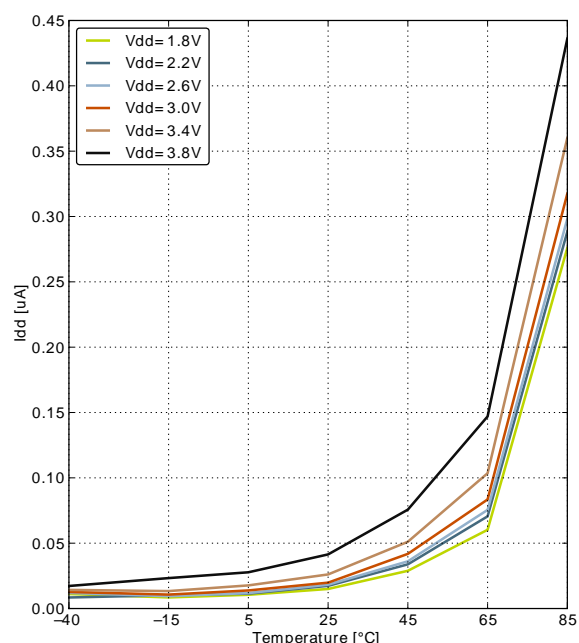
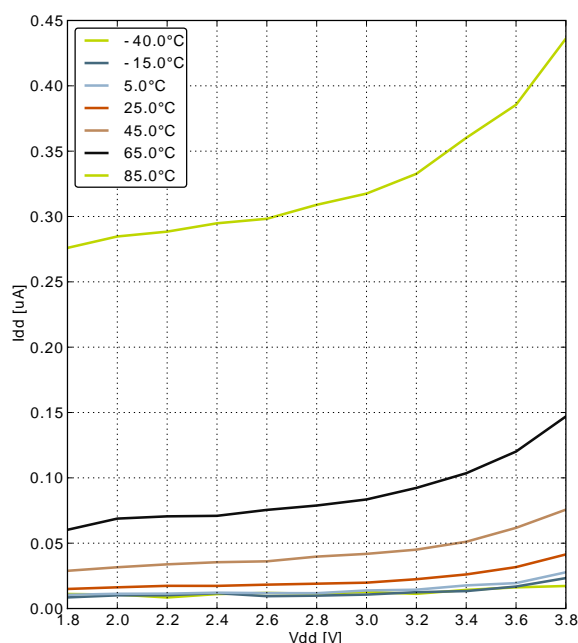
### 3.4.4 EM3 Current Consumption

Figure 3.12. EM3 current consumption.



### 3.4.5 EM4 Current Consumption

Figure 3.13. EM4 current consumption.



## 3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
$t_{EM10}$	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
$t_{EM20}$	Transition time from EM2 to EM0		2		$\mu\text{s}$
$t_{EM30}$	Transition time from EM3 to EM0		2		$\mu\text{s}$
$t_{EM40}$	Transition time from EM4 to EM0		163		$\mu\text{s}$

## 3.6 Power Management

The EFM32G requires the AVDD\_x, VDD\_DREG and IOVDD\_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".



**Table 3.5. Power Management**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>BODextthr-</sub>	BOD threshold on falling external supply voltage		1.74		1.96	V
V <sub>BODextthr+</sub>	BOD threshold on rising external supply voltage			1.85		V
V <sub>PORthr+</sub>	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t <sub>RESETdy</sub>	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
t <sub>RESET</sub>	negative pulse length to ensure complete reset of device		50			ns
C <sub>DECOUPLE</sub>	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF

## 3.7 Flash

**Table 3.6. Flash**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC <sub>FLASH</sub>	Flash erase cycles before failure		20000			cycles
RET <sub>FLASH</sub>	Flash data retention	T <sub>AMB</sub> <150°C	10000			h
		T <sub>AMB</sub> <85°C	10			years
		T <sub>AMB</sub> <70°C	20			years
t <sub>W_PROG</sub>	Word (32-bit) programming time		20			μs
t <sub>P_ERASE</sub>	Page erase time		20	20.4	20.8	ms
t <sub>D_ERASE</sub>	Device erase time		40	40.8	41.6	ms
I <sub>ERASE</sub>	Erase current				7 <sup>1</sup>	mA
I <sub>WRITE</sub>	Write current				7 <sup>1</sup>	mA
V <sub>FLASH</sub>	Supply voltage during flash erase and write		1.98		3.8	V

<sup>1</sup> Measured at 25°C

## 3.8 General Purpose Input Output

**Table 3.7. GPIO**

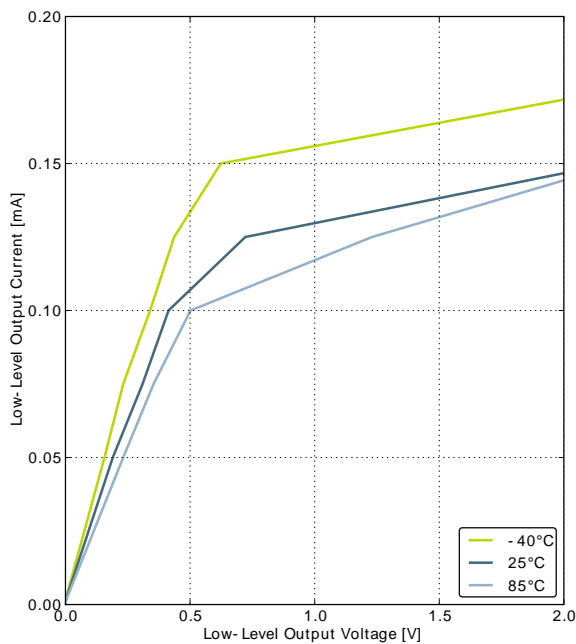
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>IOIL</sub>	Input low voltage				0.30V <sub>DD</sub> <sup>1</sup>	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>IOIH</sub>	Input high voltage		0.70V <sub>DD</sub> <sup>1</sup>			V
V <sub>IOOH</sub>	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V <sub>DD</sub>		V
		Sourcing 0.1 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V <sub>DD</sub>		V
		Sourcing 1 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V <sub>DD</sub>		V
		Sourcing 1 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V <sub>DD</sub>		V
		Sourcing 6 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V <sub>DD</sub>			V
		Sourcing 6 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V <sub>DD</sub>			V
		Sourcing 20 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60V <sub>DD</sub>			V
		Sourcing 20 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80V <sub>DD</sub>			V
V <sub>IOOL</sub>	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.20V <sub>DD</sub>		V
		Sinking 0.1 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.10V <sub>DD</sub>		V
		Sinking 1 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.10V <sub>DD</sub>		V
		Sinking 1 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.05V <sub>DD</sub>		V
		Sinking 6 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.30V <sub>DD</sub>	V
		Sinking 6 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.20V <sub>DD</sub>	V
		Sinking 20 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.35V <sub>DD</sub>	V
		Sinking 20 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.25V <sub>DD</sub>	V
I <sub>IOLEAK</sub>	Input leakage current	High Impedance IO connected to GROUND or V <sub>DD</sub>		±0.1	±40	nA

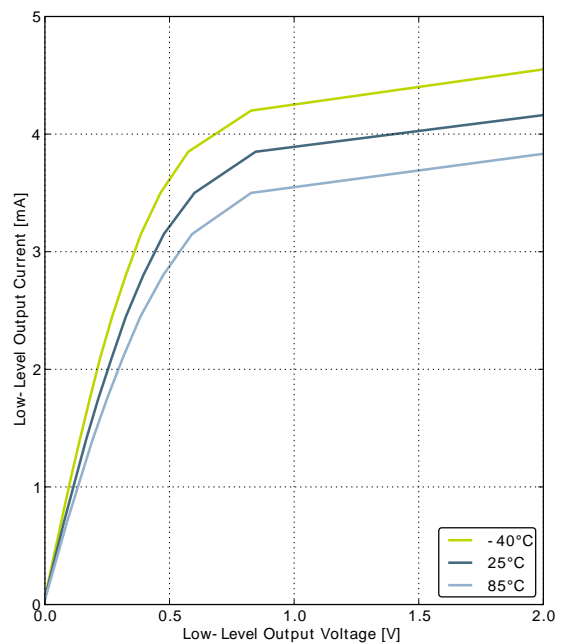
Symbol	Parameter	Condition	Min	Typ	Max	Unit
R <sub>PU</sub>	I/O pin pull-up resistor			40		kOhm
R <sub>PD</sub>	I/O pin pull-down resistor			40		kOhm
R <sub>IOESD</sub>	Internal ESD series resistor			200		Ohm
t <sub>IOGLITCH</sub>	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t <sub>IOOF</sub>	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C <sub>L</sub> =12.5-25pF.	20+0.1C <sub>L</sub>		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C <sub>L</sub> =350-600pF	20+0.1C <sub>L</sub>		250	ns
V <sub>IOHYST</sub>	I/O pin hysteresis (V <sub>IOTHR+</sub> - V <sub>IOTHR-</sub> )	V <sub>DD</sub> = 1.98 - 3.8 V	0.1V <sub>DD</sub>			V

<sup>†</sup>If the GPIO input voltage is between 0.3V<sub>DD</sub> and 0.7V<sub>DD</sub>, the current consumption will increase.

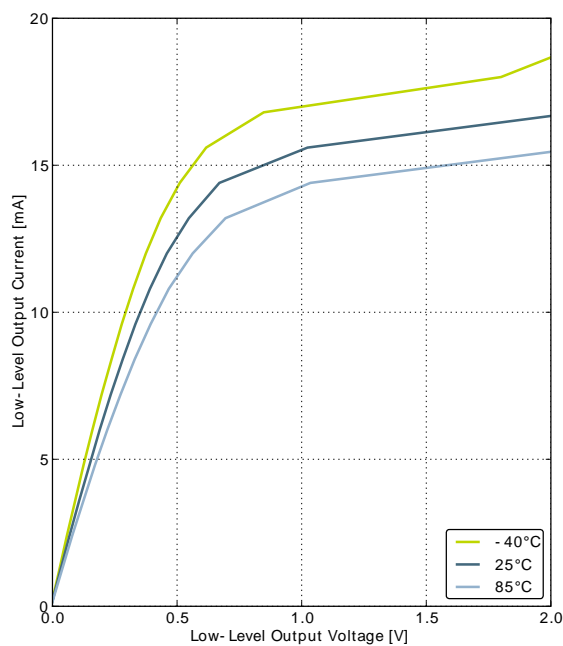
Figure 3.14. Typical Low-Level Output Current, 2V Supply Voltage



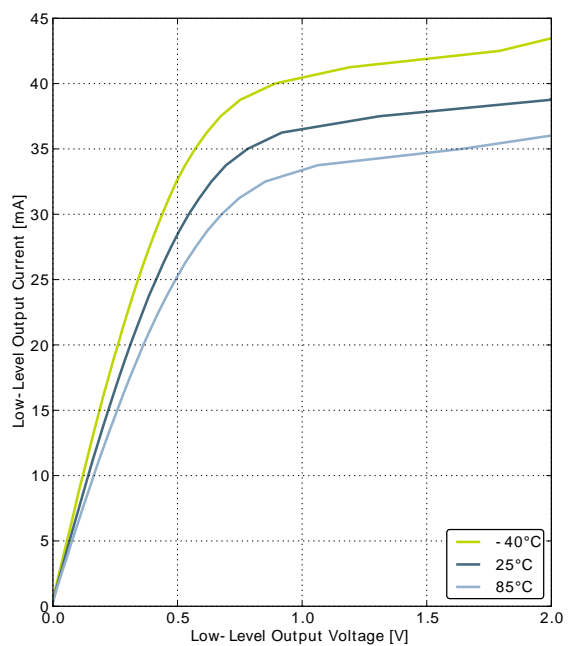
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW

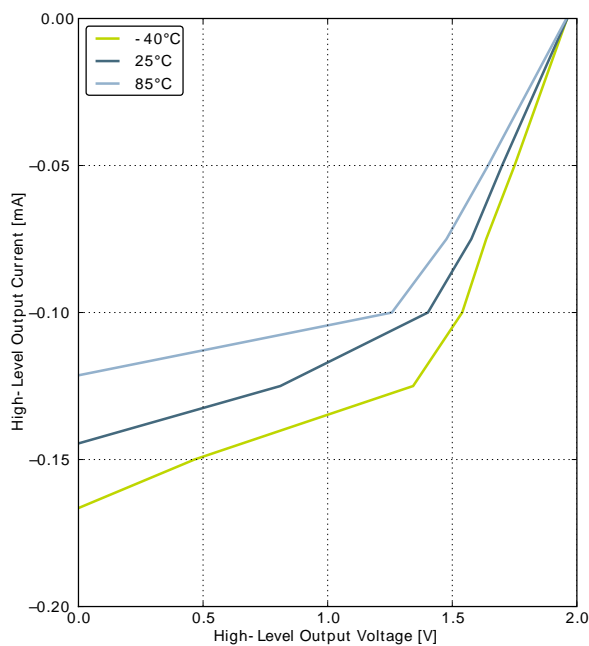


GPIO\_Px\_CTRL DRIVEMODE = STANDARD

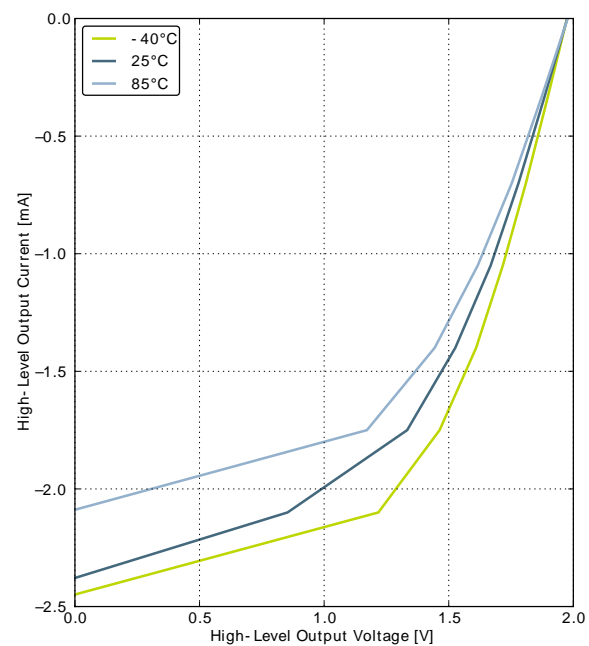


GPIO\_Px\_CTRL DRIVEMODE = HIGH

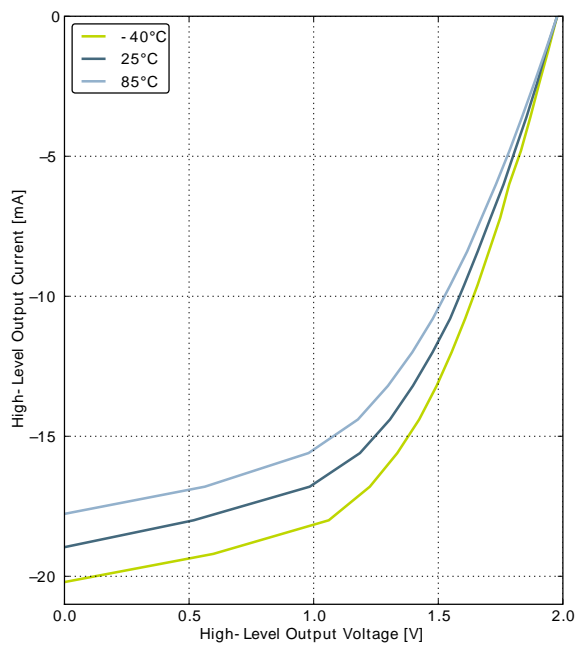
Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage



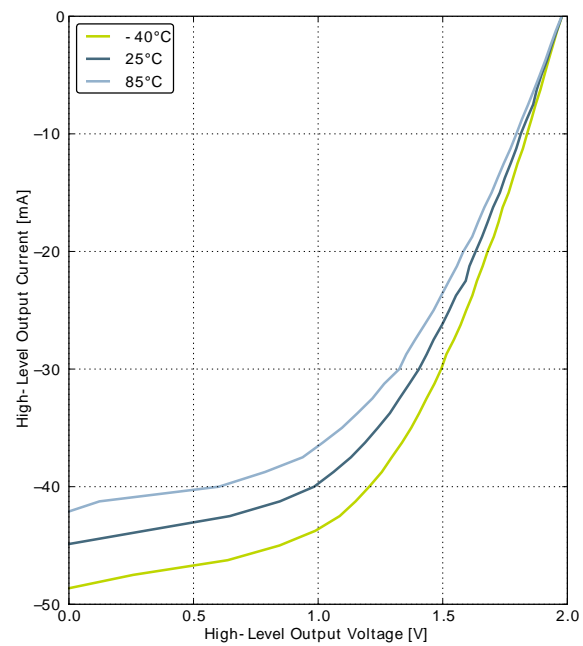
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW

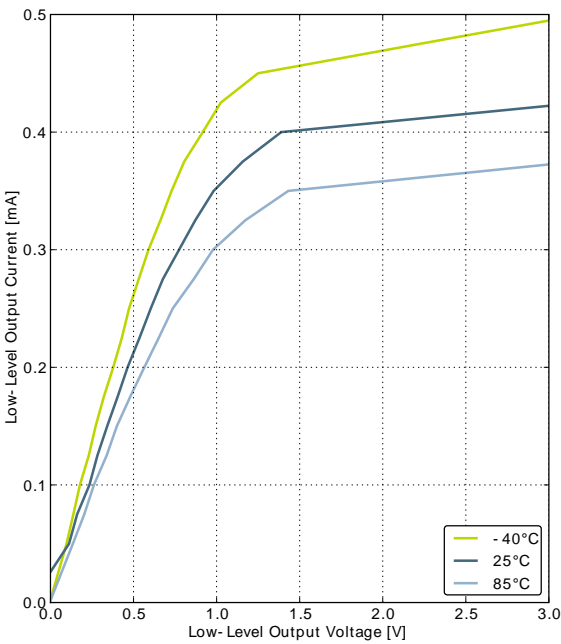


GPIO\_Px\_CTRL DRIVEMODE = STANDARD

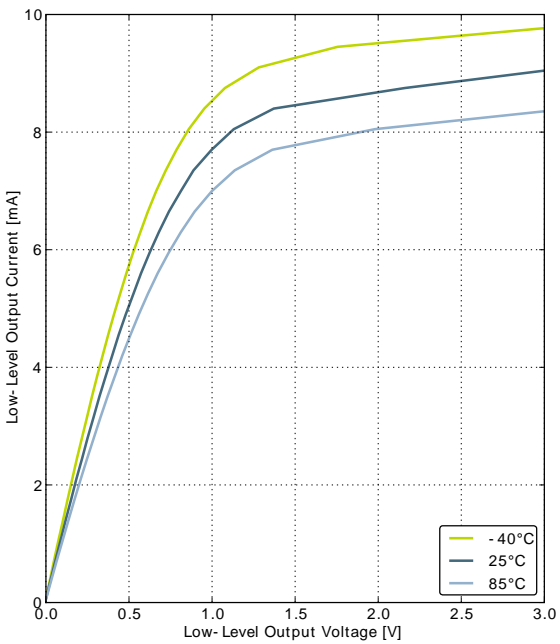


GPIO\_Px\_CTRL DRIVEMODE = HIGH

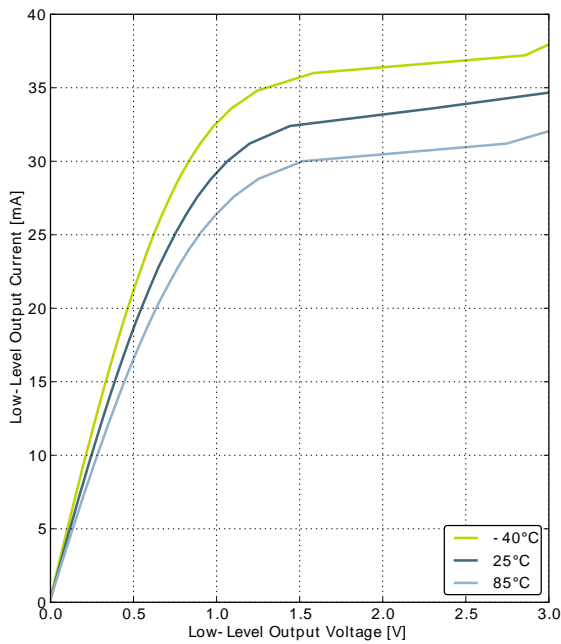
Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage



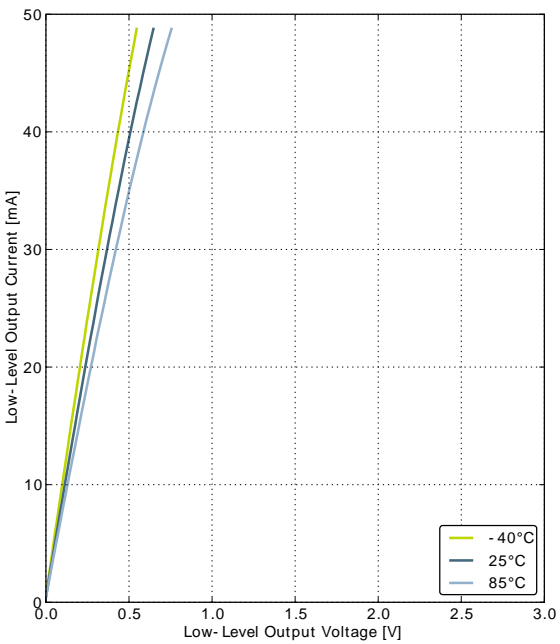
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW

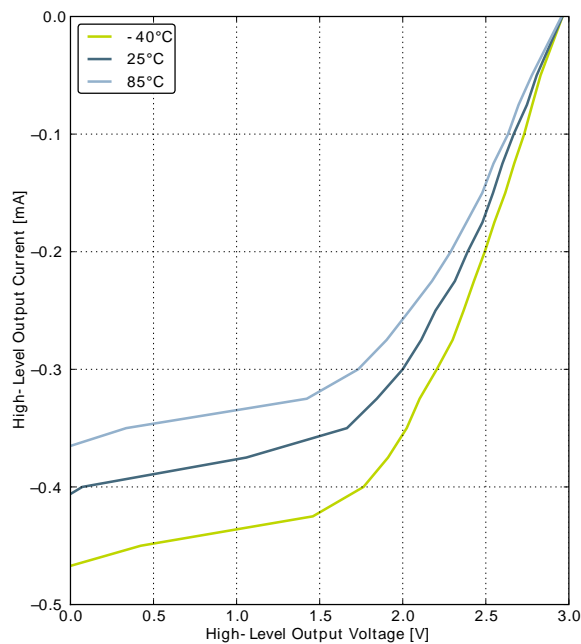


GPIO\_Px\_CTRL DRIVEMODE = STANDARD

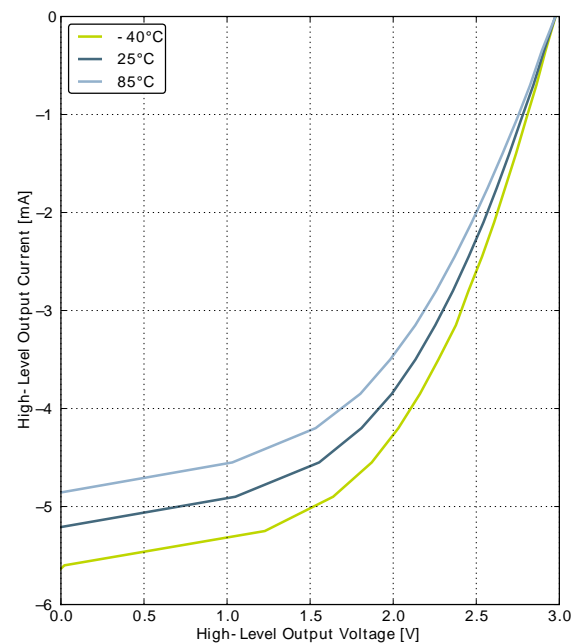


GPIO\_Px\_CTRL DRIVEMODE = HIGH

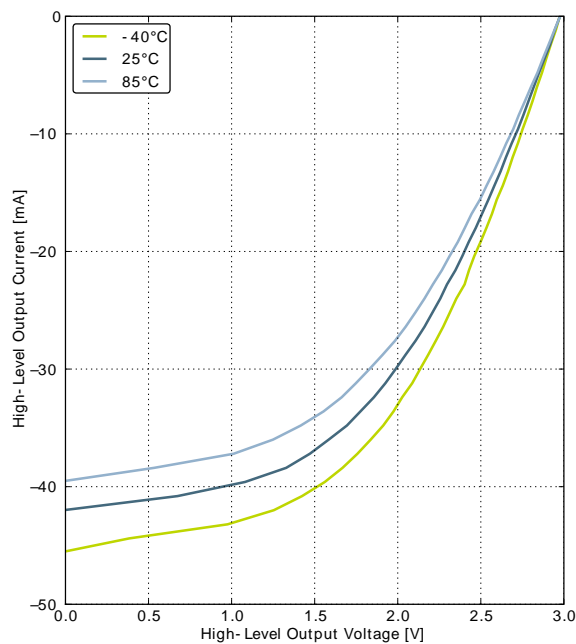
Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage



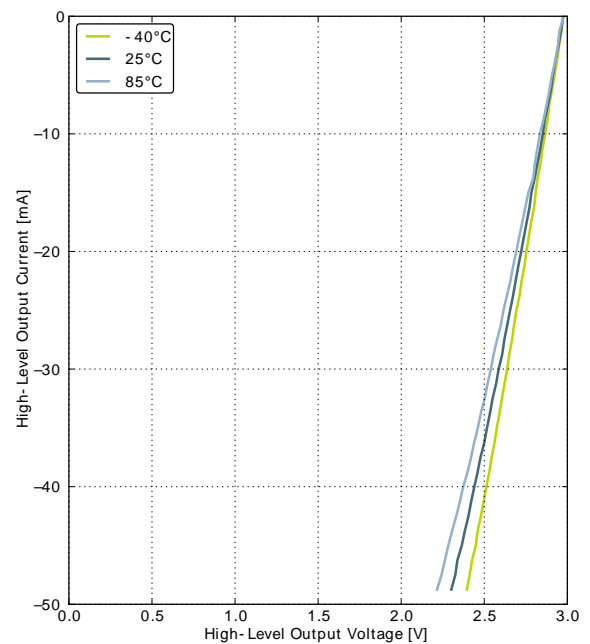
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW

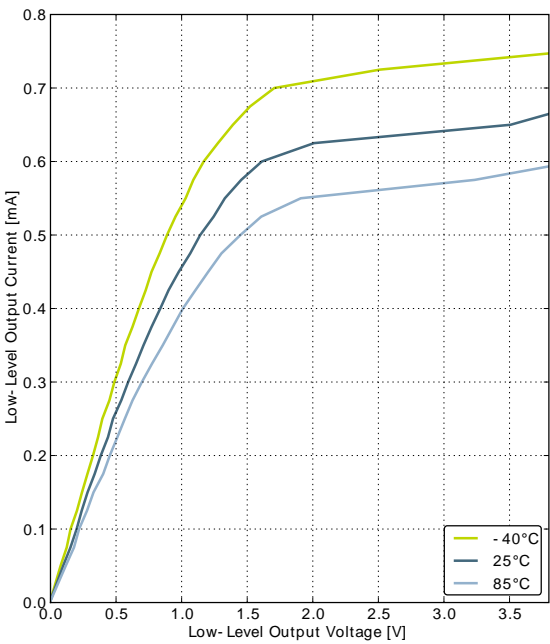


GPIO\_Px\_CTRL DRIVEMODE = STANDARD

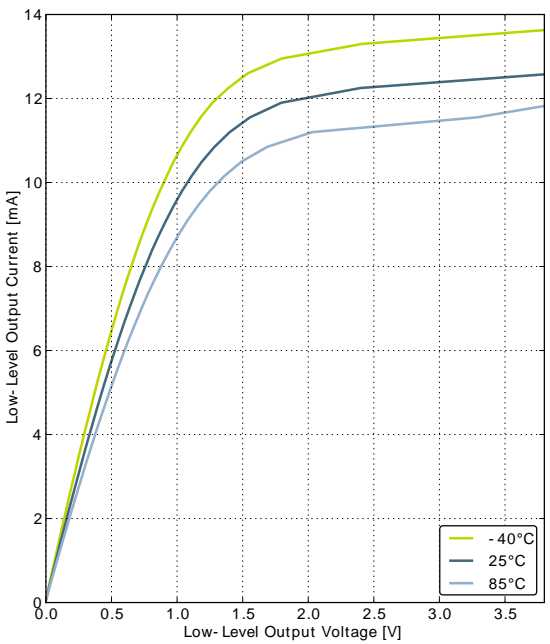


GPIO\_Px\_CTRL DRIVEMODE = HIGH

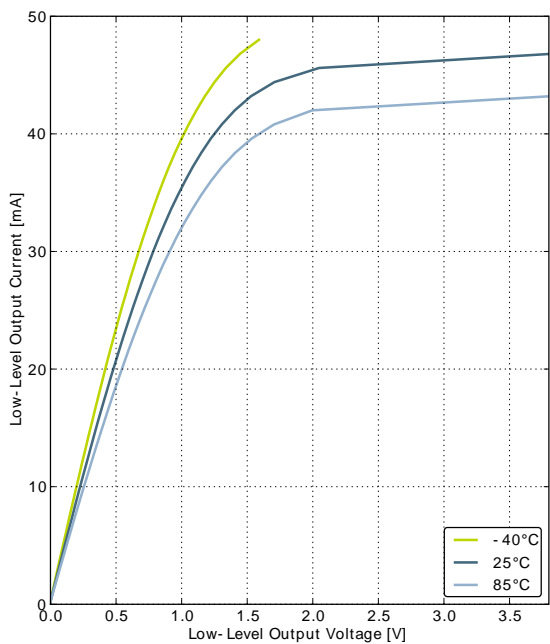
Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage



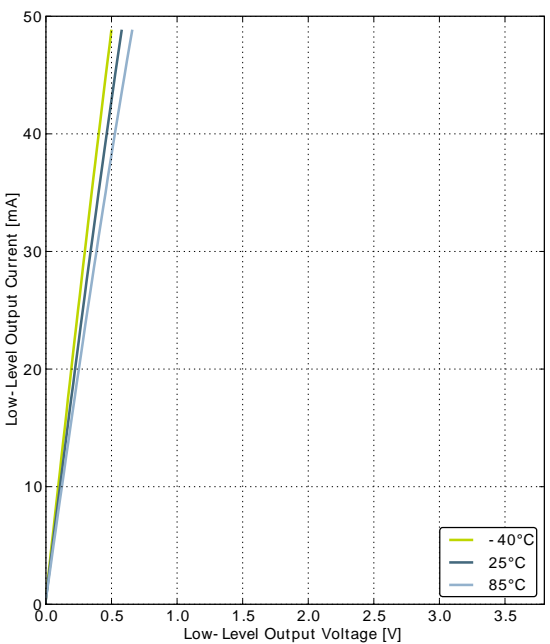
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW



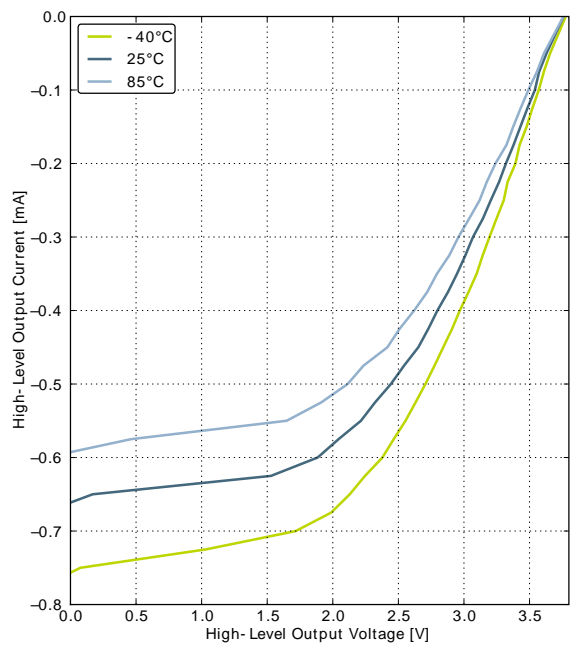
GPIO\_Px\_CTRL DRIVEMODE = STANDARD



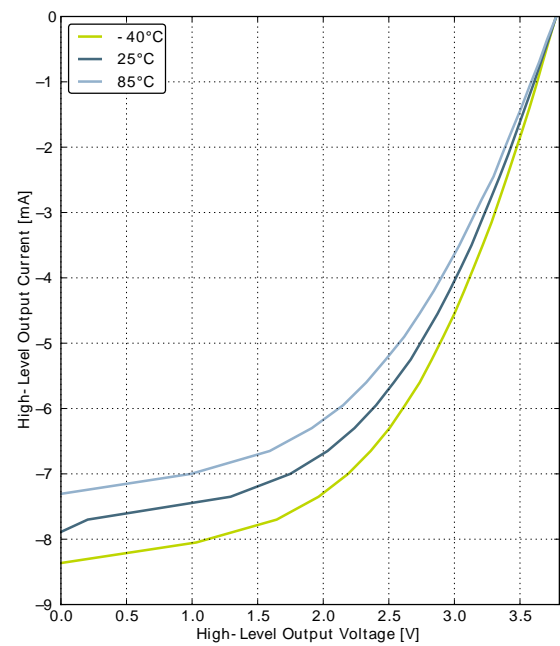
GPIO\_Px\_CTRL DRIVEMODE = HIGH



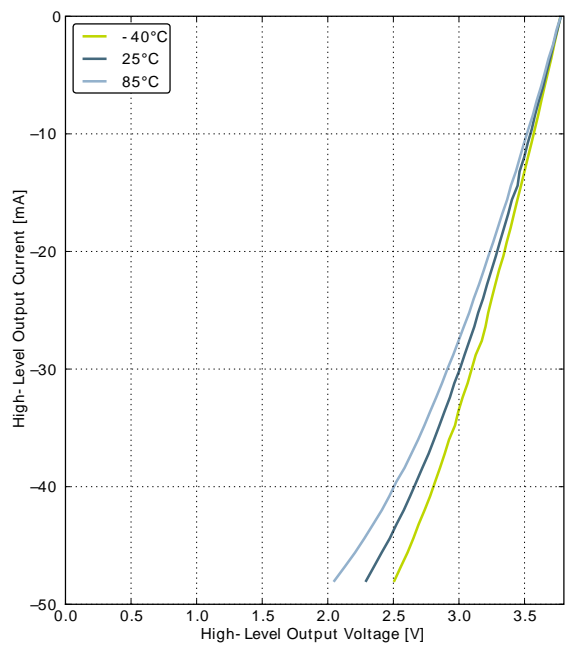
Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage



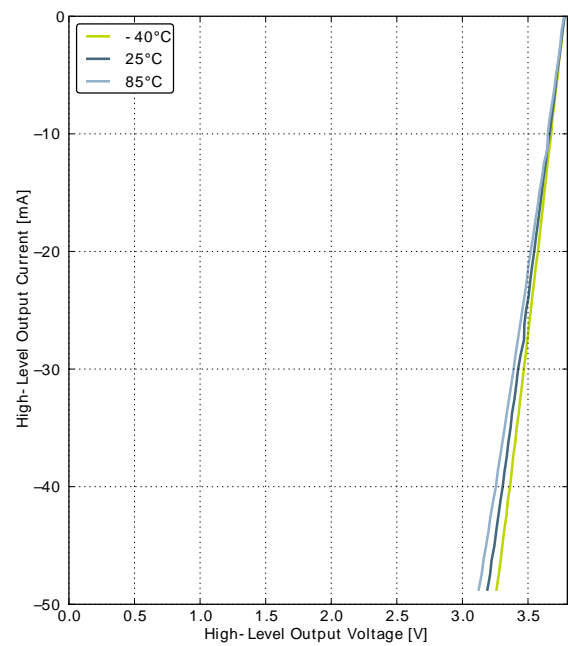
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW



GPIO\_Px\_CTRL DRIVEMODE = STANDARD



GPIO\_Px\_CTRL DRIVEMODE = HIGH

## 3.9 Oscillators

### 3.9.1 LFXO

**Table 3.8. LFXO**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{LFXO}$	Supported nominal crystal frequency			32.768		kHz
$ESR_{LFXO}$	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
$C_{LFXOL}$	Supported crystal external load range		$\times^1$		25	pF
$I_{LFXO}$	Current consumption for core and buffer after startup.	ESR=30 kOhm, $C_L$ =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
$t_{LFXO}$	Start- up time.	ESR=30 kOhm, $C_L$ =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

<sup>1</sup>See Minimum Load Capacitance ( $C_{LFXOL}$ ) Requirement For Safe Crystal Startup in Configurator in Simplicity Studio

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

### 3.9.2 HFXO

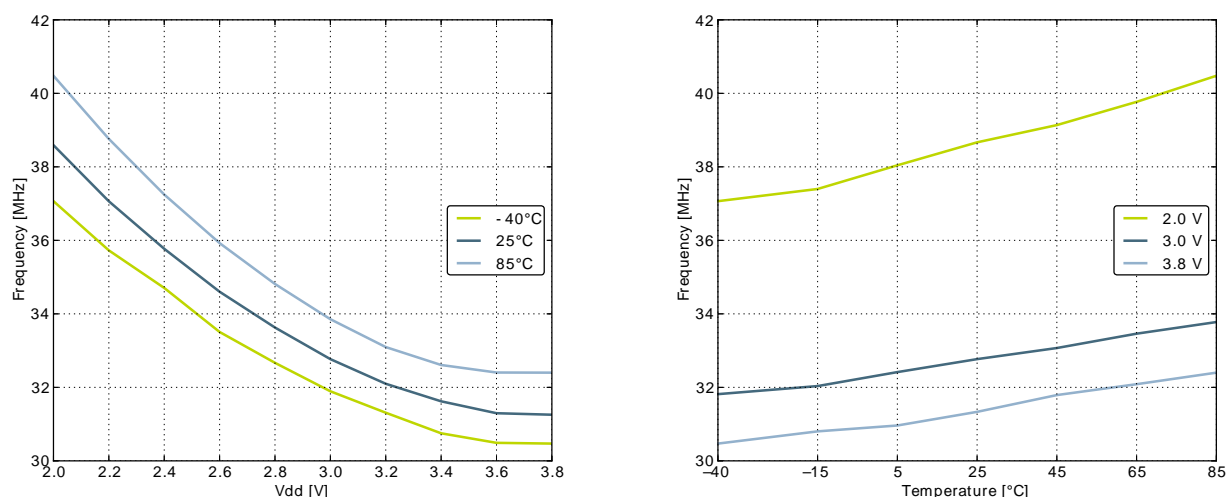
**Table 3.9. HFXO**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{\text{HFXO}}$	Supported nominal crystal Frequency		4		32	MHz
$\text{ESR}_{\text{HFXO}}$	Supported crystal equivalent series resistance (ESR)	Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
$g_{\text{mHFXO}}$	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
$C_{\text{HFXOL}}$	Supported crystal external load range		5		25	pF
$I_{\text{HFXO}}$	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, $C_L=20$ pF, HFXOBOOST in CMU_CTRL equals 0b11		85		$\mu\text{A}$
		32 MHz: ESR=30 Ohm, $C_L=10$ pF, HFXOBOOST in CMU_CTRL equals 0b11		165		$\mu\text{A}$
$t_{\text{HFXO}}$	Startup time	32 MHz: ESR=30 Ohm, $C_L=10$ pF, HFXOBOOST in CMU_CTRL equals 0b11		400		$\mu\text{s}$
	Pulse width removed by glitch detector		1		4	ns

### 3.9.3 LFRCO

**Table 3.10. LFRCO**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{\text{LFRCO}}$	Oscillation frequency, $V_{\text{DD}}=3.0$ V, $T_{\text{AMB}}=25^\circ\text{C}$		31.29	32.768	34.24	kHz
$t_{\text{LFRCO}}$	Startup time not including software calibration			150		$\mu\text{s}$
$I_{\text{LFRCO}}$	Current consumption			190		nA
$\text{TC}_{\text{LFRCO}}$	Temperature coefficient			$\pm 0.02$		%/ $^\circ\text{C}$
$\text{VC}_{\text{LFRCO}}$	Supply voltage coefficient			$\pm 15$		%/V
$\text{TUNESTEP}_{\text{LFRCO}}$	Frequency step for LSB change in TUNING value			1.5		%

**Figure 3.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage**

### 3.9.4 HFRCO

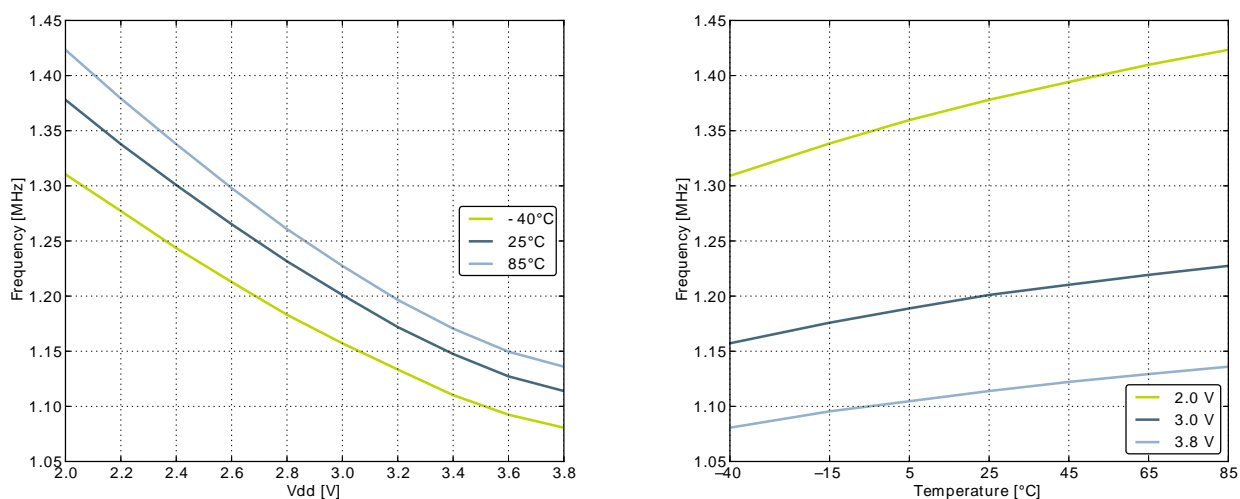
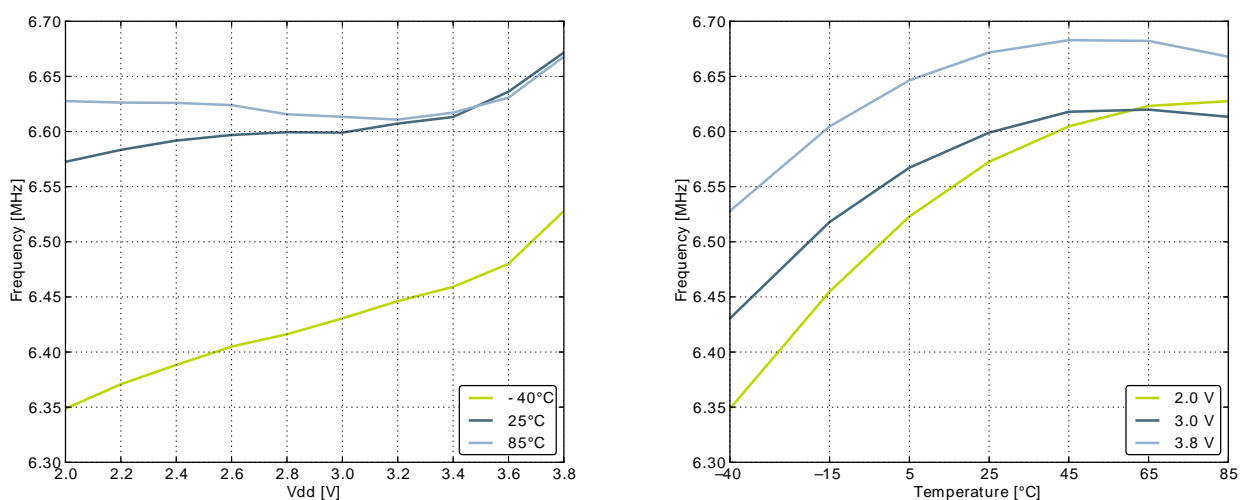
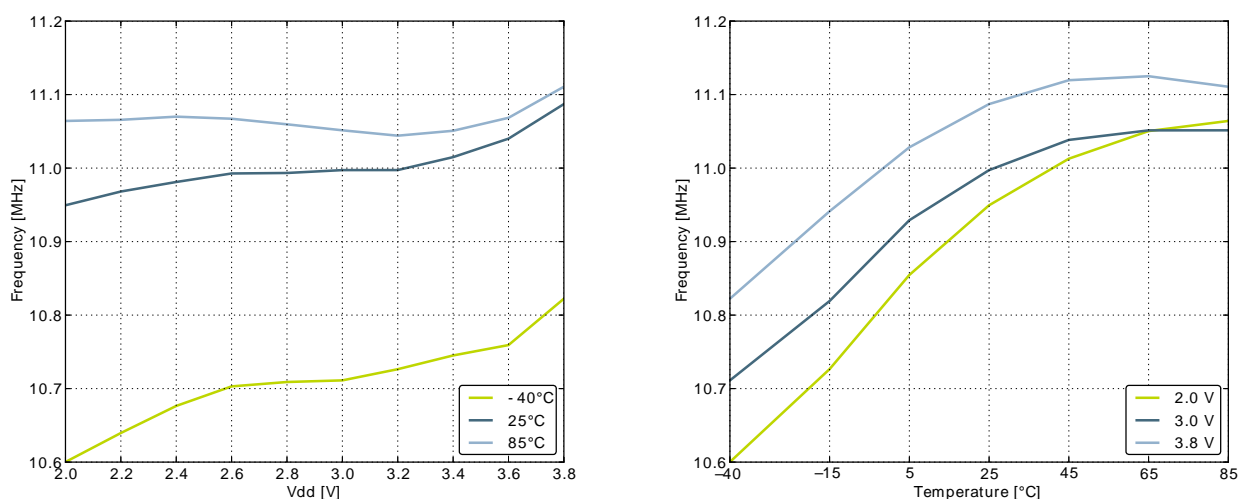
**Table 3.11. HFRCO**

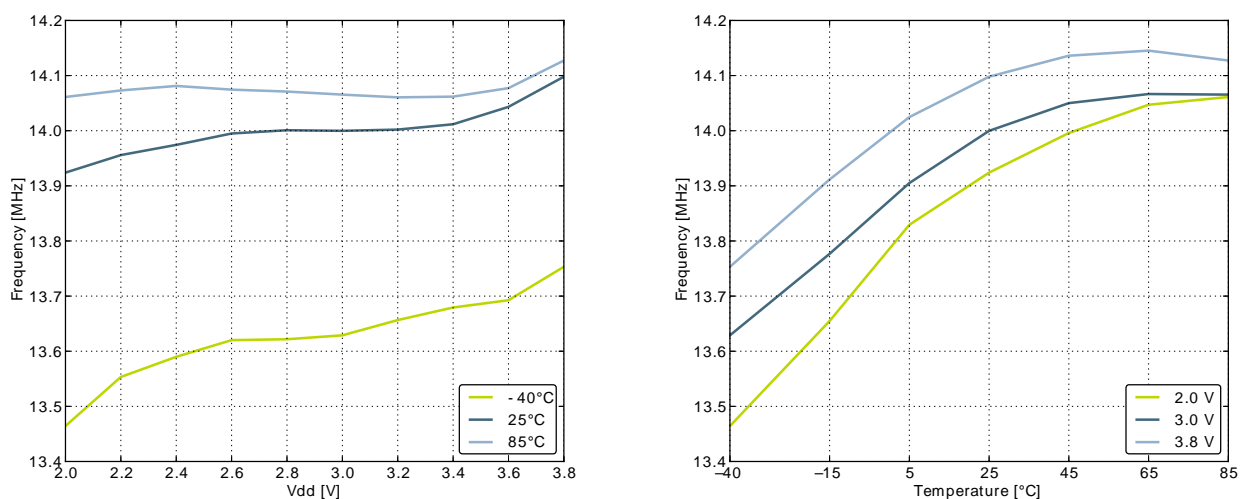
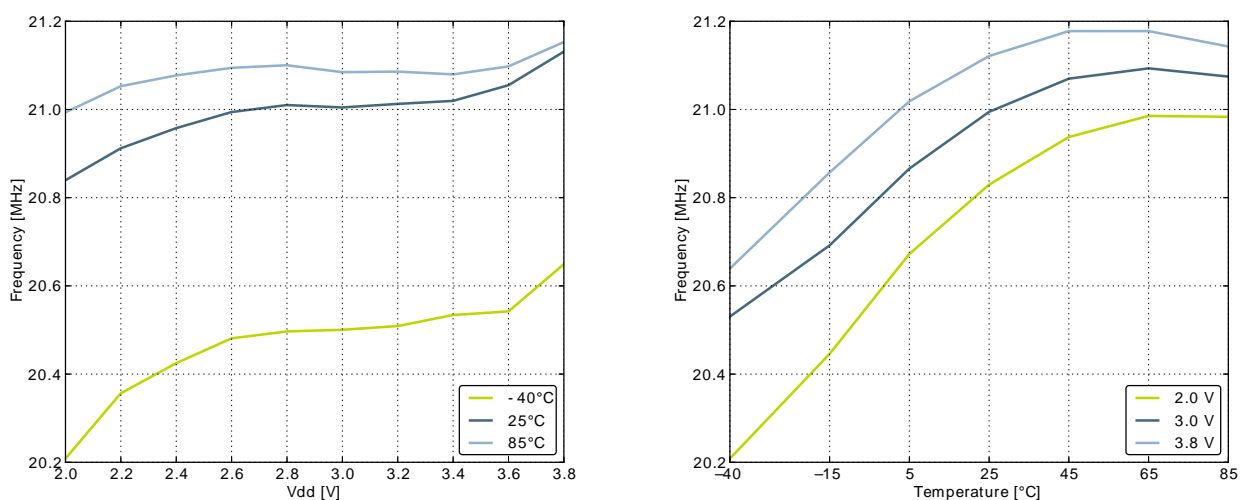
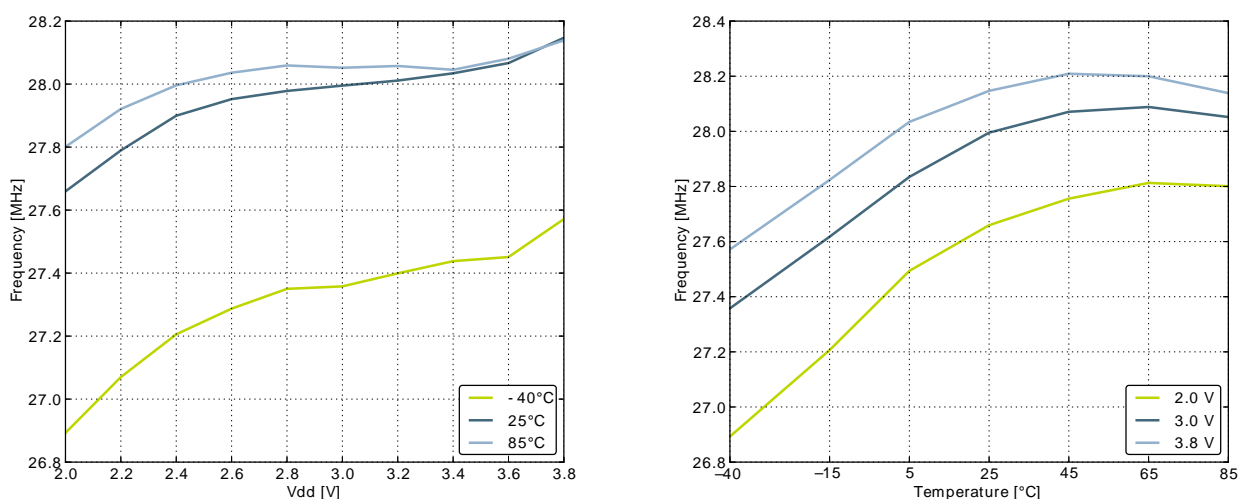
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{\text{HFRCO}}$	Oscillation frequency, $V_{\text{DD}} = 3.0 \text{ V}$ , $T_{\text{AMB}} = 25^\circ\text{C}$	28 MHz frequency band	27.16	28	28.84	MHz
		21 MHz frequency band	20.37	21	21.63	MHz
		14 MHz frequency band	13.58	14	14.42	MHz
		11 MHz frequency band	10.67	11	11.33	MHz
		7 MHz frequency band	6.402	6.6 <sup>1</sup>	6.798	MHz
		1 MHz frequency band	1.164	1.2 <sup>2</sup>	1.236	MHz
$t_{\text{HFRCO\_settling}}$	Settling time after start-up	$f_{\text{HFRCO}} = 14 \text{ MHz}$		0.6		Cycles
	Settling time after band switch			25		Cycles
$I_{\text{HFRCO}}$	Current consumption (Production test condition = 14 MHz)	$f_{\text{HFRCO}} = 28 \text{ MHz}$		106	190	$\mu\text{A}$
		$f_{\text{HFRCO}} = 21 \text{ MHz}$		93	155	$\mu\text{A}$
		$f_{\text{HFRCO}} = 14 \text{ MHz}$		77	120	$\mu\text{A}$
		$f_{\text{HFRCO}} = 11 \text{ MHz}$		72	110	$\mu\text{A}$
		$f_{\text{HFRCO}} = 6.6 \text{ MHz}$		63	90	$\mu\text{A}$
		$f_{\text{HFRCO}} = 1.2 \text{ MHz}$		22	32	$\mu\text{A}$
$\text{DC}_{\text{HFRCO}}$	Duty cycle	$f_{\text{HFRCO}} = 14 \text{ MHz}$	48.5	50	51	%
$\text{TUNESTEP}_{\text{HFRCO}}$	Frequency step for LSB change in TUNING value			0.3 <sup>3</sup>		%

<sup>1</sup>For devices with prod. rev. < 19, Typ = 7 MHz and Min/Max values not applicable.

<sup>2</sup>For devices with prod. rev. < 19, Typ = 1 MHz and Min/Max values not applicable.

<sup>3</sup>The TUNING field in the CMU\_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

**Figure 3.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature****Figure 3.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature****Figure 3.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature**

**Figure 3.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature****Figure 3.25. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature****Figure 3.26. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature**

### 3.9.5 AUXHFRCO

**Table 3.12. AUXHFRCO**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{\text{AUXHFRCO}}$	Oscillation frequency, $V_{\text{DD}} = 3.0 \text{ V}$ , $T_{\text{AMB}} = 25^\circ\text{C}$	14 MHz frequency band	13.580	14.0	14.420	MHz
$t_{\text{AUXHFRCO\_settling}}$	Settling time after start-up	$f_{\text{AUXHFRCO}} = 14 \text{ MHz}$		0.6		Cycles
$\text{DC}_{\text{AUXHFRCO}}$	Duty cycle	$f_{\text{AUXHFRCO}} = 14 \text{ MHz}$	48.5	50	51	%
$\text{TUNESTEP}_{\text{AUXHFRCO}}$	Frequency step for LSB change in TUNING value			0.3 <sup>1</sup>		%

<sup>1</sup>The TUNING field in the CMU\_AUXHFRCTRL register may be used to adjust the AUXHFRCO frequency. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value in the 14 MHz range across operating conditions.

### 3.9.6 ULFRCO

**Table 3.13. ULFRCO**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{\text{ULFRCO}}$	Oscillation frequency	25°C, 3V	0.70		1.75	kHz
$\text{TC}_{\text{ULFRCO}}$	Temperature coefficient			0.05		%/°C
$\text{VC}_{\text{ULFRCO}}$	Supply voltage coefficient			-18.2		%/V

## 3.10 Analog Digital Converter (ADC)

**Table 3.14. ADC**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{\text{ADCCIN}}$	Input voltage range	Single ended	0		$V_{\text{REF}}$	V
		Differential	$-V_{\text{REF}}/2$		$V_{\text{REF}}/2$	V
$V_{\text{ADCCREFIN}}$	Input range of external reference voltage, single ended and differential		1.25		$V_{\text{DD}}$	V
$V_{\text{ADCCREFIN\_CH7}}$	Input range of external negative reference voltage on channel 7	See $V_{\text{ADCCREFIN}}$	0		$V_{\text{DD}} - 1.1$	V
$V_{\text{ADCCREFIN\_CH6}}$	Input range of external positive reference voltage on channel 6	See $V_{\text{ADCCREFIN}}$	0.625		$V_{\text{DD}}$	V
$V_{\text{ADCCMIN}}$	Common mode input range		0		$V_{\text{DD}}$	V
$I_{\text{ADCCIN}}$	Input current	2pF sampling capacitors		<100		nA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
CMRR <sub>ADC</sub>	Analog input common mode rejection ratio			65		dB
I <sub>ADC</sub>	Average active current	1 MSamples/s, 12 bit, external reference		351		μA
		1 MSamples/s, 12 bit, internal reference		411		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00, ADC_CLK running at 13MHz		67		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01, ADC_CLK running at 13MHz		63		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10, ADC_CLK running at 13MHz		64		μA
C <sub>ADCIN</sub>	Input capacitance			2		pF
R <sub>ADCIN</sub>	Input ON resistance		1			MΩ
R <sub>ADCFLT</sub>	Input RC filter resistance			10		kΩ
C <sub>ADCFLT</sub>	Input RC filter/de-coupling capacitance			250		fF
f <sub>ADCCLK</sub>	ADC Clock Frequency				13	MHz
t <sub>ADCCONV</sub>	Conversion time	6 bit	7			ADC-CLK Cycles
		8 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t <sub>ADCACQ</sub>	Acquisition time	Programmable	1		256	ADC-CLK Cycles
t <sub>ADCACQVDD3</sub>	Required acquisition time for VDD/3 reference		2			μs
t <sub>ADCSTART</sub>	Startup time of reference generator and ADC core in NORMAL mode			5		μs
	Startup time of reference generator and ADC core in			1		μs



Symbol	Parameter	Condition	Min	Typ	Max	Unit
	KEEPADCWARM mode					
SNR <sub>ADC</sub>	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V <sub>DD</sub> reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V <sub>DD</sub> reference		67		dB
		1 MSamples/s, 12 bit, differential, 2xV <sub>DD</sub> reference		69		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V <sub>DD</sub> reference		67		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V <sub>DD</sub> reference	63	69		dB
		200 kSamples/s, 12 bit, differential, 2xV <sub>DD</sub> reference		70		dB
SINAD <sub>ADC</sub>	Signal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V <sub>DD</sub> reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, $V_{DD}$ reference		66		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, $V_{DD}$ reference	62	68		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
SFDR <sub>ADC</sub>	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, $V_{DD}$ reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference		76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, $V_{DD}$ reference	68	79		dBc
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		79		dBc
$V_{ADCOFFSET}$	Offset voltage	After calibration, single ended	-4	0.3	4	mV
		After calibration, differential		0.3		mV
$TGRAD_{ADCTH}$	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/°C
$DNL_{ADC}$	Differential non-linearity (DNL)	$V_{DD} = 3.0$ V, external 2.5V reference	-1	$\pm 0.7$	4	LSB
$INL_{ADC}$	Integral non-linearity (INL), End point method	$V_{DD} = 3.0$ V, external 2.5V reference		$\pm 1.2$	$\pm 3$	LSB
$MC_{ADC}$	No missing codes		11.999 <sup>1</sup>	12		bits

<sup>1</sup>On the average every ADC will have one missing code, most likely to appear around  $2048 \pm n \cdot 512$  where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.27 (p. 36) and Figure 3.28 (p. 37) , respectively.

**Figure 3.27. Integral Non-Linearity (INL)**

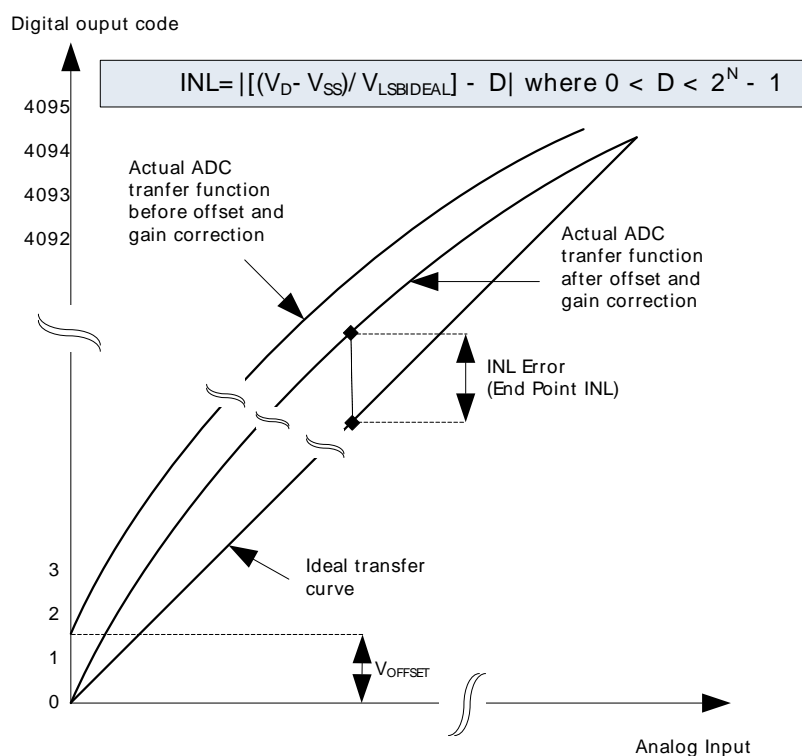
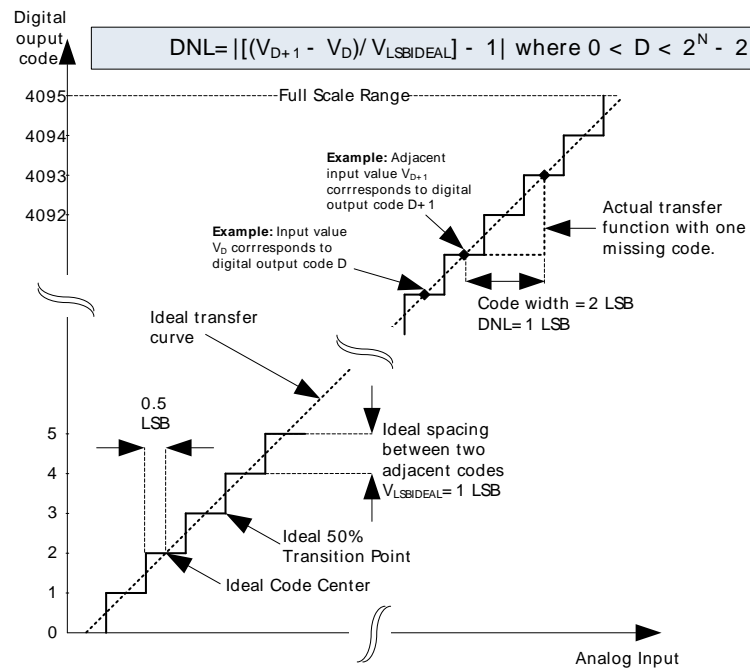
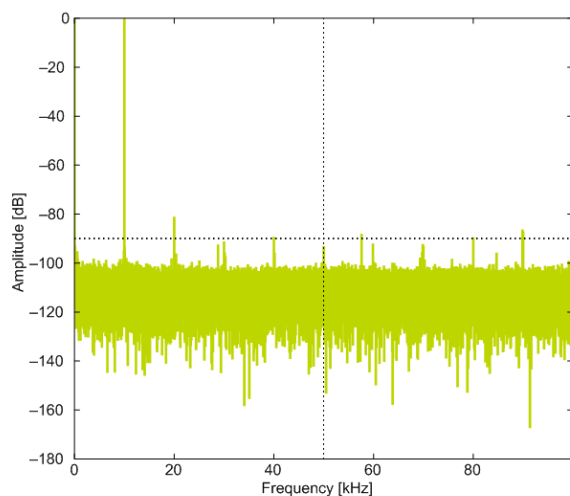


Figure 3.28. Differential Non-Linearity (DNL)

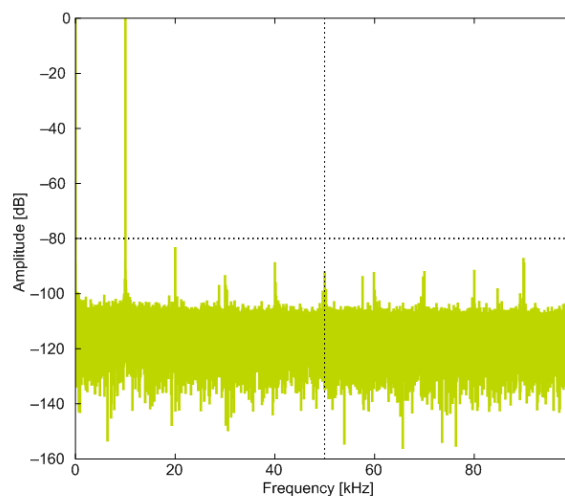


### 3.10.1 Typical performance

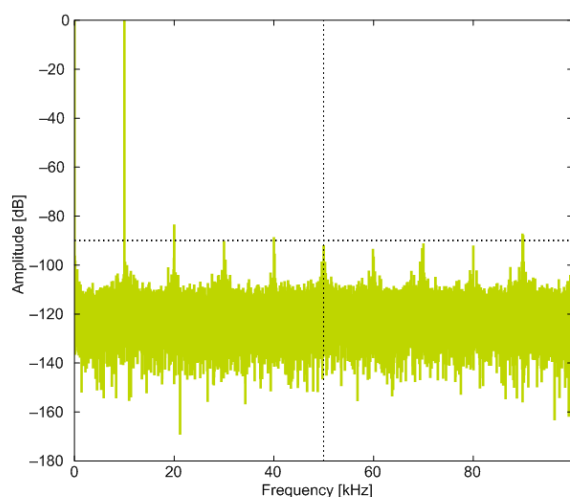
Figure 3.29. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C



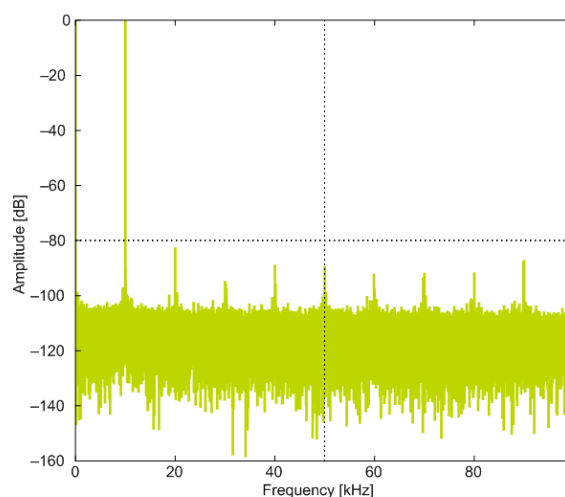
1.25V Reference



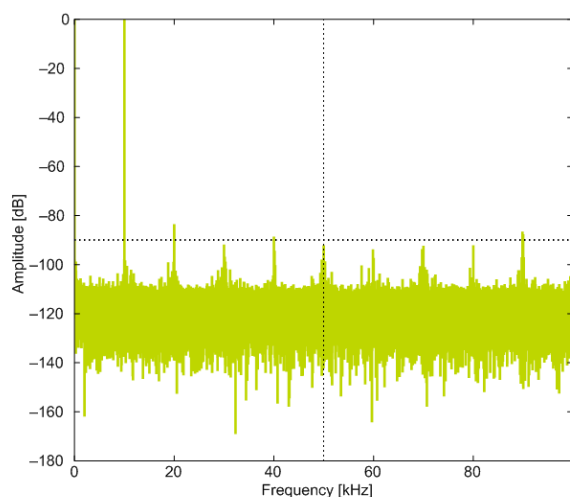
2.5V Reference



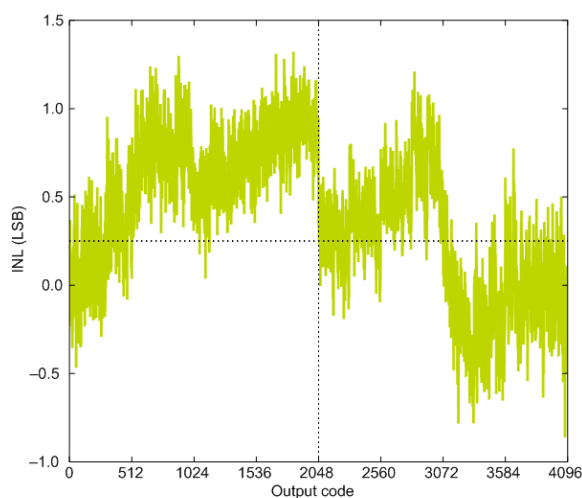
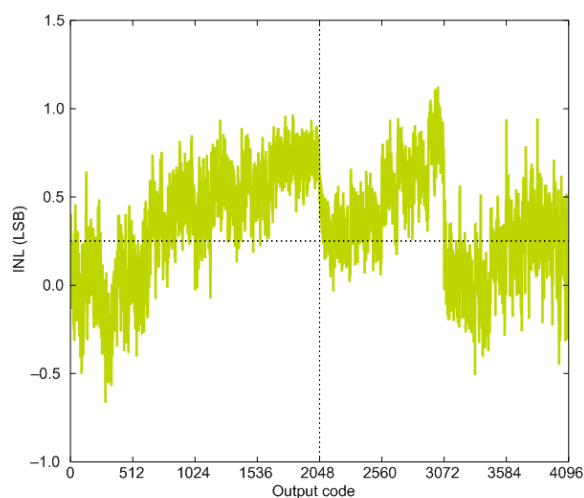
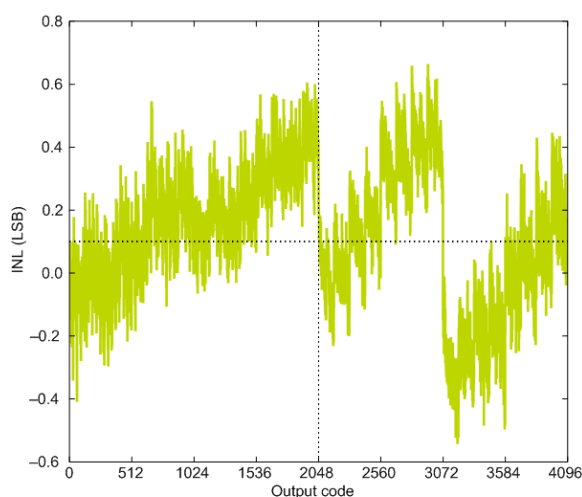
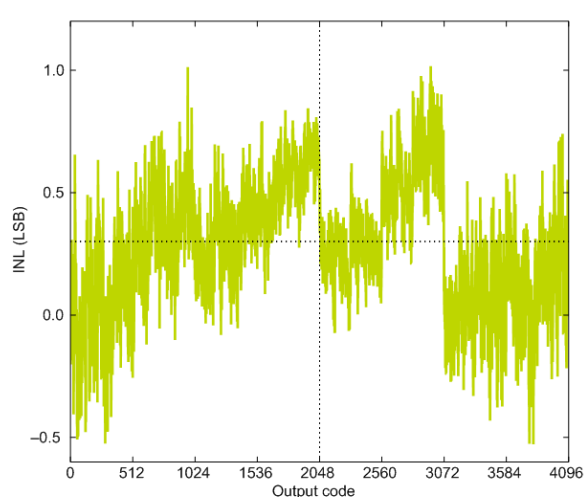
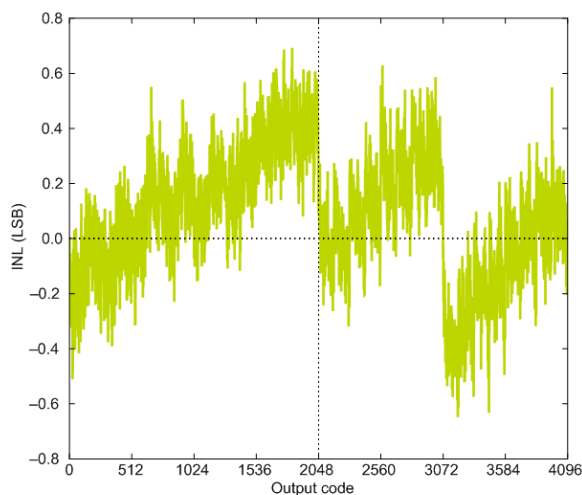
2XVDDVSS Reference

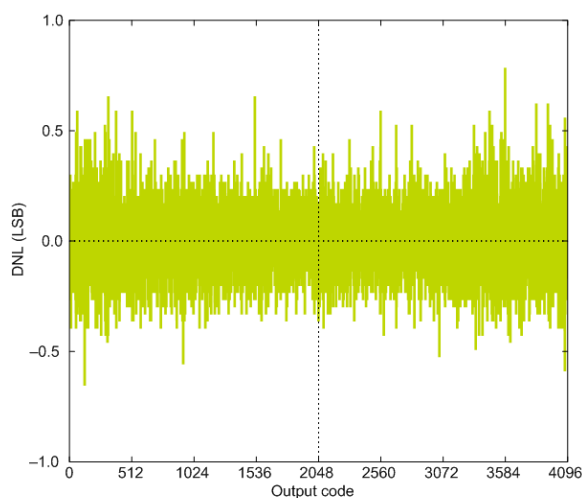
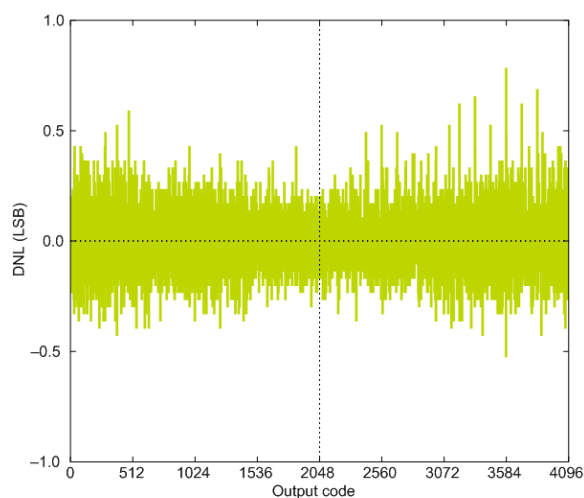
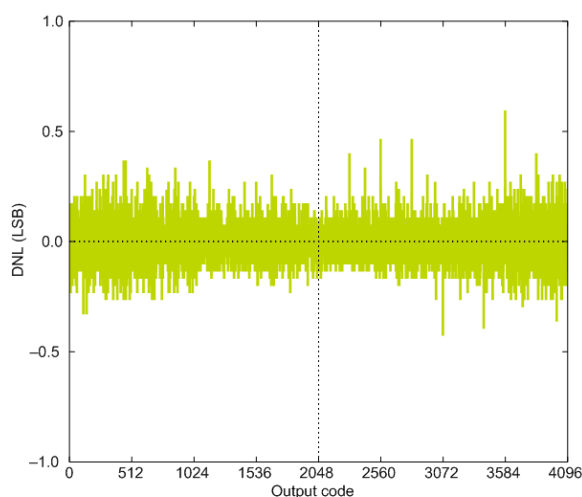
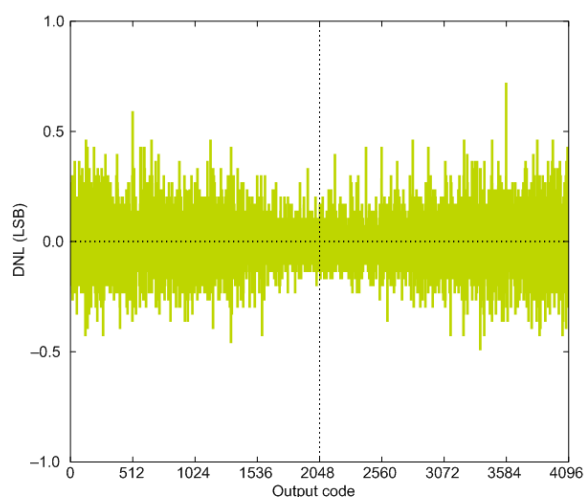
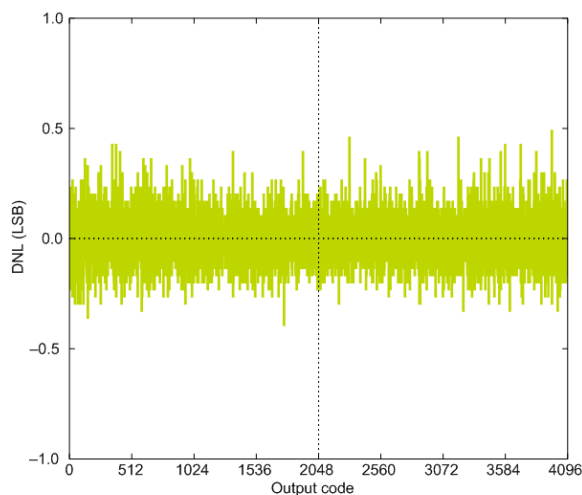


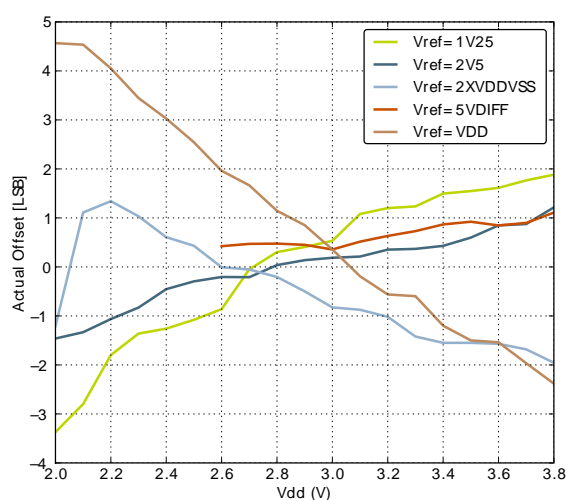
5VDIFF Reference



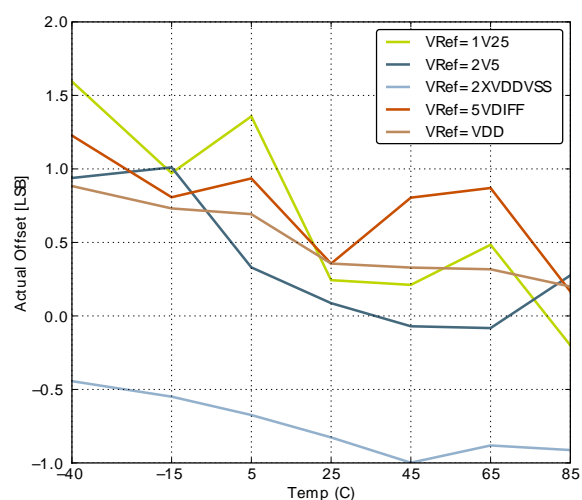
VDD Reference

**Figure 3.30. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C****1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

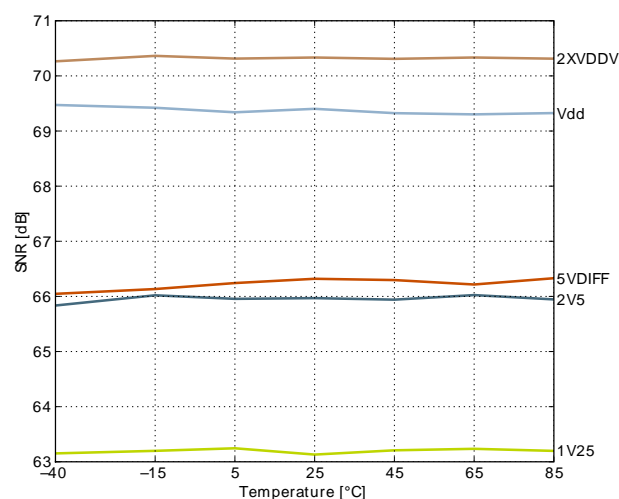
**Figure 3.31. ADC Differential Linearity Error vs Code,  $V_{dd} = 3V$ , Temp = 25°C****1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

**Figure 3.32. ADC Absolute Offset, Common Mode =  $V_{DD}/2$** 

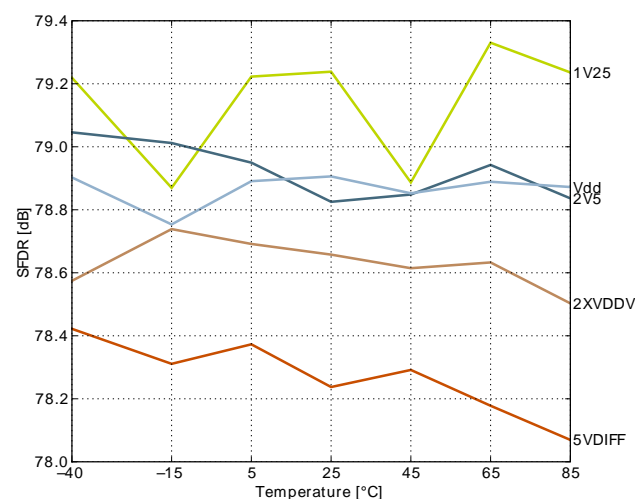
Offset vs Supply Voltage, Temp = 25°C



Offset vs Temperature, VDD = 3V

**Figure 3.33. ADC Dynamic Performance vs Temperature for all ADC References, VDD = 3V**

Signal to Noise Ratio (SNR)



Spurious-Free Dynamic Range (SFDR)

## 3.11 Digital Analog Converter (DAC)

**Table 3.15. DAC**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DACOUT}$	Output voltage range	VDD voltage reference, single ended	0		$V_{DD}$	V
$V_{DACCM}$	Output common mode voltage range		0		$V_{DD}$	V
$I_{DAC}$	Active current including references for 2 channels	500 kSamples/s, 12bit		400 <sup>1</sup>	650	μA
		100 kSamples/s, 12 bit		200 <sup>1</sup>	250	μA
		1 kSamples/s 12 bit		17 <sup>1</sup>	25	μA
$SR_{DAC}$	Sample rate				500	ksamples/s



Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{DAC}$	DAC clock frequency	Continuous Mode			1000	kHz
		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
$CYC_{DACCONV}$	Clock cycles per conversion			2		
$t_{DACCONV}$	Conversion time		2			$\mu s$
$t_{DACSETTLE}$	Settling time			5		$\mu s$
$SNR_{DAC}$	Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
$SNDR_{DAC}$	Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		57		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		54		dB
$SFDR_{DAC}$	Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		56		dBc
$V_{DACOFFSET}$	Offset voltage	After calibration, single ended		2		mV
$V_{DACSHMDRIFT}$	Sample-hold mode voltage drift			540		$\mu V/ms$
$DNL_{DAC}$	Differential non-linearity			$\pm 1$		LSB
$INL_{DAC}$	Integral non-linearity			$\pm 5$		LSB
$MC_{DAC}$	No missing codes			12		bits

<sup>†</sup> Measured with a static input code and no loading on the output.

## 3.12 Analog Comparator (ACMP)

**Table 3.16. ACMP**

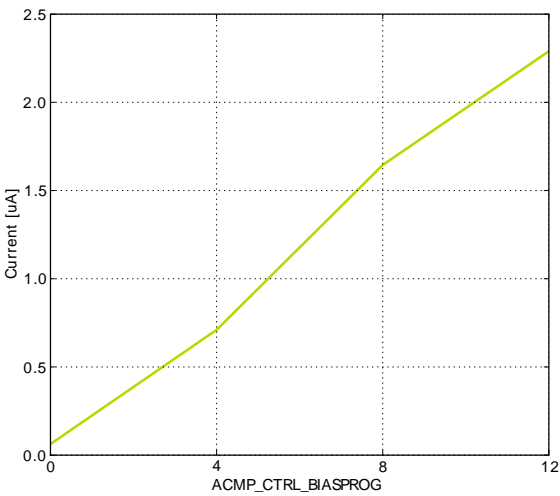
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{ACMPIN}$	Input voltage range		0		$V_{DD}$	V
$V_{ACMPCM}$	ACMP Common Mode voltage range		0		$V_{DD}$	V
$I_{ACMP}$	Active current	BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		55	600	nA
		BIASPROG=0b1111, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.82	12	$\mu$ A
		BIASPROG=0b1111, FULL-BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	$\mu$ A
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0	0.5	$\mu$ A
		Internal voltage reference, LPREF=1		0.050	3	$\mu$ A
		Internal voltage reference, LPREF=0		6		$\mu$ A
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
$R_{CSRES}$	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm
$t_{ACMPSTART}$	Startup time				10	$\mu$ s

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 43) .  $I_{ACMPREF}$  is zero if an external voltage reference is used.

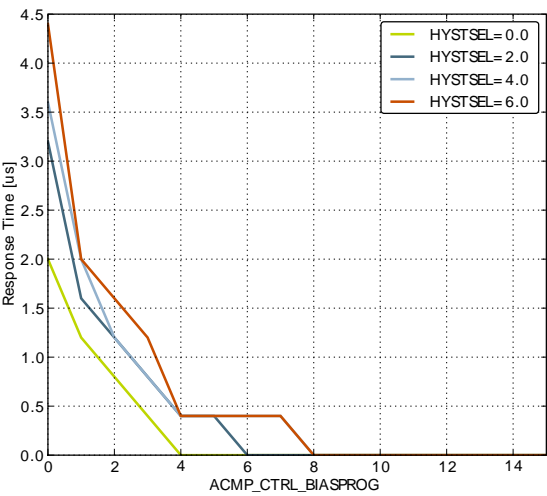
### Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

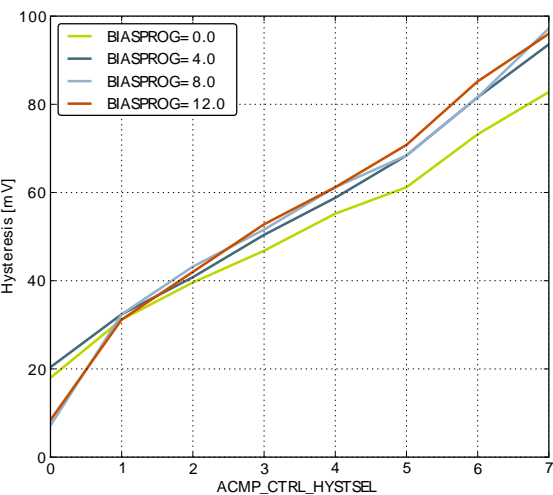
Figure 3.34. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time



Hysteresis

### 3.13 Voltage Comparator (VCMP)

**Table 3.17. VCMP**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>VCMPIN</sub>	Input voltage range			V <sub>DD</sub>		V
V <sub>VCMP<sub>CM</sub></sub>	VCMP Common Mode voltage range			V <sub>DD</sub>		V
I <sub>VCMP</sub>	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.3	1	μA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	30	μA
t <sub>VCMPREF</sub>	Startup time reference generator	NORMAL		10		μs
V <sub>VCMP<sub>OFFSET</sub></sub>	Offset voltage	Single ended		10		mV
		Differential		10		mV
V <sub>VCMPHYST</sub>	VCMP hysteresis			17		mV
t <sub>VCMPSTART</sub>	Startup time				10	μs

The V<sub>DD</sub> trigger level can be configured by setting the TRIGLEVEL field of the VCMP\_CTRL register in accordance with the following equation:

#### VCMP Trigger Level as a Function of Level Setting

$$V_{DD} \text{ Trigger Level} = 1.667V + 0.034 \times \text{TRIGLEVEL} \quad (3.2)$$

### 3.14 I2C

**Table 3.18. I2C Standard-mode (Sm)**

Symbol	Parameter	Min	Typ	Max	Unit
f <sub>SCL</sub>	SCL clock frequency	0		100 <sup>1</sup>	kHz
t <sub>LOW</sub>	SCL clock low time	4.7			μs
t <sub>HIGH</sub>	SCL clock high time	4.0			μs
t <sub>SU,DAT</sub>	SDA set-up time	250			ns
t <sub>HD,DAT</sub>	SDA hold time	8		3450 <sup>2,3</sup>	ns
t <sub>SU,STA</sub>	Repeated START condition set-up time	4.7			μs
t <sub>HD,STA</sub>	(Repeated) START condition hold time	4.0			μs
t <sub>SU,STO</sub>	STOP condition set-up time	4.0			μs
t <sub>BUF</sub>	Bus free time between a STOP and START condition	4.7			μs

<sup>1</sup>For the minimum HPPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32G Reference Manual.

<sup>2</sup>The maximum SDA hold time (t<sub>HD,DAT</sub>) needs to be met only when the device does not stretch the low time of SCL (t<sub>LOW</sub>).

<sup>3</sup>When transmitting data, this number is guaranteed only when I2Cn\_CLKDIV < ((3450\*10<sup>-9</sup> [s] \* f<sub>HPPERCLK</sub> [Hz]) - 4).

**Table 3.19. I2C Fast-mode (Fm)**

Symbol	Parameter	Min	Typ	Max	Unit
f <sub>SCL</sub>	SCL clock frequency	0		400 <sup>1</sup>	kHz
t <sub>LOW</sub>	SCL clock low time	1.3			µs
t <sub>HIGH</sub>	SCL clock high time	0.6			µs
t <sub>SU,DAT</sub>	SDA set-up time	100			ns
t <sub>HD,DAT</sub>	SDA hold time	8		900 <sup>2,3</sup>	ns
t <sub>SU,STA</sub>	Repeated START condition set-up time	0.6			µs
t <sub>HD,STA</sub>	(Repeated) START condition hold time	0.6			µs
t <sub>SU,STO</sub>	STOP condition set-up time	0.6			µs
t <sub>BUF</sub>	Bus free time between a STOP and START condition	1.3			µs

<sup>1</sup>For the minimum HPPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32G Reference Manual.

<sup>2</sup>The maximum SDA hold time (t<sub>HD,DAT</sub>) needs to be met only when the device does not stretch the low time of SCL (t<sub>LOW</sub>).

<sup>3</sup>When transmitting data, this number is guaranteed only when  $I2Cn\_CLKDIV < ((900 \cdot 10^{-9} [s] \cdot f_{HPPERCLK} [Hz]) - 4)$ .

**Table 3.20. I2C Fast-mode Plus (Fm+)**

Symbol	Parameter	Min	Typ	Max	Unit
f <sub>SCL</sub>	SCL clock frequency	0		1000 <sup>1</sup>	kHz
t <sub>LOW</sub>	SCL clock low time	0.5			µs
t <sub>HIGH</sub>	SCL clock high time	0.26			µs
t <sub>SU,DAT</sub>	SDA set-up time	50			ns
t <sub>HD,DAT</sub>	SDA hold time	8			ns
t <sub>SU,STA</sub>	Repeated START condition set-up time	0.26			µs
t <sub>HD,STA</sub>	(Repeated) START condition hold time	0.26			µs
t <sub>SU,STO</sub>	STOP condition set-up time	0.26			µs
t <sub>BUF</sub>	Bus free time between a STOP and START condition	0.5			µs

<sup>1</sup>For the minimum HPPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32G Reference Manual.

## 3.15 Digital Peripherals

**Table 3.21. Digital Peripherals**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I <sub>USART</sub>	USART current	USART idle current, clock enabled		7.5		µA/ MHz
I <sub>UART</sub>	UART current	UART idle current, clock enabled		5.63		µA/ MHz
I <sub>LEUART</sub>	LEUART current	LEUART idle current, clock enabled		150		nA
I <sub>I2C</sub>	I2C current	I2C idle current, clock enabled		6.25		µA/ MHz
I <sub>TIMER</sub>	TIMER current	TIMER_0 idle current, clock enabled		8.75		µA/ MHz
I <sub>LETIMER</sub>	LETIMER current	LETIMER idle current, clock enabled		150		nA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I <sub>PCNT</sub>	PCNT current	PCNT idle current, clock enabled		100		nA
I <sub>RTC</sub>	RTC current	RTC idle current, clock enabled		100		nA
I <sub>AES</sub>	AES current	AES idle current, clock enabled		2.5		μA/ MHz
I <sub>GPIO</sub>	GPIO current	GPIO idle current, clock enabled		5.31		μA/ MHz
I <sub>PRS</sub>	PRS current	PRS idle current		2,81		μA/ MHz
I <sub>DMA</sub>	DMA current	Clock enable		8.12		μA/ MHz

## 4 Pinout and Package

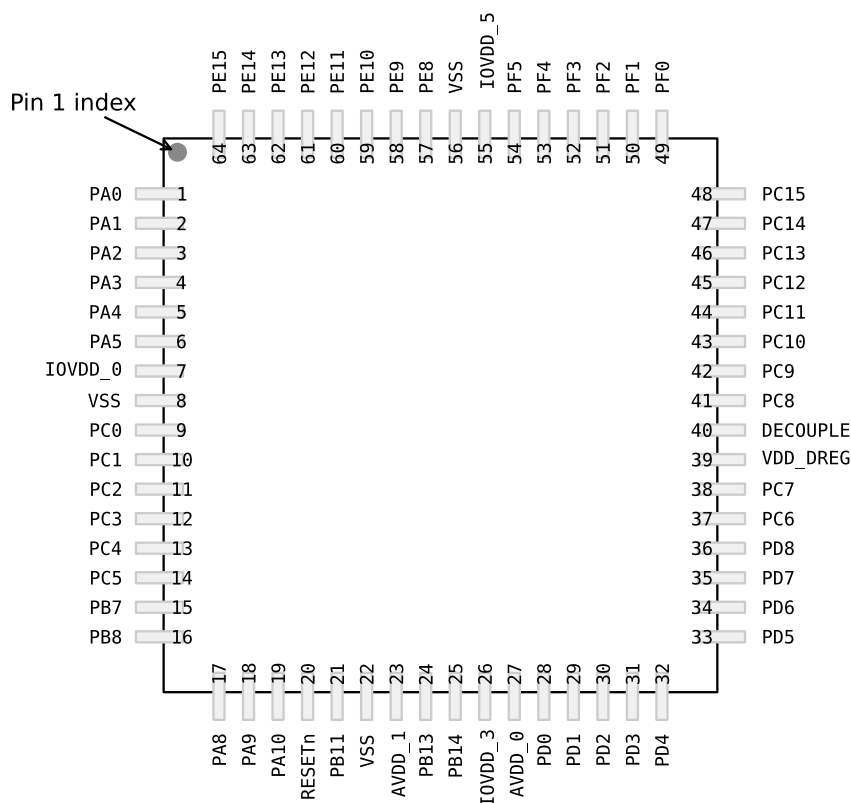
### Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32G232.

### 4.1 Pinout

The EFM32G232 pinout is shown in Figure 4.1 (p. 48) and Table 4.1 (p. 48). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the \*\_ROUTE register in the module in question.

**Figure 4.1. EFM32G232 Pinout (top view, not to scale)**



**Table 4.1. Device Pinout**

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC0 #0/1	I2C0_SDA #0	
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
4	PA3		TIM0_CDTI0 #0		
5	PA4		TIM0_CDTI1 #0		
6	PA5		TIM0_CDTI2 #0	LEU1_TX #1	
7	IOVDD_0	Digital IO power supply 0.			
8	VSS	Ground.			
9	PC0	ACMP0_CH0	PCNT0_S0IN #2	US1_TX #0	
10	PC1	ACMP0_CH1	PCNT0_S1IN #2	US1_RX #0	
11	PC2	ACMP0_CH2		US2_TX #0	
12	PC3	ACMP0_CH3		US2_RX #0	
13	PC4	ACMP0_CH4	LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0	
14	PC5	ACMP0_CH5	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0	
15	PB7	LFXTAL_P		US1_CLK #0	
16	PB8	LFXTAL_N		US1_CS #0	
17	PA8		TIM2_CC0 #0		
18	PA9		TIM2_CC1 #0		
19	PA10		TIM2_CC2 #0		
20	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0	LETIM0_OUT0 #1		
22	VSS	Ground.			
23	AVDD_1	Analog power supply 1.			
24	PB13	HFXTAL_P		LEU0_TX #1	
25	PB14	HFXTAL_N		LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	
30	PD2	ADC0_CH2	TIM0_CC1 #3	US1_CLK #1	
31	PD3	ADC0_CH3	TIM0_CC2 #3	US1_CS #1	
32	PD4	ADC0_CH4		LEU0_TX #0	
33	PD5	ADC0_CH5		LEU0_RX #0	
34	PD6	ADC0_CH6	LETIM0_OUT0 #0	I2C0_SDA #1	
35	PD7	ADC0_CH7	LETIM0_OUT1 #0	I2C0_SCL #1	
36	PD8				CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	



QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C <sub>DECOUPLE</sub> is required at this pin.			
41	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	
42	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	
43	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	
44	PC11	ACMP1_CH3		US0_TX #2	
45	PC12	ACMP1_CH4			CMU_CLK0 #1
46	PC13	ACMP1_CH5	TIM0_CDTI0 #1/3 TIM1_CC0 #0 PCNT0_S0IN #0		
47	PC14	ACMP1_CH6	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0		
48	PC15	ACMP1_CH7	TIM0_CDTI2 #1/3 TIM1_CC2 #0		DBG_SWO #1
49	PF0		LETIM0_OUT0 #2		DBG_SWCLK #0/1
50	PF1		LETIM0_OUT1 #2		DBG_SWDIO #0/1
51	PF2				ACMP1_O #0 DBG_SWO #0
52	PF3		TIM0_CDTI0 #2		
53	PF4		TIM0_CDTI1 #2		
54	PF5		TIM0_CDTI2 #2		
55	IOVDD_5	Digital IO power supply 5.			
56	VSS	Ground.			
57	PE8		PCNT2_S0IN #1		
58	PE9		PCNT2_S1IN #1		
59	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
60	PE11		TIM1_CC1 #1	US0_RX #0	BOOT_RX
61	PE12		TIM1_CC2 #1	US0_CLK #0	
62	PE13			US0_CS #0	ACMP0_O #0
63	PE14			LEU0_TX #2	
64	PE15			LEU0_RX #2	

## 4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 51). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

### Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 4.2. Alternate functionality overview**

Alternate	LOCATION				
Functionality	0	1	2	3	Description
ACMP0_CH0	PC0				Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1				Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2				Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3				Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4				Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5				Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6				Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7				Analog comparator ACMP0, channel 7.
ACMP0_O	PE13				Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8				Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9				Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10				Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11				Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12				Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13				Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14				Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15				Analog comparator ACMP1, channel 7.
ACMP1_O	PF2				Analog comparator ACMP1, digital output.
ADC0_CH0	PD0				Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1				Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2				Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3				Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4				Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5				Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6				Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7				Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11				Bootloader RX.
BOOT_TX	PE10				Bootloader TX.
CMU_CLK0	PA2	PC12			Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8			Clock Management Unit, clock output number 1.
DAC0_OUT0	PB11				Digital to Analog Converter DAC0 output channel number 0.
DBG_SWCLK	PF0	PF0			Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1			Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15			Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
HFX TAL_N	PB14				High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13				High Frequency Crystal positive pin.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
I2C0_SCL	PA1	PD7	PC7		I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		I2C0 Serial Data input / output.
LETIM0_OUT0	PD6	PB11	PF0	PC4	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1	PC5	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15		LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7				LEUART1 Receive input.
LEU1_TX	PC6	PA5			LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8				Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7				Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1		Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4				Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5				Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8			Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9			Pulse Counter PCNT2 input number 1.
TIM0_CC0	PA0	PA0		PD1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8		PC8		Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9		PC9		Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10		PC10		Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12		PC9		USART0 clock input / output.
US0_CS	PE13		PC8		USART0 chip select input / output.
US0_RX	PE11		PC10		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10		PC11		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2			USART1 clock input / output.
US1_CS	PB8	PD3			USART1 chip select input / output.
US1_RX	PC1	PD1			USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0			USART1 Asynchronous Transmit. Also used as receive input in half duplex communication.

Alternate	LOCATION				
Functionality	0	1	2	3	Description
					USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4				USART2 clock input / output.
US2_CS	PC5				USART2 chip select input / output.
US2_RX	PC3				USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2				USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

## 4.3 GPIO Pinout Overview

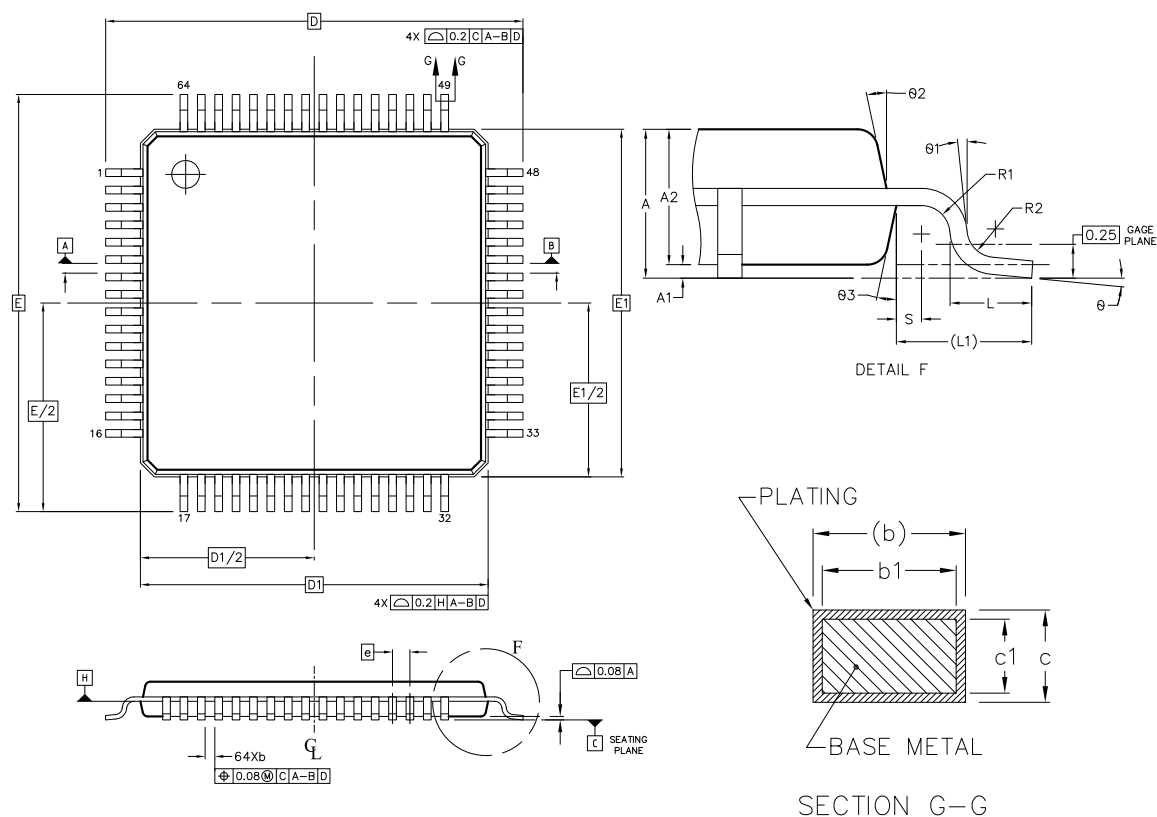
The specific GPIO pins available in *EFM32G232* is shown in Table 4.3 (p. 53). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 4.3. GPIO Pinout**

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	PA10	PA9	PA8	-	-	PA5	PA4	PA3	PA2	PA1	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	-	-	-	-	-	-	-	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	PF5	PF4	PF3	PF2	PF1	PF0

## 4.4 TQFP64 Package

**Figure 4.2. TQFP64**



**Note:**

1. All dimensions & tolerancing confirm to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package body size.
3. Datum 'A,B', and 'B' to be determined at datum plane 'H'.
4. To be determined at seating place 'C'.
5. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25mm per side. 'D1' and 'E1' are maximum plastic body size dimension including mold mismatch. Dimension 'D1' and 'E1' shall be determined at datum plane 'H'.
6. Detail of Pin 1 indicator are optional but must be located within the zone indicated.
7. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm
8. Exact shape of each corner is optional.
9. These dimension apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. All dimensions are in millimeters.

**Table 4.4. QFP64 (Dimensions in mm)**

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	-	1.10	1.20	L1	-		
A1	0.05	-	0.15	R1	0.08	-	-
A2	0.95	1.00	1.05	R2	0.08	-	0.20

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
b	0.17	0.22	0.27	S	0.20	-	-
b1	0.17	0.20	0.23	θ	0°	3.5°	7°
c	0.09	-	0.20	θ1	0°	-	-
C1	0.09	-	0.16	θ2	11°	12°	13°
D	12.0 BSC			θ3	11°	12°	13°
D1	10.0 BSC						
e	0.50 BSC						
E	12.0 BSC						
E1	10.0 BSC						
L	0.45	0.60	0.75				

The TQFP64 Package is 10 by 10 mm in size and has a 0.5 mm pin pitch.

The TQFP64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:

<http://www.silabs.com/support/quality/pages/default.aspx>

# 5 PCB Layout and Soldering

## 5.1 Recommended PCB Layout

Figure 5.1. TQFP64 PCB Land Pattern

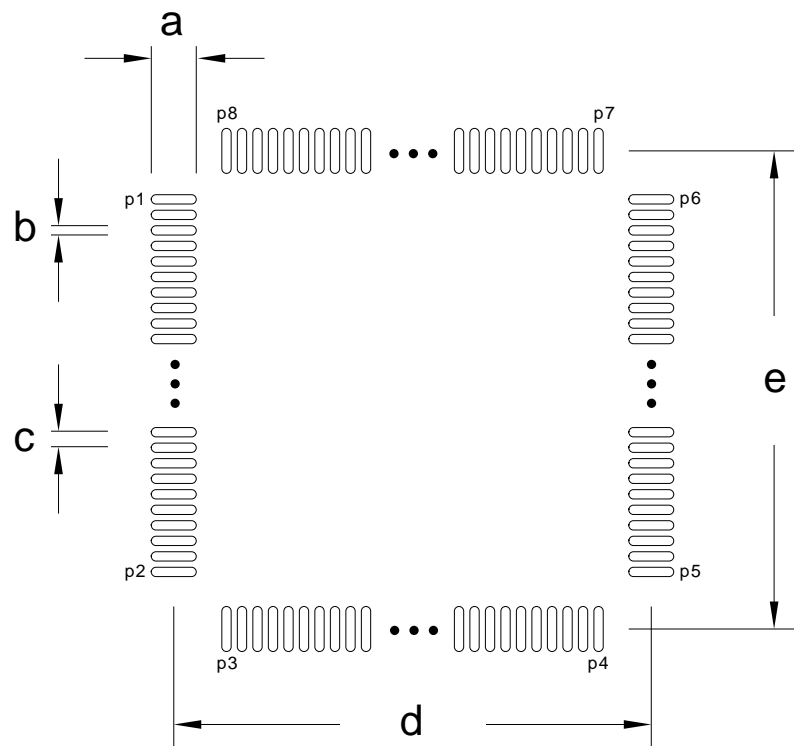


Table 5.1. QFP64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	1.60	P1	1	P6	48
b	0.30	P2	16	P7	49
c	0.50	P3	17	P8	64
d	11.50	P4	32	-	-
e	11.50	P5	33	-	-

Figure 5.2. TQFP64 PCB Solder Mask

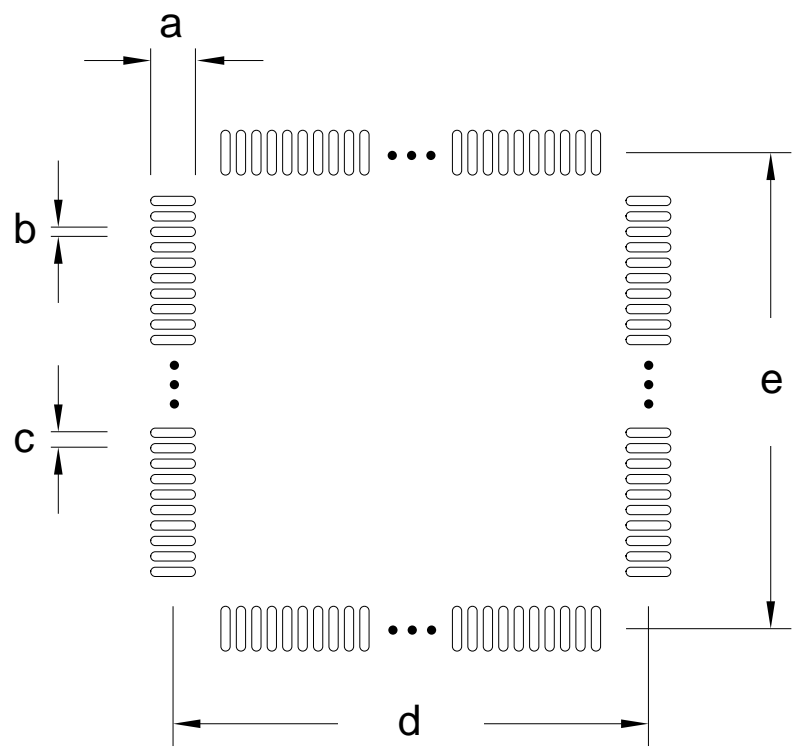
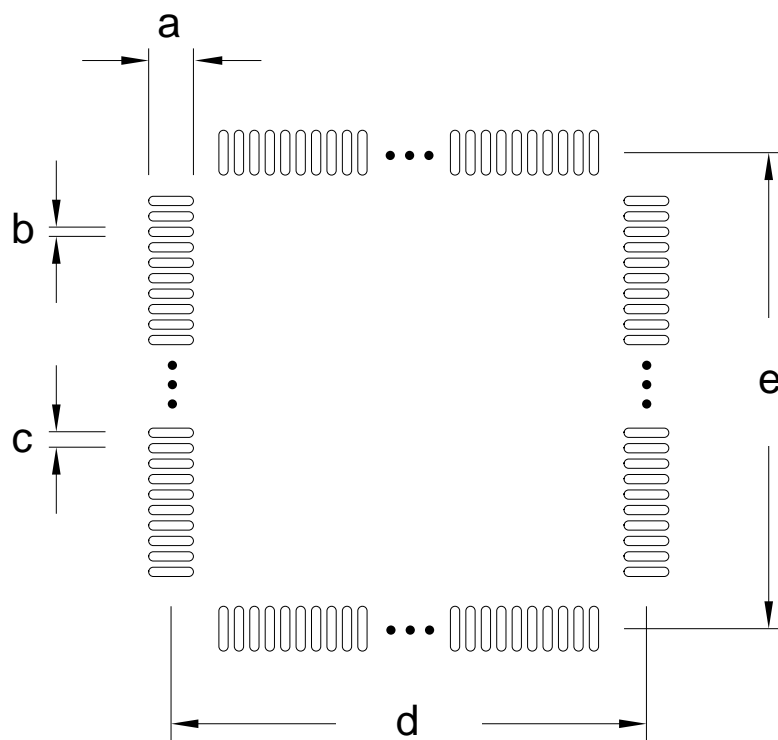


Table 5.2. QFP64 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.72
b	0.42
c	0.50
d	11.50
e	11.50



**Figure 5.3. TQFP64 PCB Stencil Design****Table 5.3. QFP64 PCB Stencil Design Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)
a	1.50
b	0.20
c	0.50
d	11.50
e	11.50

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.2 (p. 54) .

## 5.2 Soldering Information

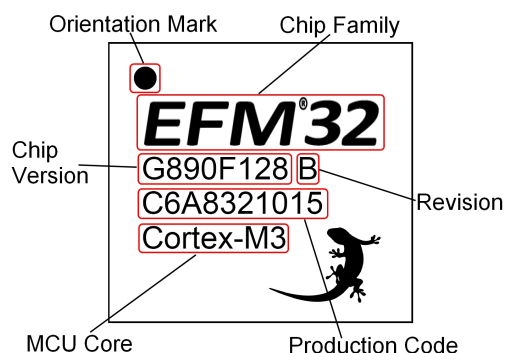
The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

## 6 Chip Marking, Revision and Errata

### 6.1 Chip Marking

In the illustration below package fields and position are shown.

**Figure 6.1. Example Chip Marking (top view)**



### 6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 59) .

### 6.3 Errata

Please see the errata document for EFM32G232 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:

<http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

## 7 Revision History

### 7.1 Revision 1.90

May 22nd, 2015

Added clarification on conditions for  $INL_{ADC}$  and  $DNL_{ADC}$  parameters.

Corrected EM2 current consumption condition in Electrical Characteristics section.

Added AUXHFRCO to block diagram and Electrical Characteristics.

Updated HFRCO table in the Electrical Characteristics section.

Updated EM0, EM2, EM3, and EM4 maximum current specifications in the Electrical Characteristics section.

Updated the Output Low Voltage maximum for sinking 20 mA with  $V_{DD} = 3.0$  V in the Electrical Characteristics section.

Updated the Input Leakage Current maximum in the Electrical Characteristics section.

Updated the minimum and maximum frequency specifications for the LFRCO, HFRCO, and AUXHFRCO in the Electrical Characteristics section.

Updated the maximum current consumption of the HFRCO in the Electrical Characteristics section.

Updated the maximum current consumption of the HFRCO in the Electrical Characteristics section.

Added some minimum ADC SNR, SNDR, and SFDR specifications in the Electrical Characteristics section.

Added some minimum and maximum ADC offset voltage, DNL, and INL specifications in the Electrical Characteristics section.

Added maximum DAC current specifications in the Electrical Characteristics section.

Added maximum ACMP current and maximum and minimum offset voltage specifications in the Electrical Characteristics section.

Added maximum VCMP current and updated typical VCMP current specifications in the Electrical Characteristics section.

Updated references to energyAware Designer to Configurator.

### 7.2 Revision 1.80

July 2nd, 2014

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated current consumption.

Updated transition between energy modes.

Updated power management data.

Updated GPIO data.

Updated LFXO, HFXO, HFRCO and ULFRCO data.

Updated LFRCO and HFRCO plots.

Updated ACMP data.

## 7.3 Revision 1.71

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

Re-added missing DAC-data.

## 7.4 Revision 1.70

September 30th, 2013

Added I2C characterization data.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

## 7.5 Revision 1.60

June 28th, 2013

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

## 7.6 Revision 1.50

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

## 7.7 Revision 1.40

February 27th, 2012

Updated Power Management section.

Corrected operating voltage from 1.8 V to 1.85 V.

Corrected TGRAD<sub>ADCTH</sub> parameter.

Corrected TQFP64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

## 7.8 Revision 0.90

Initial preliminary revision, June 30th, 2011

# A Disclaimer and Trademarks

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