

Maximum Ratings – Q1 @TA = 25°C unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 4) $V_{GS} = 10V$	Steady State	$T_A = 25^\circ C$	I_D	8.0	A
		$T_A = 70^\circ C$		6.5	
Continuous Drain Current (Note 5) $V_{GS} = 10V$	Steady State	$T_A = 25^\circ C$	I_D	10	A
		$T_A = 70^\circ C$		7.8	
Continuous Drain Current (Note 5) $V_{GS} = 4.5V$	Steady State	$T_A = 25^\circ C$	I_D	8.7	A
		$T_A = 70^\circ C$		7.0	
Pulsed Drain Current (Note 6)			I_{DM}	60	A
Avalanche Current (Notes 6 & 7)			I_{AR}	16	A
Repetitive Avalanche Energy (Notes 6 & 7) $L = 0.1mH$			E_{AR}	12.8	mJ

Maximum Ratings – Q2 @TA = 25°C unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 4) $V_{GS} = 10V$	Steady State	$T_A = 25^\circ C$	I_D	6.0	A
		$T_A = 70^\circ C$		4.7	
Continuous Drain Current (Note 5) $V_{GS} = 10V$	Steady State	$T_A = 25^\circ C$	I_D	7.2	A
		$T_A = 70^\circ C$		6.0	
Continuous Drain Current (Note 5) $V_{GS} = 4.5V$	Steady State	$T_A = 25^\circ C$	I_D	6.0	A
		$T_A = 70^\circ C$		5.0	
Pulsed Drain Current (Note 6)			I_{DM}	60	A
Avalanche Current (Notes 6 & 7)			I_{AR}	16	A
Repetitive Avalanche Energy (Notes 6 & 7) $L = 0.1mH$			E_{AR}	12.8	mJ

Thermal Characteristics

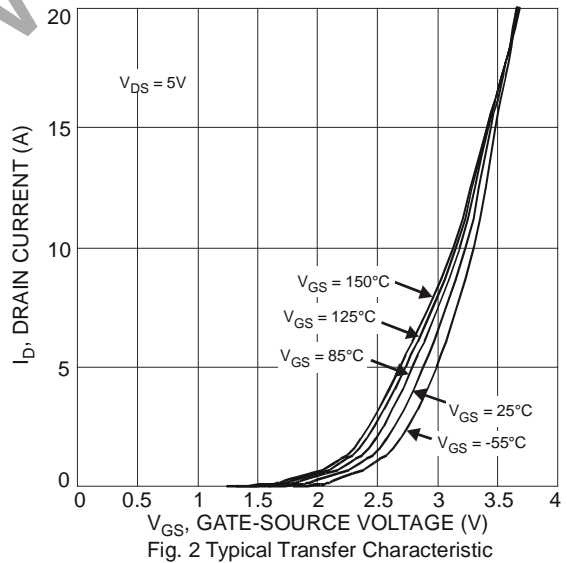
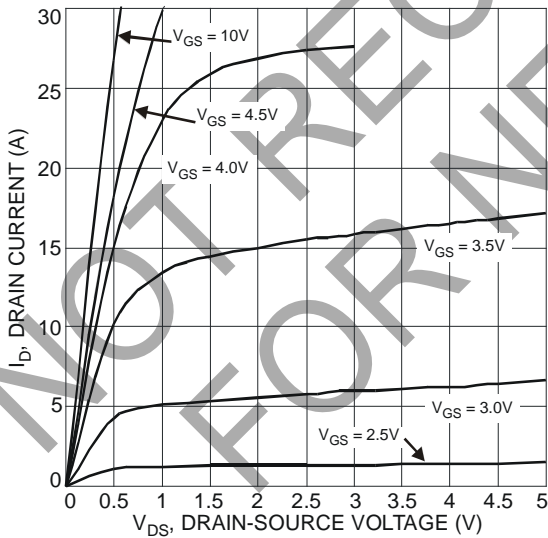
Characteristic	Symbol	Value	Unit
Power Dissipation (Note 4)	P_D	1.19	W
Thermal Resistance, Junction to Ambient @ $T_A = 25^\circ C$ (Note 4)	$R_{\theta JA}$	107	$^\circ C/W$
Power Dissipation (Note 5)	P_D	1.79	W
Thermal Resistance, Junction to Ambient @ $T_A = 25^\circ C$ (Note 5)	$R_{\theta JA}$	70	$^\circ C/W$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

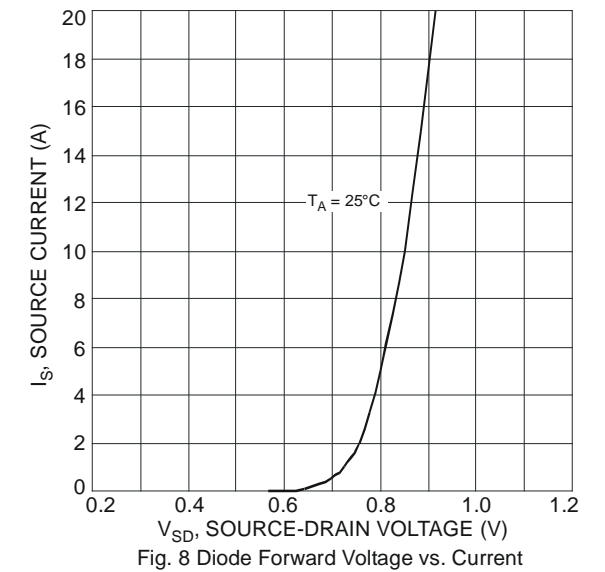
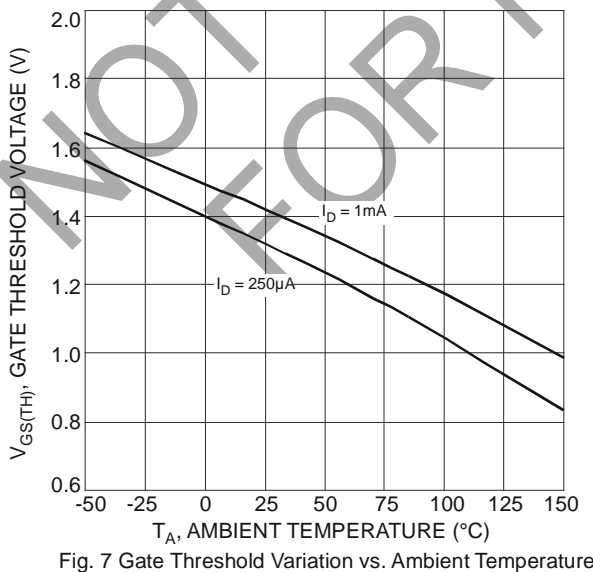
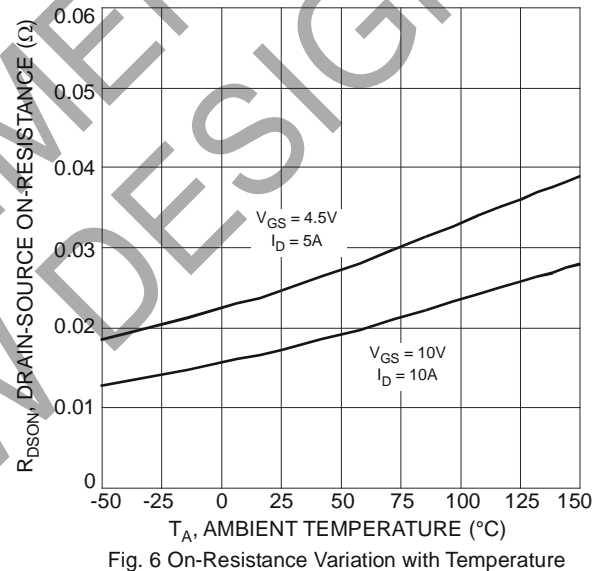
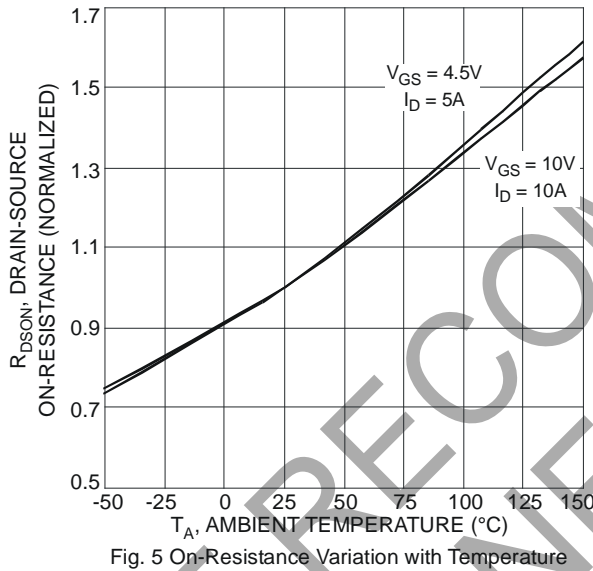
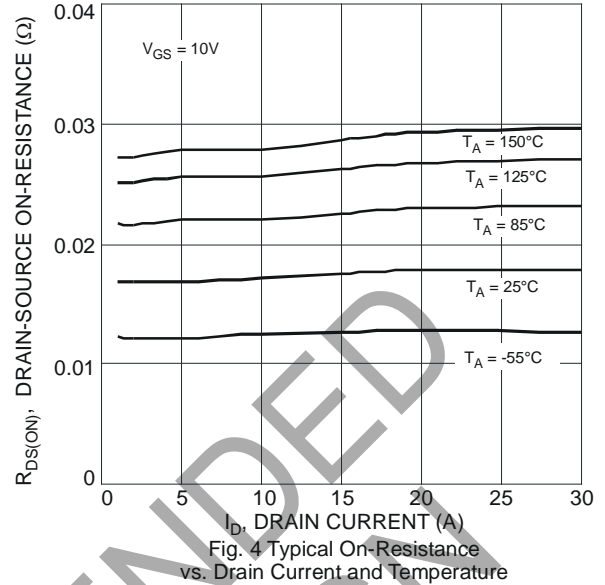
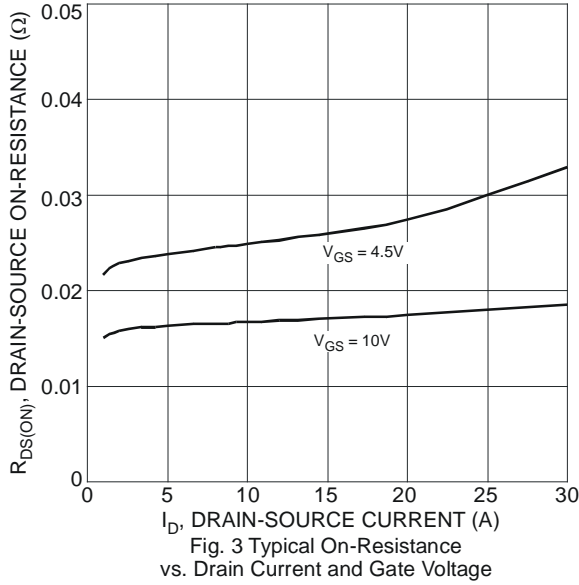
- Notes:
- Device mounted on FR-4 substrate PCB, with minimum recommended pad layout. The value in any given application depends on the user's specific board design. Device contains two active die running at equal power.
 - Device mounted on 1 inch x 1 inch FR4 PCB with high coverage of single sided 1oz copper, in still air conditions. Device contains two active die running at equal power.
 - Repetitive rating, pulse width limited by junction temperature.
 - I_{AR} and E_{AR} rating are based on low frequency and duty cycles to keep $T_J = 25^\circ C$

Electrical Characteristics – Q1 @ T_A = 25°C unless otherwise stated

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	100	μA	V _{DS} = 30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	1.0	—	2.5	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	8.5	12	mΩ	V _{GS} = 10V, I _D = 9.5A
			9.5	15		V _{GS} = 4.5V, I _D = 8.8A
Forward Transfer Admittance	Y _{fs}	—	18	—	S	V _{DS} = 5V, I _D = 9.5A
Diode Forward Voltage	V _{SD}	—	0.45	0.60	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	1276	—	pF	V _{DS} = 15V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	160	—		
Reverse Transfer Capacitance	C _{rss}	—	136	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Gate Resistance	R _g	—	1.48	2.7		
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	14.3	—	nC	V _{DS} = 15V, V _{GS} = 4.5V, I _D = 8.8A
Total Gate Charge (V _{GS} = 10V)	Q _g	—	30.6	—		
Gate-Source Charge	Q _{gs}	—	3.4	—	ns	V _{DS} = 15V, V _{GS} = 10V, I _D = 8.8A
Gate-Drain Charge	Q _{gd}	—	4.3	—		
Turn-On Delay Time	t _{D(on)}	—	15.8	—	ns	V _{GS} = 4.5V, V _{DS} = 15V, R _G = 1.8Ω, I _D = 8.8A
Turn-On Rise Time	t _r	—	27.8	—		
Turn-Off Delay Time	t _{D(off)}	—	29.7	—		
Turn-Off Fall Time	t _f	—	13.6	—		

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.





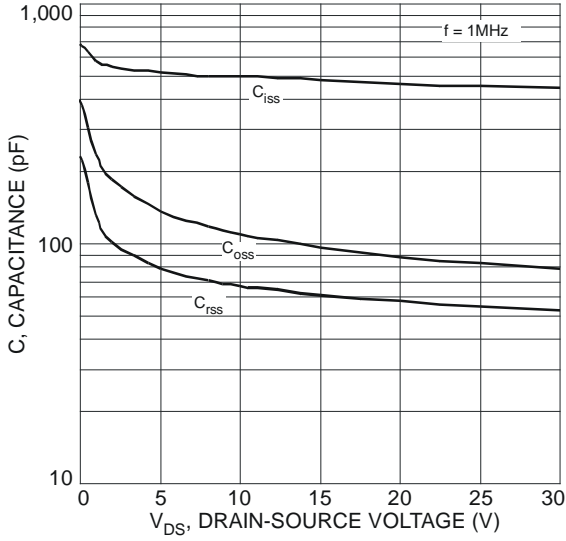


Fig. 9 Typical Total Capacitance

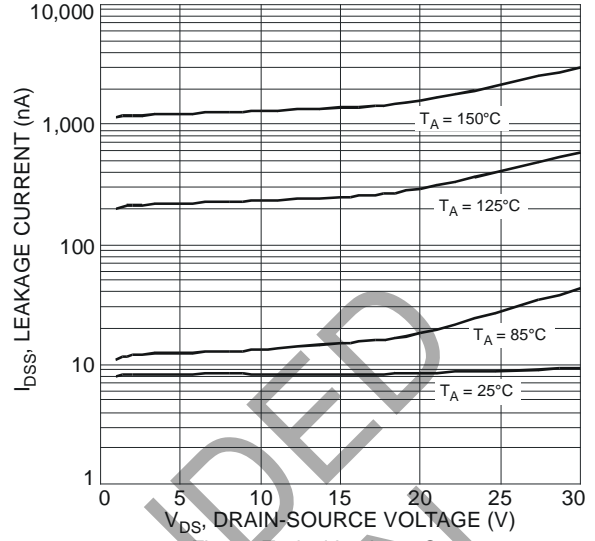


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

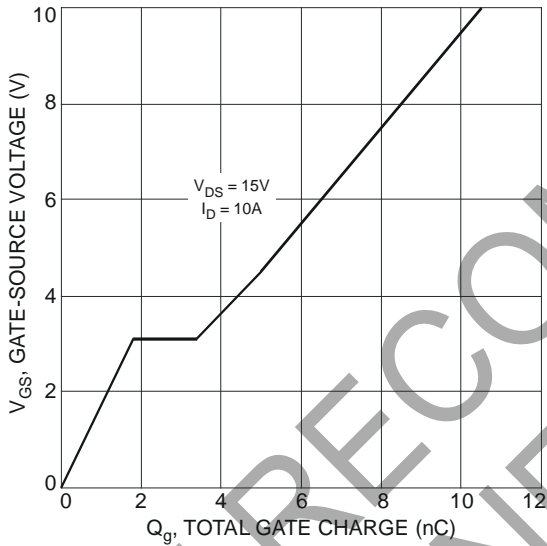


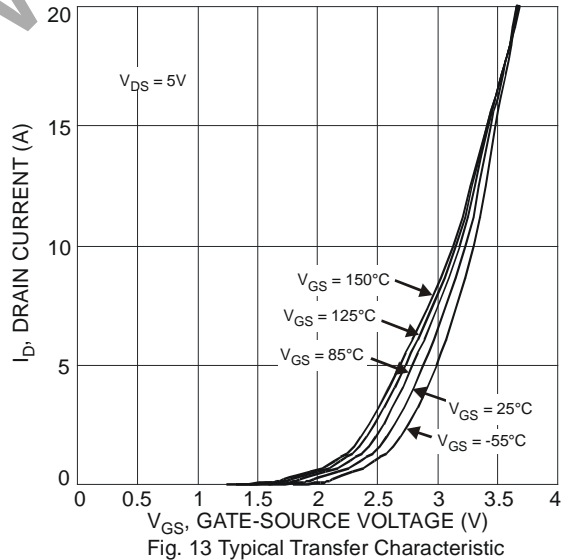
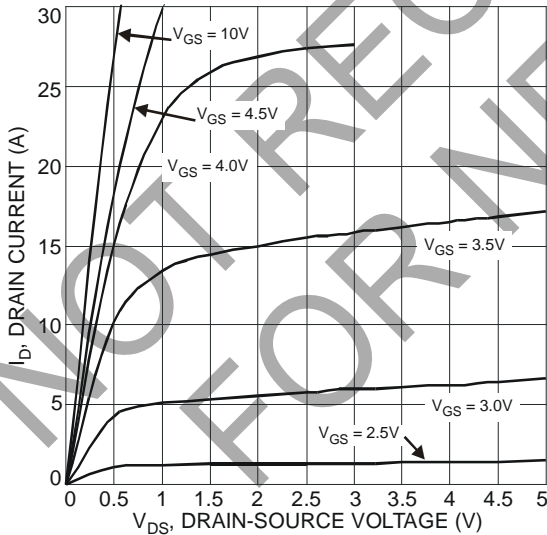
Fig. 11 Gate-Charge Characteristics

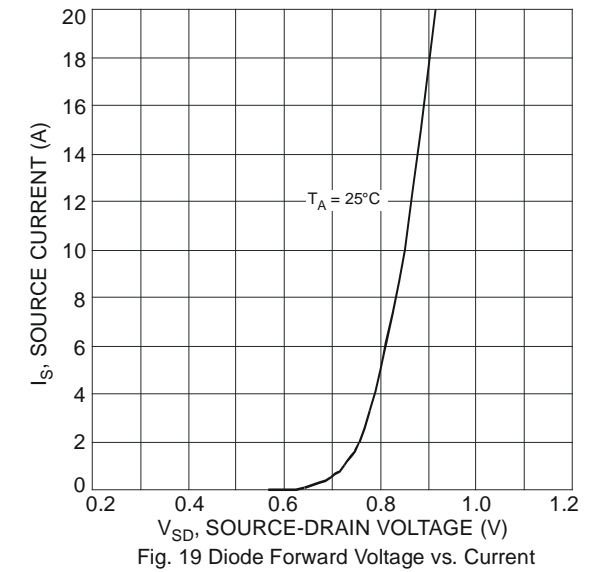
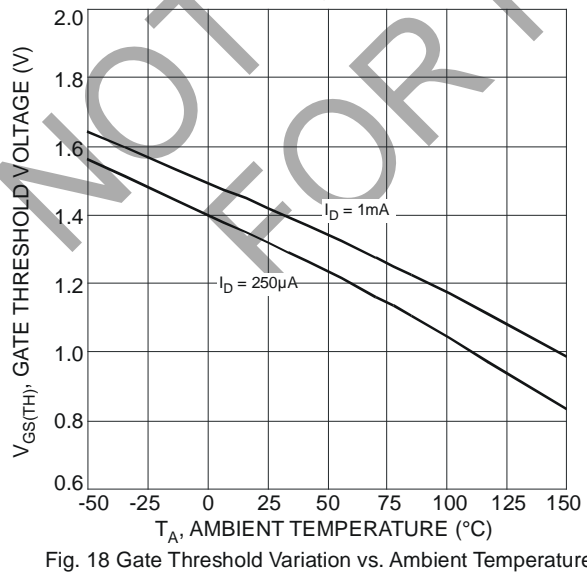
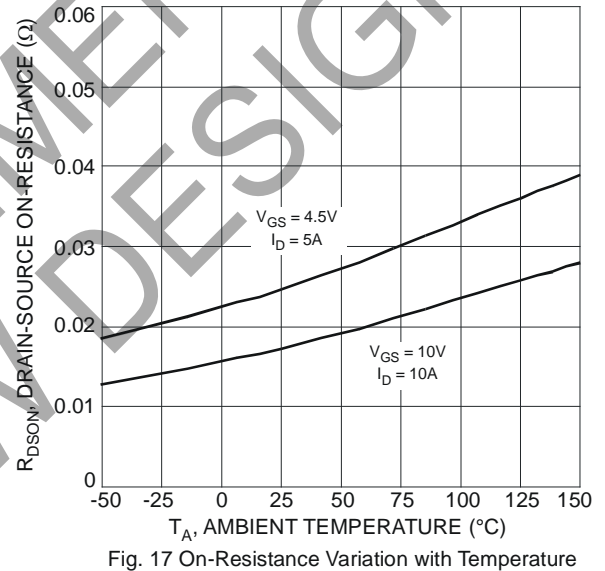
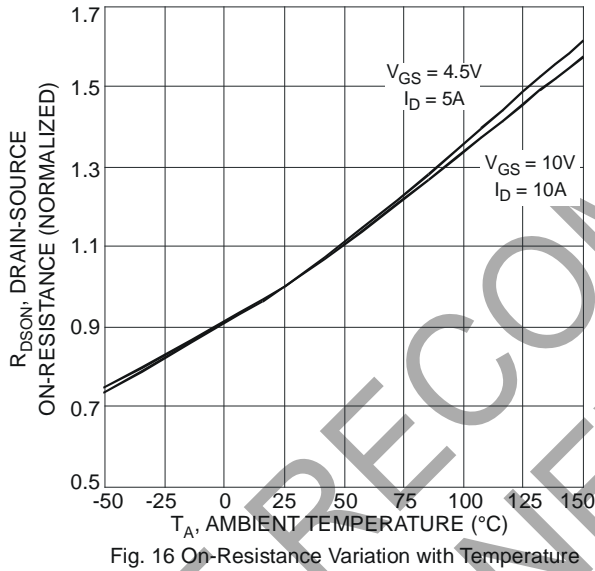
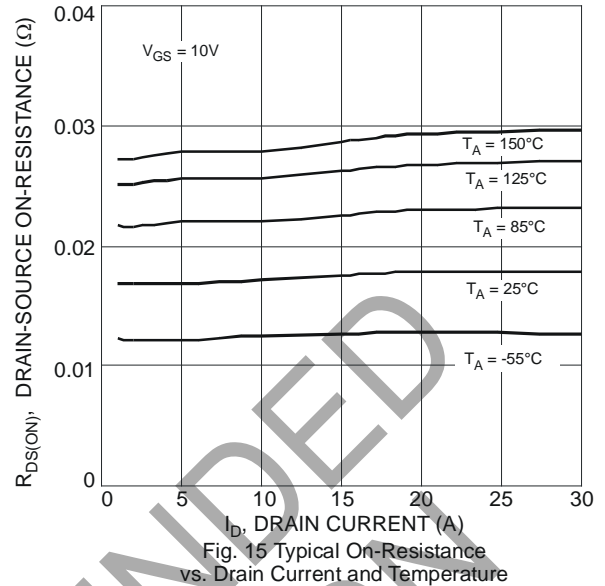
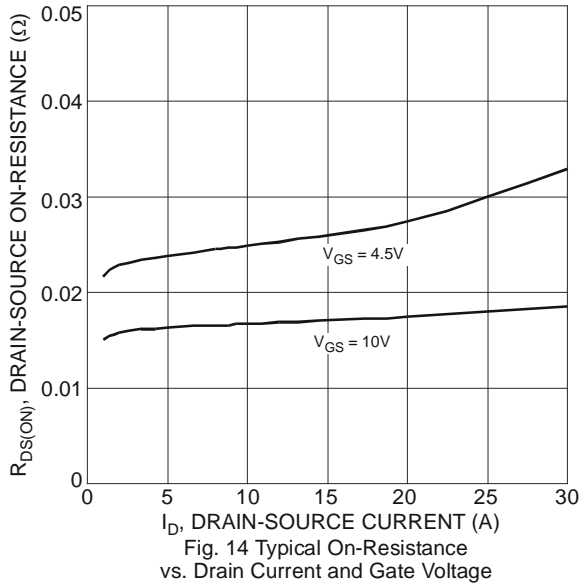
NOT RECOMMENDED FOR NEW DESIGN

Electrical Characteristics – Q2 @ T_A = 25°C unless otherwise stated

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	—	V	V _{GS} = 0V, I _D = 1mA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	—	μA	V _{DS} = 30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	1.0	-	2.4	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	15	22	mΩ	V _{GS} = 10V, I _D = 8.8A
			25	32		V _{GS} = 4.5V, I _D = 7A
Forward Transfer Admittance	Y _{fs}	—	2.5	—	S	V _{DS} = 5V, I _D = 8.8A
Diode Forward Voltage	V _{SD}	—	0.7	1	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	478.9	—	pF	V _{DS} = 15V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	96.7	—		
Reverse Transfer Capacitance	C _{rss}	—	61.4	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Gate Resistance	R _g	—	1.1	—		
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	5.0	—	nC	V _{DS} = 15V, V _{GS} = 4.5V, I _D = 10A
Total Gate Charge (V _{GS} = 10V)	Q _g	—	10.5	—		
Gate-Source Charge	Q _{gs}	—	1.8	—	ns	V _{DS} = 15V, V _{GS} = 10V, I _D = 10A
Gate-Drain Charge	Q _{gd}	—	1.6	—		
Turn-On Delay Time	t _{D(on)}	—	2.9	—	ns	V _{GS} = 10V, V _{DS} = 15V, R _G = 3Ω, R _L = 1.5Ω
Turn-On Rise Time	t _r	—	7.9	—		
Turn-Off Delay Time	t _{D(off)}	—	14.6	—		
Turn-Off Fall Time	t _f	—	3.1	—		

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.





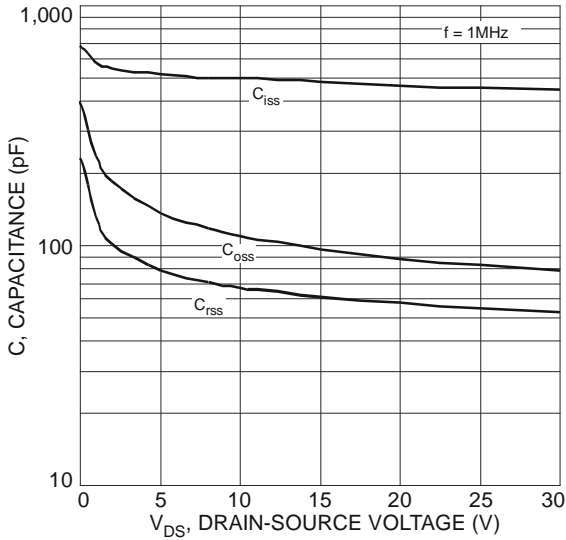


Fig. 20 Typical Total Capacitance

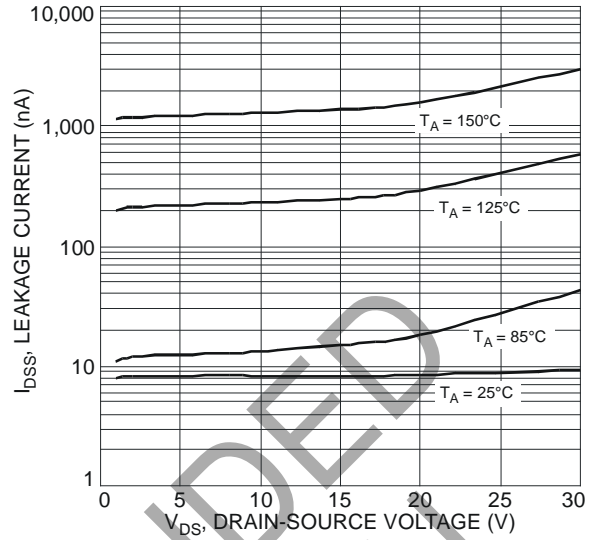


Fig. 21 Typical Leakage Current vs. Drain-Source Voltage

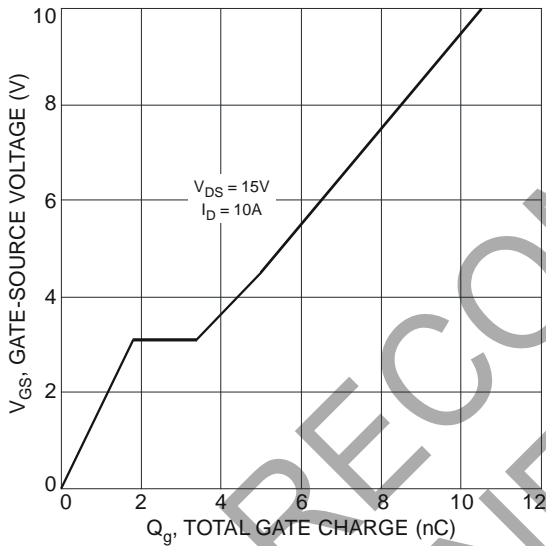


Fig. 22 Gate-Charge Characteristics

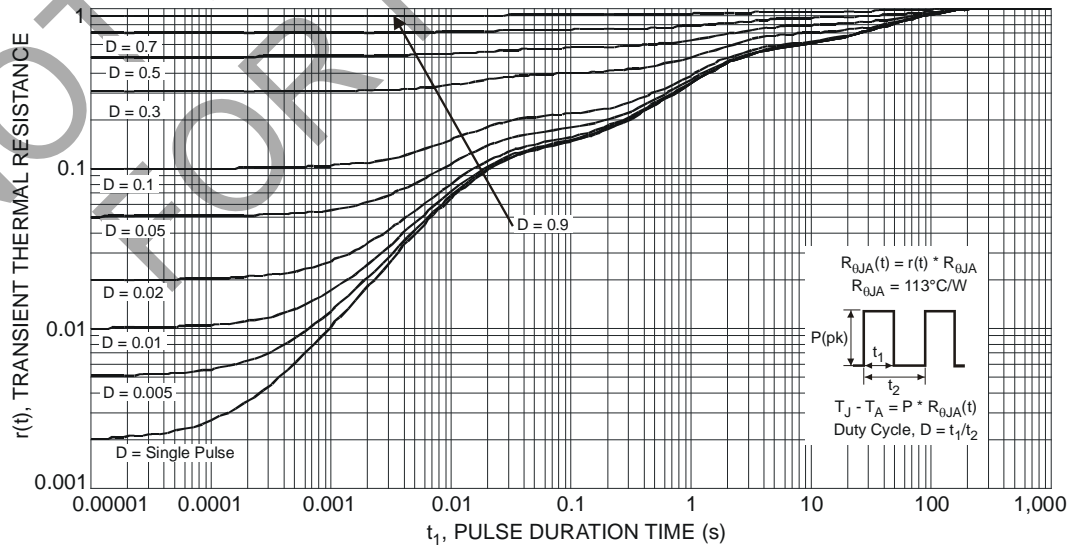
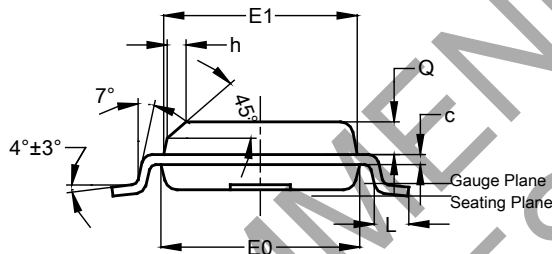
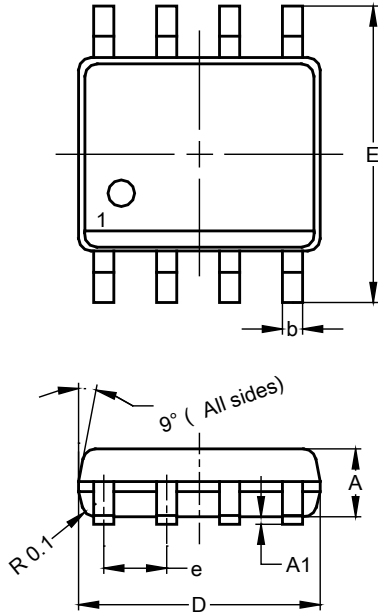


Fig. 23 Transient Thermal Response

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8



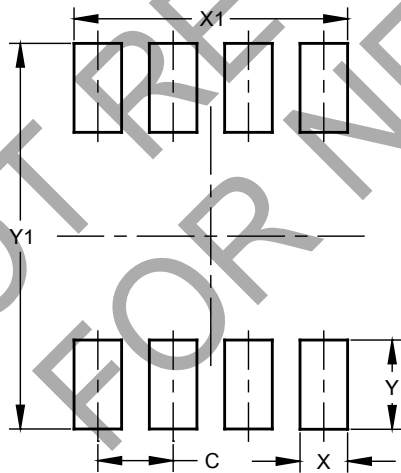
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Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	-	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

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