Maximum Ratings @T_A = 25°C unless otherwise specified

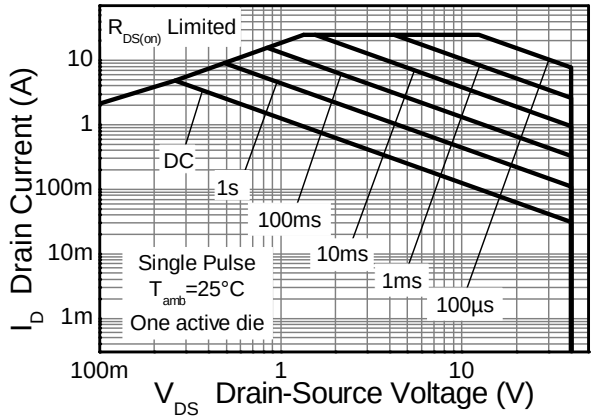
Characteristic			Symbol	Value	Unit
Drain-Source voltage			V_{DSS}	40	V
Gate-Source voltage		(Note 2)	V_{GS}	±20	V
Single Pulsed Avalanche Energy		(Note 9)	E_{AS}	27	mJ
Single Pulsed Avalanche Current		(Note 9)	I_{AS}	15.25	A
Continuous Drain current	V_{GS} = 10V	(Note 4)	I_D	6.3	A
		T_A = 70°C (Note 4)		5.0	
		(Note 3)		4.8	
Pulsed Drain current	V_{GS} = 10V	(Note 5)	I_{DM}	24.8	A
Continuous Source current (Body diode)		(Note 4)	I_S	3.3	A
Pulsed Source current (Body diode)		(Note 5)	I_{SM}	24.8	A

Thermal Characteristics @T_A = 25°C unless otherwise specified

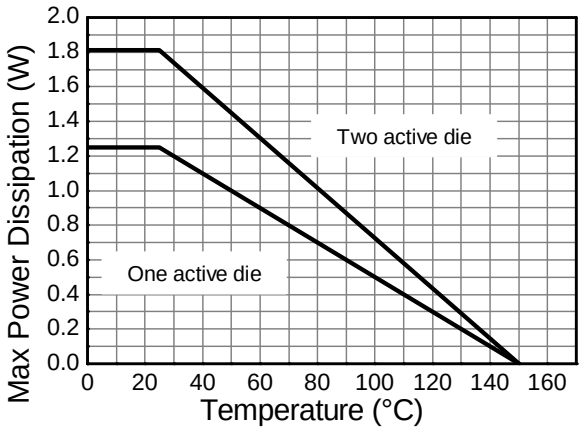
Characteristic		Symbol	Value	Unit
Power dissipation Linear derating factor	(Notes 3 & 6)	P_D	1.25 10.0	W mW/°C
	(Notes 3 & 7)		1.80 14.3	
	(Notes 4 & 6)		2.14 17.2	
Thermal Resistance, Junction to Ambient	(Notes 3 & 6)	$R_{\theta JA}$	100	°C/W
	(Notes 3 & 7)		70	
	(Notes 4 & 6)		58	
Thermal Resistance, Junction to Lead	(Notes 6 & 8)	$R_{\theta JL}$	55	
Operating and storage temperature range		T_J, T_{STG}	-55 to 150	°C

Notes:
2. AEC-Q101 V_{GS} maximum is ±16V.
3. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
4. Same as note (3), except the device is measured at t ≤ 10 sec.
5. Same as note (3), except the device is pulsed with D = 0.02 and pulse width 300µs. The pulse current is limited by the maximum junction temperature.
6. For a dual device with one active die.
7. For a device with two active die running at equal power.
8. Thermal resistance from junction to solder-point (at the end of the drain lead).
9. UIS in production with L = 100µH, V_{DD} = 40V.

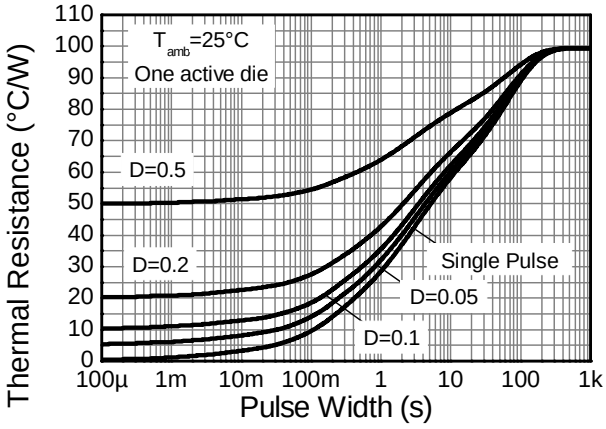
Thermal Characteristics



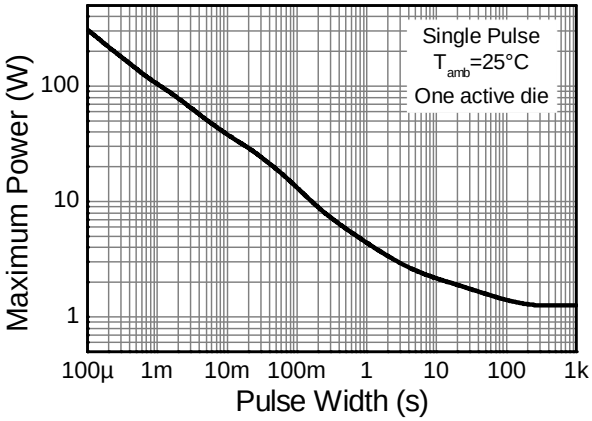
Safe Operating Area



Derating Curve



Transient Thermal Impedance



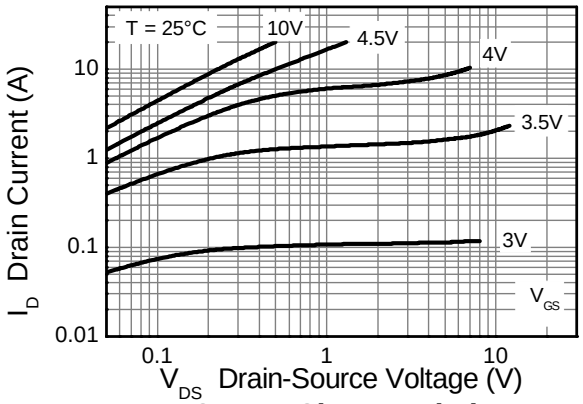
Pulse Power Dissipation

Electrical Characteristics @T_A = 25°C unless otherwise specified

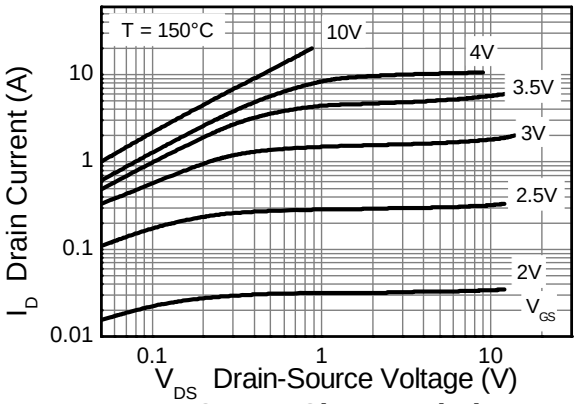
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	I_D = 250μA, V_{GS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	3.0	V	I_D = 250μA, V_{DS} = V_{GS}
Static Drain-Source On-Resistance (Note 10)	$R_{DS\ (ON)}$	—	0.023	0.034	Ω	V_{GS} = 10V, I_D = 6A
			0.039	0.059		V_{GS} = 4.5V, I_D = 5A
Forward Transconductance (Notes 10 & 11)	g_{fs}	—	20.5	—	S	V_{DS} = 15V, I_D = 6A
Diode Forward Voltage (Note 10)	V_{SD}	—	0.87	1.1	V	I_S = 6A, V_{GS} = 0V
Reverse recovery time (Note 11)	t_{rr}		11.2	—	ns	I_S = 2A, di/dt= 100A/μs
Reverse recovery charge (Note 11)	Q_{rr}	—	4.8	—	nC	
DYNAMIC CHARACTERISTICS (Note 11)						
Input Capacitance	C_{iss}	—	453	—	pF	V_{DS} = 20V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	79.1	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	40.5	—	pF	
Total Gate Charge (Note 12)	Q_g	—	4.9	8	nC	V_{GS} = 4.5V
Total Gate Charge (Note 12)	Q_g	—	10	18	nC	V_{GS} = 10V; V_{DS} = 20V, I_D = 6A
Gate-Source Charge (Note 12)	Q_{gs}	—	1.8	—	nC	
Gate-Drain Charge (Note 12)	Q_{gd}	—	2.4	—	nC	
Turn-On Delay Time (Note 12)	$t_{D(on)}$	—	2.7	—	ns	V_{DD} = 20V, V_{GS} = 10V I_D = 1A, $R_G \cong 6.0\Omega$
Turn-On Rise Time (Note 12)	t_r	—	2.7	—	ns	
Turn-Off Delay Time (Note 12)	$t_{D(off)}$	—	14	—	ns	
Turn-Off Fall Time (Note 12)	t_f	—	6	—	ns	

Notes: 10. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
11. For design aid only, not subject to production testing.
12. Switching characteristics are independent of operating junction temperatures.

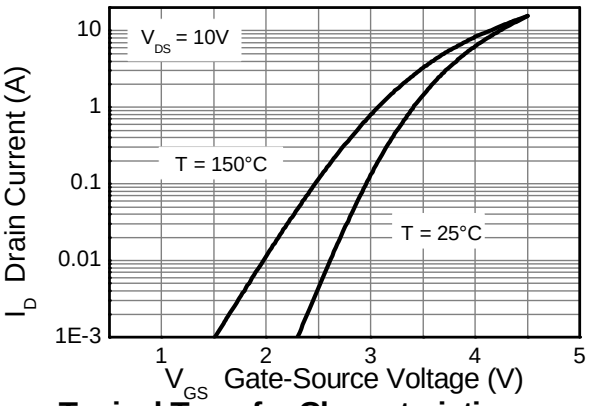
Typical Characteristics



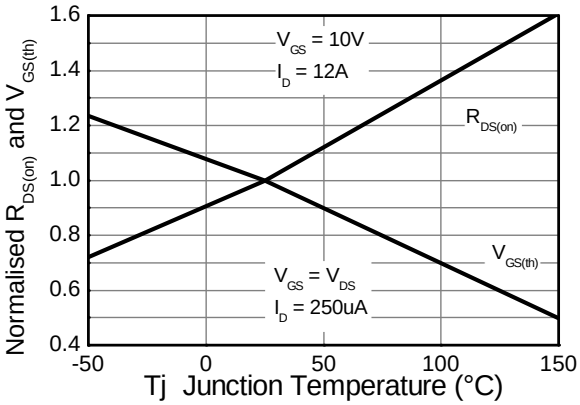
Output Characteristics



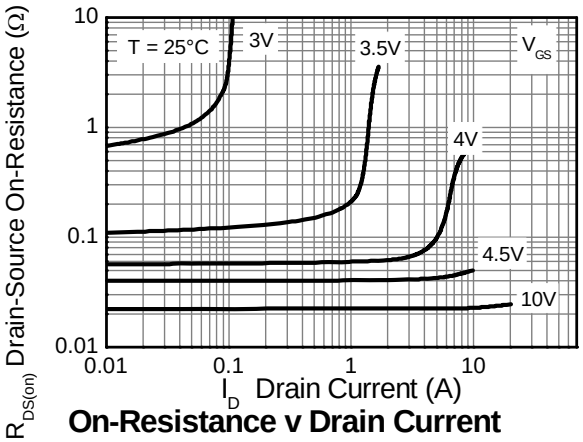
Output Characteristics



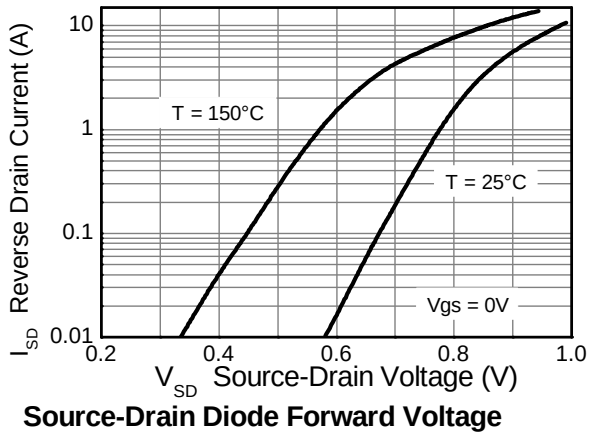
Typical Transfer Characteristics



Normalised Curves v Temperature

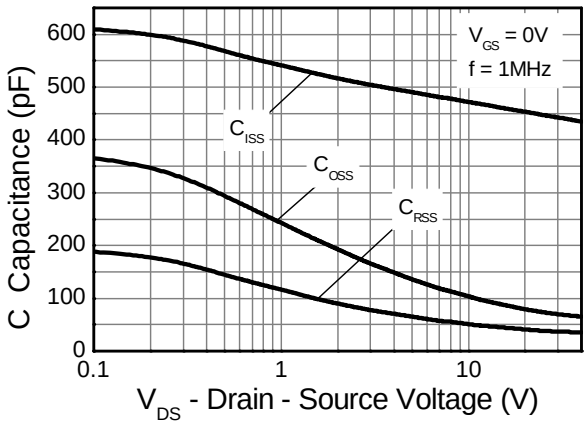


On-Resistance v Drain Current

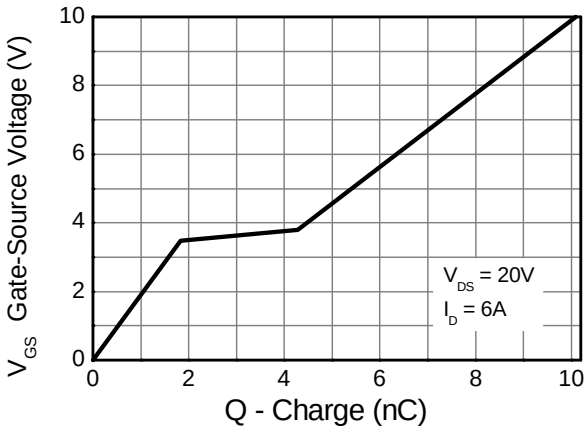


Source-Drain Diode Forward Voltage

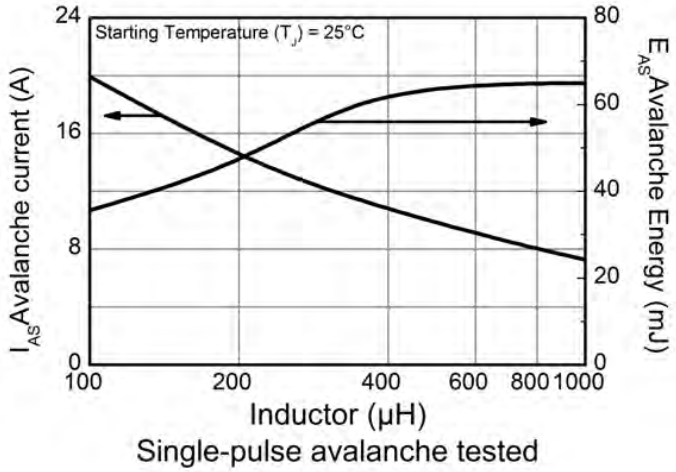
Typical Characteristics – continued



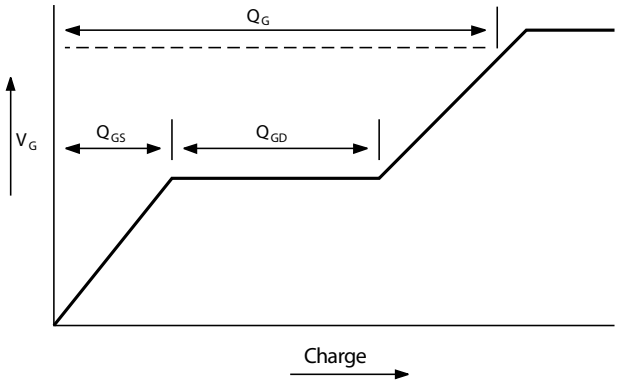
Capacitance v Drain-Source Voltage



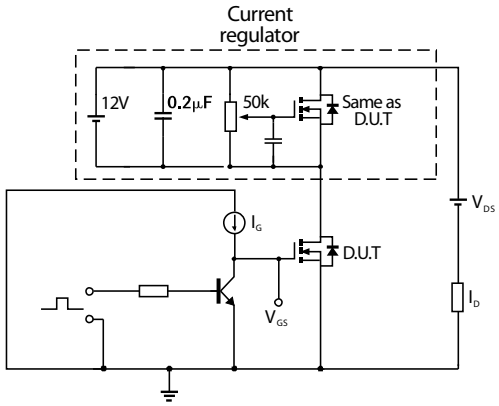
Gate-Source Voltage v Gate Charge



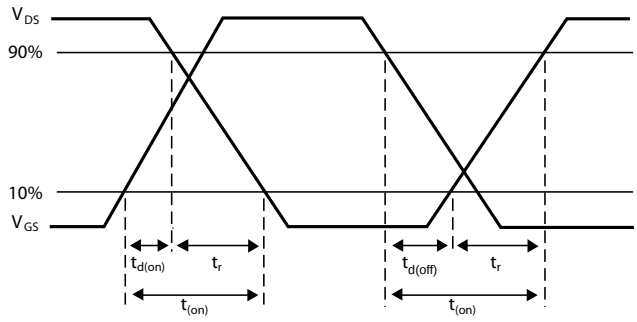
Test Circuits



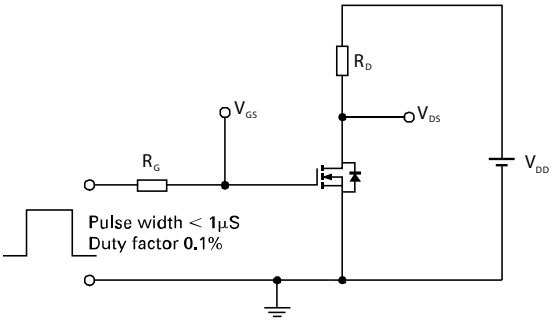
Basic gate charge waveform



Gate charge test circuit

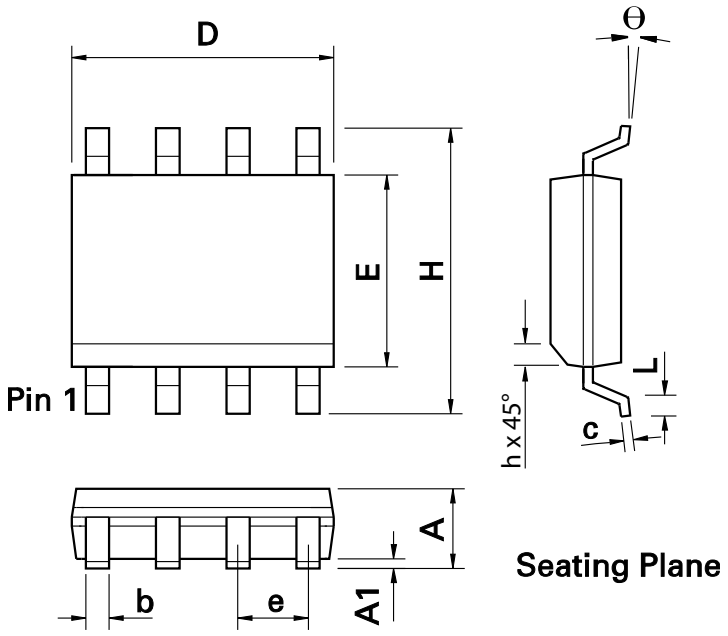


Switching time waveforms



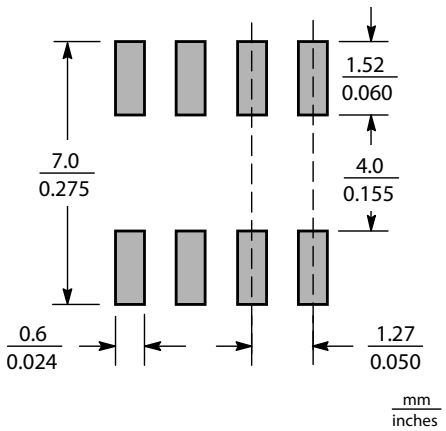
Switching time test circuit

Package Outline Dimensions



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Suggested Pad Layout



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