

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied..... -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[2]..... -0.5V to +4.6V

DC Voltage Applied to Outputs^[2]

in High Z State -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[2] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-12		-15		-17		Unit	
				Min.	Max.	Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = −4.0 mA		2.4		2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA			0.4		0.4		0.4	V	
V _{IH}	Input HIGH Voltage			2.2	V _{CC} + 0.5	2.2	V _{CC} + 0.5	2.2	V _{CC} + 0.5	V	
V _{IL}	Input LOW Voltage ^[2]			−0.5	0.8	−0.5	0.8	−0.5	0.8	V	
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		−1	+1	−1	+1	−1	+1	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled		−1	+1	−1	+1	−1	+1	μA	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., f = f _{MAX} = 1/t _{RC}	Comm'l		200		180		170	mA	
			Ind'l		220		200		180	mA	
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}			30		30		30	mA	
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} − 0.3V, V _{IN} ≥ V _{CC} − 0.3V, or V _{IN} ≤ 0.3V, f = 0	Com'l/Ind'l			8		8		8	mA
			Com'l	L		0.5		0.5		0.5	mA

Note:

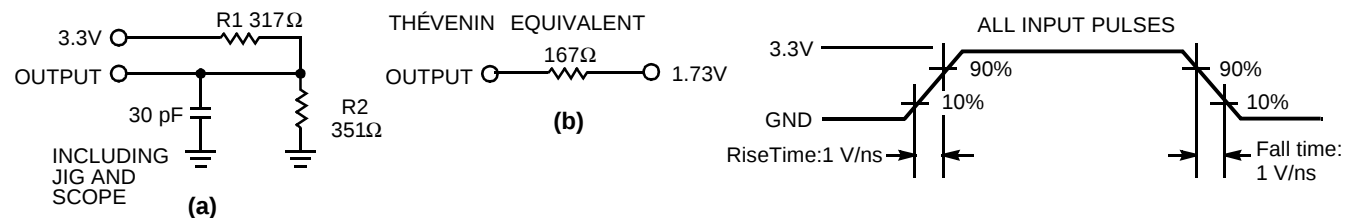
2. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.

DC Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	-20		-25		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC},$ Output Disabled	-1	+1	-1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$		160		150	mA
		Com'I		170		170	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}, \overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		30		30	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}, CE \geq V_{CC} - 0.3\text{V},$ $V_{IN} \geq V_{CC} - 0.3\text{V},$ or $V_{IN} \leq 0.3\text{V}, f = 0$		8		8	mA
		Com'I/Ind'I		0.5		0.5	mA

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$ $V_{CC} = 3.3\text{V}$	8	pF
C_{OUT}	I/O Capacitance		8	pF

AC Test Loads and Waveforms

Note:

- Tested initially and after any design or process changes that may affect these parameters.

AC Switching Characteristics^[4] Over the Operating Range

Parameter	Description	-12		-15		-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{power}	V _{CC} (typical) to the First Access ^[5]	1		1		1		μs
t _{RC}	Read Cycle Time	12		15		17		ns
t _{AA}	Address to Data Valid		12		15		17	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		12		15		17	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		6		7		8	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	0		0		0		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[6, 7]		6		7		8	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[7]	3		3		3		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[6, 7]		6		7		8	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		12		15		17	ns
Write Cycle ^[8, 9]								
t _{WC}	Write Cycle Time	12		15		17		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	10		12		13		ns
t _{AW}	Address Set-Up to Write End	10		12		13		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	10		12		13		ns
t _{SD}	Data Set-Up to Write End	7		8		9		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[7]	3		3		3		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[6, 7]		6		7		8	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{\text{OL}}/I_{\text{OH}}$ and 30-pF load capacitance.
- This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally. T_{power} time has to be provided initially before a read/write operation is started.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW. $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .

AC Switching Characteristics^[4] Over the Operating Range (continued)

Parameter	Description	-20		-25		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{power}	V _{CC} (typical) to the First Access ^[6]	1		1		μs
t _{RC}	Read Cycle Time	20		25		ns
t _{AA}	Address to Data Valid		20		25	ns
t _{OHA}	Data Hold from Address Change	3		3		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		20		25	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		8		10	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	0		0		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[6, 7]		8		10	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[7]	3		3		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[6, 7]		8		10	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		20		25	ns
Write Cycle ^[9]						
t _{WC}	Write Cycle Time	20		25		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	13		15		ns
t _{AW}	Address Set-Up to Write End	13		15		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	13		15		ns
t _{SD}	Data Set-Up to Write End	9		10		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[7]	3		3		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[6, 7]		8		10	ns

Data Retention Characteristics Over the Operating Range (For L version only)

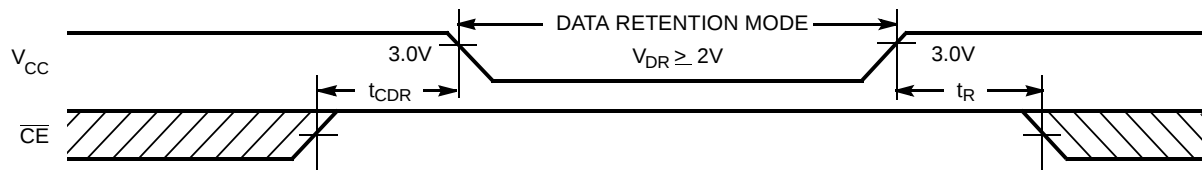
Parameter	Description	Conditions ^[10]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{\text{CC}} = V_{\text{DR}} = 2.0\text{V}$, $\text{CE} \geq V_{\text{CC}} - 0.3\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.3\text{V}$ or $V_{\text{IN}} \leq 0.3\text{V}$		330	μA
$t_{\text{CDR}}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_{\text{R}}^{[11]}$	Operation Recovery Time		t_{RC}		ns

Notes:

10. No input may exceed $V_{\text{CC}} + 0.5\text{V}$

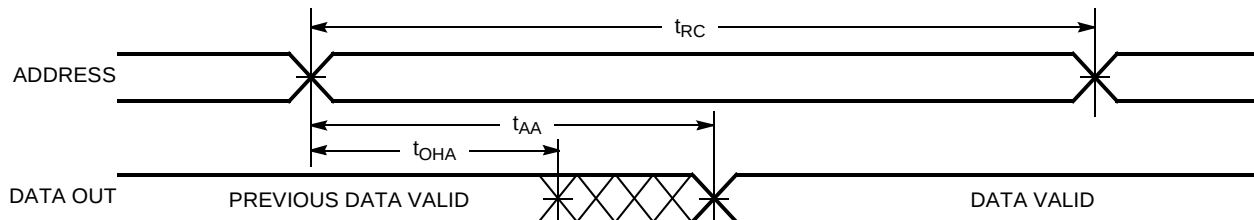
11. $t_{\text{r}} \leq 3\text{ ns}$ for the -12 and -15 speeds. $t_{\text{r}} \leq 5\text{ ns}$ for the -20 ns and slower speeds.

Data Retention Waveform

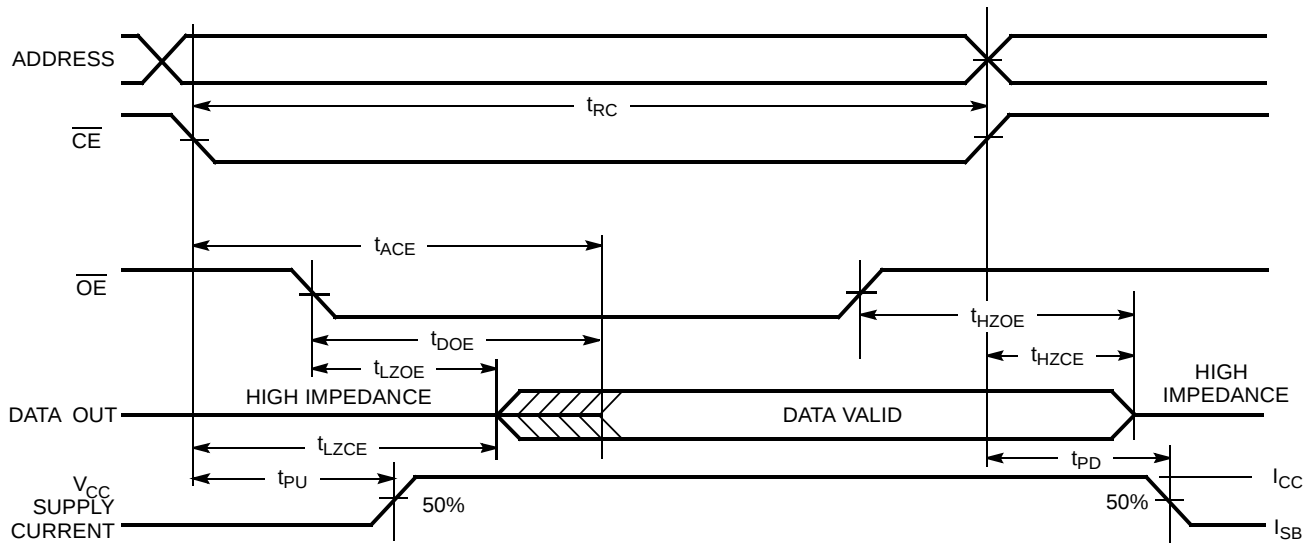


Switching Waveforms

Read Cycle No. 1^[12, 13]



Read Cycle No. 2 ($\overline{OE}$ Controlled)^[13, 14]

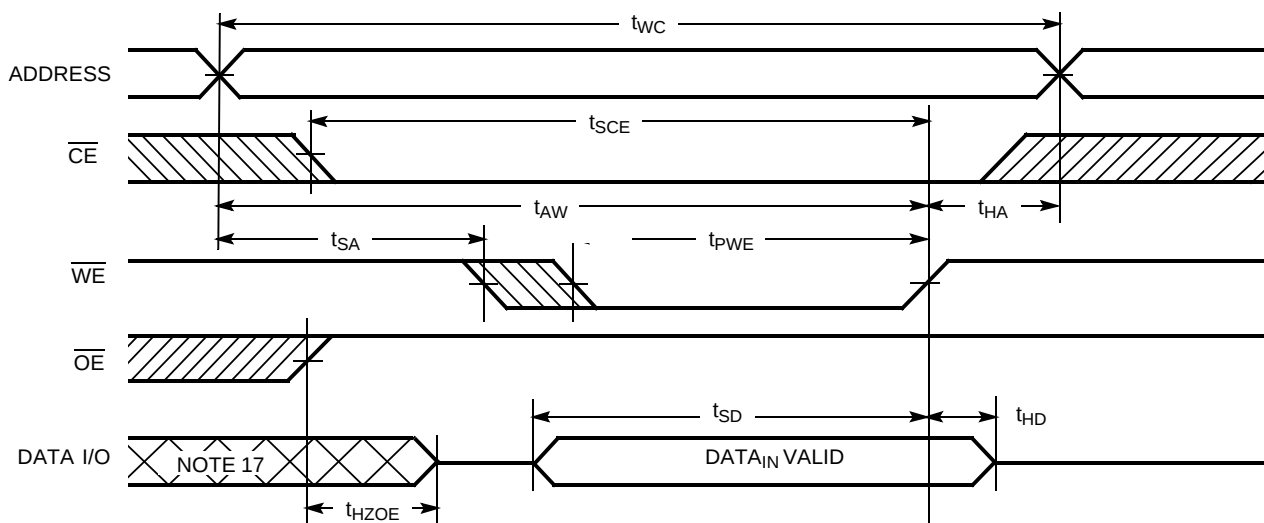


Notes:

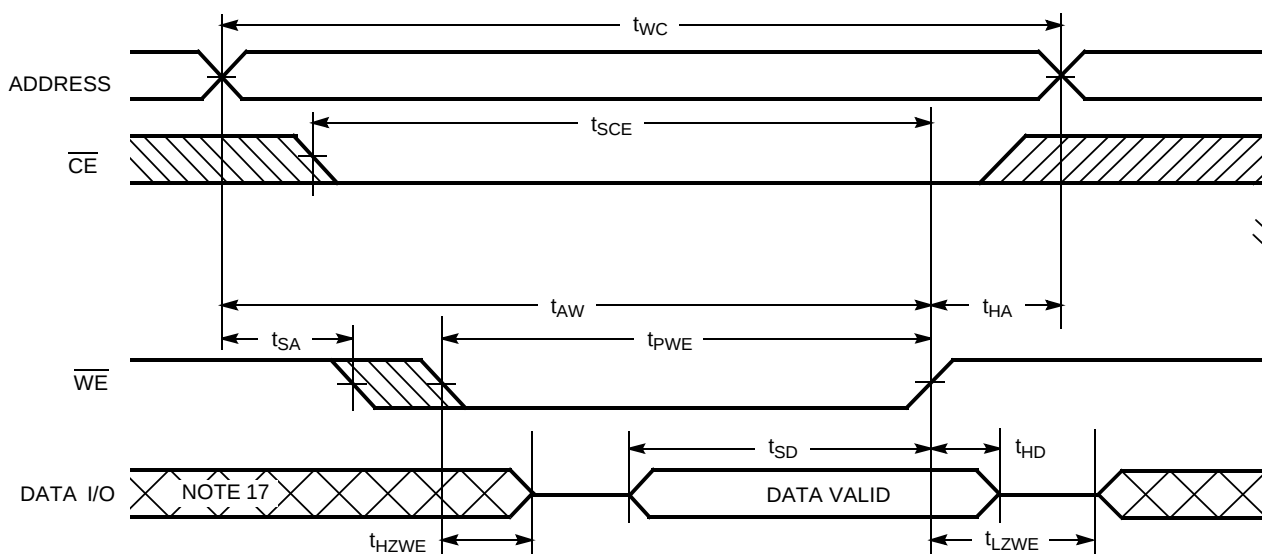
12. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)^[15, 16]



Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[16]



Truth Table

CE	OE	WE	I/O ₀ - I/O ₇	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Notes:

15. Data I/O is high-impedance if $\overline{\text{OE}} = V_{\text{IH}}$.

16. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

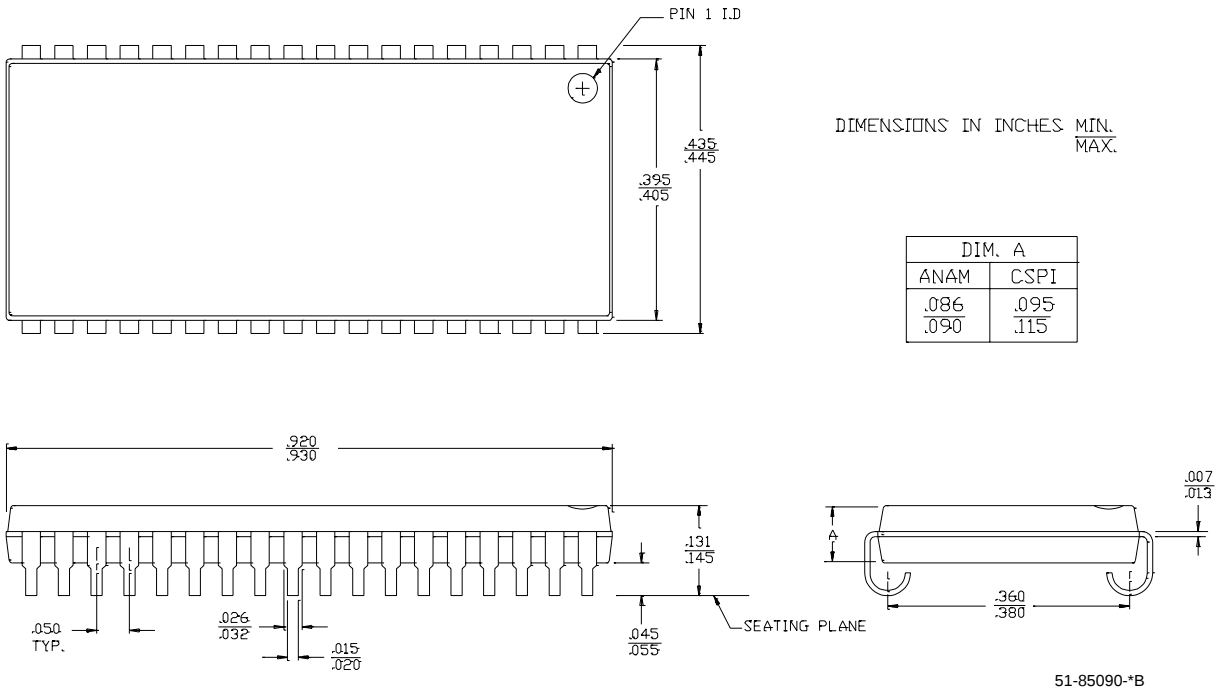
17. During this period the I/Os are in the output state and input signals should not be applied.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1049BV33-12VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BV33-12ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33L-12VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-12VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
15	CY7C1049BV33-15VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BV33L-15VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-15ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33L-15ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33-15VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BV33-15ZI	Z44	44-Pin TSOP II Z44	
17	CY7C1049BV33-17VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BV33L-17VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-17ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33L-17ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33-17VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BV33L-17VI	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-17ZI	Z44	44-Pin TSOP II Z44	
20	CY7C1049BV33-20VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BV33L-20VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-20ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33L-20ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33-20VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BV33-20ZI	Z44	44-Pin TSOP II Z44	
25	CY7C1049BV33-25VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BV33L-25VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049BV33-25ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33L-25ZC	Z44	44-Pin TSOP II Z44	
	CY7C1049BV33-25VI	v36	36-Lead (400-Mil) Molded SOJ	Industrial

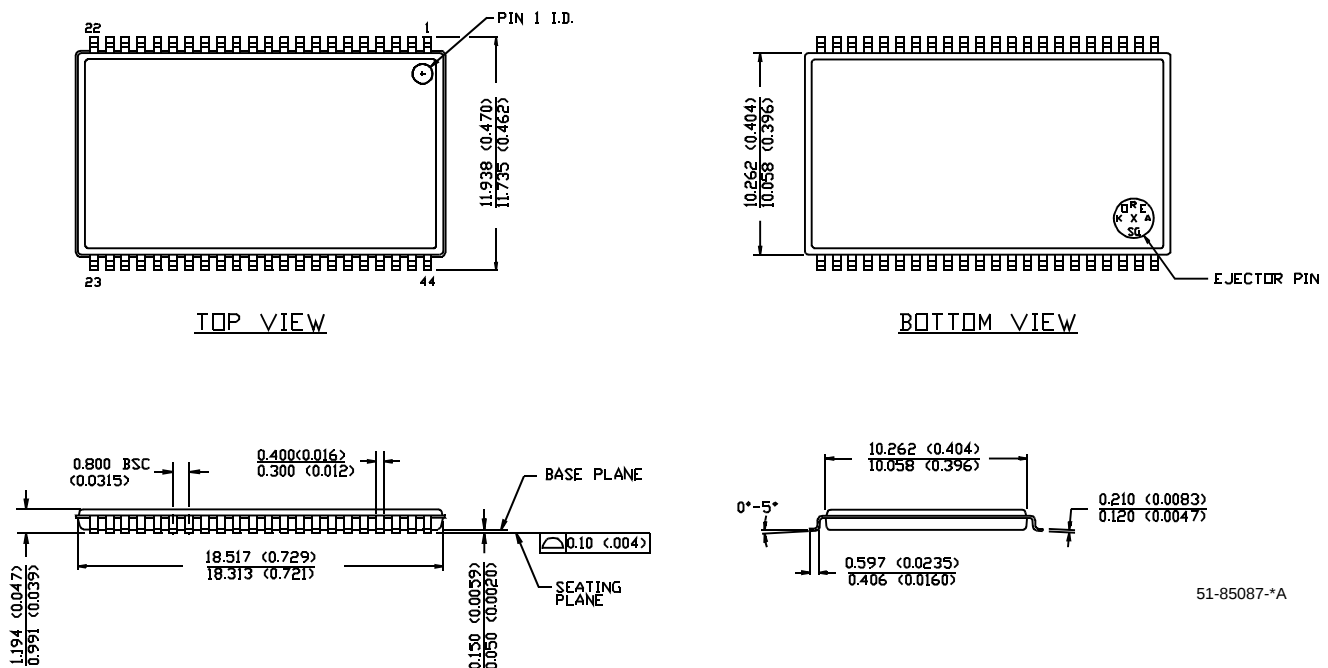
Package Diagrams

36-Lead (400-Mil) Molded SOJ V36



44-Pin TSOP II Z44

DIMENSION IN MM (INCH)
MAX
MIN.



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Document History Page

Document Title: CY7C1049BV33 512K x 8 Static RAM Document Number: 38-05139				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113091	02/13/02	DSG	Change from Spec number: 38-00931 to 38-05139
*A	116475	09/16/02	CEA	Add applications foot note to data sheet, page 1