

## 4-Mbit (256K x 16) Static RAM

### Features

- **Very high speed: 45 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Pin-compatible with CY62146CV30**
- **Ultra-low active power**
  - Typical active current: 1.5 mA @  $f = 1 \text{ MHz}$
  - Typical active current: 8 mA @  $f = f_{\text{max}}$
- **Ultra low standby power**
- **Easy memory expansion with  $\overline{\text{CE}}$ , and  $\overline{\text{OE}}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered 48-ball BGA and 44-pin TSOPII**
- **Also available in Lead-free packages**

### Functional Description<sup>[1]</sup>

The CY62146DV30 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has

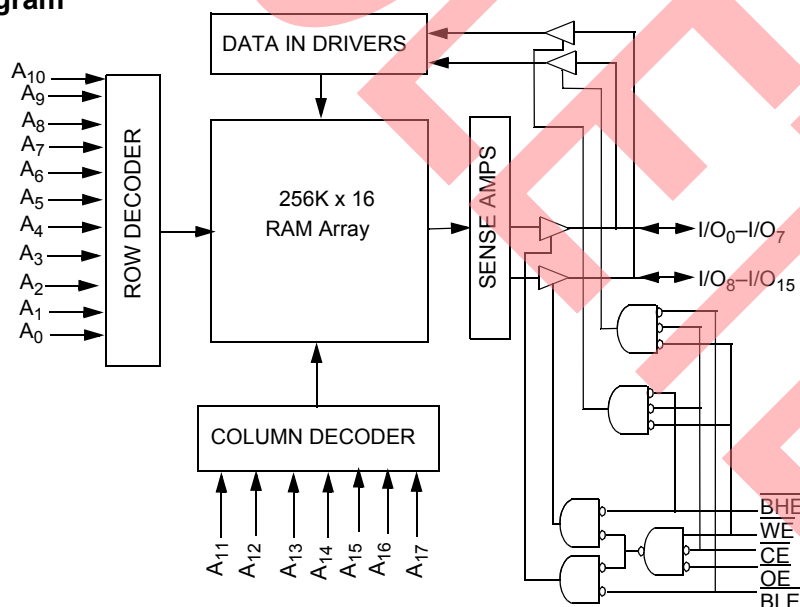
an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{\text{CE}}$  HIGH). The input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{\text{CE}}$  HIGH), outputs are disabled ( $\overline{\text{OE}}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from  $\text{I/O}$  pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ), is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{17}$ ). If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from  $\text{I/O}$  pins ( $\text{I/O}_8$  through  $\text{I/O}_{15}$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{17}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable ( $\overline{\text{WE}}$ ) HIGH. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $\text{I/O}_0$  to  $\text{I/O}_7$ . If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from memory will appear on  $\text{I/O}_8$  to  $\text{I/O}_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

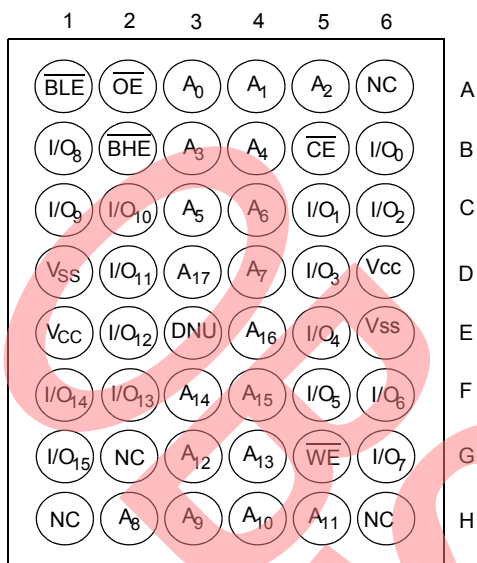
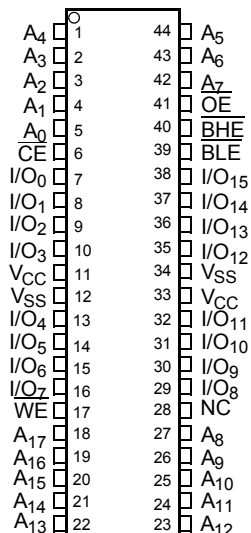
The CY62146DV30 is available in a 48-ball VFBGA, 44-pin TSOPII packages.

### Logic Block Diagram



#### Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration**<sup>[2, 3, 4]</sup>
**VFBGA (Top View)**

**44 TSOP II (Top View)**

**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
					f = 1MHz		f = f <sub>max</sub>			
	Min.	Typ. <sup>[5]</sup>	Max.		Typ. <sup>[5]</sup>	Max.	Typ. <sup>[5]</sup>	Max.	Typ. <sup>[5]</sup>	Max.
CY62146DV30L	2.20V	3.0	3.60	45	1.5	3	10	20	2	12
CY62146DV30LL										8
CY62146DV30L	2.20V	3.0	3.60	55	1.5	3	8	15	2	12
CY62146DV30LL										8
CY62146DV30L	2.20V	3.0	3.60	70	1.5	3	8	15	2	12
CY62146DV30LL										8

**Notes:**

- NC pins are not internally connected on the die.
- DNU pins have to be left floating or tied to V<sub>SS</sub> to ensure proper application.
- Pins H1, G2, and H6 in the BGA package are address expansion pins for 8 Mb, 16 Mb, and 32 Mb, respectively.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage to Ground  
Potential ..... -0.3V to +  $V_{CC(MAX)}$  + 0.3V

DC Voltage Applied to Outputs  
in High-Z State<sup>[6, 7]</sup> ..... -0.3V to  $V_{CC(MAX)}$  + 0.3V

DC Input Voltage<sup>[6, 7]</sup> ..... -0.3V to  $V_{CC(MAX)}$  + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

## Operating Range

Device	Range	Ambient Temperature ( $T_A$ )	$V_{CC}$ <sup>[8]</sup>
CY62146DV30L	Industrial	-40°C to +85°C	2.20V to 3.60V
CY62146DV30LL			

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62146DV30-45			CY62146DV30-55			CY62146DV30-70			Unit
			Min.	Typ. <sup>[5]</sup>	Max.	Min.	Typ. <sup>[5]</sup>	Max.	Min.	Typ. <sup>[5]</sup>	Max.	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -0.1 \text{ mA}$ , $V_{CC} = 2.20\text{V}$	2.0			2.0			2.0			V
		$I_{OH} = -1.0 \text{ mA}$ , $V_{CC} = 2.70\text{V}$	2.4			2.4			2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 0.1 \text{ mA}$ , $V_{CC} = 2.20\text{V}$			0.4			0.4			0.4	V
		$I_{OL} = 2.1 \text{ mA}$ , $V_{CC} = 2.70\text{V}$			0.4			0.4			0.4	V
$V_{IH}$	Input HIGH Voltage	$V_{CC} = 2.2\text{V to } 2.7\text{V}$	1.8		$V_{CC} + 0.3\text{V}$	1.8		$V_{CC} + 0.3\text{V}$	1.8		$V_{CC} + 0.3\text{V}$	V
		$V_{CC} = 2.7\text{V to } 3.6\text{V}$	2.2		$V_{CC} + 0.3\text{V}$	2.2		$V_{CC} + 0.3\text{V}$	2.2		$V_{CC} + 0.3\text{V}$	V
$V_{IL}$	Input LOW Voltage	$V_{CC} = 2.2\text{V to } 2.7\text{V}$	-0.3		0.6	-0.3		0.6	-0.3		0.6	V
		$V_{CC} = 2.7\text{V to } 3.6\text{V}$	-0.3		0.8	-0.3		0.8	-0.3		0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-1		+1	-1		+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	-1		+1	-1		+1	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$ , $V_{CC} = V_{CCmax}$ , $I_{OUT} = 0 \text{ mA}$ , CMOS levels		10	20		8	15		8	15	mA
		$f = 1 \text{ MHz}$		1.5	3		1.5	3		1.5	3	mA
$I_{SB1}$	Automatic CE Power-down Current — CMOS Inputs	$CE \geq V_{CC} - 0.2\text{V}$ , $V_{IN} \geq V_{CC} - 0.2\text{V}$ , $V_{IN} \leq 0.2\text{V}$ , $f = f_{MAX}$ (Address and Data Only), $f = 0$ ( $\overline{OE}$ , $\overline{WE}$ , $\overline{BHE}$ and $\overline{BLE}$ ), $V_{CC} = 3.60\text{V}$	L	2	12		2	12		2	12	$\mu\text{A}$
			LL		8			8			8	
$I_{SB2}$	Automatic CE Power-down Current — CMOS Inputs	$CE \geq V_{CC} - 0.2\text{V}$ , $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$ , $f = 0$ , $V_{CC} = 3.60\text{V}$	L	2	12		2	12		2	12	$\mu\text{A}$
			LL		8			8			8	

### Notes:

6.  $V_{IL(min)}$  = -2.0V for pulse durations less than 20 ns.

7.  $V_{IH(max)}$  =  $V_{CC} + 0.75\text{V}$  for pulse durations less than 20 ns.

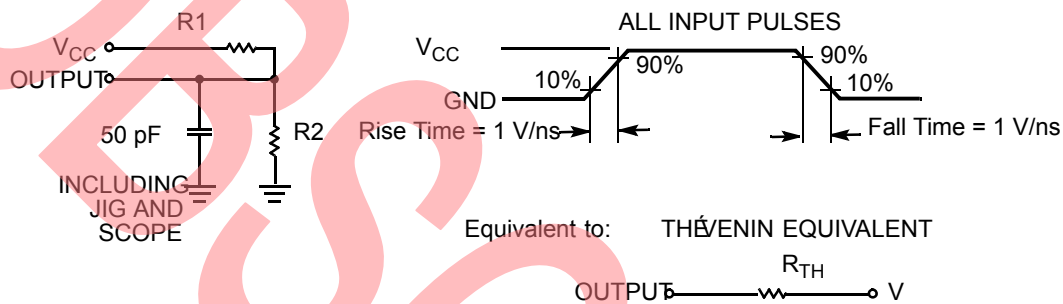
8. Full device AC operation assumes a 100- $\mu\text{s}$  ramp time from 0 to  $V_{CC(min)}$  and 200  $\mu\text{s}$  wait time after  $V_{CC}$  stabilization.

**Capacitance** (for all packages)<sup>[9]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC}(\text{typ})$	10	pF
$C_{OUT}$	Output Capacitance		10	pF

**Thermal Resistance**<sup>[9]</sup>

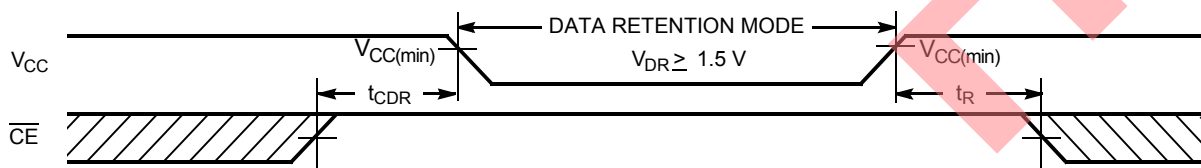
Parameter	Description	Test Conditions	BGA	TSOP II	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	72	75.13	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		8.86	8.95	$^\circ\text{C/W}$

**AC Test Loads and Waveforms**<sup>[10]</sup>


Parameters	2.50V	3.0V	Unit
R1	16667	1103	$\Omega$
R2	15385	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.20	1.75	V

**Data Retention Characteristics** (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.5			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.5\text{V}$ $CE \geq V_{CC} - 0.2\text{V}$ , $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	L		9	$\mu\text{A}$
			LL		6	
$t_{CDR}^{[9]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[11]}$	Operation Recovery Time		$t_{RC}$			ns

**Data Retention Waveform**

**Notes:**

9. Tested initially and after any design or process changes that may affect these parameters.  
 10. Test condition for the 45 ns part is a load capacitance of 30 pF.  
 11. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC}(\text{min.}) \geq 100\ \mu\text{s}$  or stable at  $V_{CC}(\text{min.}) \geq 100\ \mu\text{s}$ .

**Switching Characteristics** Over the Operating Range <sup>[12]</sup>

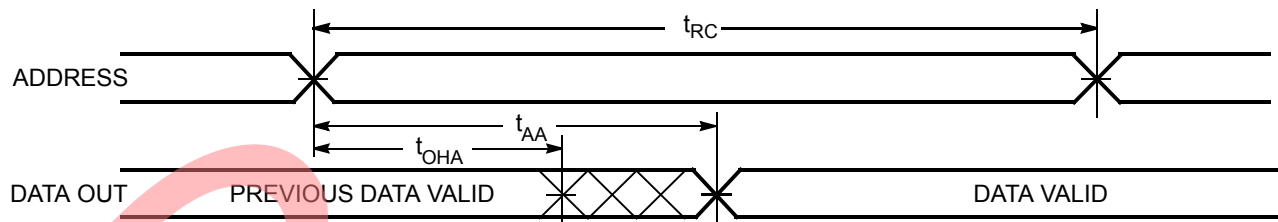
Parameter	Description	45 ns <sup>[10]</sup>		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t <sub>RC</sub>	Read Cycle Time	45		55		70		ns
t <sub>AA</sub>	Address to Data Valid		45		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		10		ns
t <sub>ACE</sub>	CE LOW to Data Valid		45		55		70	ns
t <sub>DOE</sub>	OE LOW to Data Valid		25		25		35	ns
t <sub>LZOE</sub>	OE LOW to Low Z <sup>[13]</sup>	5		5		5		ns
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[13, 14]</sup>		15		20		25	ns
t <sub>LZCE</sub>	CE LOW to Low Z <sup>[13]</sup>	10		10		10		ns
t <sub>HZCE</sub>	CE HIGH to High Z <sup>[13, 14]</sup>		20		20		25	ns
t <sub>PU</sub>	CE LOW to Power-Up	0		0		0		ns
t <sub>PD</sub>	CE HIGH to Power-Down		45		55		70	ns
t <sub>DBE</sub>	BLE/BHE LOW to Data Valid		25		25		35	ns
t <sub>LZBE</sub>	BLE/BHE LOW to Low Z <sup>[13]</sup>	10		10		10		ns
t <sub>HZBE</sub>	BLE/BHE HIGH to High Z <sup>[13, 14]</sup>		15		20		25	ns
Write Cycle <sup>[15]</sup>								
t <sub>WC</sub>	Write Cycle Time	45		55		70		ns
t <sub>SCE</sub>	CE LOW to Write End	40		40		60		ns
t <sub>AW</sub>	Address Set-up to Write End	40		40		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		0		ns
t <sub>PWE</sub>	WE Pulse Width	35		40		45		ns
t <sub>BW</sub>	BLE/BHE LOW to Write End	40		40		60		ns
t <sub>SD</sub>	Data Set-up to Write End	25		25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>HZWE</sub>	WE LOW to High-Z <sup>[13, 14]</sup>		15		20		25	ns
t <sub>LZWE</sub>	WE HIGH to Low-Z <sup>[13]</sup>	10		10		10		ns

**Notes:**

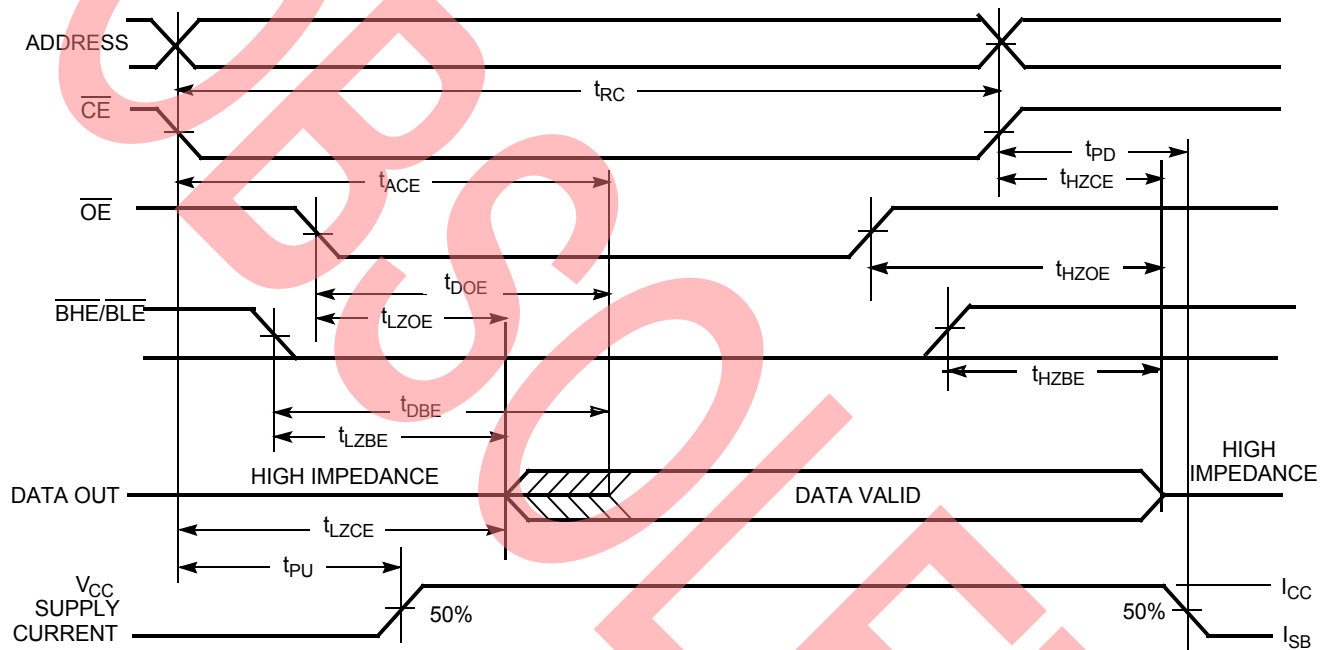
12. Test conditions for all parameters other than three-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
13. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
14. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high-impedance state.
15. The internal Write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{IL}$ ,  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

### Read Cycle 1 (Address Transition Controlled)<sup>[16, 17]</sup>

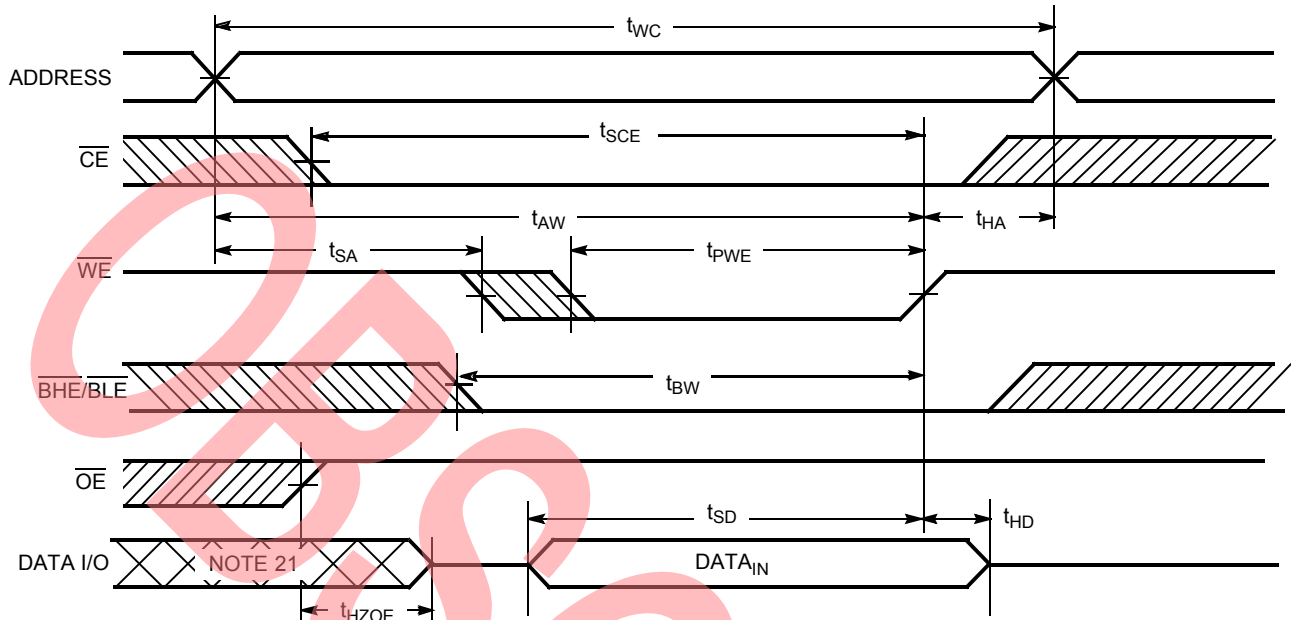
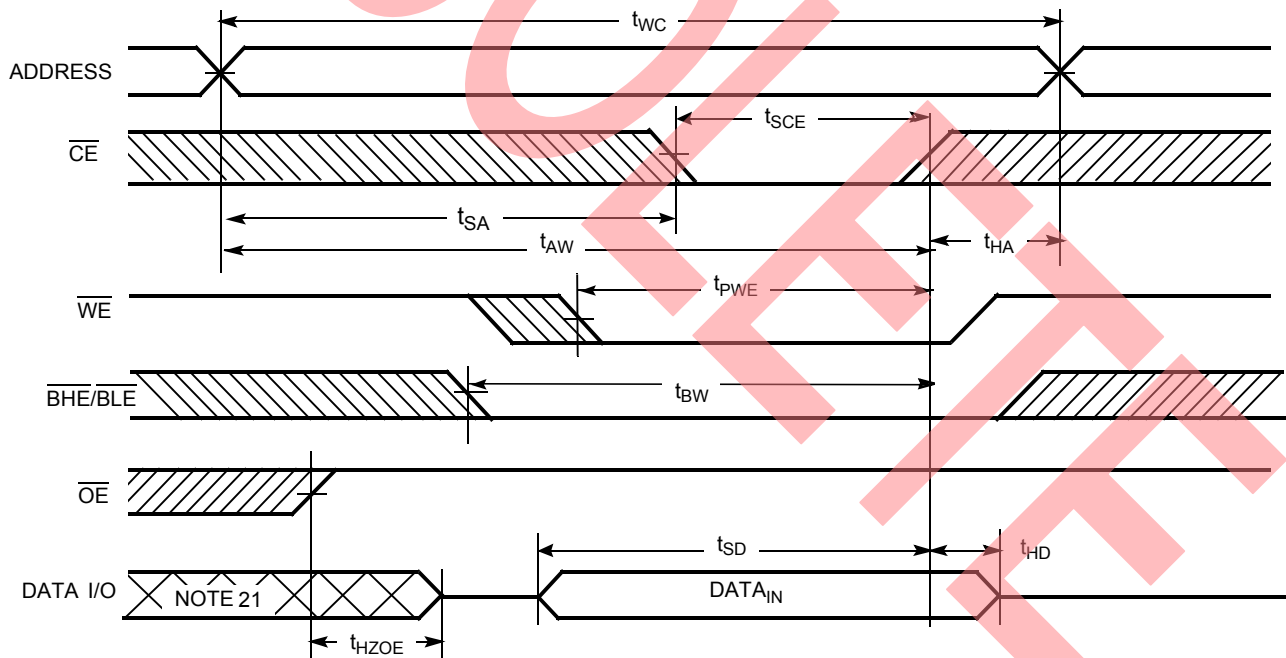


### Read Cycle No. 2 ( $\overline{OE}$ Controlled)<sup>[17, 18]</sup>

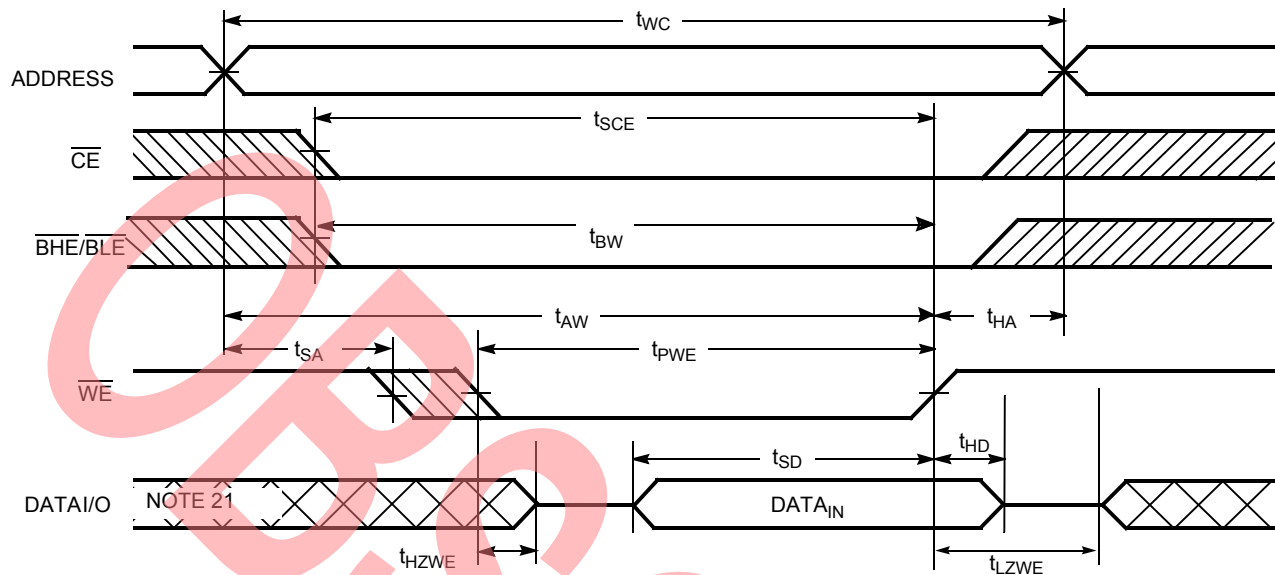
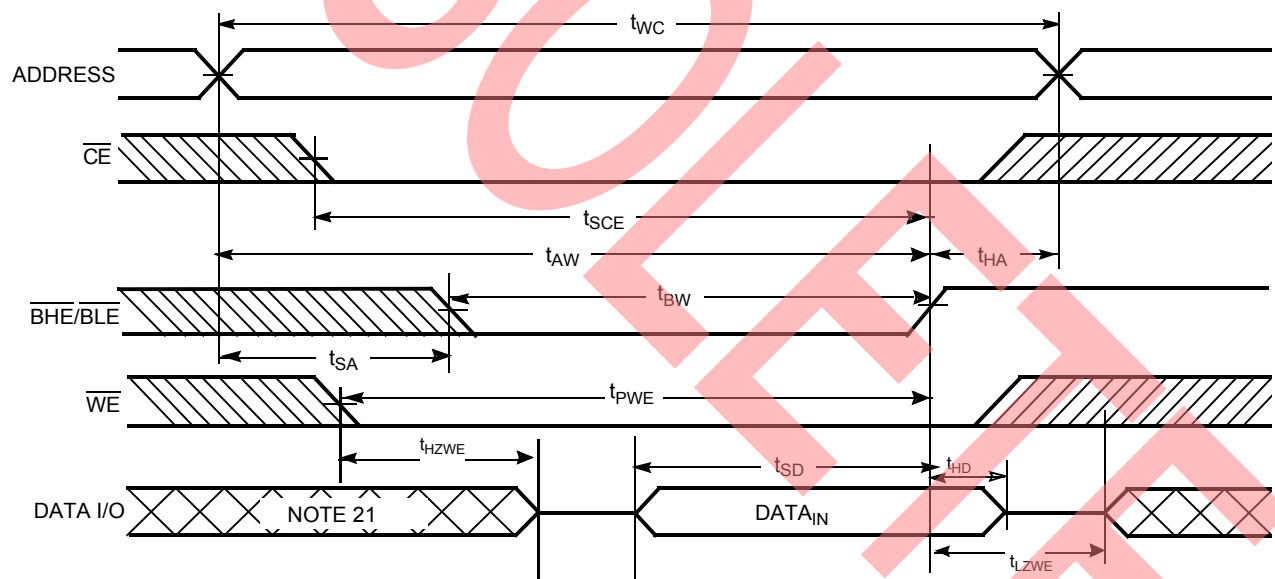


#### Notes:

16. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .
17.  $\overline{WE}$  is HIGH for read cycle.
18. Address valid prior to or coincident with  $\overline{CE}$  and  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)<sup>[15, 19, 20]</sup>**

**Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)<sup>[15, 19, 20]</sup>**

**Notes:**

19. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .  
 20. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\text{WE} = V_{\text{IH}}$ , the output remains in a high-impedance state.  
 21. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[20]</sup>**

**Write Cycle No. 4 ( $\overline{\text{BHE/BL}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[20]</sup>**


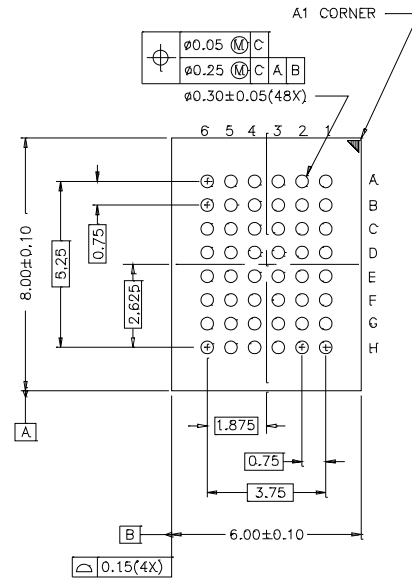
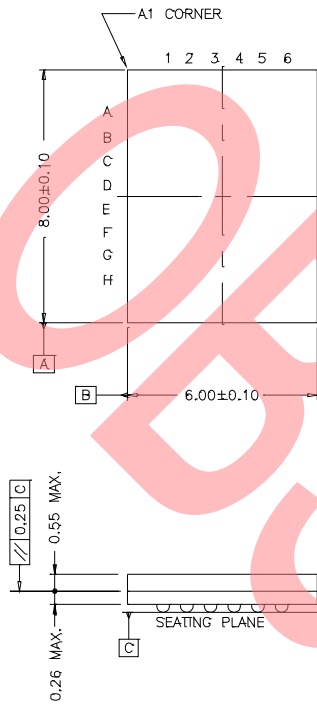


**Truth Table**

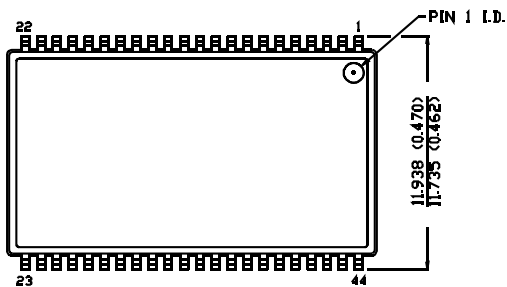
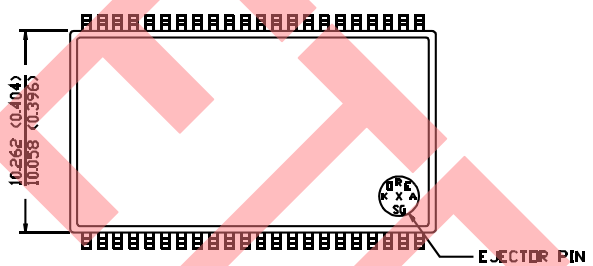
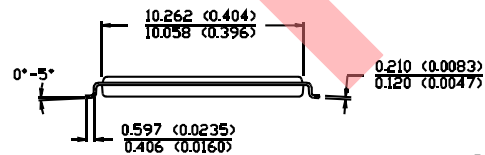
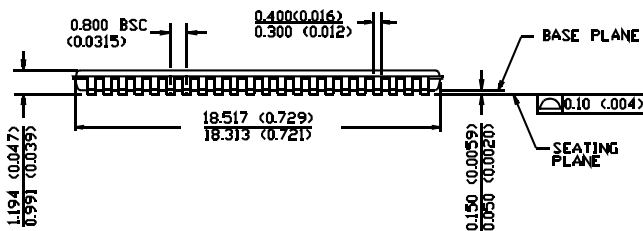
<b>CE</b>	<b>WE</b>	<b>OE</b>	<b>BHE</b>	<b>BLE</b>	<b>Inputs/Outputs</b>	<b>Mode</b>	<b>Power</b>
H	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	X	X	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High Z	Write	Active ( $I_{CC}$ )

**Ordering Information**

<b>Speed (ns)</b>	<b>Ordering Code</b>	<b>Package Name</b>	<b>Package Type</b>	<b>Operating Range</b>
45	CY62146DV30LL-45BVI	BV48A	48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62146DV30LL-45BVXI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm) (Pb-free)	
	CY62146DV30LL-45ZSXI	ZS-44	44-pin TSOP II (Pb-free)	
55	CY62146DV30L-55BVI	BV48A	48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62146DV30L-55BVXI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm) (Pb-free)	
	CY62146DV30LL-55BVI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm)	
	CY62146DV30LL-55BVXI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm) (Pb-free)	
	CY62146DV30L-55ZSXI	ZS-44	44-pin TSOP II (Pb-free)	
	CY62146DV30LL-55ZSXI			
70	CY62146DV30L-70BVI	BV48A	48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62146DV30L-70BVXI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm) (Pb-free)	
	CY62146DV30LL-70BVI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm)	
	CY62146DV30LL-70BVXI		48-ball Very Fine Pitch BGA (6 mm × 8mm × 1 mm) (Pb-free)	
	CY62146DV30L-70ZSXI	ZS-44	44-pin TSOP II (Pb-free)	Industrial
	CY62146DV30LL-70ZSXI			

**Package Diagram**
**TOP VIEW**
**48-Lead VFBGA (6 x 8 x 1 mm) BV48A**
**BOTTOM VIEW**


51-85150-\*B

**44-Pin TSOP II ZS44**
**MIN**

**TOP VIEW**

**BOTTOM VIEW**


51-85087-\*A

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**Document History Page**

Document Title: CY62146DV30 MoBL <sup>®</sup> 4-Mbit (256K x 16) Static RAM Document Number: 38-05339				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	213251	See ECN	AJU	New Data Sheet
*A	316039	See ECN	PCI	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote #10 on page #4 Added Pb-free package ordering information on page # 9 Changed 44-lead TSOP-II package name on page 10 from Z44 to ZS44 Standardized lcc values across 'L' and 'LL' bins
*B	3094410	11/24/2010	RAME	The parts specified in the ordering informaion table are being pruned. Obsolete Datasheet.