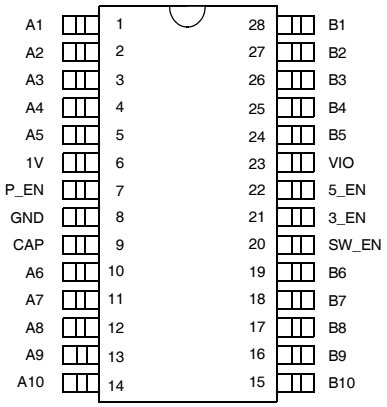
PACKAGE / PINOUT DIAGRAM

Top View



28-pin TSSOP

Note: This drawing is not to scale.

PIN DESCRIPTIONS

PIN(S)	NAME	DESCRIPTION
1-5	A1 - A5	The backplane-side input signals for channels 1 through 5, respectively.
10-14	A6 - A10	The backplane-side input signals for channels 6 through 10, respectively.
24-28	B1 - B5	The device-side connection for channels 1 through 5, respectively.
15-19	B6 - B10	The device-side connection for channels 6 through 10, respectively.
6	1V	A precharge supply voltage input for all channels. This voltage can be less than or equal to VIO.
7	P_EN	The precharge enable input which controls the precharge pull-up resistors. When this active high control signal is set to '1', the precharge of all channels is enabled.
8	GND	The ground voltage reference for the CMCPCI102BT/BR.
9	CAP	A capacitor must be placed from this pin to GND. The recommended value is 0.01µF,16V.
20	SW_EN	The series switch enable input. When this active high control signal is set to '1', the series switch between the channel's backplane-side terminal and device-side terminal is closed. When this signal is cleared to '0', the switch is open.
21	3_EN	The enable signal for the device-side channel pull-up mechanism when 3.3V is the supply voltage. When this active high control signal is set to '1', the 2.7kΩ pull-up resistor which pulls up the channel to the supply rail is engaged. Otherwise, this pin should be set to '0'.
22	5_EN	The enable signal for the device-side channel pull-up mechanism when 5V is the supply voltage. When this active high control signal is set to '1', the 1kΩ pull-up resistor which pulls up the channel to the supply rail is engaged. Otherwise, this pin should be set to '0'.
23	VIO	The positive supply voltage for the CMCPCI102BT/BR. Either 3.3V or 5V may be used.

Ordering Information

PART NUMBERING INFORMATION					
		Standard Finish		Lead-free Finish	
Pins	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
28	TSSOP	CMCPCI102BT	CPCI102B	CMCPCI102BR	CPCI102BR

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
VIO (supply voltage)	-0.5 to +6	V
Pin Voltages 1V, P_EN, 3_EN, 5_EN, SW_EN A1-A10 B1-B10	 -0.5 to (VIO+0.5) -0.5 to (VIO+0.5) -0.5 to (VIO+0.5)	 V V V
ESD Withstand Voltage Human Body Model, MIL-STD-883D, Method 3015 (Notes 1, 2)	 ±2000	 V
Storage Temperature Range	-65 to +150	°C
Operating Temperature Range (Ambient)	-40 to +85	°C
DC Power per Resistor	62	mW
Package Power Rating	1	W

Note 1: ESD is applied to input / output pins with respect to GND, one at a time; unused pins are left open.
Note 2: This parameter guaranteed by design.

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
VIO (supply voltage)	3 to 5.5	V
Pin Voltages P_EN, 3_EN, 5_EN, SW_EN, 1V A1-A10 B1-B10	 0 to VIO 0 to VIO 0 to VIO	 V V V
Ambient Operating Temperature Range	-40 to +85	°C

Specifications (Cont'd)

ELECTRICAL OPERATING CHARACTERISTICS(NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
R_{S1}	Series Resistance through R_S	A to B; switch SW_S closed; T_A=25°C	5	10	15	Ω
R_{S2}	Series Resistance through R_S	A to B; switch SW_S open; T_A=25°C	1			MΩ
R_{PU1}	Resistance of R_{PU1} pull-up	T_A=25°C	9.5		18	kΩ
TOL_{RPU2} TOL_{RPU3}	Resistance Tolerance (R_{PU2} and R_{PU3})	T_A=25°C			±5	%
TCR_{PU}	Temperature Coefficient of Resistance (R_{PU1}, R_{PU2}, R_{PU3})			-100		ppm/°C
C_1	Capacitance on backplane side (A side) of series resistor R_S	Measured @ 66MHz, 0VDC, SW_EN=0V; Note 2		1.9		pF
C_2	Capacitance on device side (B side) of series resistor R_S and series switch SW_S	Measured @ 66MHz, 0VDC, VIO=5V, 5_EN=5V SW_EN=0V; Note 2		4.2		pF
V_{IL}	Logic Low Input Voltage to P_EN, 3_EN, 5_EN, SW_EN		-0.5		[VIO] x 0.3	V
V_{IH}	Logic High Input Voltage to P_EN, 3_EN, 5_EN, SW_EN		[VIO] x 0.7		[VIO] + 0.5	V
I_{LEAK}	Leakage Current into P_EN, 3_EN, 5_EN, SW_EN	GND < V < VIO		±1	±10	µA
I_{GND}	Supply Current for internal circuits (measured at GND pin)			0.25	1	mA
t_{PLH}	Switch SW_S closure delay from the low-to-high transition of SW_EN	Note 2, 'CAP' pin capacitor=0.01µF		14		ms
t_{PHL}	Switch SW_S delay from the high-to-low transition of SW_EN	Note 2, 'CAP' pin capacitor=0.01µF		12		µs
t_{PPU}	Propagation delay for pull-up switches SW_{PU1}, SW_{PU2}, and SW_{PU3}, all transitions	Note 2			10	ns

Note 1: Operating Characteristics are over Standard Operating Conditions unless otherwise specified.
Note 2: This parameter is guaranteed by design; it is not tested 100%.

Performance Information

Resistance Variation with Input Voltage

The series resistance R_S varies with input voltage and supply voltage, as shown in Figure 1.

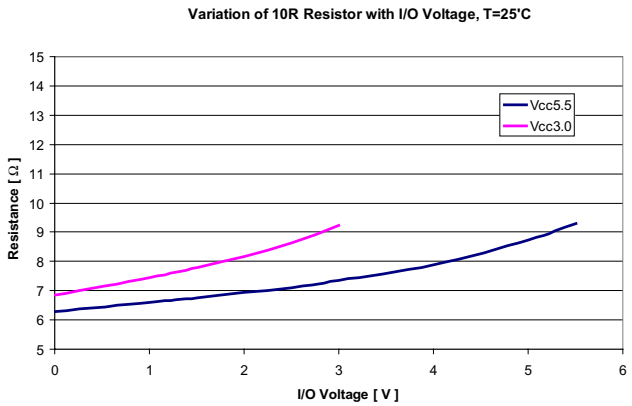
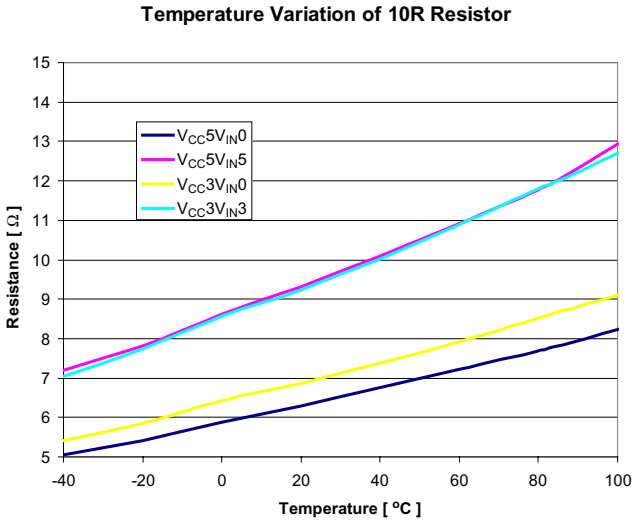


Figure 1. Resistance Variation vs. Input Voltage

Resistance Variation with Temperature

The series resistance R_S also varies with temperature, as shown in Figure 2.



CONDITIONS:		
Curve $V_{CC}3V_{IN}0$:	V_{IO} = 3.0V	channel voltage = 0.0V
Curve $V_{CC}3V_{IN}3$:	V_{IO} = 3.0V	channel voltage = 3.0V
Curve $V_{CC}5V_{IN}0$:	V_{IO} = 5.5V	channel voltage = 0.0V
Curve $V_{CC}5V_{IN}5$:	V_{IO} = 5.5V	channel voltage = 5.5V

Figure 2. Resistance Variation vs. Temperature

CAP Pin Capacitance

Some external capacitance is necessary to prevent the voltage on the CAP pin from falling during sustained data transfers through the device. This ensures that the logic 1 level does not degrade.

The time required to open and close the series switch, SWs, varies according to how much capacitance is present on the CAP pin.

The minimum usable value is 200pF, placed close to the pins. A 0.01uF, 16V capacitor is recommended. See Figure 3 and Figure 4 for variation of switch on/off times vs. capacitance.

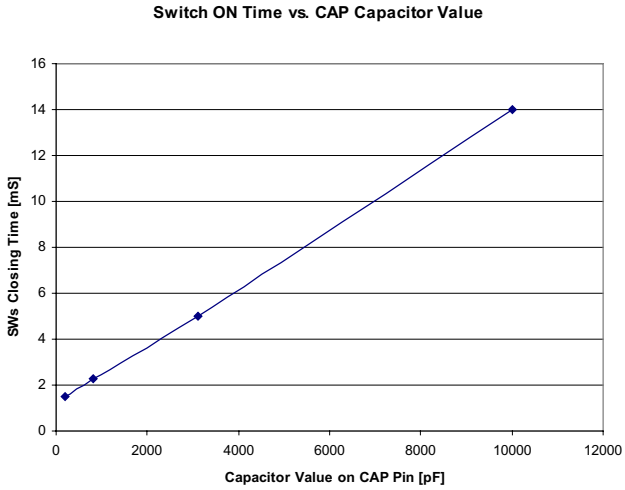


Figure 3. Switch ON Time vs. CAP Capacitor Value

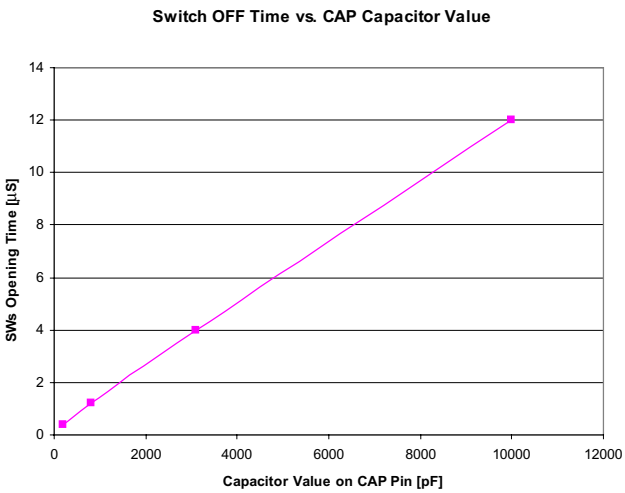


Figure 4. Switch OFF Time vs. CAP Capacitor Value

Performance Information (cont'd)

Capacitance Variation with Frequency

The A-side and B-side capacitances, C_1 and C_2, will vary with frequency. The backplane capacitance, C_1, is very linear over a wide frequency range. Figure 5 shows a plot of input line A3 (pin 3), measured with SW_EN=0V and VIO=5V.

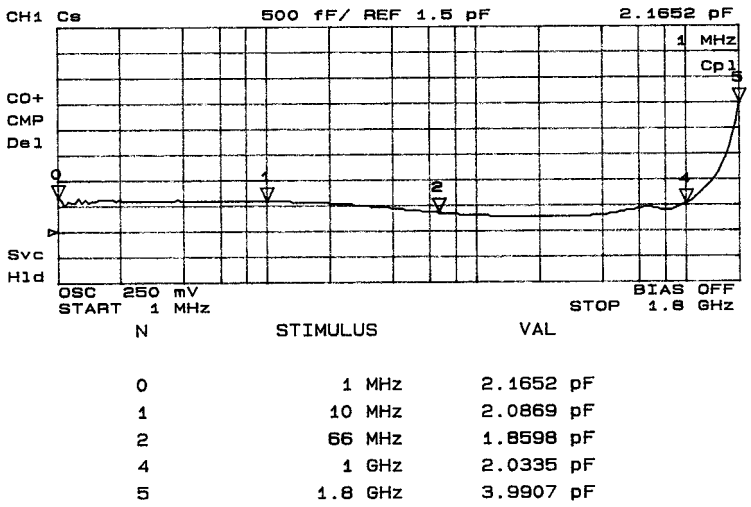


Figure 5. C_1 (Backplane-side) Capacitance Variation vs. Frequency

The CompactPCI device side of the CMCPCI102BT/BR has a fairly low capacitance (C_2) at 66MHz, but it is higher at lower frequencies.

Figure 6 shows a plot of output line B3 (pin 26), measured at the worst-case (for capacitance) conditions of SW_EN=0V, 5_EN=0V, 3_EN=0V and VIO=5V.

The increased capacitance at low frequencies is due to the parasitic capacitance of the switches connected to the pull-up resistors. At high frequencies, this parasitic capacitance is decoupled by the pull-up resistors.

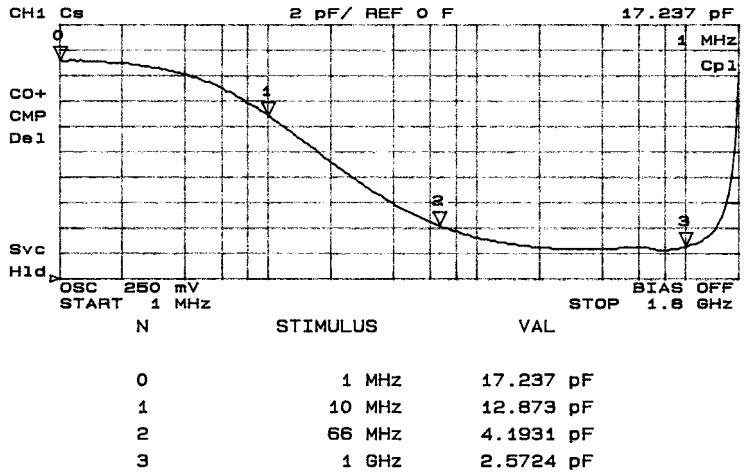


Figure 6. C_2 (Device-side) Capacitance Variation vs. Frequency

Application Information

Board Layout Recommendations

The CMCPCI102BT/BR devices should be located on the board as close as possible to the CompactPCI connector. Whether a signal is terminated or not depends upon application, as shown in the following table:

SIGNAL(S)	SYSTEM SLOT BOARDS	
	32-Bit	64-Bit
AD0-AD31	terminate	terminate
C/BE0#-C/BE3#	terminate	terminate
PAR	terminate	terminate
FRAME#	terminate	terminate
IRDY#	terminate	terminate
TRDY#	terminate	terminate
STOP#	terminate	terminate
LOCK#	terminate	terminate
DEVSEL#	terminate	terminate
PERR#	terminate	terminate
SERR#	terminate	terminate
RST#	terminate	terminate
REQ64#	terminate	terminate
ACK64#	terminate	terminate
INTA#, INTB#, INTC#, INTD# (if used)	terminate	terminate
AD32-AD63	N/A	terminate
C/BE4#-C/BE7	N/A	terminate
PAR64	N/A	terminate

Figure 7 shows a 64-bit system board connection between the CMCPCI102BT/BR termination and the CompactPCI 5-row connector (2 mm pitch) labeled A to E (row F is Ground). The System slot should have signal lengths not exceeding 63.5 mm (2.5 inches). To minimize trace length, it is recommended that the CMCPCI102BT/BRs be placed on alternate sides of the PC board. The configuration shown illustrates a fully-terminated 64-bit board utilizing 10 CMCPCI102BT/BR devices. Some applications (e.g. 32-bit boards) do not require all lines to be terminated, per the above table.

The CMCPCI102BT/BR resistors have a very low TCR (typically -100ppm/°C) so that resistance will not fluctuate over temperature. Buffers are implemented on P_EN, 5_EN and 3_EN inputs to ensure that switches turn on and off completely.

A typical system slot card may use 10 CMCPCI102BT/BR devices to replace 10 10-bit FET bus switches and 76 4-resistor packs (0805 form factor), thus providing significant reduction in both component count and assembly costs. At the same time this highly integrated solution improves reliability and manufacturing efficiency, saves board area for space-critical designs, and satisfies CompactPCI height requirements.

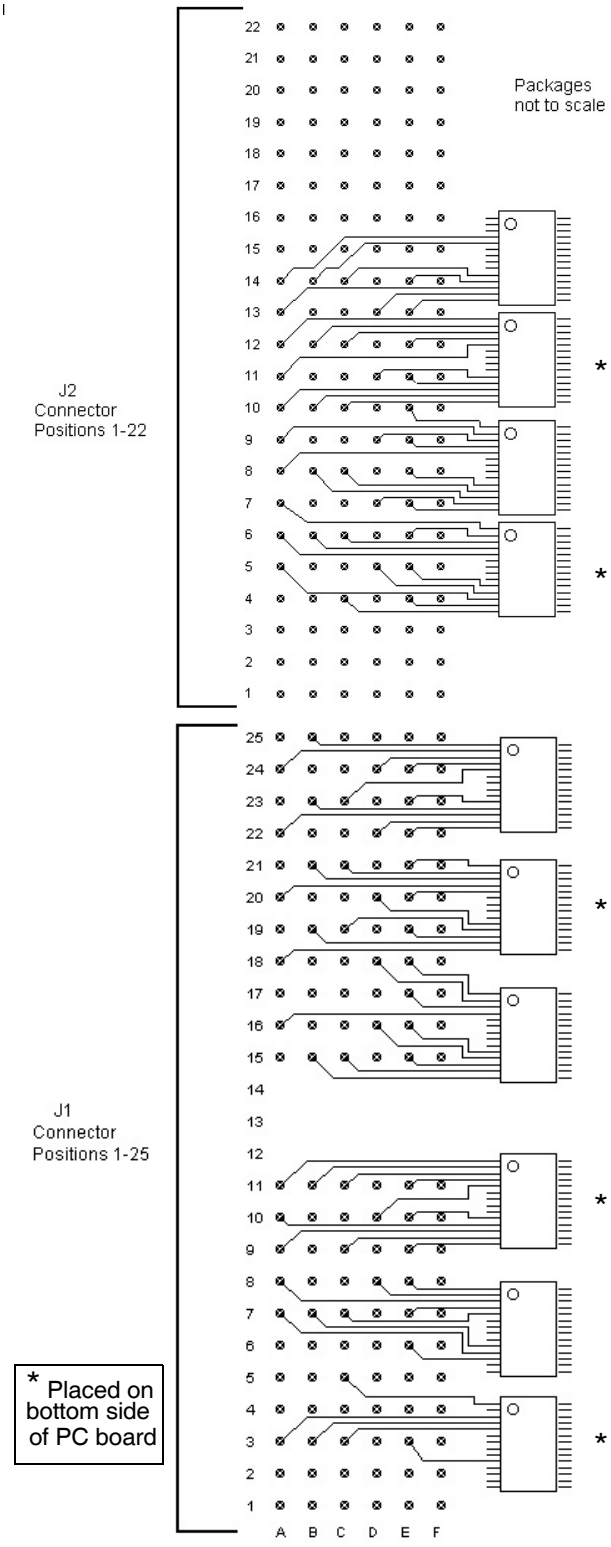


Figure 7. Schematic for 64-bit System Board

Mechanical Details

TSSOP Mechanical Specifications

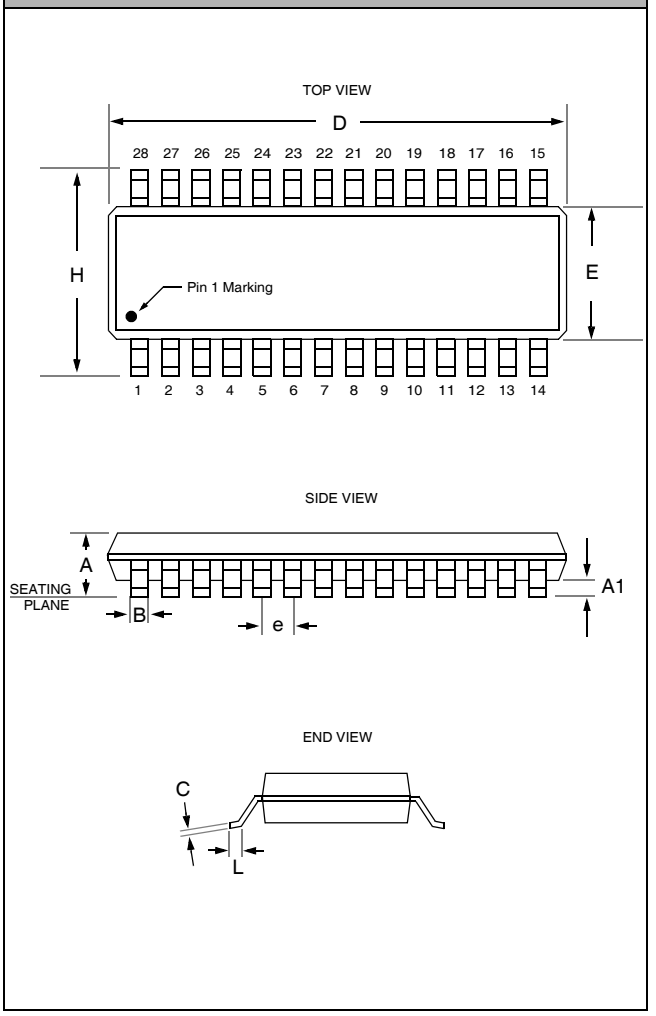
CMCPCI102BT/BR devices are supplied in 28-pin TSSOP packages. Dimensions are shown below.

For complete information on the TSSOP-28 package, see the California Micro Devices TSSOP Package Information document.

PACKAGE DIMENSIONS				
Package	TSSOP			
Pins	28			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	—	1.10	—	0.0433
A1	0.05	0.15	0.002	0.006
B	0.19	0.30	0.0075	0.0118
C	0.09	0.20	0.0035	0.0079
D	9.60	9.80	0.378	0.386
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.0256 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
# per tube	50 pieces*			
# per tape and reel	1000 pieces			
Controlling dimension: millimeters				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for TSSOP-28