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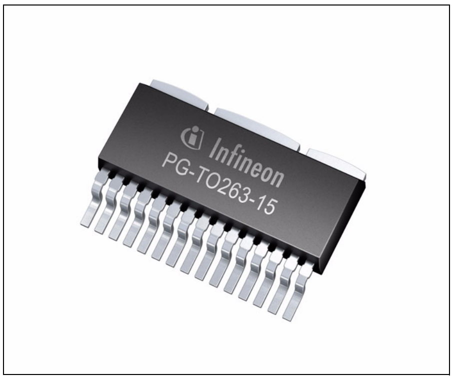
1 Overview



P-TO263-15-1

Features

- Quad D-MOS switch driver
- Free configurable as bridge or quad-switch
- Optimized for DC motor management applications
- Low $R_{\text{DS ON}}$
  High side: 70 mΩ typ. @ 25°C,165 mΩ max. @ 110°C
  Low side: 45 mΩ typ. @ 25°C, 100 mΩ max. @ 110°C
- Maximum peak current: typ. 12 A @ 25 °C
- Very low quiescent current: typ. 5 µA @ 25 °C
- Small outline, enhanced power PG-DSO-package
- Operates up to 40 V
- Status flag diagnosis
- Short-circuit-protection
- Overtemperature shut down with hysteresis
- Internal clamp diodes
- Under-voltage detection with hysteresis
- Green Product (RoHS compliant)
- AEC Qualified

Description

The **BTM7750GP** is part of the **TrilithIC** family containing three dies in one package: One double high-side switch and two low-side switches. The drains of these three vertical DMOS chips are mounted on separated lead frames. The sources are connected to individual pins, so the **BTM7750GP** can be used in H-bridge- as well as in any other configuration. The double high-side switch is manufactured in SMART SIPMOS® technology which combines low $R_{\text{DS ON}}$ vertical DMOS power stages with CMOS circuitry for control, protection and diagnosis. To achieve low $R_{\text{DS ON}}$ and fast switching performance, the low-side switches are manufactured in S-FET logic level technology.

Type	Package	Marking
BTM7750GP	P-TO263-15-1	BTM7750GP

2 Pin Configuration

2.1 Pin Assignment

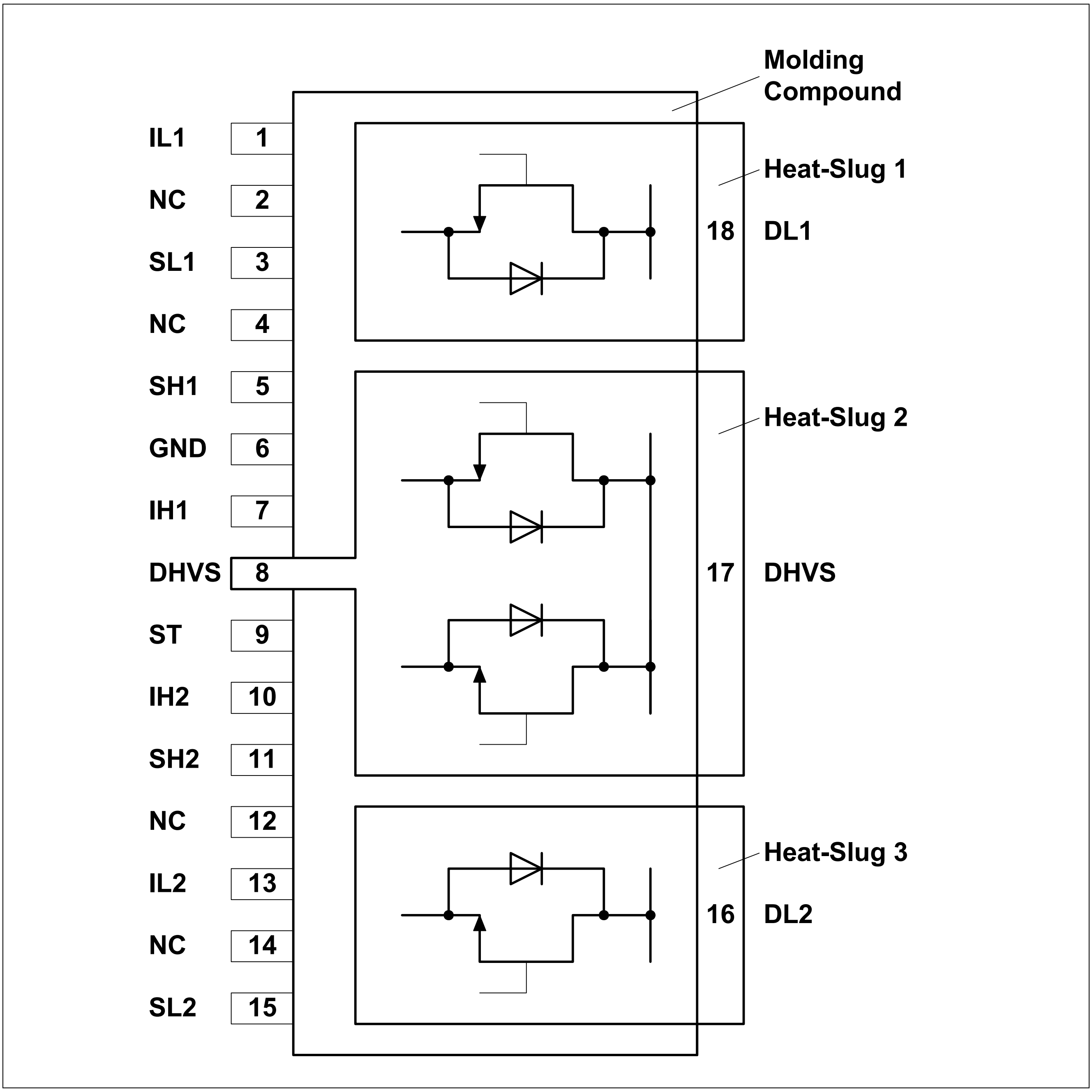


Figure 1 Pin Assignment BTM7750GP (Top View)

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	IL1	Analog input of low-side switch 1
2	NC	Not connected
3	**SL1**	**Source of low-side switch 1**
4	NC	Not connected
5	**SH1**	**Source of high-side switch 1**
6	GND	Ground of high-side switches
7	IH1	Digital input of high-side switch 1
8	**DHVS**	**Drain of high-side switches and power supply voltage**
9	ST	Status; open Drain output
10	IH2	Digital input of high-side switch 2
11	**SH2**	**Source of high-side switch 2**
12	NC	Not connected
13	IL2	Analog input of low-side switch 2
14	NC	Not connected
15	**SL2**	**Source of low-side switch 2**
16	**DL2**	**Drain of low-side switch 2** **Heat-Slug 3 or Heat-Dissipator**
17	**DHVS**	**Drain of high-side switches and power supply voltage** **Heat-Slug 2 or Heat-Dissipator**
18	**DL1**	**Drain of low-side switch 1** **Heat-Slug 1 or Heat-Dissipator**

Pins written in **bold type** need power wiring.

2.2 Terms

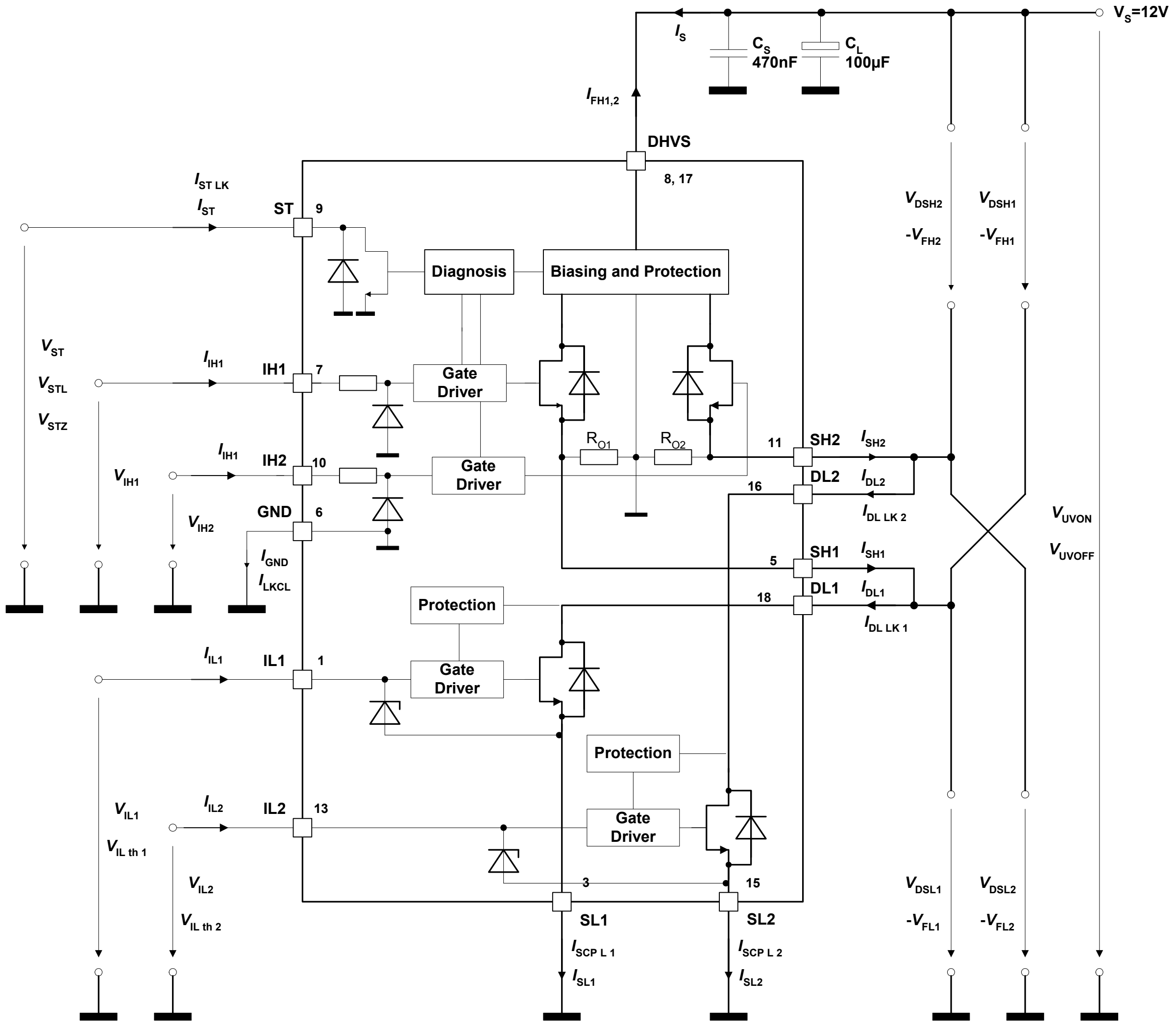
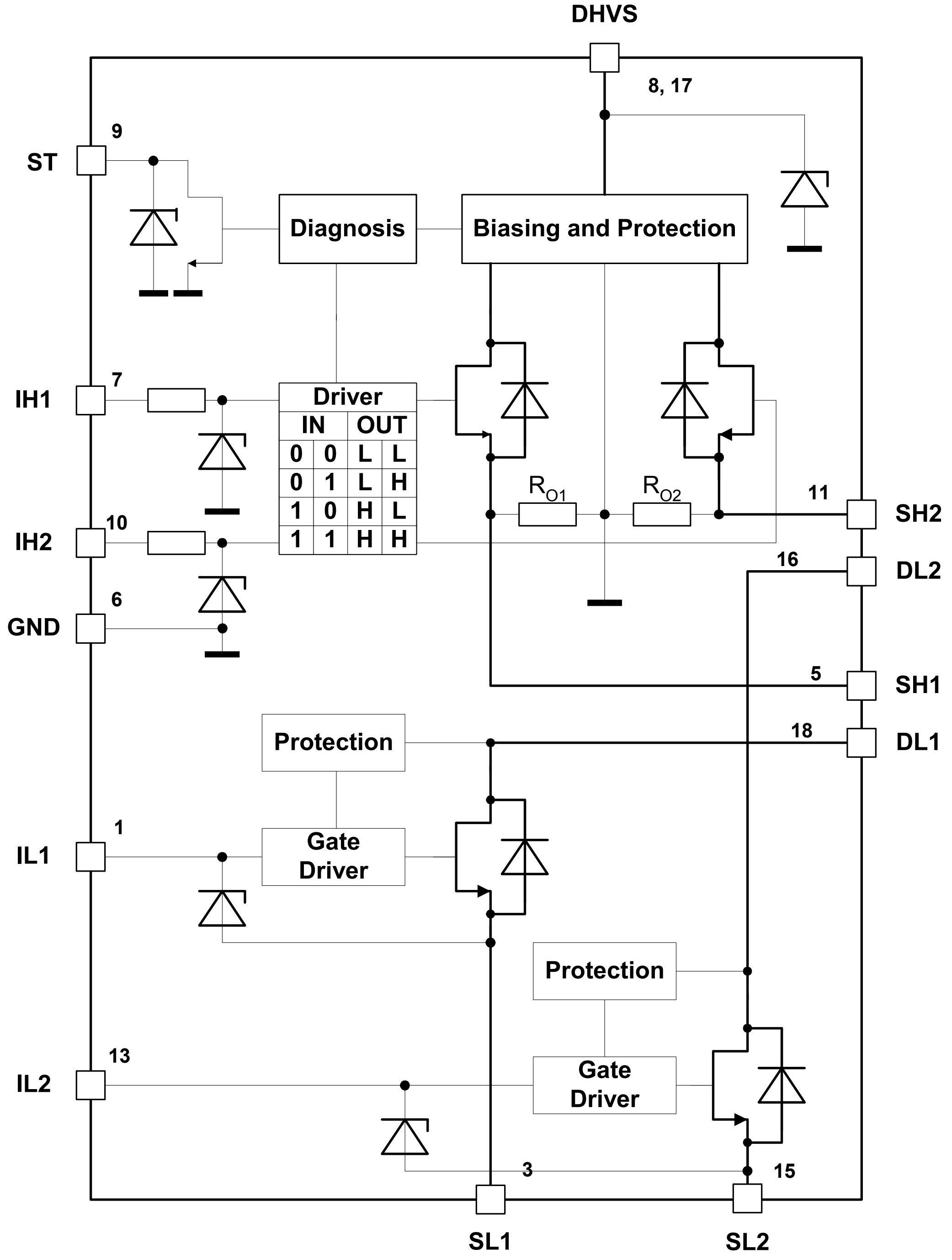


Figure 2 Terms BTM7750GP

Table 2

HS-Source-Current	Named during Short Circuit	Named during Leakage-Cond.
$I_{SH1,2}$	$I_{SCP\ H}$	$I_{DL\ LK}$

3 Block Diagram



IN		OUT	
0	0	L	L
0	1	L	H
1	0	H	L
1	1	H	H

Figure 3 Block Diagram BTM7750GP

4 Circuit Description

4.1 Input Circuit

The control inputs IH1,2 consist of TTL/CMOS compatible Schmitt-Triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages. The inputs are protected by ESD clamp-diodes. The inputs IL1 and IL2 are connected to the internal gate-driving units of the N-channel vertical power-MOS-FETs.

4.2 Output Stages

The output stages consist of an low R_{DSON} Power-MOS H-bridge. In H-bridge configuration, the D-MOS body diodes can be used for freewheeling when communicating inductive loads. If the high-side switches are used as single switches, positive and negative voltage spikes which occur when driving inductive loads are limited by integrated power clamp diodes.

4.3 Short Circuit Protection

The outputs are protected against

- output short circuit to ground
- output short circuit to the supply voltage, and
- overload (load short circuit).

An internal OP-Amp controls the Drain-Source-Voltage by comparing the DS-Voltage-Drop with an internal reference voltage. Above this trip point the OP-Amp reduces the output current depending on the junction temperature and the drop voltage.

4.4 Overtemperature Protection

The high-side and the low-side switches also incorporate an over temperature protection circuit with hysteresis which switches off the output transistors. In the case of the high-side switches, the status output is set to low.

4.5 Undervoltage Lockout

When V_{S} reaches the switch-on voltage V_{UVON} the IC becomes active with a hysteresis. The High-Side output transistors are switched off if the supply voltage V_{S} drops below the switch off value V_{UVOFF}.

4.6 Status Flag

The status flag output is an open drain output with zener-diode which requires a pull-up resistor, as shown in the application circuit in **Figure 4 “Application Example BTM7750GP” on Page 15**. Various errors as listed in the table “Diagnosis” are reported by switching the open drain output ST to low.

Table 3 Truth table and Diagnosis (valid only for the High-Side-Switches)

Flag	IH1	IH2	SH1	SH2	ST	Remarks
	Inputs		Outputs			
Normal operation; identical with functional truth table	0	0	L	L	1	stand-by mode
	0	1	L	H	1	switch2 active
	1	0	H	L	1	switch1 active
	1	1	H	H	1	both switches active
Overtemperature high-side switch1	0	X	L	X	1	
	1	X	L	X	0	detected
Overtemperature high-side switch2	X	0	X	L	1	
	X	1	X	L	0	detected
Overtemperature both high-side switches	0	0	L	L	1	
	X	1	L	L	0	detected
	1	X	L	L	0	detected
Under voltage	X	X	L	L	1	not detected

Inputs:
0 = Logic LOW
1 = Logic HIGH
X = don’t care

Outputs:
Z = Output in tristate condition
L = Output in sink condition
H = Output in source condition
X = Voltage level undefined

Status:
1 = No error
0 = Error

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1]

$-40\ °C < T_j < 110\ °C$

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
High-Side-Switches (Pins DHVS, IH1,2 and SH1,2)						
5.1.1	Supply voltage	V_S	– 0.3	42	V	–
5.1.2	Supply voltage for full short circuit protection	$V_{S(SCP)}$	–	28	V	
5.1.3	HS-drain current[2]	I_S	– 10	[3]	A	T_A = 25°C; t_P < 100 ms$_j$
5.1.4	HS-input current	I_{IH}	– 5	5	mA	Pin IH1 and IH2
5.1.5	HS-input voltage	V_{IH}	– 10	16	V	Pin IH1 and IH2
Status Output ST						
5.1.6	Status pull up voltage	V_{ST}	– 0.3	5.4	V	
5.1.7	Status Output current	I_{ST}	– 5	5	mA	Pin ST
Low-Side-Switches (Pins DL1,2, IL1,2 and SL1,2)						
5.1.8	Drain-Source-Clamp voltage	V_{DSL}	42	–	V	V_{IL} = 0 V; $I_D \leq$ 1 mA; T_j = 25°C
5.1.9	Supply voltage for short circuit protection	$V_{DSL(SCP)}$	–	36	V	V_{IL} = 5 V
5.1.10			–	20	V	V_{IL} = 10 V
5.1.11	LS-drain current[2]	I_{DL}	– 12	[3]	A	T_A = 25°C; t_P < 100 ms
5.1.12	LS-input voltage	V_{IL}	– 0.3	10	V	–
Temperatures						
5.1.13	Junction temperature	T_j	– 40	110	°C	–
5.1.14	Storage temperature	T_{stg}	– 55	150	°C	–
ESD Protection[4]						
5.1.15	Input LS-Switch	V_{ESD}	–	2	kV	
5.1.16	Input HS-Switch	V_{ESD}	–	1	kV	
5.1.17	Status HS-Switch	V_{ESD}	–	2	kV	
5.1.18	Output LS and HS-Switch	V_{ESD}	–	8	kV	all other pins connected to Ground

1) Not subject to production test; specified by design

2) Single pulse

3) Internally limited

4) ESD susceptibility HBM according to EIA/JESD22-A114-B (1.5kΩ, 100pF)

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

5.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
5.2.19	Supply voltage	V_S	V_{UVOFF}	42	V	After V_S rising above V_{UVON}
5.2.20	Input voltage HS	V_{IH}	– 0.3	15	V	–
5.2.21	Input voltage LS	V_{IL}	– 0.3	10	V	–
5.2.22	Status output current	I_{ST}	0	2	mA	–
5.2.23	Junction temperature	T_j	– 40	110	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table

5.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.24	LS-junction to soldering point1)	R_{thJSP}	–	–	1.7	K/W	
5.3.25	HS-junction to soldering point1)	R_{thJSP}	–	–	1.7	K/W	
5.3.26	Junction to Ambient1) $R_{thJA} = T_{j(HS)} / (P_{(HS)} + P_{(LS)})$	R_{thJA}	–	16	–	K/W	2)

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (chip+package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

5.4 Electrical Characteristics

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 110 °C; 8 V < V_S < 18 V
unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Current Consumption HS-switch							
5.4.27	Quiescent current	I_S	–	5	9	µA	IH1 = IH2 = 0 V T_j = 25 °C
			–	–	12	µA	IH1 = IH2 = 0 V1)
5.4.28	Supply current; one HS-switch active	I_S	–	1.65	3.3	mA	IH1 or IH2 = 5 V V_S = 12 V
5.4.29	Supply current; both HS-switches active	I_S	–	3.3	6.6	mA	IH1 and IH2 = 5 V V_S = 12 V
5.4.30	Leakage current of high-side switch	$I_{SH\ LK}$	–	–	6	µA	$V_{IH} = V_{SH}$ = 0 V V_S = 12 V
5.4.31	Leakage current through logic GND in free wheeling condition	$I_{LKCL} = I_{FH} + I_{SH}$	–	–	10	mA	I_{FH} = 3 A V_S = 12 V
Current Consumption LS-switch							
5.4.32	Input current	I_{IL}	–	8	30	µA	V_{IL} = 5 V; normal operation
			–	160	300	µA	V_{IL} = 5 V; failure mode
5.4.33	Leakage current of low-side switch	$I_{DL\ LK}$	–	2	10	µA	V_{IL} = 0 V V_{DSL} = 18 V
Under Voltage Lockout HS-switch							
5.4.34	Switch-ON voltage	V_{UVON}	–	–	4.8	V	V_S increasing
5.4.35	Switch-OFF voltage	V_{UVOFF}	1.8	–	3.5	V	V_S decreasing
5.4.36	Switch ON/OFF hysteresis	V_{UVHY}	–	1	–	V	$V_{UVON} - V_{UVOFF}$
Output stages							
5.4.37	Inverse diode of high-side switch; Forward-voltage	V_{FH}	–	0.8	1.2	V	I_{FH} = 3 A
5.4.38	Inverse diode of low-side switch; Forward-voltage	V_{FL}	–	0.8	1.2	V	I_{FL} = 3 A
5.4.39	Static drain-source on-resistance of high-side switch	$R_{DS\ ON\ H}$	–	70	–	mΩ	I_{SH} = 1 A; V_S = 12 V T_j = 25 °C
			–	110	165	mΩ	I_{SH} = 1 A; V_S = 12 V T_j = 110 °C1)
5.4.40	Static drain-source on-resistance of low-side switch	$R_{DS\ ON\ L}$	–	45	–	mΩ	I_{SL} = 1 A; V_{IL} = 5 V T_j = 25 °C
			–	65	100	mΩ	I_{SL} = 1 A; V_{IL} = 5 V T_j = 110 °C1)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 110 °C; 8 V < V_S < 18 V
unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Short Circuit of high-side switch to GND							
5.4.41	Initial peak SC current t_{del} = 100 µs; V_S = 12 V; V_{DSH} = 12V	$I_{SCP\ H}$	13	15	18	A	T_j = – 40 °C
			–	12	–	A	T_j = + 25 °C
			8	10	12	A	T_j = + 110 °C1)
Short Circuit of high-side switch to V_S							
5.4.42	Output pull-down-resistor	R_O	8	15	35	kΩ	V_{DSL} = 3 V
Short Circuit of low-side switch to V_s							
5.4.43	Initial peak SC current V_{DSL} = 12V; V_{IL} = 5V; t_{del} = 250 µs	$I_{SCP\ L}$	21	28	34	A	T_j = – 40 °C
			–	22	–	A	T_j = 25 °C
			13	17	21	A	T_j = 110 °C1)
Thermal Shutdown1)							
5.4.44	Thermal shutdown junction temperature	$T_{j\ SD}$	155	180	190	°C	–
5.4.45	Thermal switch-on junction temperature	$T_{j\ SO}$	150	170	180	°C	–
5.4.46	Temperature hysteresis	ΔT	–	10	–	°C	$\Delta T = T_{jSD} - T_{jSO}$
Status Flag Output ST of high-side switch							
5.4.47	Low output voltage	$V_{ST\ L}$	–	0.2	0.6	V	I_{ST} = 1.6 mA
5.4.48	Leakage current	$I_{ST\ LK}$	–	–	10	µA	V_{ST} = 5 V
5.4.49	Zener-limit-voltage	$V_{ST\ Z}$	5.4	–	–	V	I_{ST} = 1.6 mA

**$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 110 °C; 8 V < V_S < 18 V
unless otherwise specified**

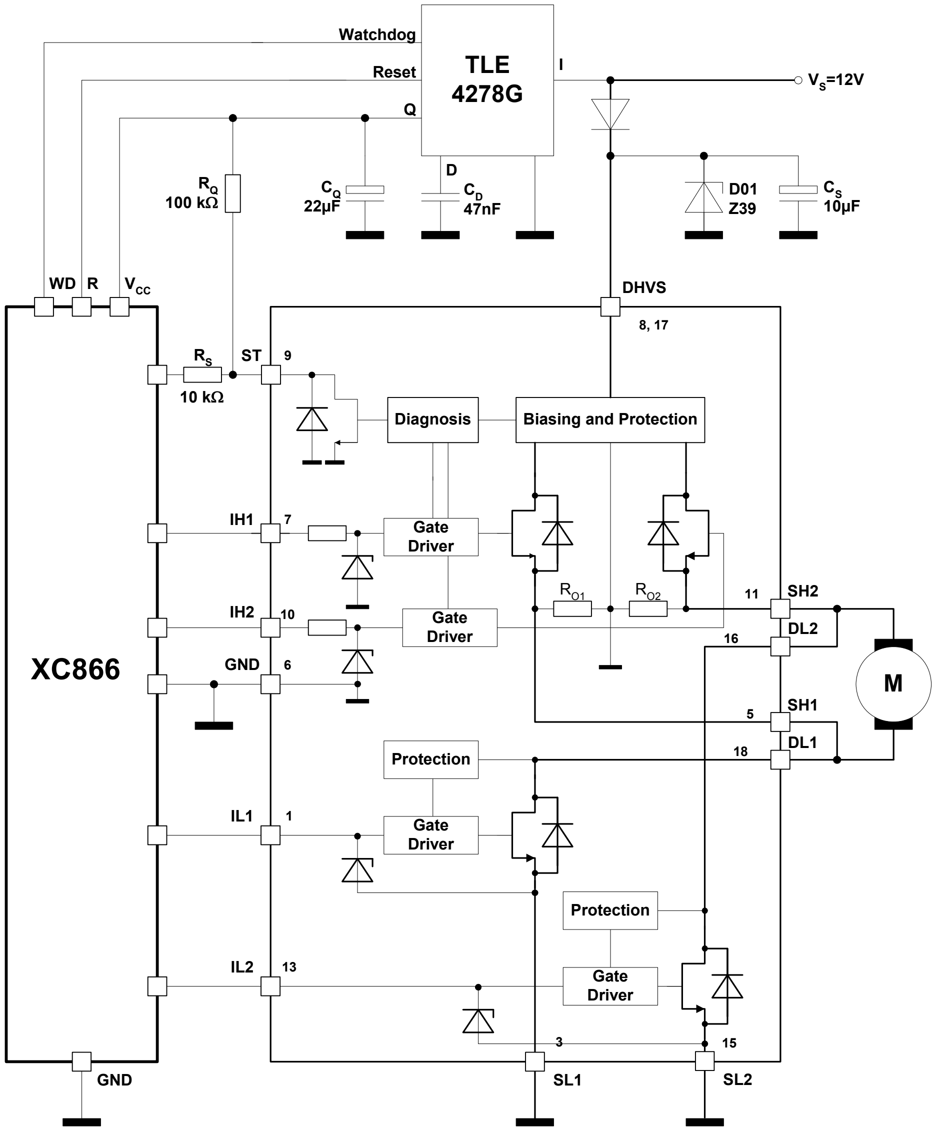
Pos.	**Parameter**	**Symbol**	**Limit Values**			**Unit**	**Test Condition**
			min.	**typ.**	**max.**		
Switching times of high-side switch[1]							
5.4.50	Turn-ON-time to 90% V_{SH}	t_{ON}	–	85	180	µs	R_{Load} = 12 Ω V_S = 12 V
5.4.51	Turn-OFF-time to 10% V_{SH}	t_{OFF}	–	80	180	µs	
5.4.52	Slew rate on 10 to 30% V_{SH}	dV/d_{tON}	–	–	1.2	V/µs	
5.4.53	Slew rate off 70 to 40% V_{SH}	$-dV/d_{tOFF}$	–	–	1.6	V/µs	
Switching times of low-side switch[1]							
5.4.54	Turn-ON-time to 10% V_{DL}	t_{ON}	–	60	150	µs	R_{Load} = 10 Ω V_S = 12 V V_{IL} = 0 to 5 V
5.4.55	Turn-OFF-time to 90% V_{DL}	t_{OFF}	–	60	150	µs	
5.4.56	Slew rate on 70 to 50% V_{DL}	$-dV/d_{tON}$	–	1	1.5	V/µs	R_{Load} = 4.7 Ω V_S = 12 V V_{IL} = 0 to 5 V
5.4.57	Slew rate off 50 to 70% V_{DL}	dV/d_{tOFF}	–	1	1.5	V/µs	
Control Inputs of high-side switches IH 1, 2							
5.4.58	H-input voltage	$V_{IH\ High}$	–	–	2.5	V	–
5.4.59	L-input voltage	$V_{IH\ Low}$	1	–	–	V	–
5.4.60	Input voltage hysteresis	$V_{IH\ HY}$	–	0.3	–	V	–
5.4.61	H-input current	$I_{IH\ High}$	15	30	60	µA	V_{IH} = 5 V
5.4.62	L-input current	$I_{IH\ Low}$	5	–	20	µA	V_{IH} = 0.4 V
5.4.63	Input series resistance	R_I	2.7	4	5.5	kΩ	–
5.4.64	Zener limit voltage	$V_{IH\ Z}$	5.4	–	–	V	I_{IH} = 1.6 mA
Control Inputs IL1, 2							
5.4.65	Gate-threshold-voltage	$V_{IL\ th}$	0.9	1.7	2.2	V	I_{DL} = 2 mA

1) Not subject to production test; specified by design

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specified mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

6 Application Information

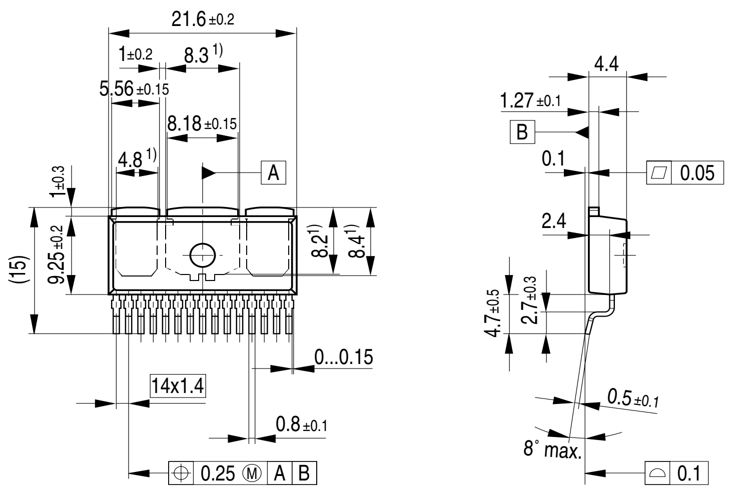
Note: The following simplified application examples are given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the described circuits must be verified in the real application



In case of V_{DSL}<-0.6V or reverse battery the current into the µC might be limited by external resitors to protect the µC

Figure 4 Application Example BTM7750GP

7 Package Outlines



1) Typical
All metal surfaces tin plated, except area of cut.

GPT09151

Footprint

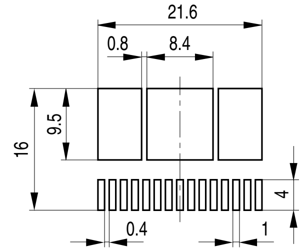


Figure 5 P-TO263-15-1 (Plastic Transistor Single Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

8 Revision History

Rev.	Date	Changes
1.0	2008-07-07	Initial Version

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