

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨ ⑩	—	0.65	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑨	—	40	

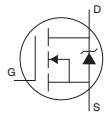
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.035	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1.0mA$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.0	1.3	mΩ	$V_{GS} = 10V, I_D = 100A$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.2	—	3.9	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	—	2.2	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

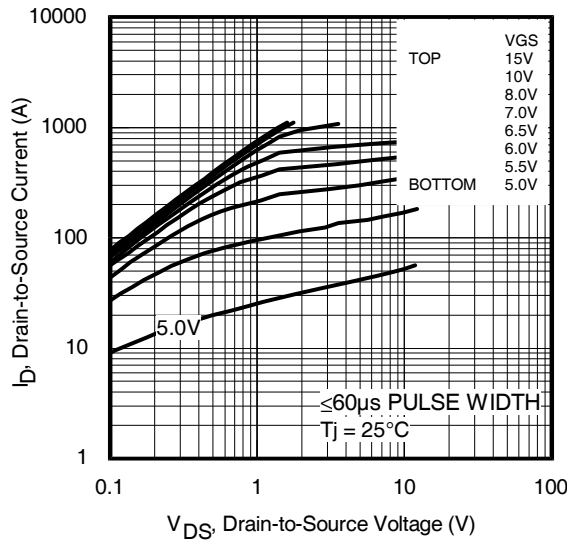
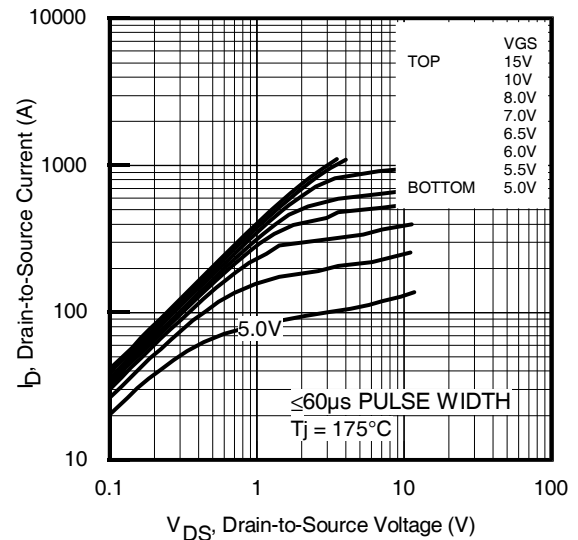
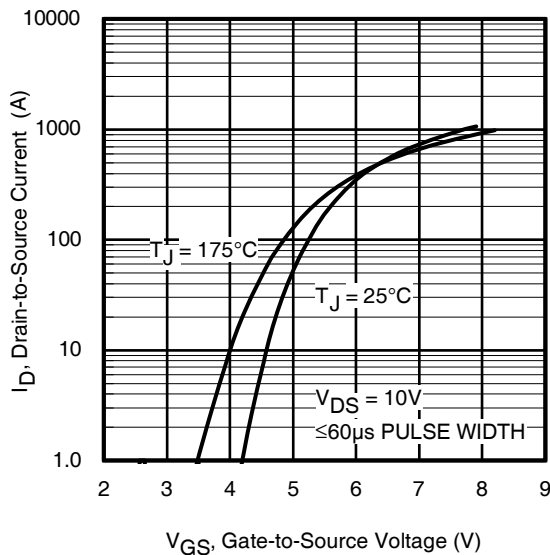
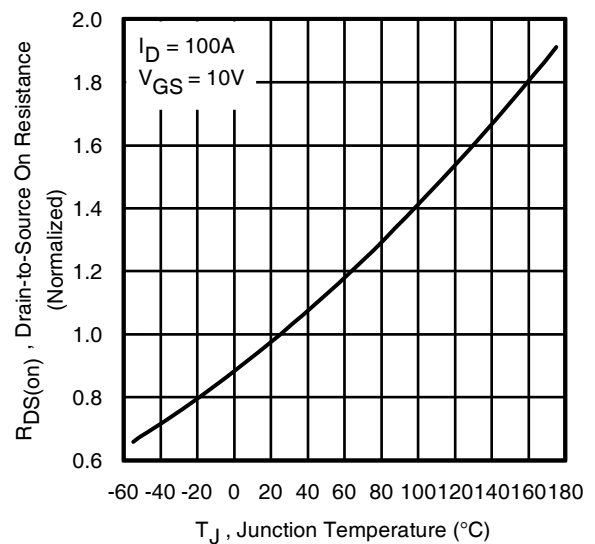
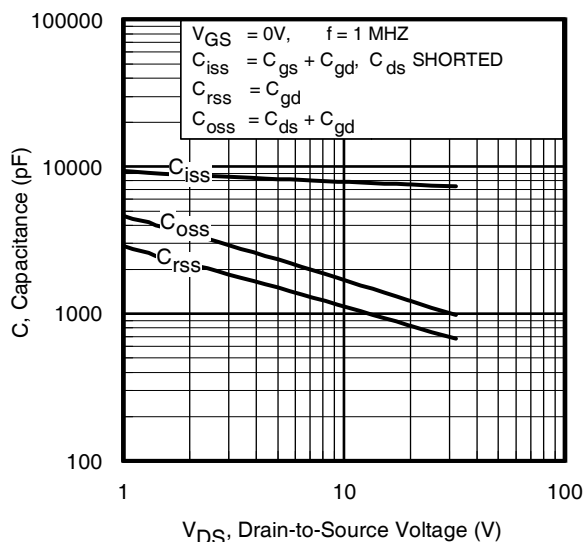
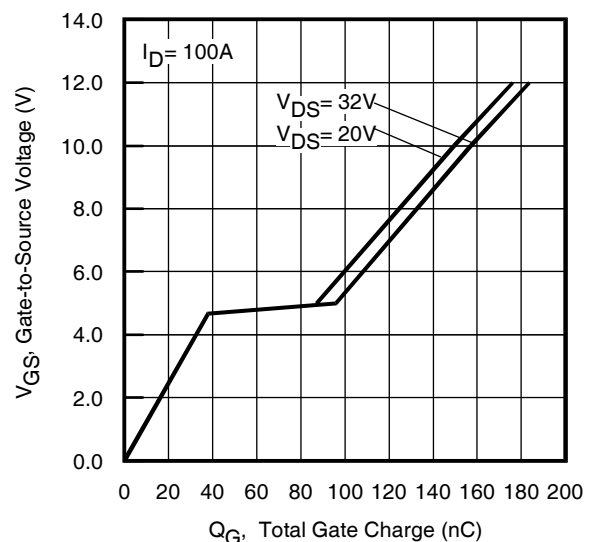
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	122	—	—	S	$V_{DS} = 10V, I_D = 100A$
Q_g	Total Gate Charge	—	150	225	nC	$I_D = 100A$
Q_{gs}	Gate-to-Source Charge	—	41	—		$V_{DS} = 20V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	51	—		$V_{GS} = 10V$ ⑤
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	99	—		$I_D = 100A, V_{DS} = 0V, V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 20V$
t_r	Rise Time	—	62	—		$I_D = 30A$
$t_{d(off)}$	Turn-Off Delay Time	—	78	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	51	—		$V_{GS} = 10V$ ⑤
C_{iss}	Input Capacitance	—	7437	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1097	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	748	—		$f = 1.0\text{ MHz}$
$C_{oss\text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	1314	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 32V$ ⑦
$C_{oss\text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	1735	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 32V$ ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	306 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	1040		
V_{SD}	Diode Forward Voltage	—	1.0	1.3	V	$T_J = 25^\circ\text{C}, I_S = 100A, V_{GS} = 0V$ ⑤
dv/dt	Peak Diode Recovery ④	—	3.5	—	V/ns	$T_J = 175^\circ\text{C}, I_S = 100A, V_{DS} = 40V$
t_{rr}	Reverse Recovery Time	—	37	—	ns	$T_J = 25^\circ\text{C}$
		—	38	—		$T_J = 125^\circ\text{C}$
Q_{rr}	Reverse Recovery Charge	—	34	—	nC	$T_J = 25^\circ\text{C}$
		—	36	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	1.8	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.069mH$, $R_G = 50\Omega$, $I_{AS} = 100A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 100A$, $di/dt \leq 1288A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss\text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C .
- ⑩ $R_{\theta JC}$ value shown is at time zero.


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

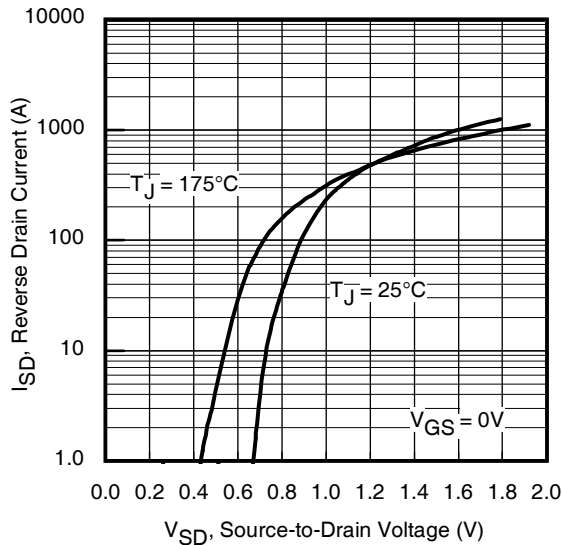


Fig 7. Typical Source-Drain Diode Forward Voltage

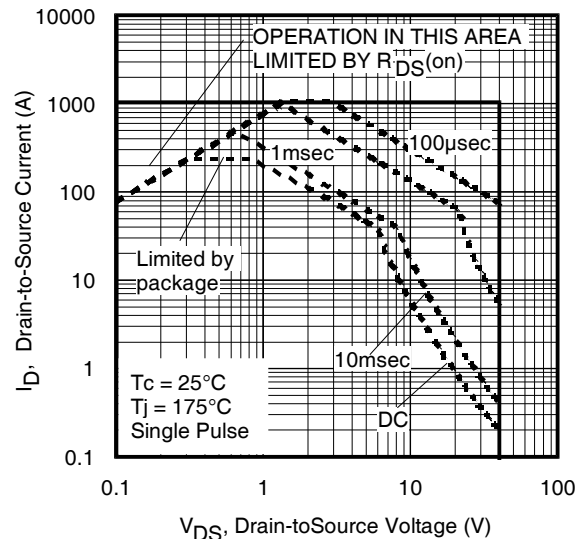


Fig 8. Maximum Safe Operating Area

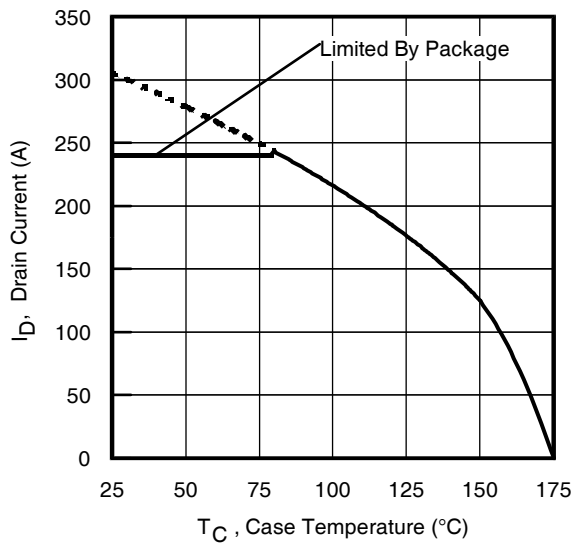


Fig 9. Maximum Drain Current vs. Case Temperature

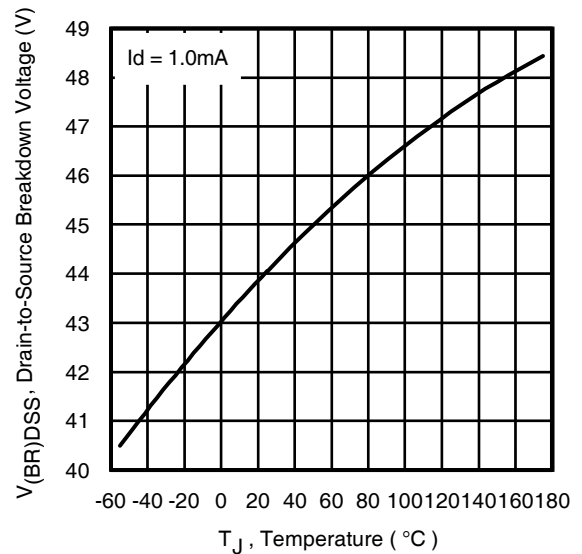


Fig 10. Drain-to-Source Breakdown Voltage

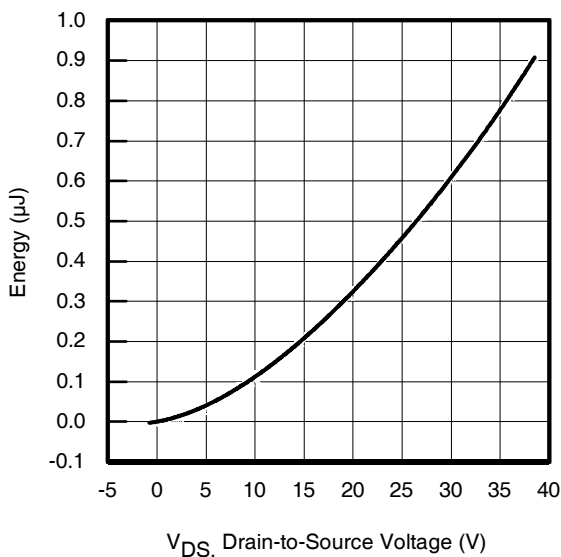


Fig 11. Typical C_{OSS} Stored Energy

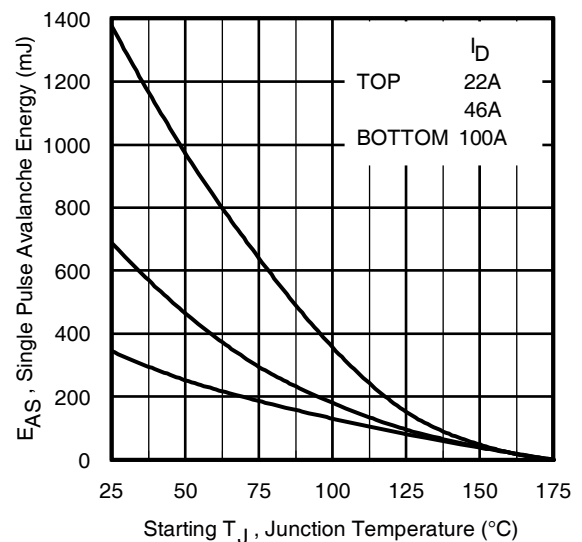
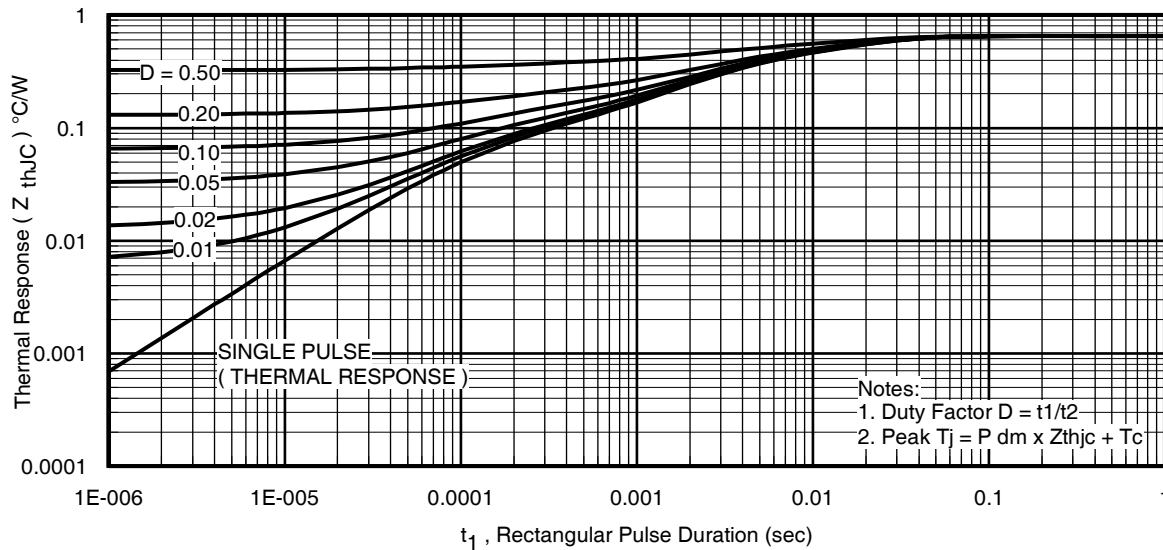
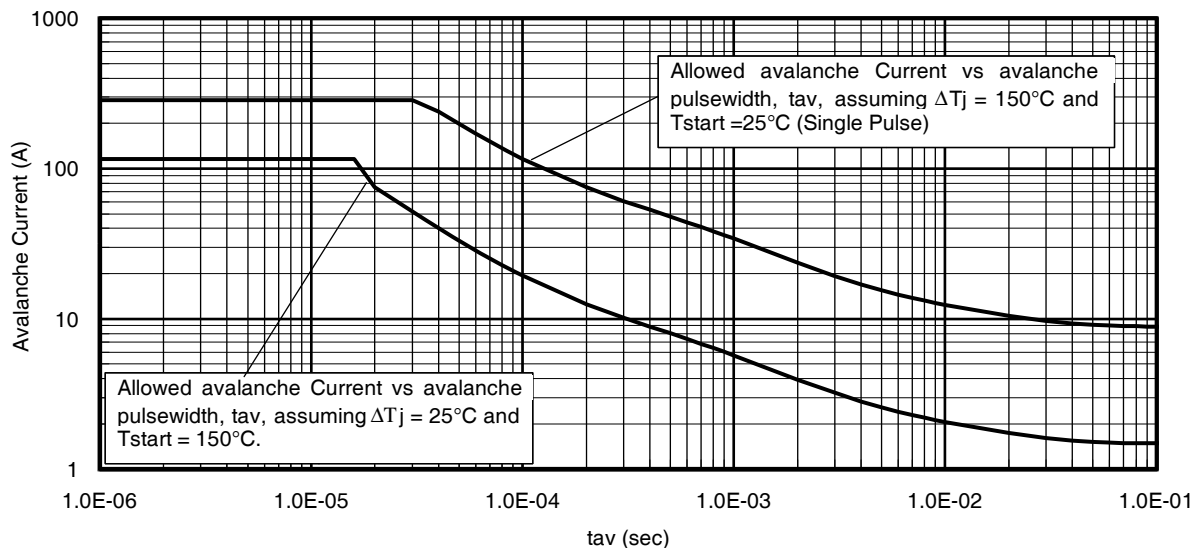
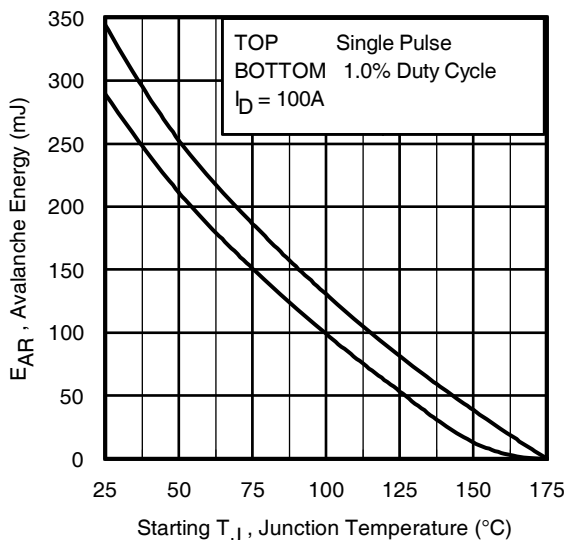


Fig 12. Maximum Avalanche Energy vs. Drain Current


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Avalanche Current vs. Pulsewidth

Fig 15. Maximum Avalanche Energy vs. Temperature

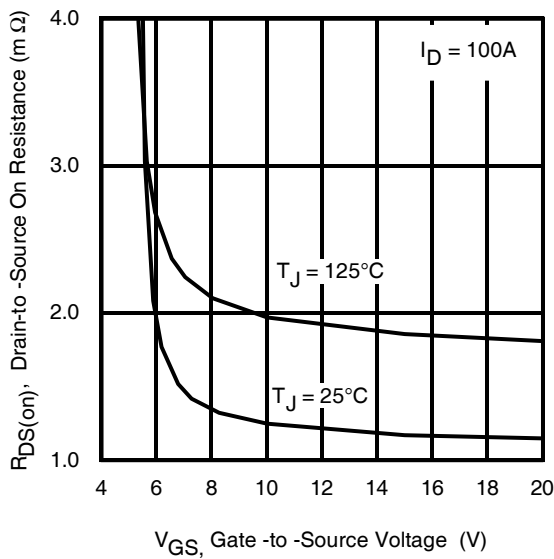
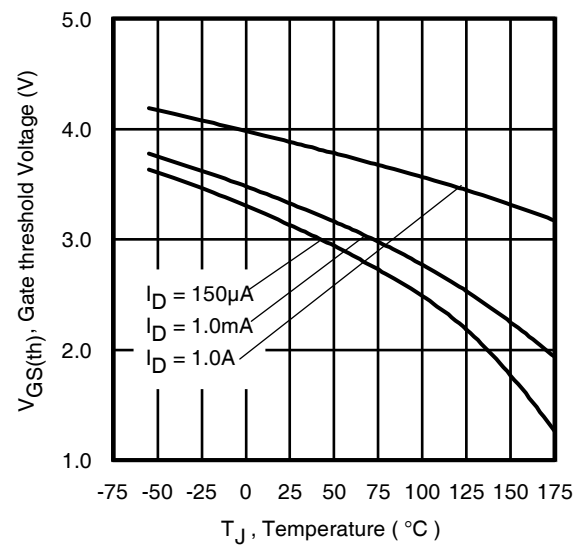
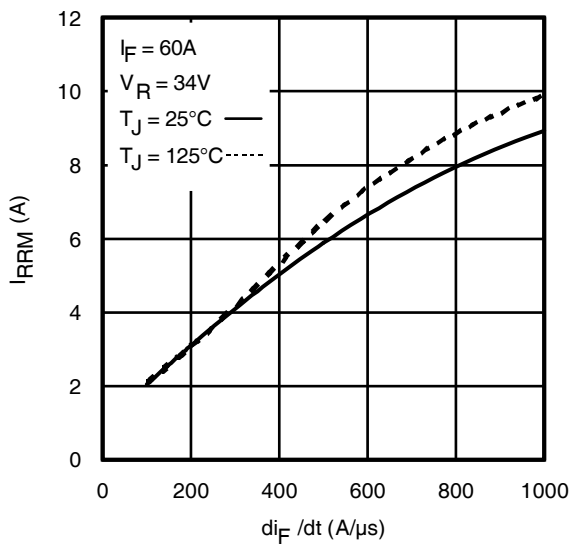
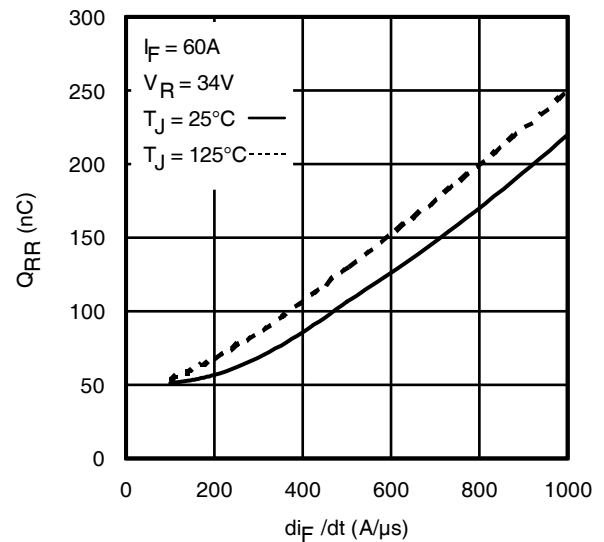
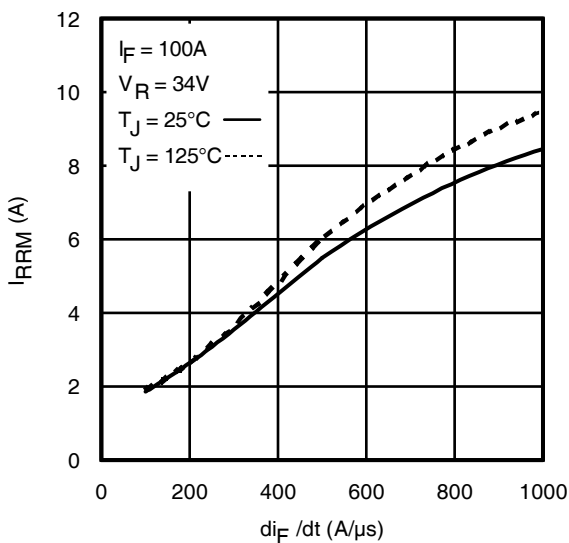
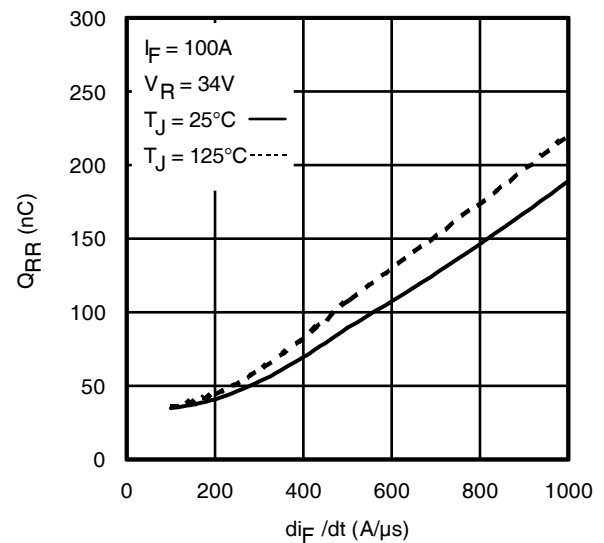
**Notes on Repetitive Avalanche Curves , Figures 14, 15
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 24a, 24b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


Fig 16. On-Resistance vs. Gate Voltage

Fig 17. Threshold Voltage vs. Temperature

Fig. 18 - Typical Recovery Current vs. di_T/dt

Fig. 19 - Typical Stored Charge vs. di_T/dt

Fig. 20 - Typical Recovery Current vs. di_T/dt

Fig. 21 - Typical Stored Charge vs. di_T/dt

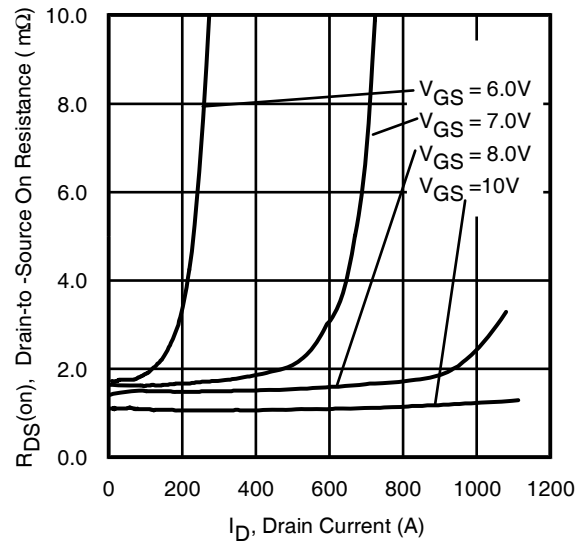


Fig 22. Typical On-Resistance vs. Drain Current

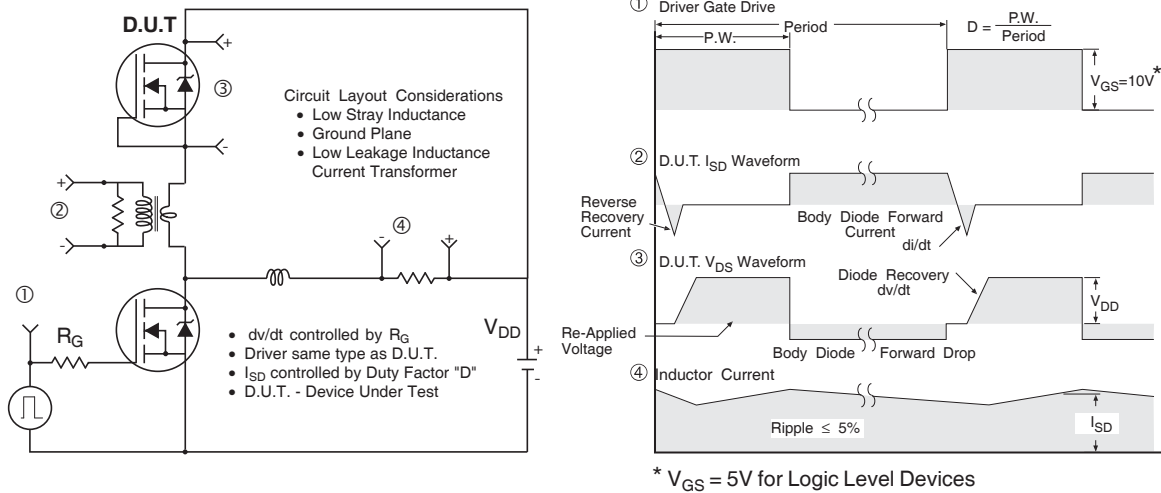


Fig 23. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

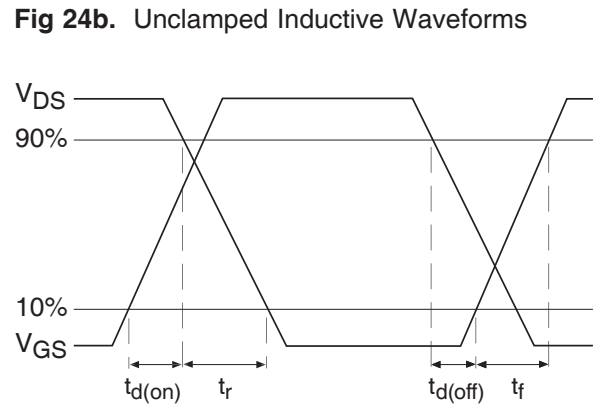
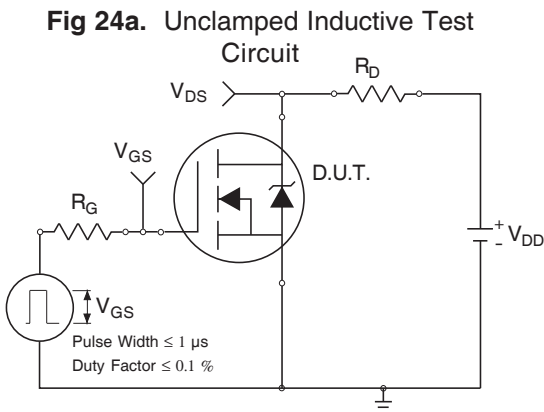
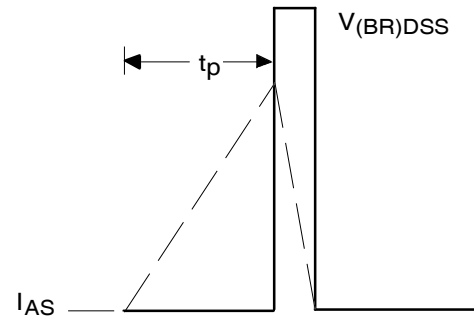
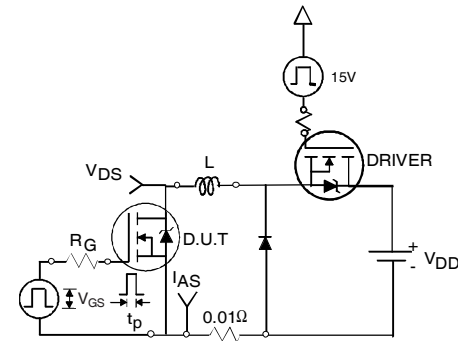


Fig 25a. Switching Time Test Circuit

Fig 25b. Switching Time Waveforms

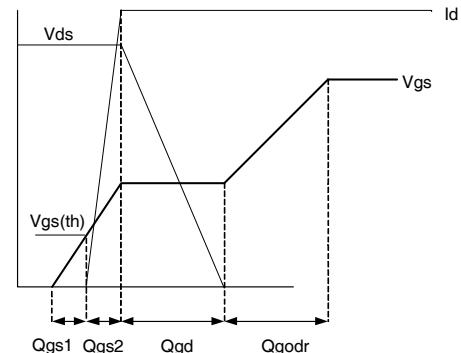
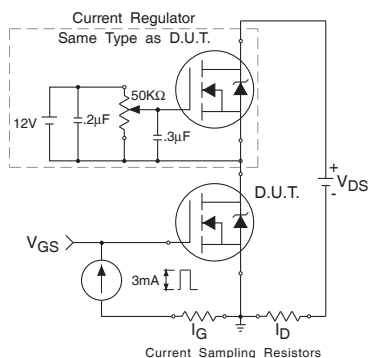
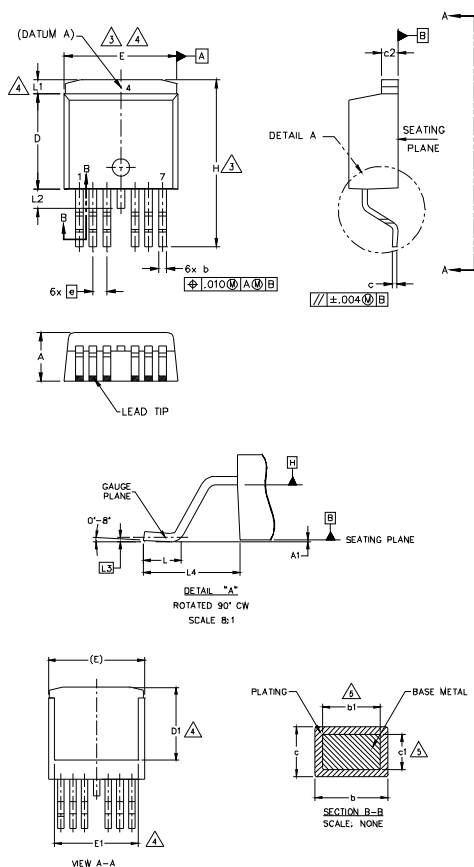


Fig 26a. Gate Charge Test Circuit

Fig 26b. Gate Charge Waveform

D²Pak - 7 Pin Package Outline

Dimensions are shown in millimeters (inches)

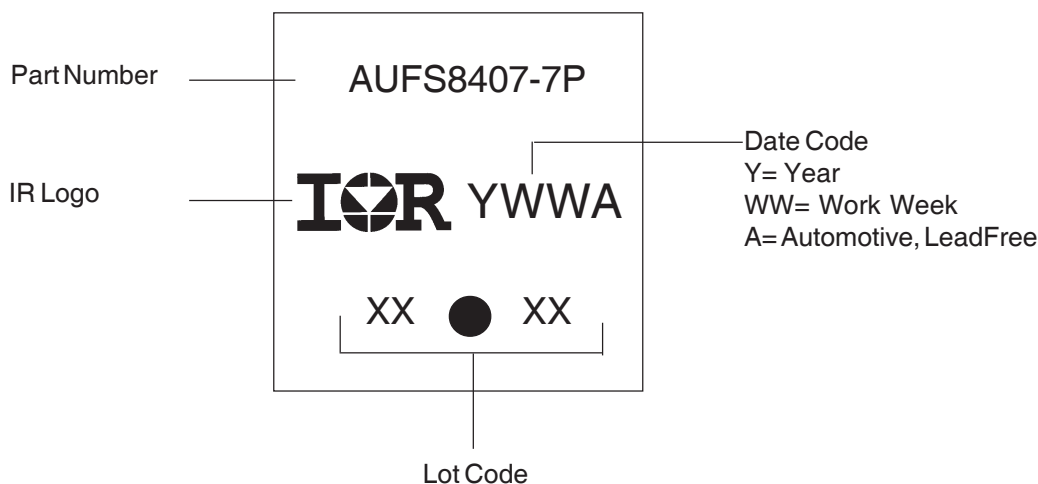


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	—	0.254	—	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	1.27 BSC		.050 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	4
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB.

D²Pak - 7 Pin Part Marking Information



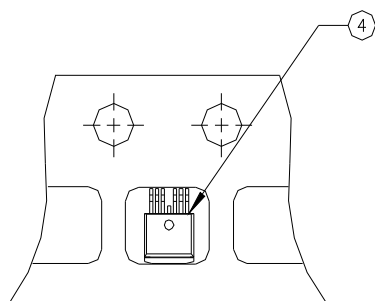
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D²Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

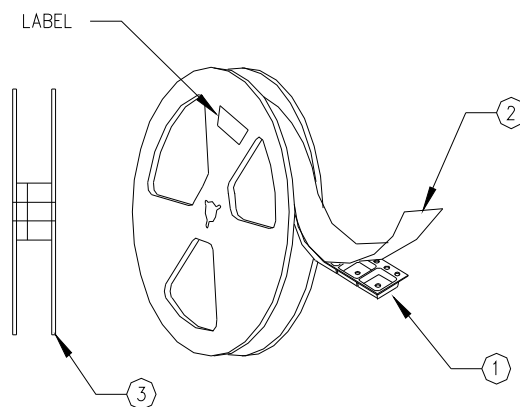
1. TAPE AND REEL.

- 1.1 REEL SIZE 13 INCH DIAMETER.
- 1.2 EACH REEL CONTAINING 800 DEVICES.
- 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
- 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
- 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
- 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS.
REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS.
HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.



2. LABELLING (REEL AND SHIPPING BAG).

- 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
- 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
- 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
- 2.4 QUANTITY:
- 2.5 VENDOR CODE: IR
- 2.6 LOT CODE:
- 2.7 DATE CODE:



Qualification Information[†]

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
		D ² PAK 7 Pin	MSL1
ESD	Machine Model	Class M3 (+/- 400V) ^{††} AEC-Q101-002	
	Human Body Model	Class H2 (+/- 4000V) ^{††} AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) ^{††} AEC-Q101-005	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

^{††} Highest passing voltage.

IMPORTANT NOTICE

Unless specifically designated for the automotive market, International Rectifier Corporation and its subsidiaries (IR) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or services without notice. Part numbers designated with the “AU” prefix follow automotive industry and / or customer specific requirements with regards to product discontinuance and process change notification. All products are sold subject to IR’s terms and conditions of sale supplied at the time of order acknowledgment.

IR warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with IR’s standard warranty. Testing and other quality control techniques are used to the extent IR deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

IR assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using IR components. To minimize the risks with customer products and applications, customers should provide adequate design and operating safeguards.

Reproduction of IR information in IR data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alterations is an unfair and deceptive business practice. IR is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of IR products or serviced with statements different from or beyond the parameters stated by IR for that product or service voids all express and any implied warranties for the associated IR product or service and is an unfair and deceptive business practice. IR is not responsible or liable for any such statements.

IR products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of the IR product could create a situation where personal injury or death may occur. Should Buyer purchase or use IR products for any such unintended or unauthorized application, Buyer shall indemnify and hold International Rectifier and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that IR was negligent regarding the design or manufacture of the product.

Only products certified as military grade by the Defense Logistics Agency (DLA) of the US Department of Defense, are designed and manufactured to meet DLA military specifications required by certain military, aerospace or other applications. Buyers acknowledge and agree that any use of IR products not certified by DLA as military-grade, in applications requiring military grade products, is solely at the Buyer’s own risk and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

IR products are neither designed nor intended for use in automotive applications or environments unless the specific IR products are designated by IR as compliant with ISO/TS 16949 requirements and bear a part number including the designation “AU”. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, IR will not be responsible for any failure to meet such requirements.

For technical support, please contact IR’s Technical Assistance Center

<http://www.irf.com/technical-info/>

WORLD HEADQUARTERS:

101 N. Sepulveda Blvd., El Segundo, California 90245

Tel: (310) 252-7105