

Qualification Information[†]

Qualification Level		Automotive (per AEC-Q100 ^{††})	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D2PAK-5L	MSL1, 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M3 (300V) (per AEC-Q100-003)	
	Human Body Model	Class H2 (2,500 V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (1000 V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

^{††} Exceptions to AEC-Q100 requirements are noted in the qualification report.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. (Tj= -40°C..150°C, Vcc=8..50V unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units
Vout	Maximum output voltage	Vcc-60	Vcc+0.3	V
Vcc-Vin max.	Maximum Vcc voltage	-32	60	V
I _{fb} , max.	Maximum feedback current	-50	10	mA
Pd	Maximum power dissipation (internally limited by thermal protection)			W
	T _{ambient} =25°C, T _j =150°C R _{th} =50°C/W D ² Pack 6cm ² footprint	—	2.5	
T _j max.	Max. storage & operating junction temperature	-40	150	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
R _{th1}	Thermal resistance junction to ambient D ² Pak Std footprint	60	—	°C/W
R _{th2}	Thermal resistance junction to ambient D ² pak 6cm ² footprint	40	—	
R _{th3}	Thermal resistance junction to case D ² pak	0.8	—	

Recommended Operating Conditions

These values are given for a quick design.

Symbol	Parameter	Min.	Max.	Units
I _{out}	Continuous output current, T _{ambient} =85°C, T _j =125°C			A
	R _{th} =40°C/W, D ² pak 6cm ² footprint	—	10	
R _{ifb}		1.5	—	kΩ

Static Electrical Characteristics

$T_j = -40..150^{\circ}\text{C}$, $V_{cc} = 8..50\text{V}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Vcc op.	Operating voltage range	8	—	50	V	
Rds(on)	ON state resistance $T_j = 25^{\circ}\text{C}$	—	6	7.5	m Ω	Ids=10A
	ON state resistance $T_j = 150^{\circ}\text{C}$	—	12	15		
Icc off	Supply leakage current	—	2	6	μA	Vin=Vcc=28V, Vifb=Vgnd Vout=Vgnd, $T_j = 25^{\circ}\text{C}$
Iout off	Output leakage current	—	2	6		
V clamp1	Vcc to Vout clamp voltage 1	60	65	—	V	Id=10mA
V clamp2	Vcc to Vout clamp voltage 2	—	66	—		Id=10A see fig. 2
Vih(2)	High level Input threshold voltage	—	5.5	6.8		Id=10mA
Vil(2)	Low level Input threshold voltage	3.5	5	—		
Rds(on) rev	Reverse On state resistance $T_j = 25^{\circ}\text{C}$	—	7	10	m Ω	Isd=10A, Vcc-Vin=7..32V
	Reverse On state resistance $T_j = 150^{\circ}\text{C}$	—	13	18		
Vf	Forward body diode voltage $T_j = 25^{\circ}\text{C}$	—	0.75	0.8	V	If=10A
	Forward body diode voltage $T_j = 125^{\circ}\text{C}$	—	0.6	0.65		
Rin	Internal input resistor	180	250	350	Ω	$T_j = -40^{\circ}\text{C}..125^{\circ}\text{C}$

(2) Input thresholds are measured directly between the input pin and the tab. See also page 6

Switching Electrical Characteristics

Vcc=28V, Resistive load=3 Ω , $T_j = 25^{\circ}\text{C}$

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
tdon	Turn on delay time to 20%	25	35	50	μs	See fig. 1
tr	Rise time from 20% to 80% of Vcc	8	17	25		
tdoff	Turn off delay time	50	80	120	μs	
tf	Fall time from 80% to 20% of Vcc	5	13	35		

Protection Characteristics

$T_j = -40..150^{\circ}\text{C}$, $V_{cc} = 8..50\text{V}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Tsd	Over temperature threshold	150(3)	165	—	$^{\circ}\text{C}$	See fig. 3 and fig. 10
Isd	Over-current shutdown	30	45	60	A	See fig. 3 and page 7
I fault	I _{fb} after an over-current or an over-temperature (latched)	2.4	4	6	mA	See fig. 3

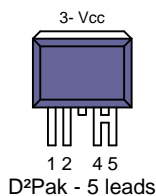
Current Sensing Characteristics

$T_j = -40..150^{\circ}\text{C}$, $V_{cc} = 8..50\text{V}$ (unless otherwise specified)

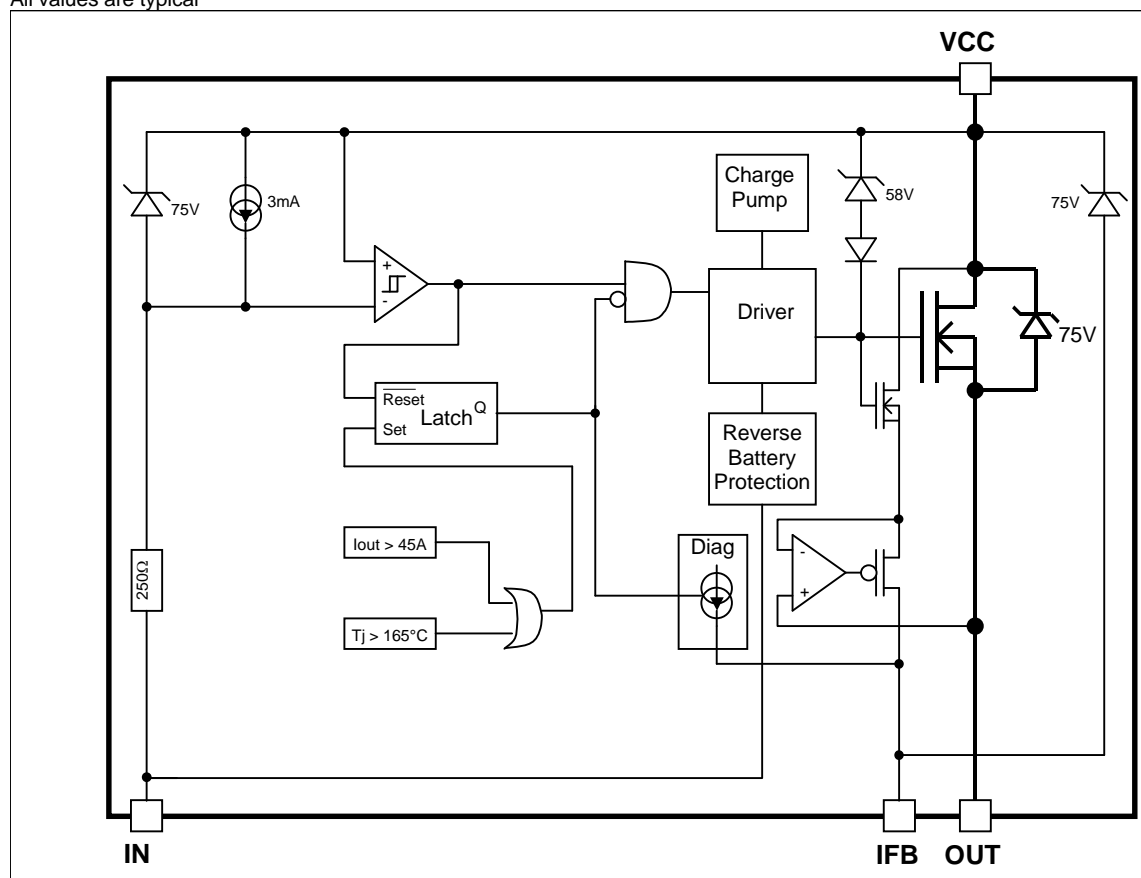
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ratio	I _{load} / I _{fb} current ratio	11000	13000	14500		Iout=10A
Ratio_TC	I _{load} / I _{fb} variation over temperature	-5%	0	+5	%	
I offset	Load current offset	-0.25	0	0.25	A	Iout<10A
I _{fb} leakage	I _{fb} leakage current on	0	6	15	μA	Iout=0A, $T_j = 25^{\circ}\text{C}$

(3) Guaranteed by design

1- In
2- Ifb
3- Vcc
4- Out
5- Out



All values are typical



Truth Table

Op. Conditions	Input	Output	I _{fb} pin voltage
Normal mode	H	L	0V
Normal mode	L	H	I _{load} x R _{fb} / Ratio
Open load	H	L	0V
Open load	L	H	I _{fb} leakage x R _{fb}
Short circuit to GND	H	L	0V
Short circuit to GND	L	L	I _{fault} x R _{fb} (latched)
Over temperature	H	L	0V
Over temperature	L	L	I _{fault} x R _{fb} (latched)

Operating voltage

Maximum V_{cc} voltage : this is the maximum voltage before the breakdown of the IC process.

Operating voltage : This is the V_{cc} range in which the functionality of the part is guaranteed. The AEC-Q100 qualification is run at the maximum operating voltage specified in the datasheet.

Reverse battery

During the reverse battery the Mosfet is turned on if the input pin is powered with a diode in parallel of the input transistor. Power dissipation in the IPS : $P = R_{\text{dson rev}} \cdot I_{\text{load}}^2 + V_{\text{cc}}^2 / 250$ (internal input resistor).

If the power dissipation I too hight in R_{fb}, a diode in serial can be added to block the current.

Active clamp

The purpose of the active clamp is to limit the voltage across the MOSFET to a value below the body diode break down voltage to reduce the amount of stress on the device during switching.

The temperature increase during active clamp can be estimated as follows:

$$\Delta T_j = P_{\text{CL}} \cdot Z_{\text{TH}}(t_{\text{CLAMP}})$$

Where: $Z_{\text{TH}}(t_{\text{CLAMP}})$ is the thermal impedance at t_{CLAMP} and can be read from the thermal impedance curves given in the data sheets.

$P_{\text{CL}} = V_{\text{CL}} \cdot I_{\text{CLavg}}$: Power dissipation during active clamp

$V_{\text{CL}} = 39\text{V}$: Typical V_{CLAMP} value

$$I_{\text{CLavg}} = \frac{I_{\text{CL}}}{2} : \text{Average current during active clamp}$$

$$t_{\text{CL}} = \frac{I_{\text{CL}}}{\left| \frac{di}{dt} \right|} : \text{Active clamp duration}$$

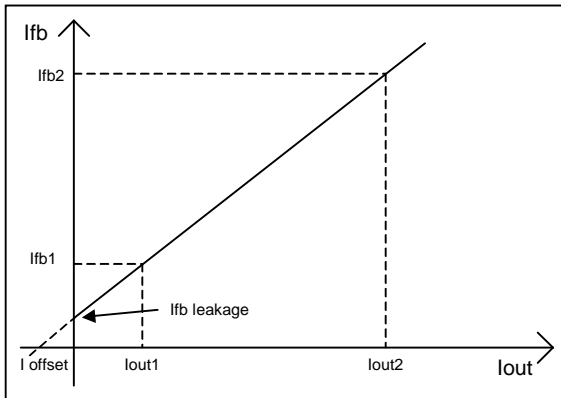
$$\frac{di}{dt} = \frac{V_{\text{Battery}} - V_{\text{CL}}}{L} : \text{Demagnetization current}$$

Figure 9 gives the maximum inductance versus the load current in the worst case : the part switch off after an over temperature detection. If the load inductance exceed the curve, a free wheeling diode is required.

Input level VIH/VIL

The input level are referenced to Vcc. When Vcc-Vin exceed VIH the part turns on and when Vcc-Vin goes below VIL the part turns off

Current sensing accuracy



The current sensing is specified by measuring 3 points :

- Ifb1 for Iout1
- Ifb2 for Iout2
- Ifb leakage for Iout=0

The parameters in the datasheet are computed with the following formula :

$$\text{Ratio} = (I_{out2} - I_{out1}) / (I_{fb2} - I_{fb1})$$

$$I_{offset} = I_{fb1} \times \text{Ratio} - I_{out1}$$

This allows the designer to evaluate the Ifb for any Iout value using :

$$I_{fb} = (I_{out} + I_{offset}) / \text{Ratio} \text{ if } I_{fb} > I_{fb \text{ leakage}}$$

For some applications, a calibration is required. In that case, the accuracy of the system will depends on the variation of the I offset and the ratio over the temperature range. The ratio variation is given by Ratio_TC specified in page 4.

The Ioffset variation depends directly of the Rdson :

$$I_{offset@-40^{\circ}\text{C}} = I_{offset@25^{\circ}\text{C}} / 0.7$$

$$I_{offset@150^{\circ}\text{C}} = I_{offset@25^{\circ}\text{C}} / 1.9$$

Over-current protection

The threshold of the over-current protection is set in order to guaranteed that the device is able to turn on a load with an inrush current lower than the minimum of Isd. Nevertheless for high current and high temperature the device may switch off for a lower current due to the over-temperature protection (see Figure 10).

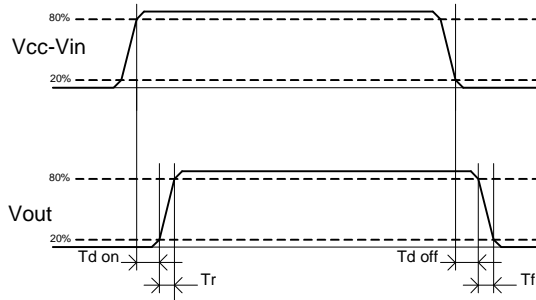


Figure 1 – IN rise time & switching definitions

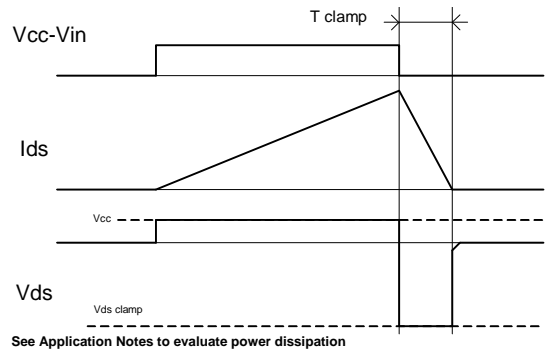


Figure 2 – Active clamp waveforms

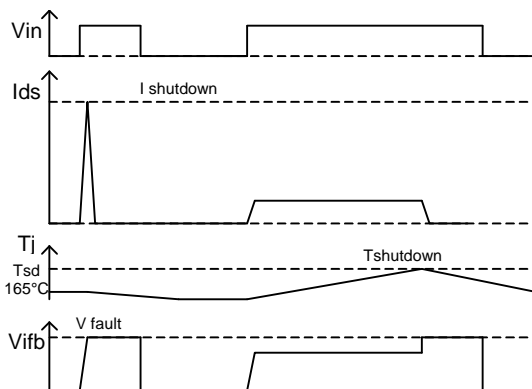


Figure 3 – Protection timing diagram

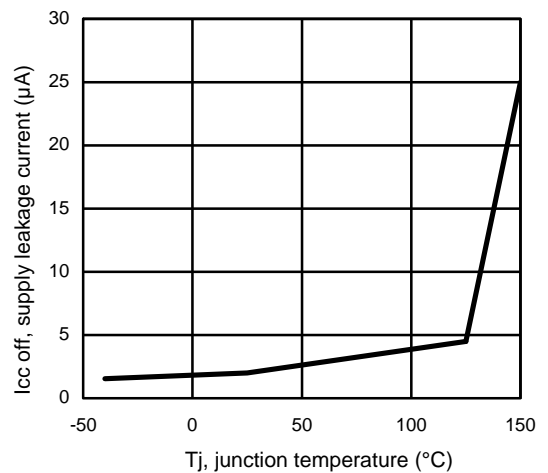


Figure 4 – Icc off (µA) Vs Tj (°C)

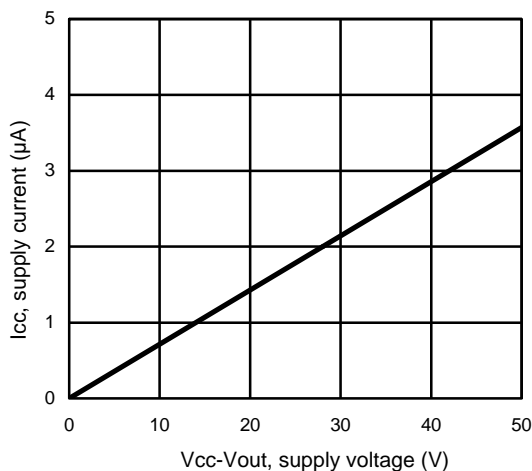


Figure 5 – Icc Off(μA) Vs Vcc-Vout (V)

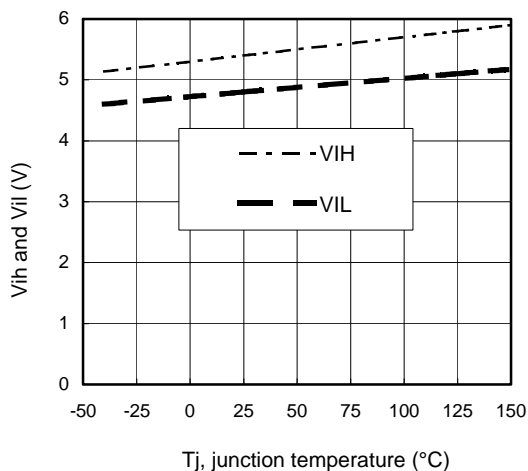


Figure 6 – Vih and Vil (V) Vs Tj (°C)

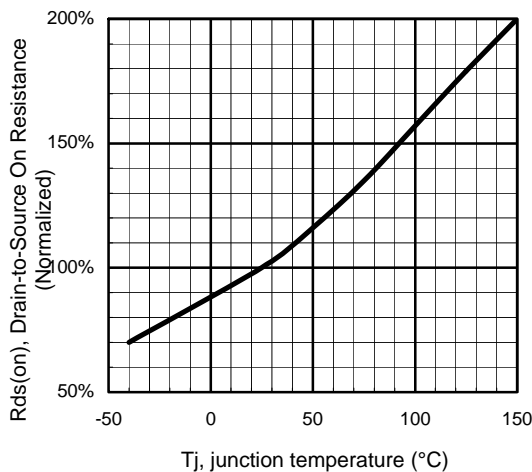


Figure 7 - Normalized Rds(on) (%) Vs Tj (°C)

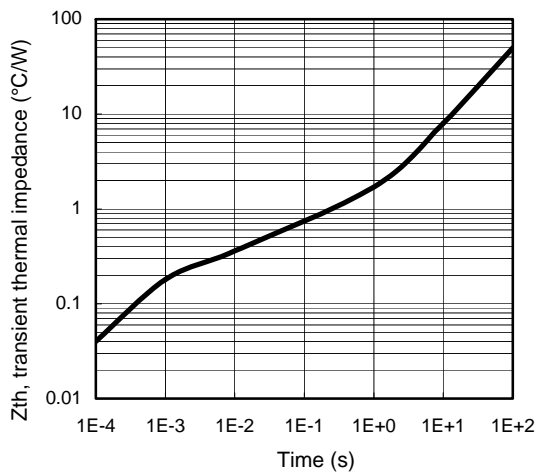


Figure 8 – Transient thermal impedance (°C/W) Vs time (s)

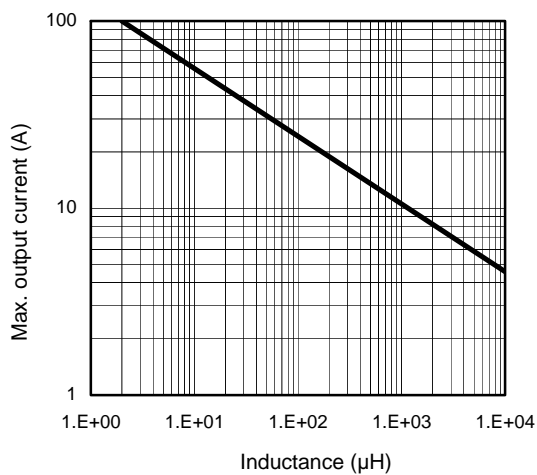


Figure 9 – Max. Iout (A) Vs inductance (μH)

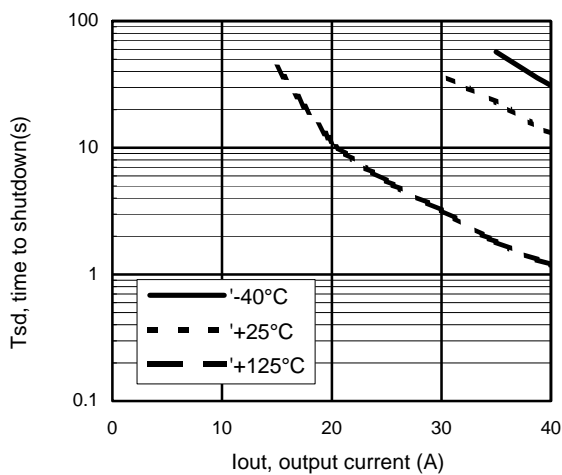
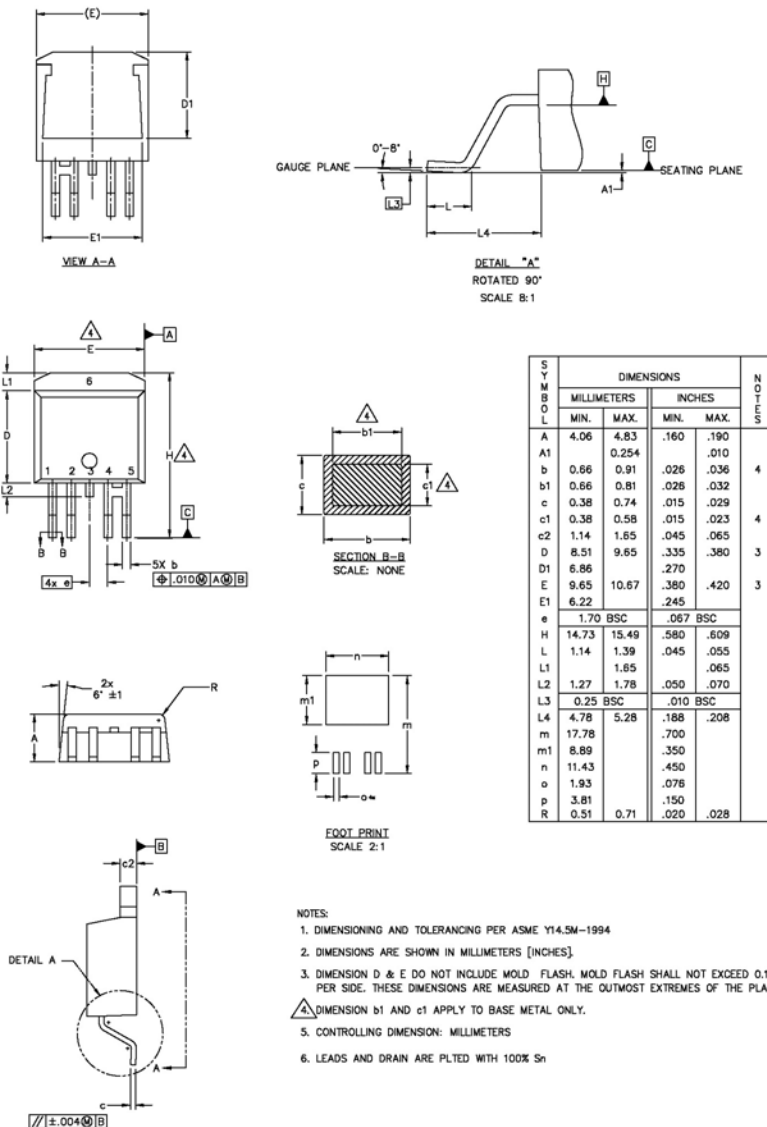
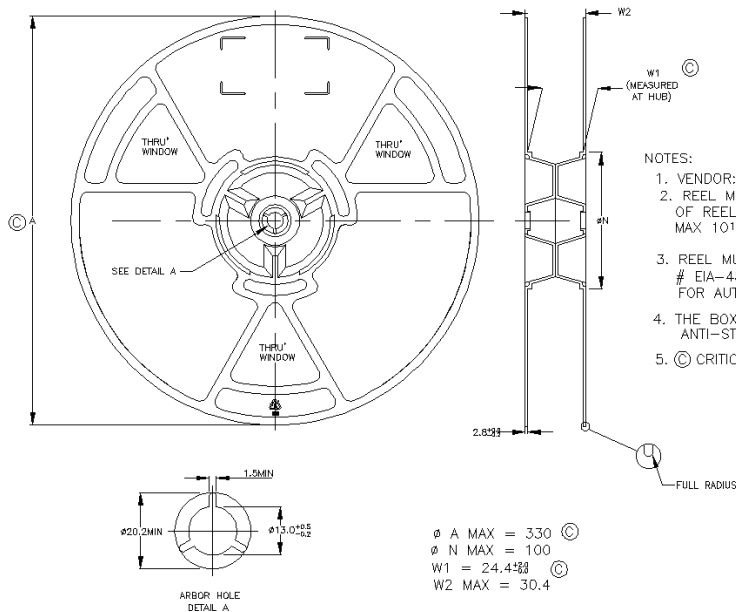


Figure 10 – Tsd (s) Vs Iout (A)
SMD with 6cm²

Case Outline D2PAK - 5 Leads



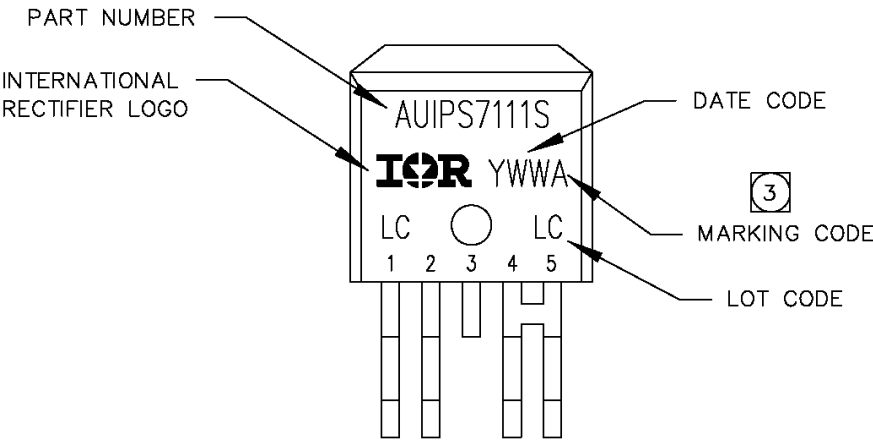
Tape & Reel D2PAK - 5 Leads



NOTES:

1. VENDOR: OPTIONAL
2. REEL MUST HAVE ANTI-STATIC COATING SURFACE RESISTIVITY OF REEL (AS PER EIA-541) μin : 10^9 ohm/SQUARE ; MAX $10^{12} \text{ ohm/SQUARE}$
3. REEL MUST ALSO MEET REQUIREMENTS OF EIA STANDARD # EIA-481A, TAPING OF SURFACE-MOUNT COMPONENTS FOR AUTOMATIC PLACEMENT.
4. THE BOX OF PACKING MUST CONTAIN THE REELS INSIDE AN ANTI-STATIC BAG.
5. C CRITICAL

Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIPS7111R	D2-Pak-5-Leads	Tube	50	AUIPS7111S
		Tape and reel left	800	AUIPS7111STRL
		Tape and reel right	800	AUIPS7111STRR

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