1. Overview of the mXT224S

1.1 Introduction

The Atmel® maXTouch family of touch controllers has set a new industry benchmark for capacitive touchscreens with their low current consumption, fast response time and high levels of accuracy. The mXT224S's single-chip solution offers the benefits of the maXTouch enhanced architecture on devices with touchscreens up to 5 inch diagonal:

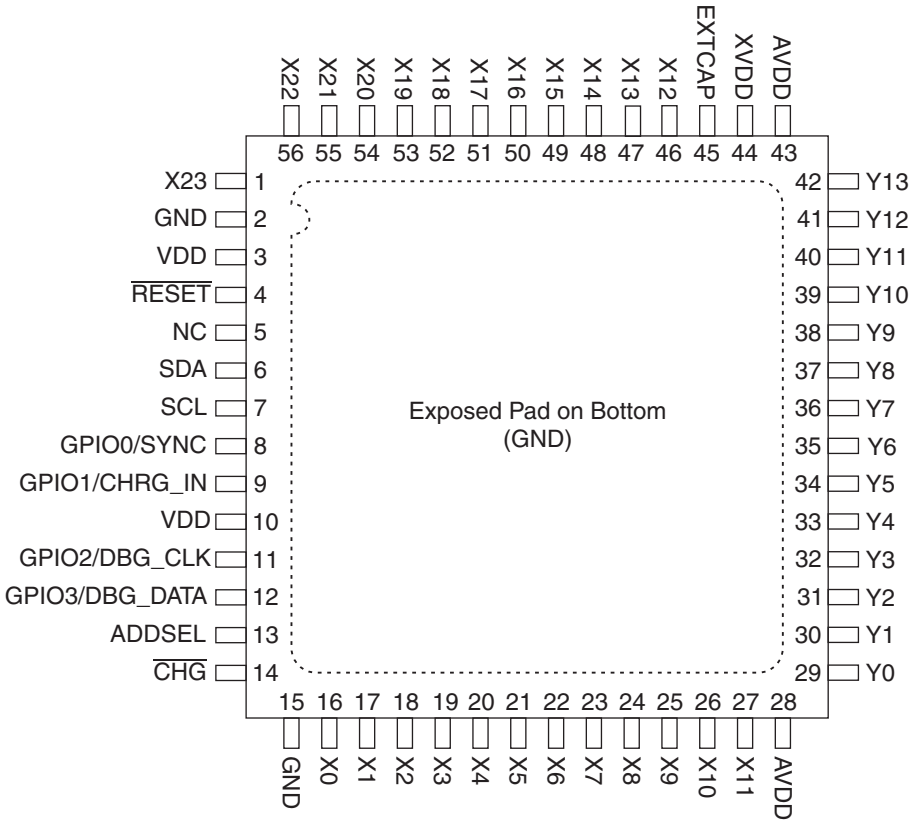
- **Patented capacitive sensing method** – The mXT224S uses a unique charge-transfer acquisition engine to implement Atmel's patented QMatrix® capacitive sensing method. This allows the measurement of up to 224 mutual capacitance nodes. Coupled with a state-of-the-art CPU, the entire touchscreen sensing solution can measure, classify and track individual finger touches with a high degree of accuracy.
- **Capacitive Touch Engine (CTE)** – The mXT224S features an acquisition engine, which uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver inputs (Y lines). The engine includes sufficient dynamic range to cope with anticipated touchscreen mutual capacitances. This allows great flexibility for use with Atmel's proprietary ITO pattern designs. One and two layer ITO sensors are possible using glass or PET substrates.
- **SlimSensor Technology** – A combination of analog circuitry, hardware noise processing, and firmware that combats display noise up to 3.5 Vpp without requiring additional listening channels or synchronization to display timing. This enables the use of shieldless touch sensor stacks, including touch-on-lens.
- **maXCharger Technology** – High voltage X line drive, combined with hardware spike suppression and active noise avoidance firmware to combat charger noise up to 240 Vpp.
- **Processing power** – The CPU has a powerful, yet low power, microsequencer coprocessor under its control. This allows the signal acquisition, preprocessing, postprocessing and housekeeping to be partitioned in an efficient and flexible way. This gives ample scope for sensing algorithms, touch tracking or advanced shape-based filtering. An in-circuit reflash can be performed over the chip's hardware-driven interface (I^2C-compatible).
- **Interpreting user intention** – Atmel's mutual capacitance method provides unambiguous multitouch performance. Algorithms in the mXT224S provide optimized touchscreen position filtering for the smooth tracking of touches. Stylus support allows stylus touches to be detected and distinguished from other touches, such as finger touches. The suppression of unintentional touches from the user's gripping fingers, resting palm or touching cheek or ear also help ensure that the user's intentions are correctly interpreted.
- **Environmental conditions** – The mXT224S brings improved performance in harsh environmental conditions. The robust mutual capacitance measurement method means that the mXT224S works well in the presence of moisture. An operating temperature as low as -40°C allows the user's designs to be used in the coldest of environments. In addition, a high signal-to-noise ratio allows the design to be used with gloves for easy operation in cold environments, during sport or in a workshop.

  Overall, the mXT224S represents a step improvement over competing technologies. Its near optimal mix of low power, small size and low part count, coupled with unrivalled true multitouch performance ensures that the mXT224S is set to take capacitive sensing to the next level.

2. Pinouts and Schematics

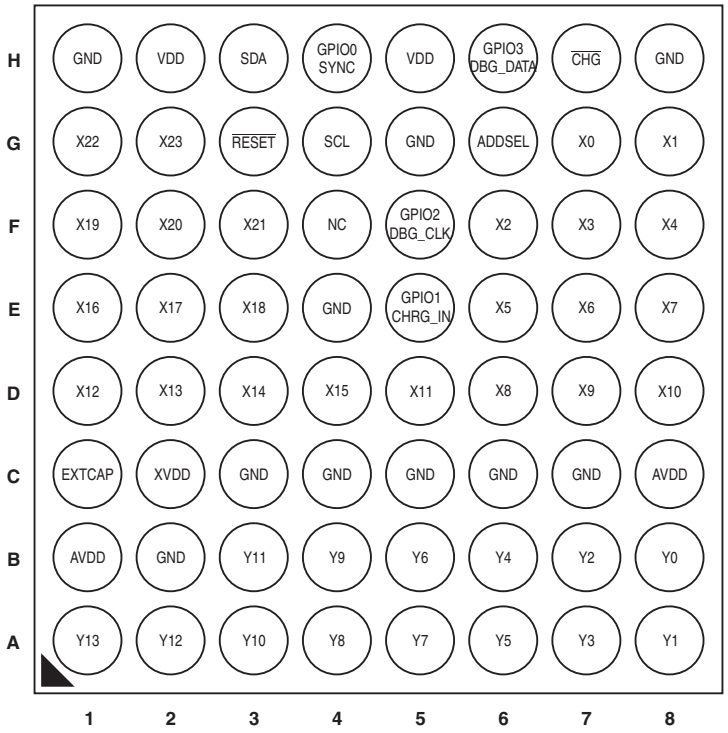
2.1 Pinouts

2.1.1 56-pin UQFN



Top View

2.1.2 64-ball UFBGA



Bottom View

2.2 Pin Descriptions

2.3 56-pin UQFN

Table 2-1. Pin Listings (56-pin UQFN)

Pin	Name	Type	Description	If Unused...
1	X23	O	X line connection	Leave open
2	GND	P	Ground	–
3	VDD	P	Power	–
4	$\overline{\text{RESET}}$	I	Reset low; has internal 20 kΩ to 60 kΩ pull-up resistor	Vdd (1)
5	N/C	–	No connection	Leave open
6	SDA	OD	Serial Interface Data	–
7	SCL	OD	Serial Interface Clock	–
8	GPIO0 SYNC	I/O	General purpose I/O External synchronization	Input: GND Output: leave open
9	GPIO1 CHRG_IN	I/O	General purpose I/O Charger present input	Input: GND Output: leave open
10	VDD	P	Power	–
11	GPIO2 DBG_CLK	I/O	General purpose I/O Debug clock	Input: GND Output: leave open
12	GPIO3 DBG_DATA	I/O	General purpose I/O Debug data	Input: GND Output: leave open
13	ADDSEL	I	I^2C-compatible address select	–
14	$\overline{\text{CHG}}$ (2)	OD	State change interrupt	–
15	GND	P	Ground	–
16	X0	O	X matrix drive line	Leave open
17	X1	O	X matrix drive line	Leave open
18	X2	O	X matrix drive line	Leave open
19	X3	O	X matrix drive line	Leave open
20	X4	O	X matrix drive line	Leave open
21	X5	O	X matrix drive line	Leave open
22	X6	O	X matrix drive line	Leave open
23	X7	O	X matrix drive line	Leave open
24	X8	O	X matrix drive line	Leave open
25	X9	O	X matrix drive line	Leave open
26	X10	O	X matrix drive line	Leave open
27	X11	O	X matrix drive line	Leave open
28	AVDD	P	Analog power	–
29	Y0	I	Y line connection	Leave open
30	Y1	I	Y line connection	Leave open

Table 2-1. Pin Listings (56-pin UQFN) (Continued)

Pin	Name	Type	Description	If Unused...
31	Y2	I	Y line connection	Leave open
32	Y3	I	Y line connection	Leave open
33	Y4	I	Y line connection	Leave open
34	Y5	I	Y line connection	Leave open
35	Y6	I	Y line connection	Leave open
36	Y7	I	Y line connection	Leave open
37	Y8	I	Y line connection	Leave open
38	Y9	I	Y line connection	Leave open
39	Y10	I	Y line connection	Leave open
40	Y11	I	Y line connection	Leave open
41	Y12	I	Y line connection	Leave open
42	Y13	I	Y line connection	Leave open
43	AVDD	P	Analog power	–
44	XVDD	P	X line drive power Normal voltage mode – connect to AVDD Voltage doubler mode – connect via capacitor to EXTCAP	–
45	EXTCAP	P	Normal voltage mode – leave open Voltage doubler mode – connect via capacitor to XVDD	–
46	X12	O	X matrix drive line	Leave open
47	X13	O	X matrix drive line	Leave open
48	X14	O	X matrix drive line	Leave open
49	X15	O	X matrix drive line	Leave open
50	X16	O	X matrix drive line	Leave open
51	X17	O	X matrix drive line	Leave open
52	X18	O	X matrix drive line	Leave open
53	X19	O	X matrix drive line	Leave open
54	X20	O	X matrix drive line	Leave open
55	X21	O	X matrix drive line	Leave open
56	X22	O	X matrix drive line	Leave open
Exposed Pad		P	Ground; exposed pad must be connected to GND	–

1. It is recommend that $\overline{\text{RESET}}$ is connected to the host system.
2. $\overline{\text{CHG}}$ is momentarily set (approximately 100 ms) as an input after power-up or reset for diagnostic purposes.

I Input only I/O Input and output OD Open drain output P Ground or power

2.4 64-ball UFBGA

Table 2-2. Pin Listings (64-ball UFBGA)

Pin	Name	Type	Description	If Unused...
A1	Y13	I	Y line connection	Leave open
A2	Y12	I	Y line connection	Leave open
A3	Y10	I	Y line connection	Leave open
A4	Y8	I	Y line connection	Leave open
A5	Y7	I	Y line connection	Leave open
A6	Y5	I	Y line connection	Leave open
A7	Y3	I	Y line connection	Leave open
A8	Y1	I	Y line connection	Leave open
B1	AVDD	P	Analog power	–
B2	GND	P	Ground	–
B3	Y11	I	Y line connection	Leave open
B4	Y9	I	Y line connection	Leave open
B5	Y6	I	Y line connection	Leave open
B6	Y4	I	Y line connection	Leave open
B7	Y2	I	Y line connection	Leave open
B8	Y0	I	Y line connection	Leave open
C1	EXTCAP	P	Normal voltage mode – leave open Voltage doubler mode – connect via capacitor to XVDD	–
C2	XVDD	P	X line drive power Normal voltage mode – connect to AVDD Voltage doubler mode – connect via capacitor to EXTCAP	–
C3	GND	P	Ground	–
C4	GND	P	Ground	–
C5	GND	P	Ground	–
C6	GND	P	Ground	–
C7	GND	P	Ground	–
C8	AVDD	P	Analog power	–
D1	X12	O	X matrix drive line	Leave open
D2	X13	O	X matrix drive line	Leave open
D3	X14	O	X matrix drive line	Leave open
D4	X15	O	X matrix drive line	Leave open
D5	X11	O	X matrix drive line	Leave open
D6	X8	O	X matrix drive line	Leave open
D7	X9	O	X matrix drive line	Leave open
D8	X10	O	X matrix drive line	Leave open

Table 2-2. Pin Listings (64-ball UFBGA) (Continued)

Pin	Name	Type	Description	If Unused...
E1	X16	O	X matrix drive line	Leave open
E2	X17	O	X matrix drive line	Leave open
E3	X18	O	X matrix drive line	Leave open
E4	GND	P	Ground	–
E5	GPIO1 CHRG_IN	I/O	General purpose I/O Charger present input	Input: GND Output: leave open
E6	X5	O	X matrix drive line	Leave open
E7	X6	O	X matrix drive line	Leave open
E8	X7	O	X matrix drive line	Leave open
F1	X19	O	X matrix drive line	Leave open
F2	X20	O	X matrix drive line	Leave open
F3	X21	O	X matrix drive line	Leave open
F4	N/C	–	No connection	–
F5	GPIO2 DBG_CLK	I/O	General purpose I/O Debug clock	Input: GND Output: leave open
F6	X2	O	X matrix drive line	Leave open
F7	X3	O	X matrix drive line	Leave open
F8	X4	O	X matrix drive line	Leave open
G1	X22	O	X matrix drive line	Leave open
G2	X23	O	X matrix drive line	Leave open
G3	$\overline{\text{RESET}}$	I	Reset low; has internal 20 kΩ to 60 kΩ pull-up resistor	Vdd [1]
G4	SCL	OD	Serial Interface Clock	–
G5	GND	P	Ground	–
G6	ADDSEL	I	I^2C-compatible address select	–
G7	X0	O	X matrix drive line	Leave open
G8	X1	O	X matrix drive line	Leave open
H1	GND	P	Ground	–
H2	VDD	P	Power	–
H3	SDA	OD	Serial Interface Data	–
H4	GPIO0 SYNC	I/O	General purpose I/O External synchronization	Input: GND Output: leave open
H5	VDD	P	Power	–
H6	GPIO3 DBG_DATA	I/O	General purpose I/O Debug data	Input: GND Output: leave open
H7	$\overline{\text{CHG}}$ [2]	OD	State change interrupt	–

Table 2-2. Pin Listings (64-ball UFBGA) (Continued)

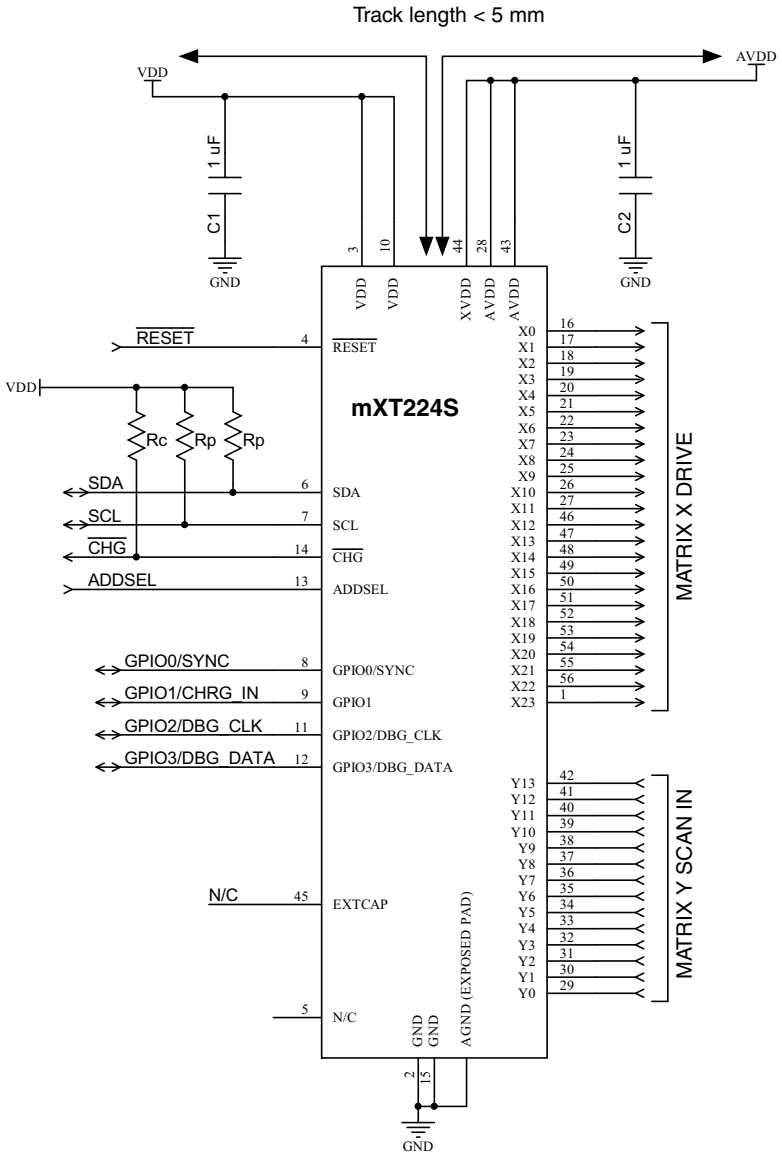
Pin	Name	Type	Description	If Unused...
H8	GND	P	Ground	–

1. It is recommend that $\overline{\text{RESET}}$ is connected to the host system.
2. $\overline{\text{CHG}}$ is momentarily set (approximately 100 ms) as an input after power-up or reset for diagnostic purposes.

I Input only I/O Input and output OD Open drain output P Ground or power

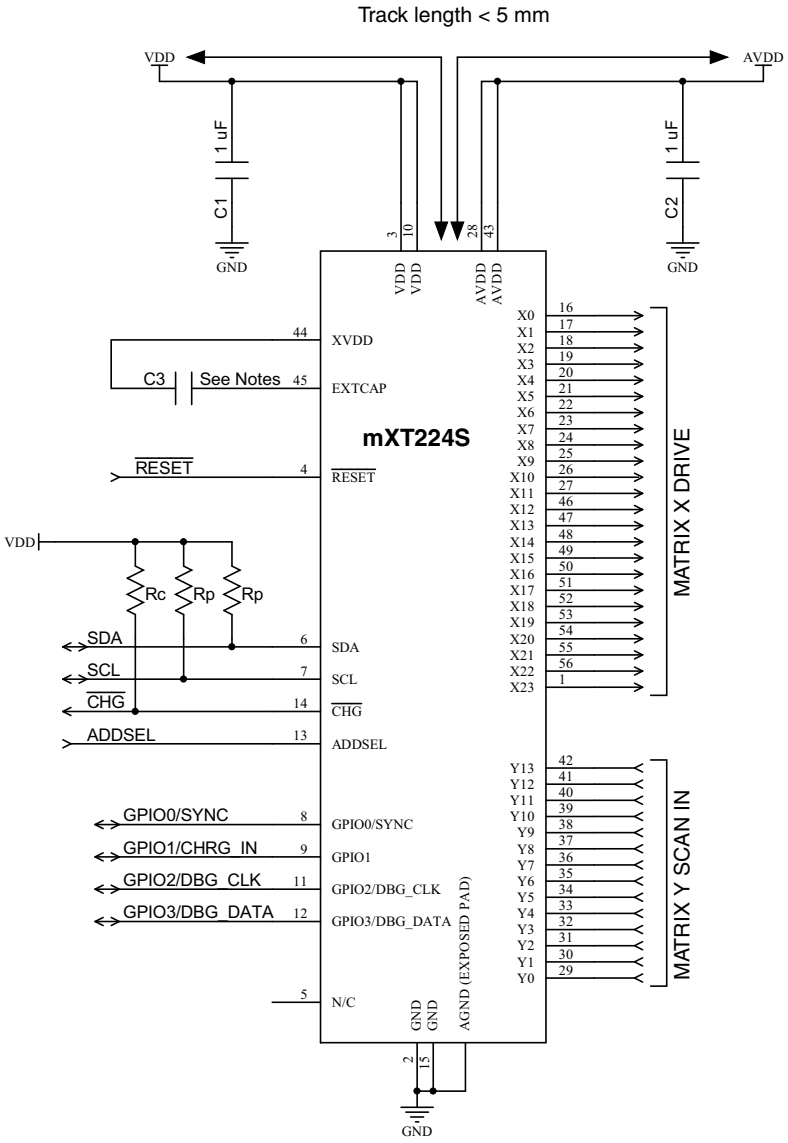
2.5 Schematics

2.5.1 56-pin UQFN – Normal Mode



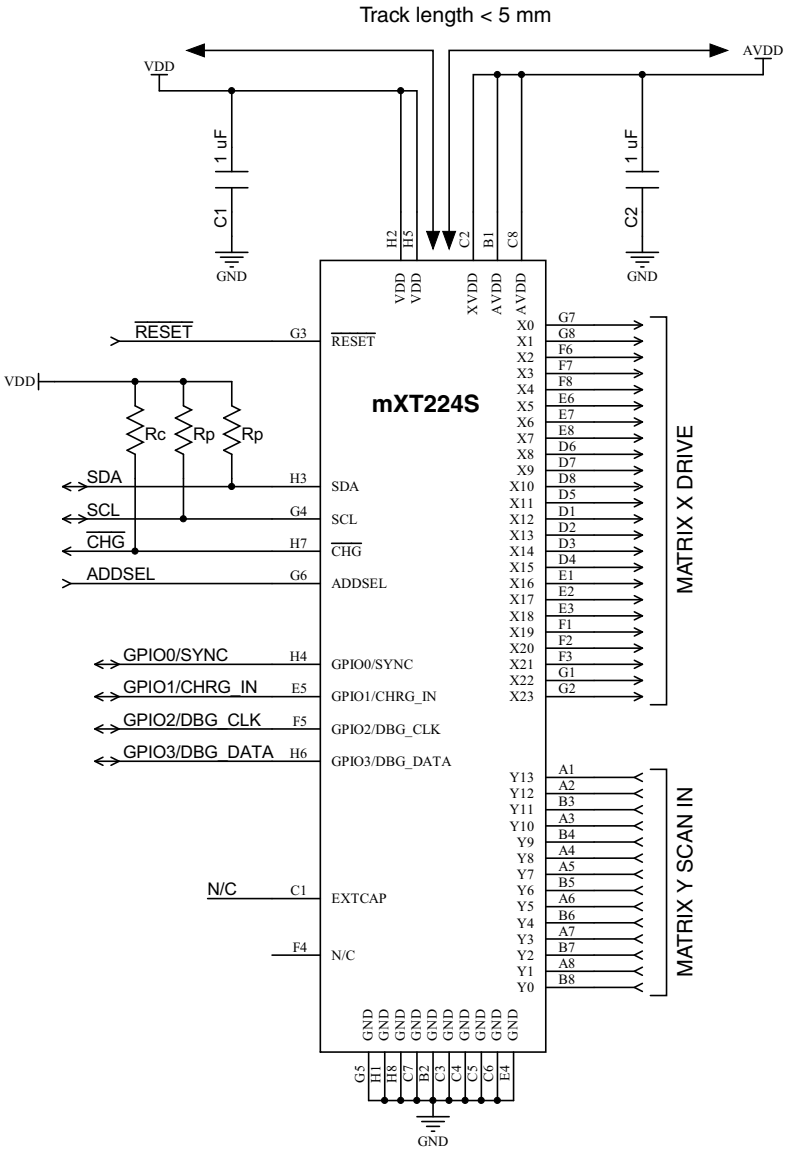
Notes:
1. Capacitors C1 and C2 must be X7R or X5R. Tracks on bypass capacitors should be <5 mm in length.
2. The number of capacitors in this schematic is recommended for optimum performance when the device is mounted on the system board and the track length between the device decoupling capacitors and onboard power supplies is < 50 mm. If the device is mounted on a tail and the track length between the device decoupling capacitors and power supplies is > 50 mm, the number of capacitors may need to be increased. See Section 4.8.2 on page 29.
3. Pin 44 (XVDD) must be connected to AVDD in normal mode.
4. Pin 45 (EXTCAP) is not connected in normal mode.
5. The exposed pad must be connected to GND.
6. A maximum of 224 XY channels can be used at any one time (see Section 4.6 on page 26).
7. See Appendix A on page 48 for detailed information on PCB layout.

2.5.2 56-pin UQFN – Voltage Doubler Mode



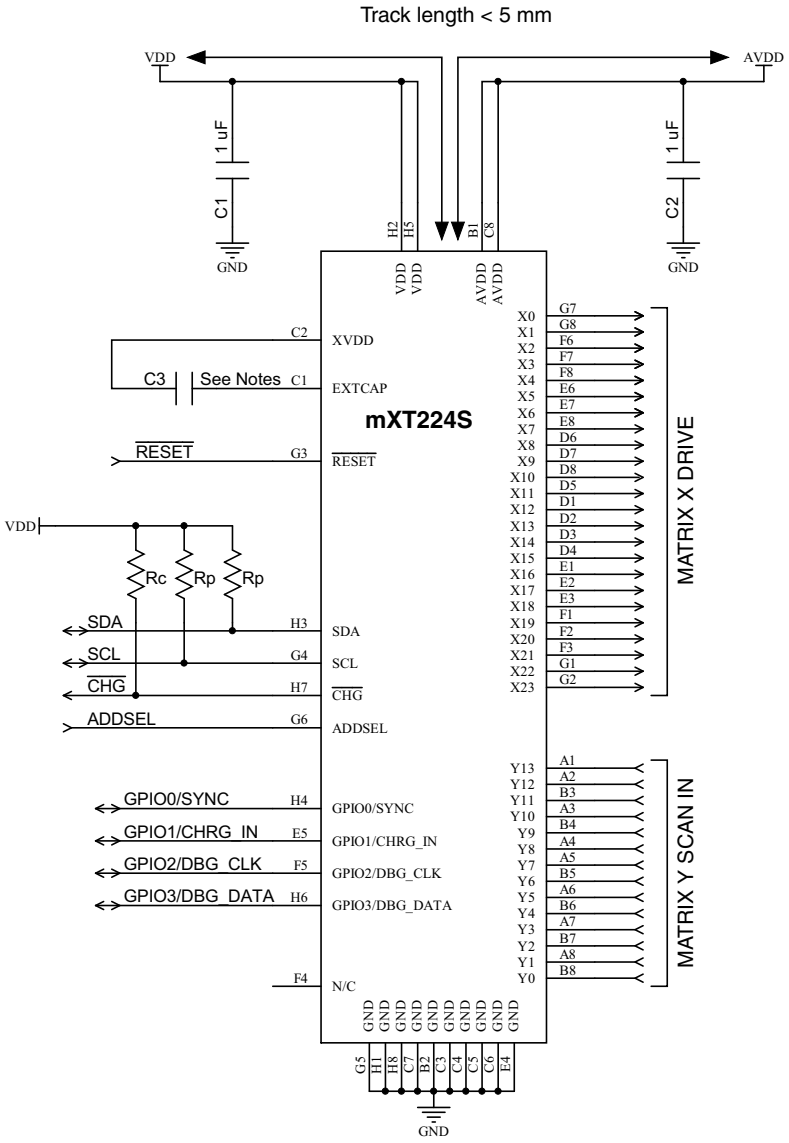
Notes:
1. Capacitors C1 to C3 must be X7R or X5R. Tracks on bypass capacitors should be <5 mm in length.
2. The number of capacitors in this schematic is recommended for optimum performance when the device is mounted on the system board and the track length between the device decoupling capacitors and onboard power supplies is < 50 mm. If the device is mounted on a tail and the track length between the device decoupling capacitors and power supplies is > 50 mm, the number of capacitors may need to be increased. See Section 4.8.2 on page 29.
3. Pin 45 (EXTCAP) must be connected to Pin 44 (XVDD) via a capacitor in voltage doubler mode.
4. The recommended value of capacitor C3 is 22nF.
5. The exposed pad must be connected to GND.
6. A maximum of 224 XY channels can be used at any one time (see Section 4.6 on page 26).
7. See Appendix A on page 48 for detailed information on PCB layout.

2.5.3 64-ball UFBGA – Normal Mode



Notes:
1. Capacitors C1 and C2 must be X7R or X5R. Tracks on bypass capacitors should be <5 mm in length.
2. The number of capacitors in this schematic is recommended for optimum performance when the device is mounted on the system board and the track length between the device decoupling capacitors and onboard power supplies is < 50 mm. If the device is mounted on a tail and the track length between the device decoupling capacitors and power supplies is > 50 mm, the number of capacitors may need to be increased. See Section 4.8.2 on page 29.
3. Pin C2 (XVDD) must be connected to AVDD in normal mode.
4. Pin C1 (EXTCAP) is not connected in normal mode.
5. A maximum of 224 XY channels can be used at any one time (see Section 4.6 on page 26).
6. See Appendix A on page 48 for detailed information on PCB layout.

2.5.4 64-ball UFBGA – Voltage Doubler Mode



Notes:
1. Capacitors C1 to C3 must be X7R or X5R. Tracks on bypass capacitors should be <5 mm in length.
2. The number of capacitors in this schematic is recommended for optimum performance when the device is mounted on the system board and the track length between the device decoupling capacitors and onboard power supplies is < 50 mm. If the device is mounted on a tail and the track length between the device decoupling capacitors and power supplies is > 50 mm, the number of capacitors may need to be increased. See Section 4.8.2 on page 29.
3. Pin C1 (EXTCAP) must be connected to Pin C2 (XVDD) via a capacitor in voltage doubler mode.
4. The recommended value of capacitor C3 is 22nF.
5. A maximum of 224 XY channels can be used at any one time (see Section 4.6 on page 26).
6. See Appendix A on page 48 for detailed information on PCB layout.

2.6 Understanding Unfamiliar Concepts

If some of the concepts mentioned in this datasheet are unfamiliar, see the following sections for more information:

- Appendix C on page 55 for a glossary of terms
- Appendix D on page 56 for QMatrix technology

2.7 Resources

The following document provides essential information on configuring the mXT224S:

- *mXT224S Protocol Guide*

The following documents may also be useful (available by contacting Atmel's Touch Technology division):

- **Configuring the mXT224S:**
  - Application Note: QTAN0058 – *Rejecting Unintentional Touches with the maXTouch Touchscreen Controllers*
  - Application Note QTAN0050 – *Using the maXTouch Debug Port*
  - Application Note QTAN0059 – *Using the maXTouch Self Test Feature*
  - Application Note QTAN0078 – *maXTouch Stylus Tuning*
  - Application Note QTAN0086 – *Touchscreen Design for Gloved Operation*
- **Touchscreen design and PCB/FPCB layout guidelines:**
  - Application Note QTAN0054 – *Getting Started with maXTouch Touchscreen Designs*
  - Application Note QTAN0048 – *maXTouch PCB/FPCB Layout Guidelines*
  - Application Note QTAN0080 – *Touchscreens Sensor Design Guide*
- **Bootloading:**
  - Application Note QTAN0051 – *Bootloading Procedure for Atmel® Touch Sensors Based on the Object Protocol*
- **Miscellaneous:**
  - Application Note QTAN0061 – *maXTouch™ Sensitivity Effects for Mobile Devices*

3. Touchscreen Basics

3.1 Sensor Construction

A touchscreen is usually constructed from a number of transparent electrodes. These are typically on a glass or plastic substrate. They can also be made using non-transparent electrodes, such as copper or carbon. Electrodes are normally formed by etching a material called Indium Tin Oxide (ITO). This is a brittle ceramic material, of high optical clarity and varying sheet resistance. Thicker ITO yields lower levels of resistance (perhaps tens to hundreds of Ω/square) at the expense of reduced optical clarity. Lower levels of resistance are generally more compatible with capacitive sensing. Thinner ITO leads to higher levels of resistance (perhaps hundreds to thousands of Ω/square) with some of the best optical characteristics.

Long thin features, such as interconnecting tracks, formed in ITO, can cause problems. The excessive RC time constants formed between the resistance of the track and the capacitance of the electrode to ground can inhibit the capacitive sensing function. In such cases, ITO tracks should be replaced by screen printed conductive inks (non-transparent) outside the touchscreen's viewing area.

A range of trade-offs also exist with regard to the number of layers used for construction. Atmel has pioneered single-layer ITO capacitive touchscreens. For many applications these offer a near optimum cost/performance balance. With a single layer screen, the electrodes are all connected using ITO out to the edges of the sensor. From there the connection is picked up with printed silver tracks. Sometimes two overprinted silver tracking layers are used to reduce the margins between the edge of the substrate and the active area of the sensor.

Two-layer designs can have a strong technical appeal where ultra-narrow edge margins are required. They are also an advantage where the capacitive sensing function needs to have a very precise cut-off as a touch is moved to just off the active sensor area. With a two-layer design the QMatrix transmitter electrodes are normally placed nearest the bottom and the receiver electrodes nearest the top. The separation between layers can range from hundreds of nanometers to hundreds of microns, with the right electrode design and considerations of the sensing environment.

3.2 Electrode Configuration

The specific electrode designs used in Atmel's touchscreens are the subject of various patents and patent applications. Further information is available on request.

A maximum of 224 channels can be used at any one time across all enabled touch objects. See Section 4.6 on page 26 for more information.

3.3 Scanning Sequence

All channels are scanned in sequence by the mXT224S. There is full parallelism in the scanning sequence to improve overall response time. The channels are scanned by measuring capacitive changes at the intersections formed between the first X line and all the Y lines. Then the intersections between the next X line and all the Y lines are scanned, and so on, until all X and Y combinations have been measured.

The device can be configured in various ways. It is possible to disable some channels so that they are not scanned at all. This can be used to improve overall scanning time.

3.4 Touchscreen Sensitivity

3.4.1 Adjustment

Sensitivity of touchscreens can vary across the extents of the electrode pattern due to natural differences in the parasitics of the interconnections, control chip, and so on. An important factor in the uniformity of sensitivity is the electrode design itself. It is a natural consequence of a touchscreen pattern that the edges form a discontinuity and hence tend to have a different sensitivity. The electrodes at the far edges do not have a neighboring electrode on one side and this affects the electric field distribution in that region.

A sensitivity adjustment is available for the whole touchscreen. This adjustment is a basic algorithmic threshold that defines when a channel is considered to have enough signal change to qualify as being in detect.

3.4.2 Mechanical Stackup

The mechanical stackup refers to the arrangement of material layers that exist above and below a touchscreen. The arrangement of the touchscreen in relation to other parts of the mechanical stackup has an effect on the overall sensitivity of the screen. QMatrix technology has an excellent ability to operate in the presence of ground planes close to the sensor. QMatrix sensitivity is attributed more to the interaction of the electric fields between the transmitting (X) and receiving (Y) electrodes than to the surface area of these electrodes. For this reason, stray capacitance on the X or Y electrodes does not strongly reduce sensitivity.

Front panel dielectric material has a direct bearing on sensitivity. Plastic front panels are usually suitable up to about 1.2 mm, and glass up to about 2.5 mm (dependent upon the screen size and layout). The thicker the front panel, the lower the signal-to-noise ratio of the measured capacitive changes and hence the lower the resolution of the touchscreen. In general, glass front panels are near optimal because they conduct electric fields almost twice as easily as plastic panels.

The mXT224S is suitable for various stackup arrangements (see Table 3-1 on page 17). In this table, three types of stackup are considered:

- Single layer co-planar construction with metal bridges at crossover points. This can use either a diamond pattern or Atmel's patented snowflake design.
- Co-planar with a ground shield; that is, a co-planar construction with a separate ground plane on another layer.
- Two layer designs in which the Y sensor is one layer and the X sensor flooded on another layer behind it (as with Atmel's flooded-X style).

Table 3-1 lists the various mechanical stackups and their suitability for use with the mXT224S.

Table 3-1. mXT224S Suitability for Various Mechanical Stackups

Display Construction	Mechanical Stackup		
	Co-planar	**Co-planar with Shield**	**Two Layers**
OLED, No Air Gap	Suitable	Suitable	Suitable
OLED, with Air Gap ≤ 0.25 mm	Not suitable (1)	Suitable	Suitable
LCD, No Air Gap	Suitable (testing advised)	Suitable	Suitable
LCD, with Air Gap ≤ 0.25 mm	Not suitable (1)	Suitable	Suitable

1. Because of the lens bending effect.

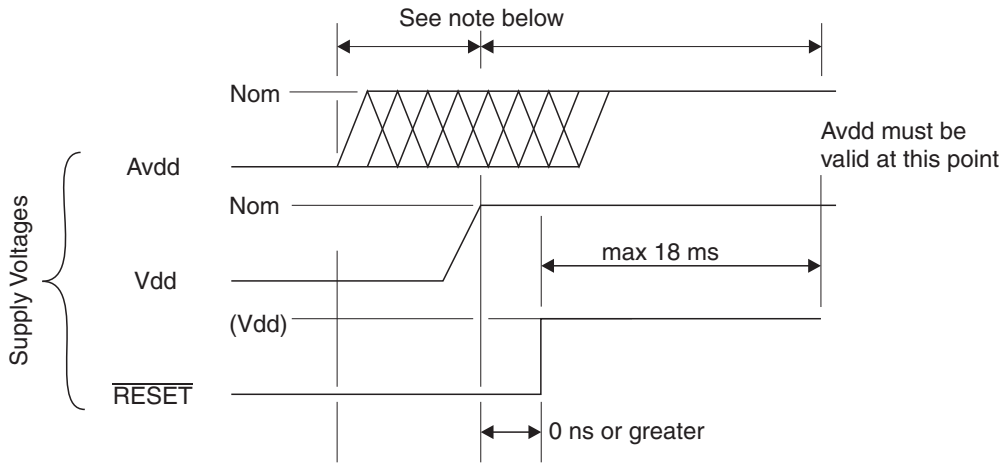
4. Detailed Operation

4.1 Power-up/Reset

There is an internal Power-on Reset (POR) in the device.

The device must be held in $\overline{\text{RESET}}$ (active low) while the digital power supply (Vdd) is powering up. If a slope or slew is applied to the digital supply, Vdd must reach its nominal value before the $\overline{\text{RESET}}$ signal is deasserted (that is, goes high). This is shown in Figure 4-1. See Section 6.3 on page 34 for nominal values of Vdd.

Figure 4-1. Power Sequencing on the mXT224S



Note: AVdd can be powered up before Vdd or a maximum of 18 ms after Vdd is valid or Reset is released.

To ensure the device does not damage itself with a broken screen, an initial pin-fault test is performed after reset (refer to the Self Test T25 object in the *mXT224S Protocol Guide*). If AVdd is not applied by the time this test is run then the pin-fault test fails and locks up the firmware operation, requiring a reset to recover.

Note: Depending on the touchscreen design, it may be necessary to adjust the PINDWELLUS setting in the Self Test T25 object in order to successfully complete an initial self test. The need for this can easily be determined by the CAL bit in the STATUS field of the Command Processor T6 object remaining permanently active. Refer to the Self Test T25 object in the *mXT224S Protocol Guide* for a detailed description of the PINDWELLUS field.

This means there must be a maximum time of 18 ms from the $\overline{\text{RESET}}$ going high to AVdd being valid. The measurement is taken from $\overline{\text{RESET}}$ going high to when the first activity occurs on X0 (this will be the initial pin-fault test running).

Make sure that any lines connected to the device are below or equal to Vdd during power-up. For example, if $\overline{\text{RESET}}$ is supplied from a different power domain to the mXT224S Vdd pin, make sure that it is held low when Vdd is off. If this is not done, the $\overline{\text{RESET}}$ signal could parasitically couple power via the mXT224S $\overline{\text{RESET}}$ pin into the Vdd supply.

After power-up, the device takes 25 ms before it is ready to start communications. Vdd must drop to below 1 V in order to effect a proper POR. See Section 6 on page 34 for further specifications.

The $\overline{\text{RESET}}$ pin can be used to reset the device whenever necessary. The $\overline{\text{RESET}}$ pin must be asserted low to cause a reset. Pulses on the $\overline{\text{RESET}}$ line must be a minimum of 90 ns duration to ensure correct operation of the reset; shorter-duration negative-going spikes on $\overline{\text{RESET}}$ must be avoided.

Note that the voltage level on the $\overline{\text{RESET}}$ pin of the device must never exceed Vdd (digital supply voltage).

A software reset command can be used to reset the chip (refer to the Command Processor T6 object in the *mXT224S Protocol Guide*). A software reset takes 25 ms. After the chip has finished it asserts the $\overline{\text{CHG}}$ line to signal to the host that a message is available. The reset flag is set in the Command Processor T6 object's STATUS message field to indicate to the host that it has just completed a reset cycle. This bit can be used by the host to detect any unexpected brownout events. This allows the host to take any necessary corrective actions, such as reconfiguration.

A checksum check is performed on the configuration settings held in the nonvolatile memory. If the checksum does not match a stored copy of the last checksum, then this indicates that the settings have become corrupted. This is signaled to the host by setting the configuration error bit in the message data for the Command Processor T6 object (refer to the *mXT224S Protocol Guide* for more information).

Note that the $\overline{\text{CHG}}$ line is momentarily set (approximately 100 ms) as an input after power-up or reset for diagnostic purposes. It is therefore particularly important that the line should be allowed to float high via the $\overline{\text{CHG}}$ line pull-up resistors during this period.

At power-on the device performs a self-test routine to check for shorts which might cause damage to the device. Please refer to Self Test T25 section of the *mXT224S Protocol Guide* for more details about this process.

4.2 Calibration

Calibration is the process by which the sensor chip assesses the background capacitance on each channel. Channels are only calibrated on power-up and when:

- The channel is enabled (that is, activated).

OR

- The channel is already enabled and one of the following applies:
  - The channel is held in detect for longer than the Touch Automatic Calibration setting (refer to the *mXT224S Protocol Guide* for more information on TCHAUTOCAL setting in the Acquisition Configuration T8 object).
  - The signal delta on a channel is at least the touch threshold (TCHTHR) in the anti-touch direction, while no other touches are present on the channel matrix (refer to the *mXT224S Protocol Guide* for more information on the TCHTHR field in the Multiple Touch Touchscreen T9 object).
  - The user issues a recalibrate command.
  - Certain configuration settings are changed.

A status message is generated on the start and completion of a calibration.

Note that the device performs a global calibration; that is, all the channels are calibrated together.

4.3 Sensor Acquisition

The maximum acquisition time for one X line on the mXT224S is 7.75 ms. Care should be taken to ensure that the total time for one X line configured by the Acquisition Configuration T8 and CTE Configuration T46 objects do not exceed this.

4.4 Communications

4.4.1 Communications Protocol

The mXT224S uses an I²C-compatible interface for communication. See Appendix E on page 58 for details of the I²C-compatible protocol.

The device presents data packets when internal changes have occurred. The $\overline{\text{CHG}}$ line going active signifies that a new data packet is available, thus providing an interrupt-style interface.

4.4.2 I²C-compatible Addresses

The mXT224S supports two I²C-compatible device addresses that are selected using the ADDSEL line at start-up. The two internal I²C-compatible device addresses are 0x4A (ADDSEL low) and 0x4B (ADDSEL high).

These are shifted left to form the SLA+W or SLA+R address when transmitted over the I²C-compatible interface, as shown in Table 4-1.

Table 4-1. Format of SLA+W and SLA+R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0x4A or 0x4B							Read/Write

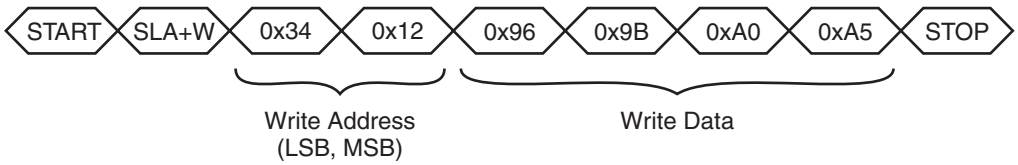
4.4.3 Writing To the Device

A WRITE cycle to the device consists of a START condition followed by the I²C-compatible address of the device (SLA+W). The next two bytes are the address of the location into which the writing starts. The first byte is the Least Significant Byte (LSByte) of the address, and the second byte is the Most Significant Byte (MSByte). This address is then stored as the address pointer.

Subsequent bytes in a multibyte transfer form the actual data. These are written to the location of the address pointer, location of the address pointer +1, location of the address pointer + 2, and so on. The address pointer returns to its starting value when the WRITE cycle's STOP condition is detected.

Figure 4-2 shows an example of writing four bytes of data to contiguous addresses starting at 0x1234.

Figure 4-2. Example of a Four-byte Write Starting at Address 0x1234

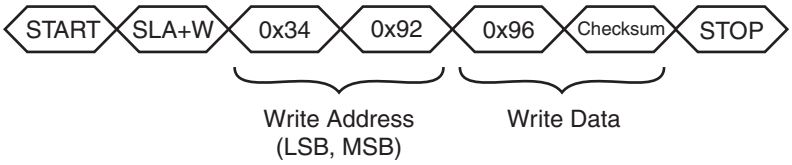


4.4.4 I²C-compatible Writes in Checksum Mode

In I²C-compatible checksum mode an 8-bit CRC is added to all I²C-compatible writes. The CRC is sent at the end of the data write as the last byte before the STOP condition. All the bytes sent are included in the CRC, including the two address bytes. Any command or data sent to the device is processed even if the CRC fails.

To indicate that a checksum is to be sent in the write, the most significant bit of the MSByte of the address is set to 1. For example, the I²C-compatible command shown in Figure 4-3 writes a value of 150 (0x96) to address 0x1234 with a checksum. The address is changed to 0x9234 to indicate checksum mode.

Figure 4-3. Example of a Write To Address 0x1234 With a Checksum



4.4.5 Reading From the Device

Two I²C-compatible bus activities must take place to read from the device. The first activity is an I²C-compatible write to set the address pointer (LSByte then MSByte). The second activity is the actual I²C-compatible read to receive the data. The address pointer returns to its starting value when the READ cycle's NACK is detected.

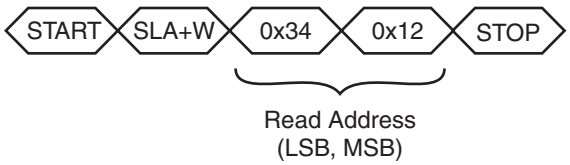
It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation. The address pointer will be correct if the reads occur in order. In particular, when reading multiple messages from the Message Processor object, the address pointer is automatically reset to allow continuous reads (see Section 4.4.6 on page 22).

The WRITE and READ cycles consist of a START condition followed by the I²C-compatible address of the device (SLA+W or SLA+R respectively).

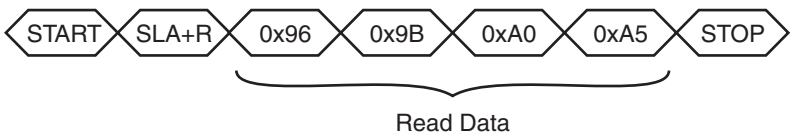
Figure 4-4 shows the I²C-compatible commands to read four bytes starting at address 0x1234.

Figure 4-4. Example of a Four-byte Read Starting at Address 0x1234

Set Address Pointer



Read Data



4.4.6 Reading Status Messages with DMA

The device facilitates the easy reading of multiple messages using a single continuous read operation. This allows the host hardware to use a direct memory access (DMA) controller for the fast reading of messages, as follows:

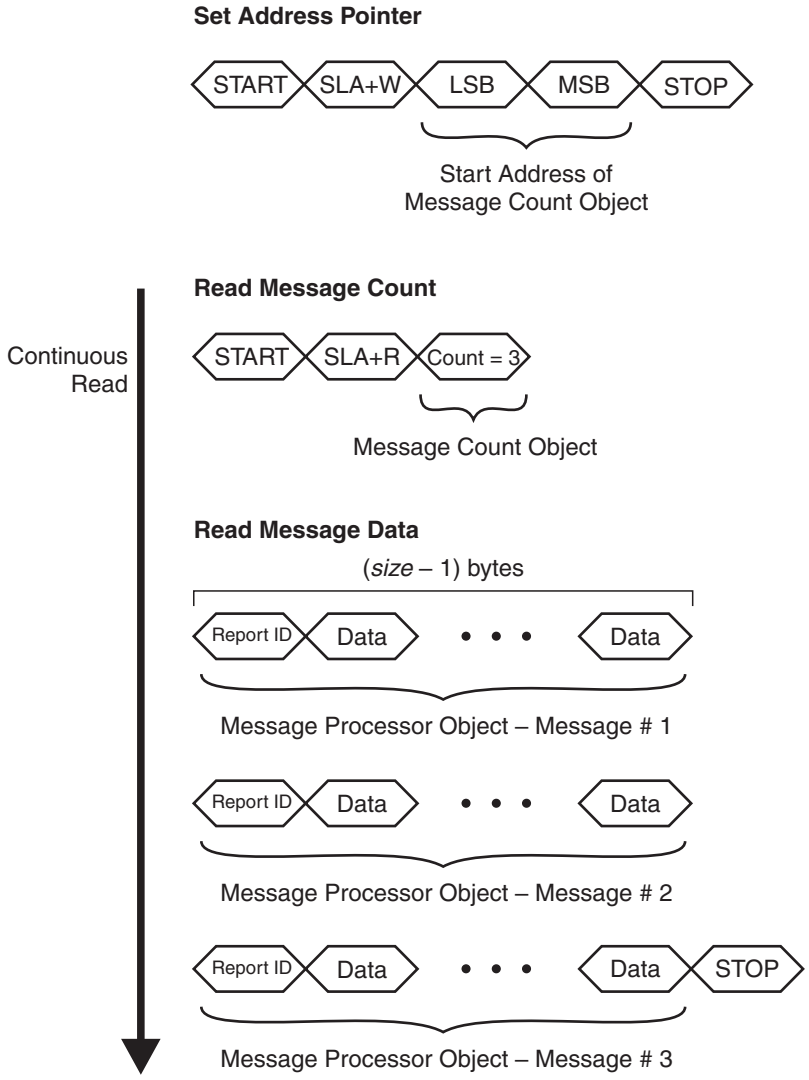
1. The host uses a write operation to set the address pointer to the start of the Message Count object, if necessary. (1) If a checksum is required on each message, the most significant bit of the MSByte of the read address must be set to 1.
2. The host starts the read operation of the message by sending a START condition.
3. The host reads the Message Count object (one byte) to retrieve a count of the pending messages (refer to the *mXT224S Protocol Guide* for details).
4. The host calculates the number of bytes to read by multiplying the message count by the size of the Message Processor object. (2)

   Note that the size of the Message Processor object as recorded in the Object Table includes a checksum byte; if a checksum is not required, this should be deducted from the size of the object. That is: number of bytes = count x (size-1).
5. The host reads the calculated number of message bytes. It is important that the host does *not* send a STOP condition during the message reads, as this will terminate the continuous read operation and reset the address pointer. No START and STOP conditions must be sent between the messages.
6. The host sends a NACK at the end of the read operation after the last message has been read. The NACK resets the address pointer to the start of Message Count object.

Figure 4-5 on page 23 shows an example of using a continuous read operation to read three messages from the device without a checksum. Figure 4-6 on page 24 shows the same example with a checksum.

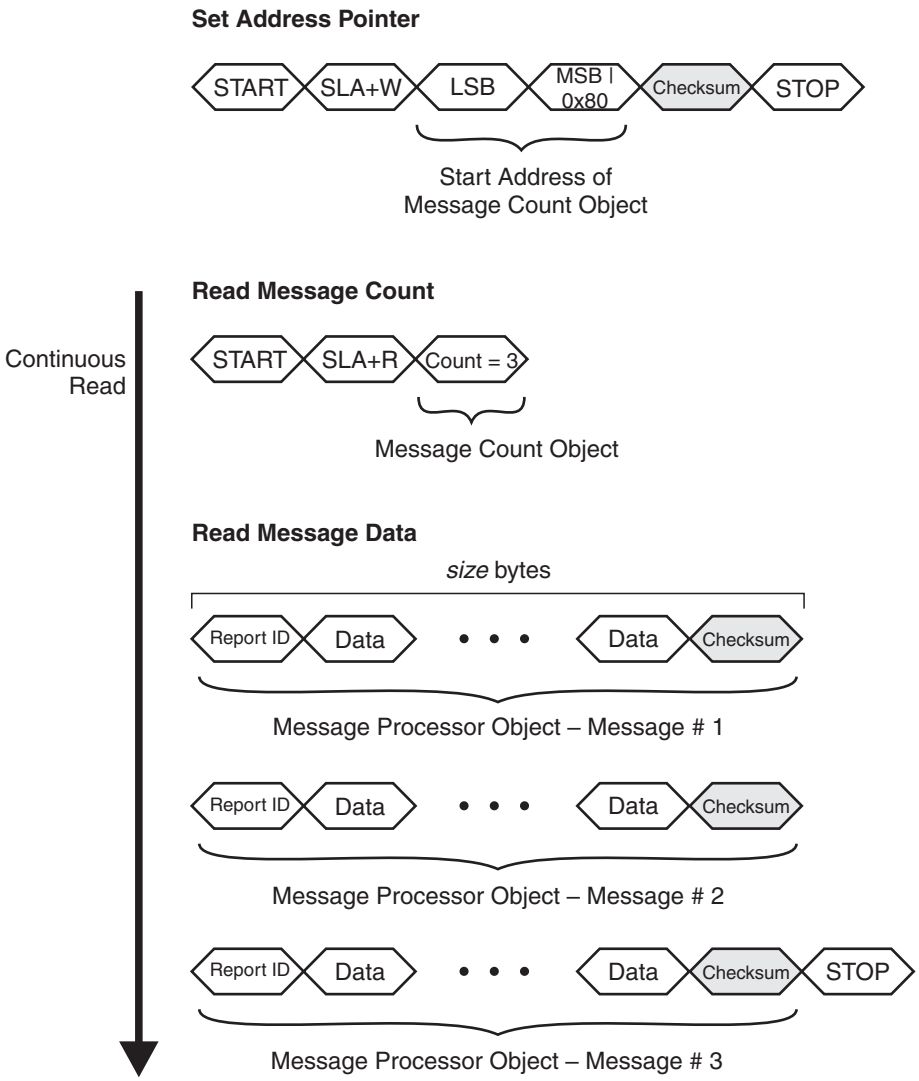
1. The NACK at the end of the read resets the address pointer to its initial location, so it may already be pointing at the Message Count object following a previous message read.
2. The host should have already read the size of the Message Processor object in its initialization code (see Section 5.3 on page 31).

Figure 4-5. Continuous Message Read Example – No Checksum



Notes:
1. STOP and START conditions are not necessary between messages.
2. The address pointer is automatically reset to the start of the Message Processor Object between reads.

Figure 4-6. Continuous Message Read Example – I²C-compatible Checksum Mode



There are no checksums added on any other I²C-compatible reads. An 8-bit CRC can be added, however, to all I²C-compatible writes, as described in Section 4.4.4 on page 21.

An alternative method of reading messages using the $\overline{\text{CHG}}$ line is given in Section 4.4.7.

4.4.7 $\overline{\text{CHG}}$ Line

The $\overline{\text{CHG}}$ line is an active-low, open-drain output that is used to alert the host that a new message is available in the Message Processor object. This provides the host with an interrupt-style interface with the potential for fast response times. It reduces the need for wasteful I²C-compatible communications.

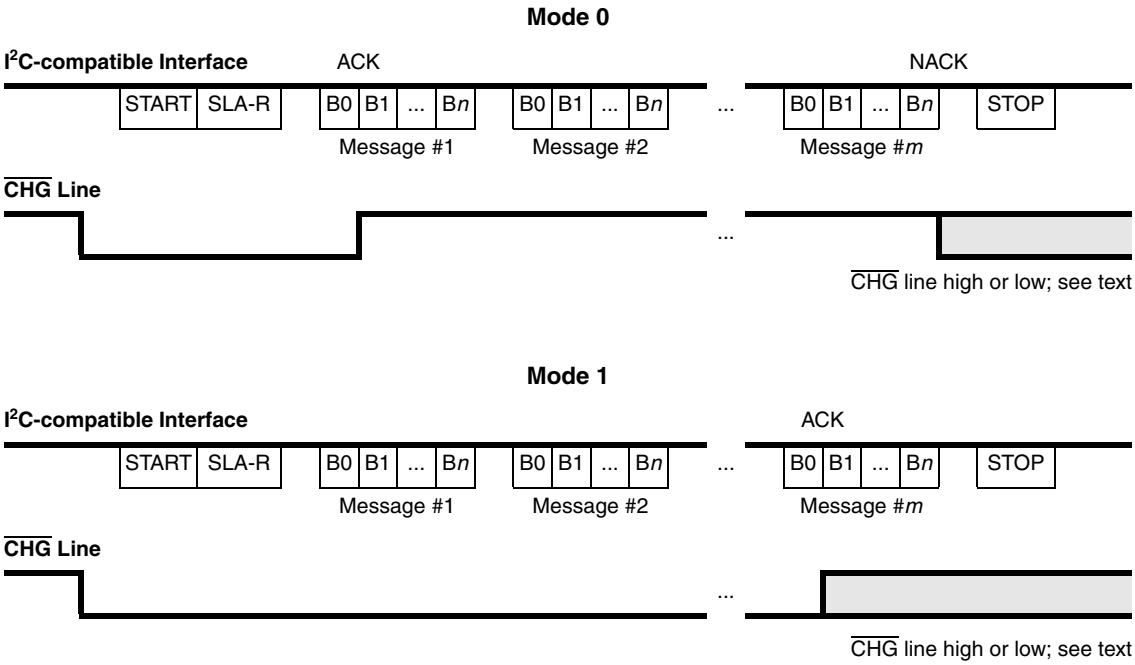
The $\overline{\text{CHG}}$ line remains low as long as there are messages to be read. The host should be configured so that the $\overline{\text{CHG}}$ line is connected to an interrupt line that is level-triggered. The host should not use an edge-triggered interrupt as this means adding extra software precautions.

The $\overline{\text{CHG}}$ line should be allowed to float during normal usage. This is particularly important after power-up or reset (see Section 4.1 on page 18).

A pull-up resistor is required, typically 10 kΩ to Vdd.

The $\overline{\text{CHG}}$ line operates in two modes (see Figure 4-7), as defined by the Communications Configuration T18 object (refer to the *mXT224S Protocol Guide*).

Figure 4-7. $\overline{\text{CHG}}$ Line Modes for I²C-compatible Transfers



In Mode 0:

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line goes high when the first byte of the first message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the buffer.
3. The NACK at the end of an I²C-compatible read causes the $\overline{\text{CHG}}$ line to stay high if there are no more messages. Otherwise the $\overline{\text{CHG}}$ line goes low to indicate a further message.

Mode 0 allows the host to read the messages until a report ID of 255 (“invalid message”) is received. Alternatively, the host can send a NACK after receiving the last byte of any message and send a STOP condition to end the transfer. If and when there is another message present, the $\overline{\text{CHG}}$ line goes low, as in step 1. In this mode the state of the $\overline{\text{CHG}}$ line does not need to be checked during the I²C-compatible read.

In Mode 1:

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line remains low while there are further messages to be sent after the current message.
3. The $\overline{\text{CHG}}$ line goes high again only after the first byte of the last message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the output buffer.

Mode 1 allows the host to continually read the messages until the $\overline{\text{CHG}}$ line goes high, and the state of the $\overline{\text{CHG}}$ line determines whether or not the host should continue reading messages from the device.

Note: The state of the $\overline{\text{CHG}}$ line should be checked only between messages and not between the bytes of a message. The precise point at which the $\overline{\text{CHG}}$ line changes state cannot be predicted and so the state of the $\overline{\text{CHG}}$ line cannot be guaranteed between bytes.

4.4.8 SDA, SCL

The I^2C-compatible bus transmits data and clock with SDA and SCL respectively. These are open-drain. The I^2C-compatible master and slave devices can only drive these lines low or leave them open. The termination resistors (Rp) pull the line up to Vdd if no I^2C-compatible device is pulling it down.

The termination resistors commonly range from 1 kΩ to 10 kΩ. They should be chosen so that the rise times on SDA and SCL meet the I^2C-compatible specifications (see Section 6.8 on page 42).

4.4.9 Clock Stretching

The mXT224S supports clock stretching in accordance with the I^2C specification. It may also instigate a clock stretch if a communications event happens during a period when the mXT224S is busy internally. The maximum clock stretch is approximately 10 to 15 ms.

The mXT224S has an internal bus monitor that can reset the internal I^2C-compatible hardware if SDA or SCL is stuck low for more than 100 – 200 ms. This means that if a clock stretch of more than 200 ms is seen by the mXT224S, then any ongoing transfers with the mXT224S may be corrupted. The bus monitor is enabled or disabled using the Communications Configuration T18 object. Refer to the *mXT224S Protocol Guide* for more information.

4.5 Operational Modes

The device operates in two modes: active (touch detected) and idle (no touches detected). Both modes operate as a series of burst cycles. Each cycle consists of a short burst (during which measurements are taken) followed by an inactive sleep period. The difference between these modes is the length of the cycles. Those in idle mode typically have longer sleep periods. The cycle length is configured using the IDLEACQINT and ACTVACQINT settings in the Power Configuration T7 object. In addition, an Active to Idle timeout (ACTV2IDLETO) setting is provided.

Refer to the *mXT224S Protocol Guide* for full information on how these modes operate, and how to use the settings provided.

4.6 Touchscreen Sensor Layout

Although there are a total of 38 lines, arranged as a matrix of 24X × 14Y lines, only a maximum of 224 channels can be used. The matrix used can be made up of any combination of X and Y lines, subject to the maximum of 224 channels. For example, the matrix could be constructed evenly as 16X × 14Y (giving 224 channels) or as a longer, thinner matrix of 18X × 12Y (giving 216 channels). The arrangement chosen depends on the application.

4.7 Signal Processing

4.7.1 Detection Integrator

The device features a touch detection integration mechanism. This acts to confirm a detection in a robust fashion. A counter is incremented each time a touch has exceeded its threshold and has remained above the threshold for the current acquisition. When this counter reaches a preset limit the sensor is finally declared to be touched. If, on any acquisition, the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

The detection integrator is configured using the Multiple Touch Touchscreen T9, Key Array T15 and Proximity Sensor T23 object. They each have their own separate controls. Refer to the *mXT224S Protocol Guide* for more information. Also, refer to Application Note *QTAN0049*, *mXT224E Power and Speed Considerations*, for more discussion on the touch detection integration (TCHDI) setting.

4.7.2 Digital Filtering and Noise Suppression

The mXT224S supports on-chip filtering of the acquisition data received from the sensor. Specifically, the maXCharger T62 object provides an algorithm to suppress the effects of noise (for example, from a noisy charger plugged into the user's product). This algorithm can automatically adjust some of the acquisition parameters on-the-fly to filter the analog-to-digital conversions (ADCs) received from the sensor. The algorithm can make use of a Grass Cutter (which rejects any samples outside a predetermined limit).

Noise suppression is triggered when a noise source is detected (typically when a charger is turned on). A hardware trigger can be implemented using the CHRG_IN pin. Alternatively, the host's driver code can indicate when a noise source is present.

An alternative burst mode on the X lines, known as Dual X Drive, is provided. This improves the signal-to-noise ratio (SNR) on a closely spaced X sensor matrix (when finger touches are likely to cover more than one X line).

Refer to the *mXT224S Protocol Guide* Protocol Guide for more information on the maXCharger T62 object.

4.7.3 Shieldless Support

The mXT224S can support shieldless sensor design even with a noisy LCD. The SlimSensor T56 object provides a number of algorithms to suppress the effect of noise emitted by the display.

The T56 display noise suppression operates on a completely different mechanism to the maXCharger T62 object. This allows the device to overcome display noise simultaneously with charger noise.

The device can make use of different mechanisms to overcome display noise.

Optimal Integration; this is not filtering as such, instead it is a feature that enables the user to use a shorter integration window. The integration window optimizes the amount of charge collected against the amount of noise collected, to ensure an optimal SNR. This feature also benefits the system in the presence of an external noise source such as a charger.

The main noise suppression method for display noise is the noise canceller. The noise canceller measures the noise generated by the display and subtracts it from the noise cancellation feature measurement. When the noise canceller is enabled the maXCharger T62 object cannot use the Grass Cutter filter.

Refer to the *mXT224S Protocol Guide* Protocol Guide for more information on the SlimSensor T56 object.

4.7.4 Stylus Support

The mXT224S allows for the particular characteristics of stylus touches, whilst still allowing conventional finger touches to be detected. Stylus touches are configured by the Stylus T47 object.

For example, stylus support ensures that the small touch area of a stylus registers as a touch, as this would otherwise by considered too small for the touchscreen. Additionally, there are controls to distinguish a stylus touch from an unwanted approaching finger (such as on the hand holding the stylus).

The sensitivity controls for stylus touches are configured separately from those for conventional finger touches so that both types of touches can be accommodated.

4.7.5 Grip Suppression

The mXT224S has a grip suppression mechanism to suppress false detections when the user grips a handheld device.

Grip suppression works by specifying a boundary around a touchscreen, within which touches can be suppressed whilst still allowing touches in the center of the touchscreen. This ensures that a “rolling” hand touch (such as when a user grips a mobile device) is suppressed. A “real” (finger) touch towards the center of the screen is allowed.

Grip suppression is configured using the Grip Suppression T40 object. Refer to the *mXT224S Protocol Guide* for more information.

4.7.6 Unintentional Touch Suppression

The mXT224S has a mechanism to suppress false detections from unintentional touches from a large body area, such as from a face, ear or palm. Touch suppression is configured using the Touch Suppression T42 object. This object also provides Maximum Touch Suppression to suppress all touches if more than a specified number of touches have been detected. Refer to the *mXT224S Protocol Guide* for more information.

4.8 Circuit Components

4.8.1 X Line Power Supply

The X line driver power supply XVdd can be used in two different ways:

- XVdd connected to AVdd. This mode limits the range of XVdd to 2.5 – 3.6 V.
- XVdd in voltage doubler mode. In this mode an internal charge pump voltage doubler is used to drive XVdd to approximately 2 x AVdd whilst the X drivers are driving high. This mode gives the benefit of higher SNR without the need for a separate power supply.

4.8.2 Bypass Capacitors

For optimum performance the capacitors (ceramic X7R or X5R) in the schematics in Section 2.5.1 on page 10 to Section 2.5.4 on page 13) are recommended. It is possible to use a different number, depending on the product, but careful consideration must be given to the layout.

The PCB tracks connecting the capacitors to the pins of the device must not exceed 5 mm in length. This limits any stray inductance that would reduce filtering effectiveness. See also Section 6.10 on page 42.

4.8.3 PCB Cleanliness

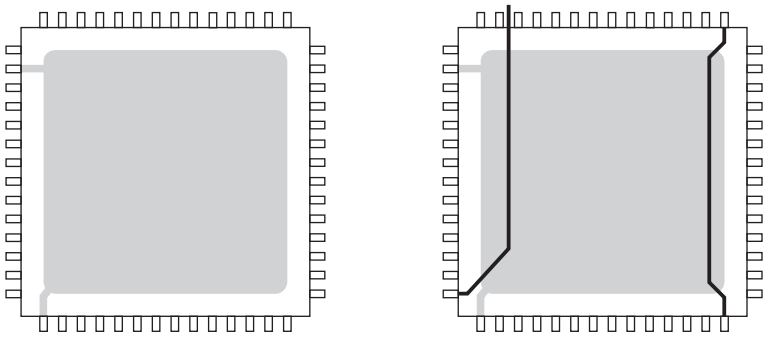
Modern no-clean flux is generally compatible with capacitive sensing circuits.

CAUTION: If a PCB is reworked to correct soldering faults relating to the mXT224S, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

4.8.4 UQFN Package Restrictions

The central pad on the underside of the UQFN chip should be connected to ground. Do not run any tracks underneath the body of the chip, only ground. Figure 4-8 shows an example of good/bad tracking.

Figure 4-8. Examples of Good and Bad Tracking



4.8.5 Supply Quality

The mXT224S has good Power Supply Rejection Ratio properties. Poorly regulated and/or noisy power can significantly reduce performance. See Section 6.10 on page 42.

Always operate the mXT224S with a well-regulated and clean AVdd supply. It supplies the sensitive analog stages in the chip.

There is no separate GND return pin for the analog stages. You are advised to consider return current paths from other current consumers in the system. Try to provide a separate heavy GND return trace or flood for the mXT224S that connects at a PSU star-point or connector pin. This helps to avoid inductive transient voltages coupling into the capacitive measurements made by the chip.

Vdd is used internally to power the digital stages in the chip and is far less critical to overall performance. It is still recommended, however, that a low noise supply is used to prevent cross-talk into the analog sections.

4.8.6 Supply Sequencing

Vdd and AVdd can be powered independently of each other without damage to the device. All voltages should be within the limits specified in Section 6.2 on page 34. See Section 4.1 on page 18 for additional information.

4.8.7 Oscillator

The device has an internal oscillator. No external oscillator or clock input is required.

4.9 Debugging

The mXT224S provides a mechanism for obtaining raw data for development and testing purposes by reading data from the Diagnostic Debug T37 object. Refer to the *mXT224S Protocol Guide* for more information on this object.

A second mechanism is provided that allows the host to read the real-time raw data using the low-level debug port. Refer to QTAN0050, *Using the maXTouch Debug Port*, for more information.

There is also a Self Test T25 object that runs self-test routines in the device to find hardware faults on the sense lines and the electrodes. Refer to the *mXT224S Protocol Guide* and QTAN0059, *Using the maXTouch Self Test Feature*, for more information.

4.10 Configuring the mXT224S

The mXT224S has an object-based protocol that organizes the features of the device into objects that can be controlled individually. This is configured using the Object Protocol common to many of Atmel's touch sensor devices. For more information on the Object Protocol and its implementation on the mXT224S, refer to the *mXT224S Protocol Guide*.

5. Getting Started With the mXT224S

5.1 Communication with the Host

The mXT224S uses an I²C-compatible bus to communicate with the host. See Section 4.4 on page 20 and Appendix E on page 58 for more information.

5.2 Establishing Contact

On power-up, the $\overline{\text{CHG}}$ line goes low to indicate that there is new data to be read from the Message Processor object. If the $\overline{\text{CHG}}$ line does not go low, there is a problem with the device.

The device runs an Initial Pin Fault Test on power-up to check that X lines aren't shorted to other X lines, Y lines, or ground. If there are any failures the device will communicate but not acquire or process any touch data. Refer to the Self Test T25 object in the *mXT224S Protocol Guide*.

The host should attempt to read any available messages to establish that the device is present and running following power-up or a reset. Examples of messages include reset or calibration messages. The host should also check that there are no configuration errors reported.

5.3 Using the Object Protocol

The mXT224S has an object-based protocol that is used to communicate with the device. Typical communication includes configuring the device, sending commands to the device and reading messages from the device. See Section 4.10 on page 30 and refer also to the *mXT224S Protocol Guide*.

The host must perform the following initialization so that it can communicate with the mXT224S:

1. Read the start positions and sizes of all the objects in the mXT224S from the Object Table and build up a list of these addresses.
2. Use the Object Table to calculate the report IDs so that messages from the device can be correctly interpreted.

5.4 Writing to the Device

See Section 4.4.3 on page 20 for information on the format of the I²C-compatible write operation.

To communicate with the mXT224S, write to the appropriate object:

- To send a command to the device, write the appropriate command to the Command Processor T6 object (for example, to send a reset, backup or calibrate command). Refer to the *mXT224S Protocol Guide* for the full list of available commands.
- To configure the device, write to an object. For example, to configure the device's power consumption write to the global Power Configuration T7 object. Some objects are optional and need to be enabled before use.

Refer to the *mXT224S Protocol Guide* for more information on the objects.

5.5 Reading from the Device

See Section 4.4.5 on page 21 for information on the format of the I²C-compatible read operation.

Status information is stored in the Message Processor T5 object. This object must be read to receive any status information from the mXT224S. The $\overline{\text{CHG}}$ line is asserted whenever a new message is available in the Message Processor object. This provides an interrupt-style interface. The host should always use the $\overline{\text{CHG}}$ line to be notified of messages. The host should not poll the device for messages. See Section 4.4.7 on page 24 for more information on using the $\overline{\text{CHG}}$ line.

5.6 Configuring the Device

The objects are designed so that a default value of zero in their fields is a safe value that typically disables functionality. The objects must be configured before use and the settings written to the nonvolatile memory using the Command Processor T6 object.

Perform the following actions for each object, where appropriate:

1. Enable the object, if the object requires it.
2. Configure the fields in the object, as required.
3. Enable reporting, if the object supports messages, to receive messages from the object.

Refer to the *mXT224S Protocol Guide* for more information.

The following objects are read-only and require no configuration:

- Debug Objects:
  - Diagnostic Debug T37
- General objects:
  - Message Processor T5
- Support objects:
  - User Data T38
  - Message Count T44

The following objects must be checked and configured as necessary:

- General objects:
  - Command Processor T6
  - Power Configuration T7
  - Acquisition Configuration T8
- Support objects:
  - Communications Configuration T18
  - CTE Configuration T46

The following objects must be enabled and configured before use:

- Touch objects:
  - Multiple Touch Touchscreen T9
  - Key Array T15
  - Proximity Sensor T23

- Signal processing objects:
  - Grip Suppression T40
  - Touch Suppression T42
  - Stylus T47
  - Adaptive Threshold T55
  - SlimSensor T56
  - Extra Touchscreen Data T57
  - maXCharger T62
- Support objects:
  - GPIO/PWM Configuration T19
  - Self Test T25
  - Timer T61 (two instances)

6. Specifications

6.1 Absolute Maximum Specifications

Vdd	3.6 V
AVdd	3.6 V
XVdd	7.2 V
Max continuous pin current, any control or drive pin	20 mA
Voltage forced onto any pin (except XVDD)	-0.5 V to (Vdd or AVdd) +0.5 V
Configuration parameters maximum writes	10,000

CAUTION: Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.

6.2 Recommended Operating Conditions

Operating temperature	-40°C to +85°C
Storage temperature	-65°C to +150°C
Vdd	1.8 V ±5%
AVdd	3.3 V ±5%
XVdd voltage doubler mode	6.6 V (2 x AVdd)
Vdd vs AVdd power sequencing	No sequencing required
Supply ripple + noise	See Section 6.10 on page 42
Cx transverse load capacitance per channel	0.32 pF to 5 pF
GPIO output current	<5 mA
Temperature slew rate	10°C per minute

6.3 DC Specifications

6.3.1 Digital Voltage Supply

Parameter	Description	Min	Typ	Max	Units	Notes
Vdd	Operating limits	1.71	–	3.47	V	
Rise time	Time for voltage to reach operating level	–	–	0.5	V/µs	No requirement for minimum rise rate.

6.3.2 Analog Voltage Supply

Parameter	Description	Min	Typ	Max	Units	Notes
AVdd	Operating limits	2.57	–	3.47	V	
Rise time	Time for voltage to reach operating level	–	–	0.5	V/µs	No requirement for minimum rise rate.

6.3.3 Input/Output Characteristics

Ta (ambient temperature) = recommended range, unless otherwise noted

Parameter	Description	Min	Typ	Max	Units	Notes
Input ($\overline{RESET}$, SDA, SCL, GPIO, ADDSEL)						
Vil	Low input logic level	-0.5	–	0.3 x Vdd	V	Vdd = 2.4 V to 3.3 V
Vil	Low input logic level	-0.5	–	0.2 x Vdd	V	Vdd = 1.8 V to 2.4 V
Vih	High input logic level	0.7 x Vdd	–	Vdd + 0.5	V	Vdd = 1.8 V to 3.3 V
Iil	Input leakage current	–	<0.001	1	µA	
Output ($\overline{CHG}$, GPIO)						
Vol	Low output voltage	–	–	0.2 x Vdd	V	Vdd = 1.8 V, I_{OL} = 5 mA
Vol	Low output voltage	–	–	0.2 x Vdd	V	Vdd = 3.0 V, I_{OL} = 10 mA
Vol	Low output voltage	–	–	0.2 x Vdd	V	Vdd = 3.3 V, I_{OL} = 15 mA
Voh	High output voltage	0.7 x Vdd	–	–	V	Vdd = 1.8 V, I_{OH} = 2.0 mA
Voh	High output voltage	0.7 x Vdd	–	–	V	Vdd = 3.0 V, I_{OH} = 6.0 mA
Voh	High output voltage	0.7 x Vdd	–	–	V	Vdd = 3.3 V, I_{OH} = 8.0 mA

6.4 Power Supply Voltage Modes

6.4.1 Analog Average Operating Current

AVdd = 3.3 V, IDLESYNCPERX = 8, ACTSYNCPERX = 16, T56 = On, T62 = Off

Condition	X Line Voltage Mode (XVdd)	Min	Typ	Max	Units
No Touches	Internal Voltage Doubler	0.08	1.6	13.2	mA
	Normal Voltage	0.09	1.6	13.0	mA
3 Touches	Internal Voltage Doubler	0.16	3.4	12.3	mA
	Normal Voltage	0.15	2.9	12.0	mA

6.4.2 Digital Average Operating Current

Vdd = 1.8 V, IDLESYNCPERX = 8, ACTSYNCPERX = 16, T56 = On, T62 = Off

Condition	X Line Voltage Mode (XVdd)	Min	Typ	Max	Units
No Touches	Internal Voltage Doubler	0.05	0.45	2.7	mA
	Normal Voltage	0.06	0.45	2.7	mA
3 Touches	Internal Voltage Doubler	0.13	2.0	3.2	mA
	Normal Voltage	0.12	1.8	2.8	mA

6.4.3 Deep Sleep

Vdd = 1.8 V, AVdd = 3.3 V, IDLESYNCPERX = 8, ACTSYNCPERX = 16, T56 = On, T62 = Off

Condition	X Line Voltage Mode (XVdd)	AVdd and XVdd	Vdd	Units
No Touches	Internal Voltage Doubler	<0.020	<0.020	mA
	Normal Voltage (3.3 V)	<0.020	<0.020	mA

6.5 ESD Information

1.5 kΩ, 100 pF, 3 pulses

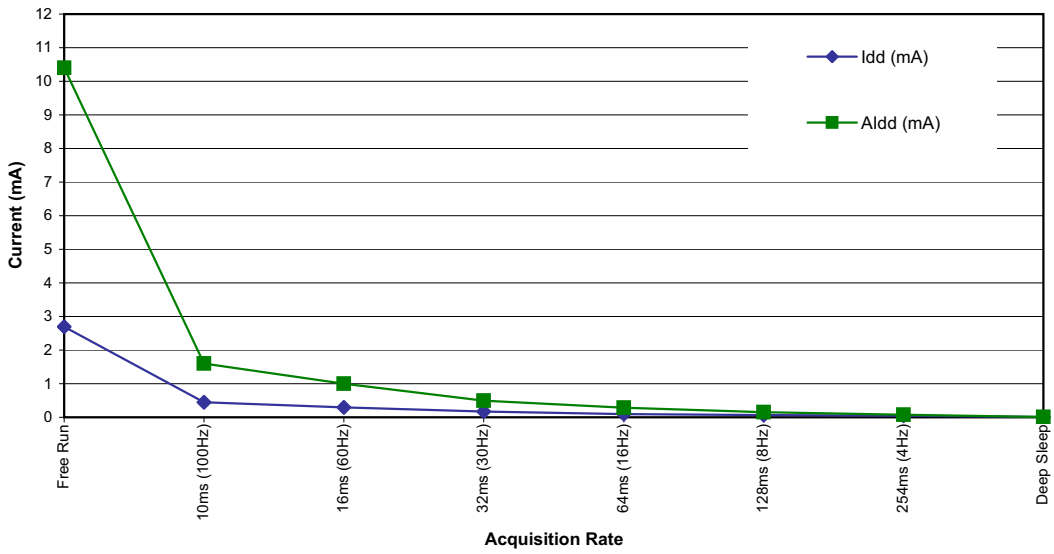
Parameter	Value	Reference Standard
Electrostatic Discharge Human Body Model (ESD HBM)	±2000 V	MIL– STD883 Method 3015.7
ESD Charge Device Model (ESD CDM)	±600 V	JEDEC-22A TEST METHOD C101-A

6.6 Power Consumption

6.6.1 Current Against Acquisition Interval

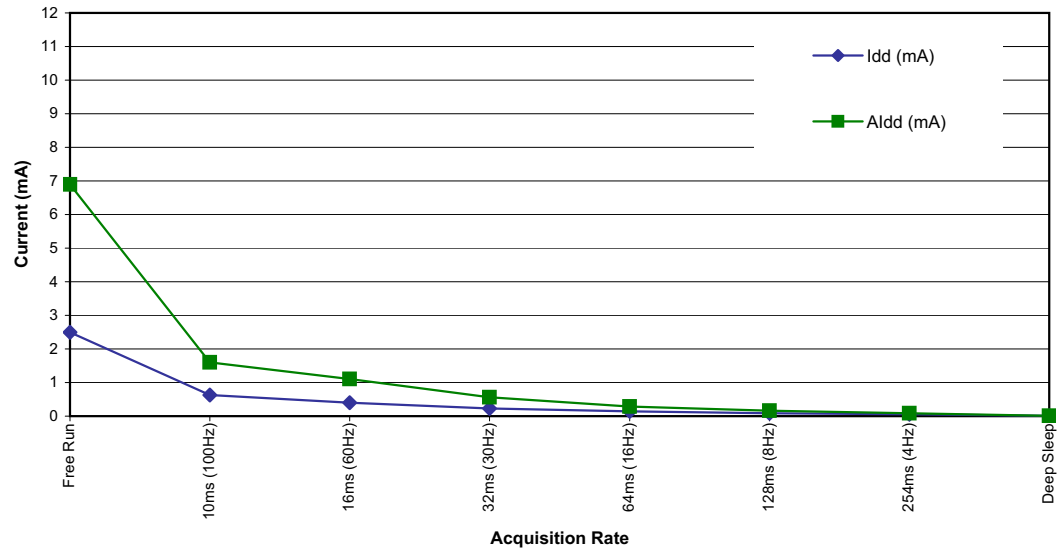
SlimSensor T56 Off, maXCharger T62 Off

I²C-compatible 1.8 V Vdd, 3.3 V AVdd Supply
XSIZE = 18, YSIZE = 12, CHRGTIME = 25, ACTVSYNCSPERX = 16, IDLESYNCSPERX = 8,
Number of Touches = 0



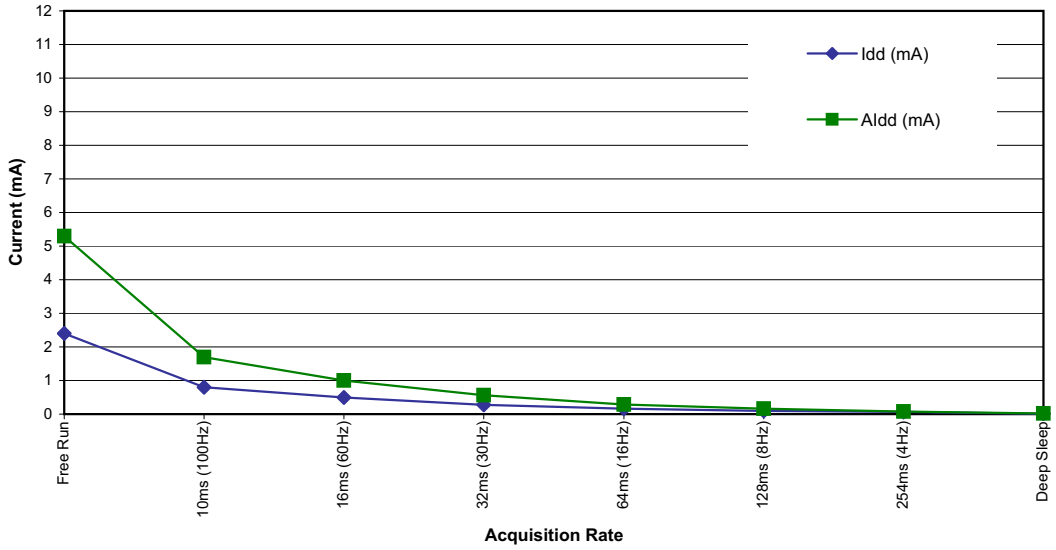
SlimSensor T56 Off, maXCharger T62 On

I²C-compatible 1.8 V Vdd, 3.3 V AVdd Supply
XSIZE = 18, YSIZE = 12, CHRGTIME = 25, ACTVSYNCSPERX = 16, IDLESYNCSPERX = 8,
Number of Touches = 0



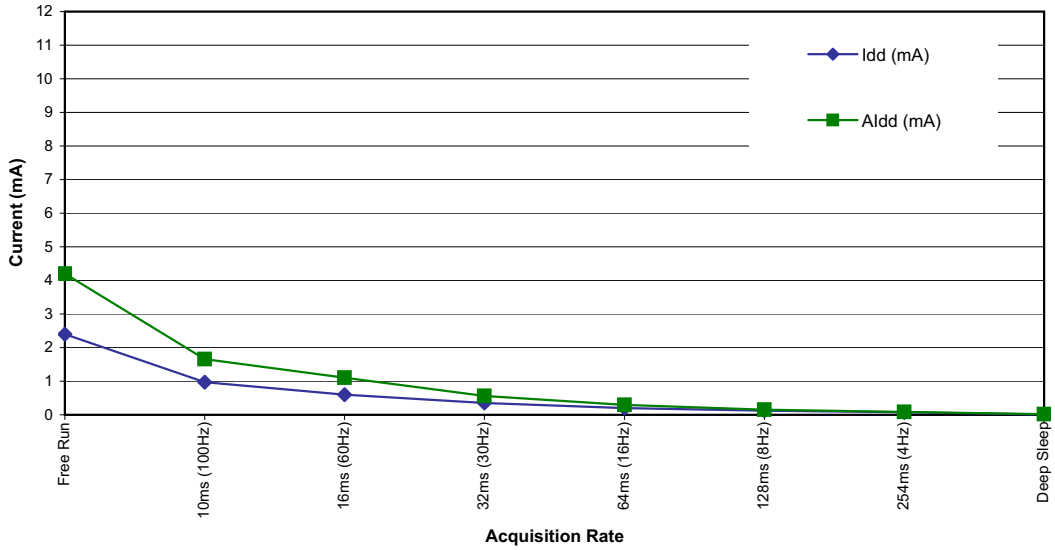
SlimSensor T56 On, maXCharger T62 Off

I²C-compatible 1.8 V Vdd, 3.3 V AVdd Supply
XSIZE = 18, YSIZE = 12, CHRGTIME = 25, ACTVSYNCSPERX = 16, IDLESYNCSPERX = 8,
Number of Touches = 0



SlimSensor T56 On, maXCharger T62 On

I²C-compatible 1.8 V Vdd, 3.3 V AVdd Supply
XSIZE = 18, YSIZE = 12, CHRGTIME = 25, ACTVSYNCSPERX = 16, IDLESYNCSPERX = 8,
Number of Touches = 0

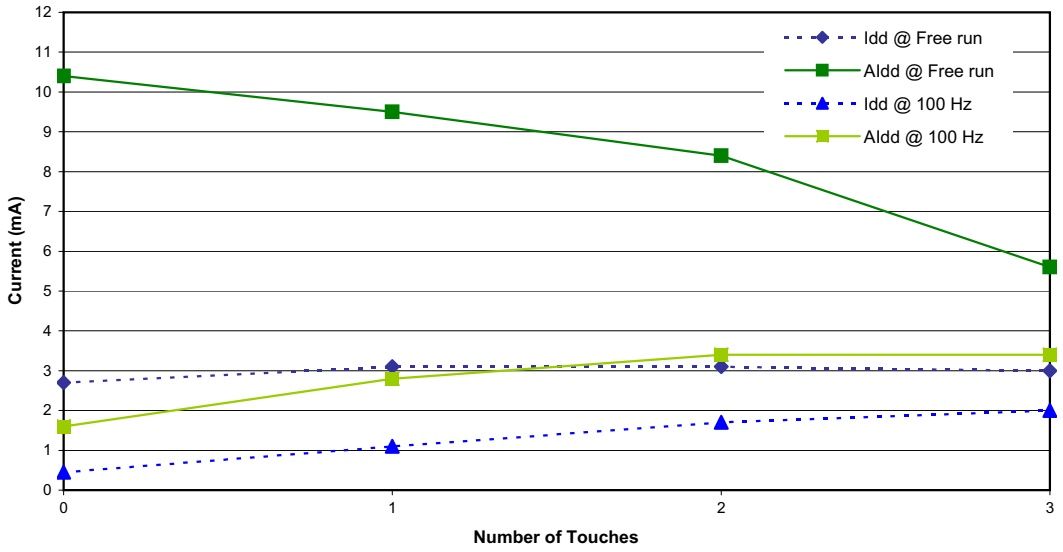


6.6.2 Current Against Number of Touches

SlimSensor T56 Off, maXCharger T62 Off

I²C-compatible 1.8 V Vdd, 3.3 V AVdd Supply

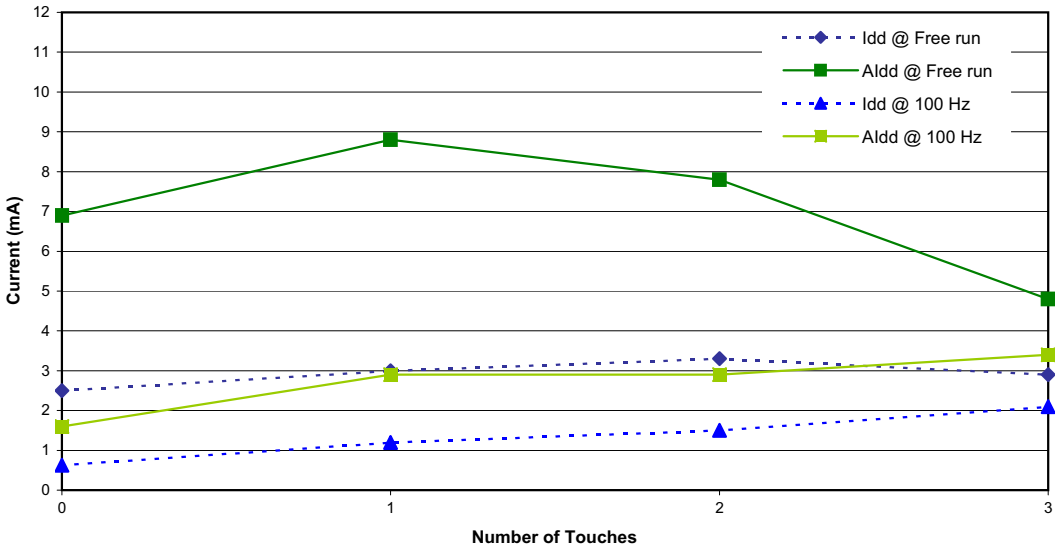
XSIZE = 18, YSIZE = 12, CHRGTIME = 25, ACTVSYNCSPERX = 16, IDLESYNCSPERX = 8



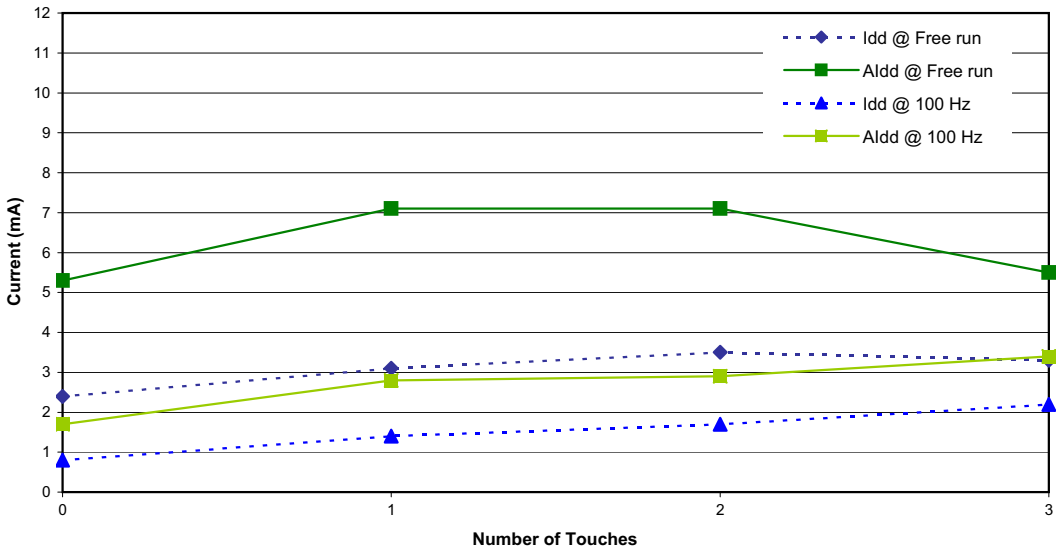
SlimSensor T56 Off, maXCharger T62 On

I²C-compatible 1.8 V Vdd, 3.3 V AVdd Supply

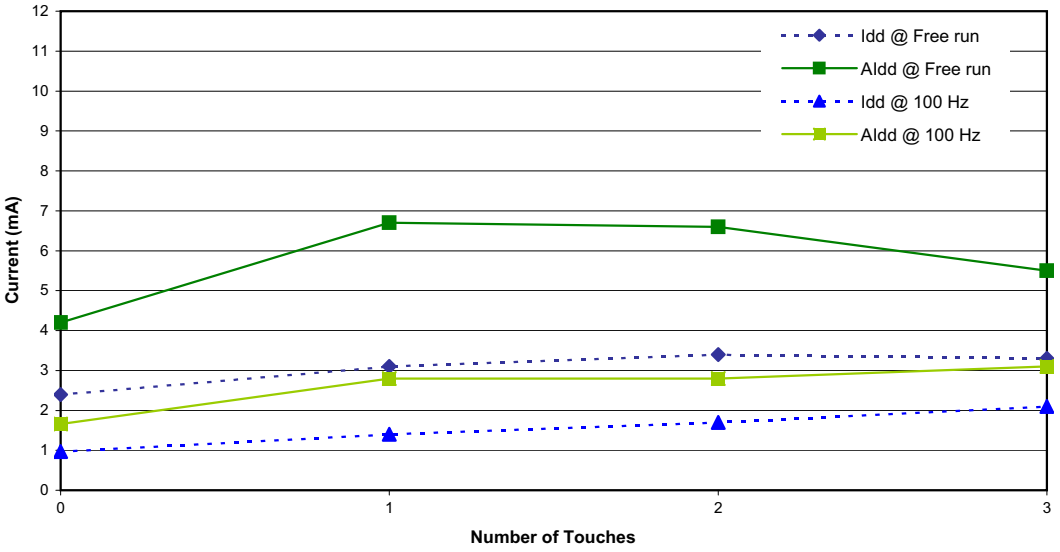
XSIZE = 18, YSIZE = 12, CHRGTIME = 25, ACTVSYNCSPERX = 16, IDLESYNCSPERX = 8



SlimSensor T56 On, maXCharger T62 Off
I²C-compatible 1.8 V Vdd, 3.3 V AVdd Supply
XSIZE = 18, YSIZE = 12, CHRGTIME = 25, ACTVSYNCSPERX = 16, IDLESYNCSPERX = 8,



SlimSensor T56 On, maXCharger T62 On
I²C-compatible 1.8 V Vdd, 3.3 V AVdd Supply
XSIZE = 18, YSIZE = 12, CHRGTIME = 25, ACTVSYNCSPERX = 16, IDLESYNCSPERX = 8,



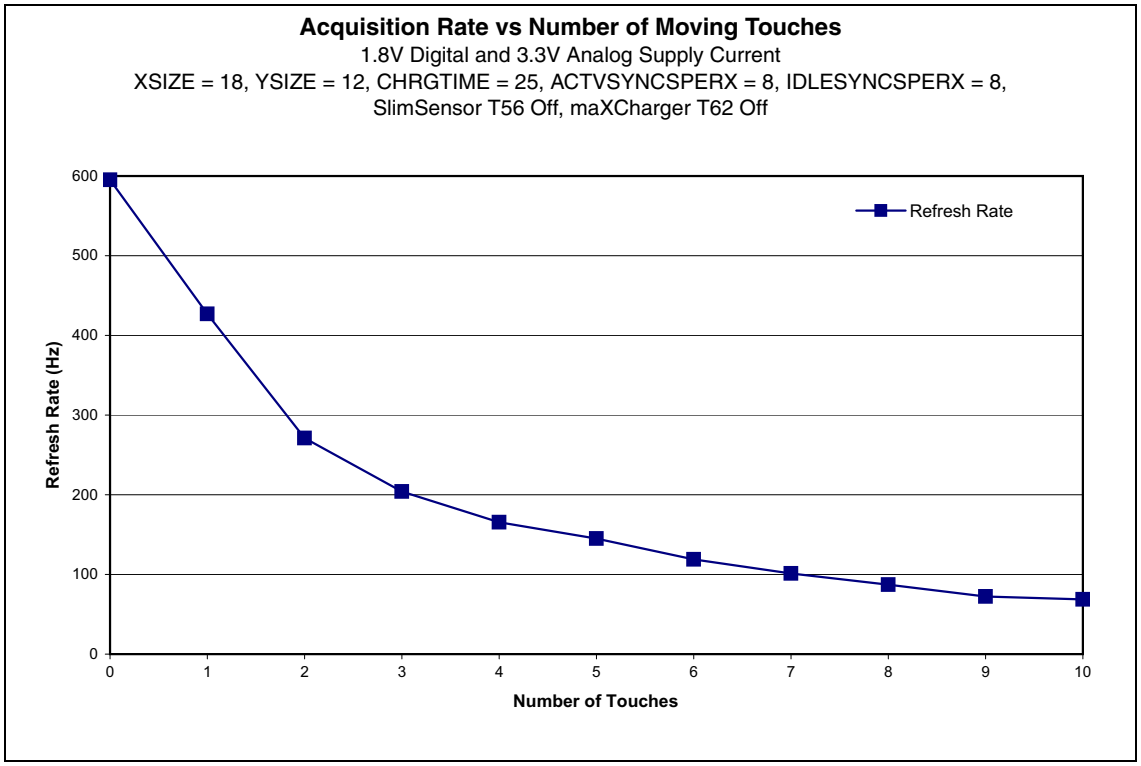
6.7 Timing Specifications

6.7.1 Touch Latency

XSIZE = 18, YSIZE = 12, CHRGTIME = 25, IDLESYNCPERX = ACTSYNCPERX = 8, TCHDI= 0, SlimSensor T56 = Off, maXCharger T62 = Off

Parameter	Description	Min	Max	Units	Notes
$T_{latency}$	80 Hz	6.5	19.8	ms	
	100 Hz	6.5	17.1	ms	
	200 Hz	6.5	13.1	ms	

6.7.2 Speed



6.7.3 Reset Timings

Parameter	Min	Typical	Max	Units	Notes
Power on		25		ms	
Hardware reset		25		ms	
Software reset		25		ms	

6.8 I²C-compatible Bus Specifications

Parameter	Operation
Addresses	0x4A, 0x4B
Maximum bus speed (SCL)	400 kHz
I²C specification	Version 2.1

6.9 Touch Accuracy and Repeatability

Touchscreen pitch= 4.7 mm, front panel = 1 mm, touch size = 8 mm

Parameter	Min	Typ	Max	Units	Notes
Linearity	–	±0.5	–	mm	
Accuracy	–	±1	–	mm	
Accuracy edge	–	±2	–	mm	
Repeatability	–	±0.25	–	%	X axis with 12-bit resolution

6.10 Power Supply Ripple and Noise

Parameter	Min	Typ	Max	Units	Notes
Vdd	–	–	±50	mV	Across frequency range 1Hz to 1 MHz
AVdd (maXCharger T62 disabled)	–	–	±25	mV	Across frequency range 1Hz to 1 MHz
AVdd (maXCharger T62 enabled)	–	–	±40	mV	Across frequency range 1Hz to 1 MHz

6.11 Thermal Considerations

6.11.1 Thermal Resistance Data

The thermal resistance data, depends on the package.

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	UQFN 56 6 × 6 mm	22.4	°C/W
θ_{JC}	Junction-to-case thermal resistance			5.2	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	UFBGA 64 5 × 5 mm	46.5	°C/W
θ_{JC}	Junction-to-case thermal resistance			7.3	

6.11.2 Junction Temperature

The average chip junction temperature, T_J in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA}= package thermal resistance, Junction to ambient (°C/W), provided in Section 6.11.1 on page 42.
- θ_{JC} = package thermal resistance, Junction to case thermal resistance (°C/W), provided in Section 6.11.1 on page 42.
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the cooling device datasheet.
- P_D = device power consumption (W) estimated from data provided in Section 6.5 on page 36.
- T_A is the ambient temperature (°C).

6.12 Soldering Profile

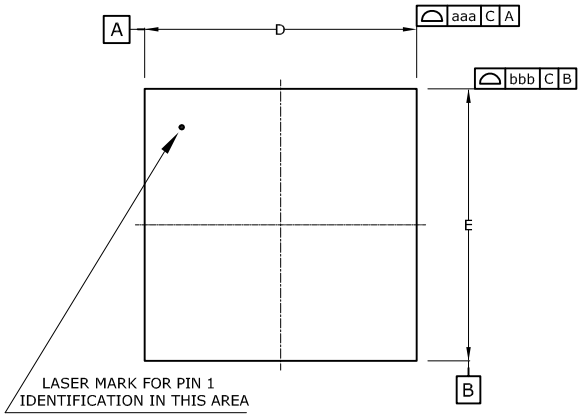
Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150 – 200°C
Time Maintained Above 217°C	60 – 150 s
Time within 5°C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

A maximum of three reflow passes is allowed per component.

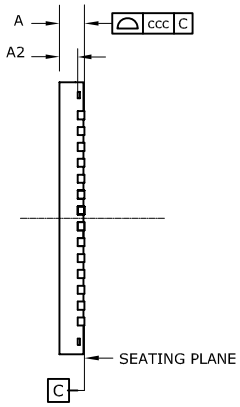
6.13 Mechanical Dimensions

6.13.1 56-pin UQFN

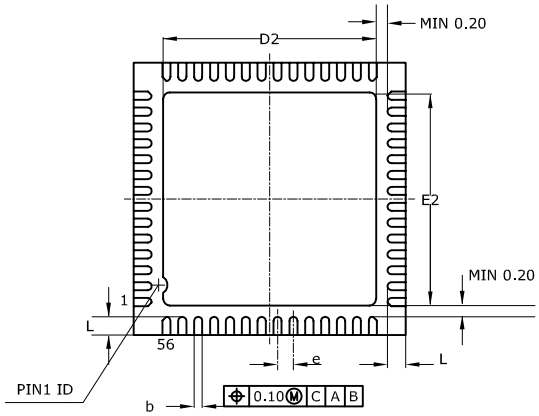
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

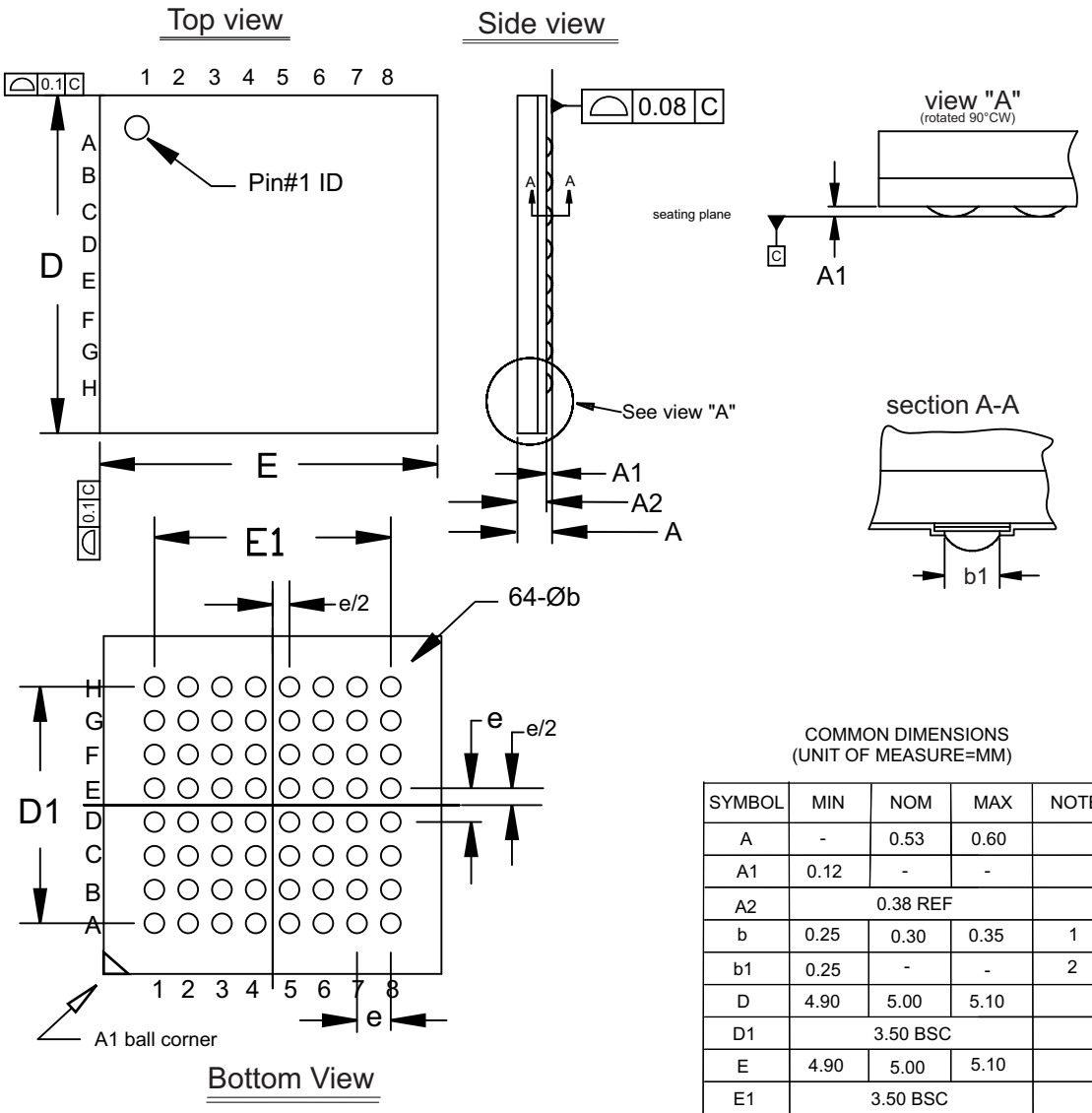
SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A2	-----	0.40	0.425	
D/E		6.00 bsc		
D2/E2	4.60	4.70	4.80	
L	0.35	0.40	0.45	
b	0.13	0.18	0.23	
e		0.35 bsc		
L/F Thickness		0.152 REF		
Stand Off		MAX 0.05		
TOLERANCES OF FORM AND POSITION				
aaa		0.05		
bbb		0.05		
ccc		0.05		

Notes : 1. This drawing is for general information only.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.

08/03/2011

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	P4, 56 Leads, 0.35mm pitch, 6 x 6 mm Ultra Thin Quad Flat No Lead Package (UQFN) Sawn	ZTG	P4	A

6.13.2 64-ball UFBGA



COMMON DIMENSIONS
(UNIT OF MEASURE=MM)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	0.53	0.60	
A1	0.12	-	-	
A2		0.38 REF		
b	0.25	0.30	0.35	1
b1	0.25	-	-	2
D	4.90	5.00	5.10	
D1		3.50 BSC		
E	4.90	5.00	5.10	
E1		3.50 BSC		
e		0.50BSC		

Note 1: Dimension "b" is measured at the maximum ball dia. in a plane parallel to seating plane.

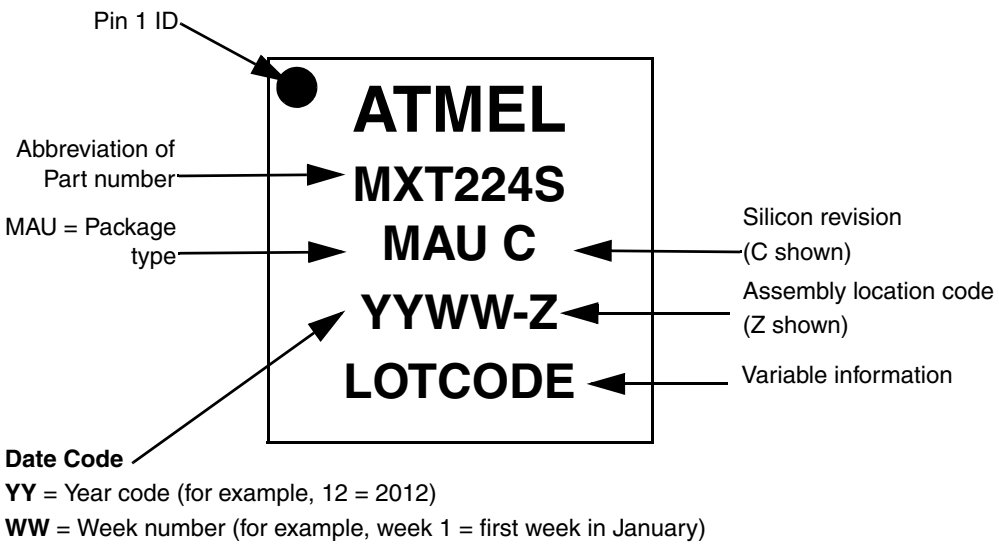
Note 2: Dimension "b1" is the solderable surface defined by the opening of the solder resist layer.

9/15/2011

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	64CC1, 64-ball, 5x5x0.6mm body,0.50mm ball pitch, (8 x 8 Array) Ultra-Thin, Fine-Pitch Ball Grid Array (UFBGA)	CAJ	64CC1	A

6.14 Part Marking

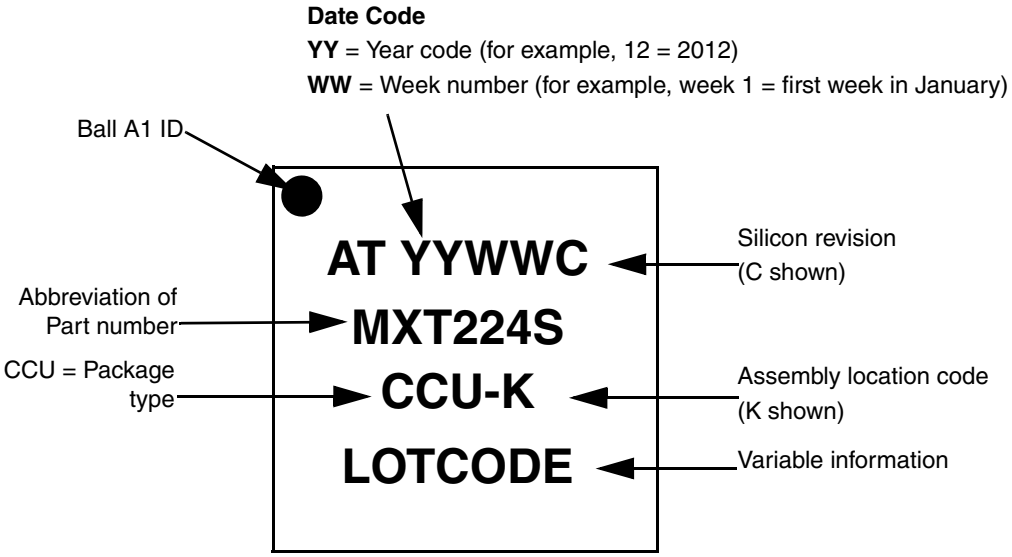
6.14.1 56-pin UQFN (ATMXT224S-MAUR)



YY = Year code (for example, 12 = 2012)

WW = Week number (for example, week 1 = first week in January)

6.14.2 64-ball UFBGA (ATMXT224S-CCUR)



6.15 Part Number

Part Number	QS Number	Description
ATMXT224S-MAUR (tape and reel)	QS636	56-pin UQFN 6 x 6 x 0.6 mm, 0.35 mm pitch, RoHS compliant
ATMXT224S-CCUR (tape and reel)	QS636	64-ball UFBGA 5 x 5 x 0.6 mm, 0.5 mm ball pitch RoHS compliant

6.16 Moisture Sensitivity Level (MSL)

Package Type	MSL Rating	Peak Body Temperature	Specifications
UQFN	MSL1	260°C	IPC/JEDEC J-STD-020
UFBGA	MSL3	260°C	IPC/JEDEC J-STD-020

Appendix A. PCB Design Considerations

A.1 Introduction

The following sections give the design considerations that should be adhered to when designing a PCB layout for use with the mXT224S. Of these, power supply and ground tracking considerations are the most critical.

By observing the following design rules, and with careful preparation for the PCB layout exercise, designers will be assured of a better chance of success and a correctly functioning product.

A.2 Printed Circuit Board

The number of layers in the printed circuit board (PCB) for mXT224S applications depends on a number of things. Different factors that can affect the decision are the type of chip, complexity of design and board architecture.

In some circumstances a four-layer PCB is recommended. This, together with a careful layout, will ensure that the board meets relevant EMC requirements for both noise radiation and susceptibility, as laid down by the various national and international standards agencies.

However, sometimes a two-layer board is the preferred option and this can be equally effective, depending on the other factors.

A.3 Supply Rails and Ground Tracking

Power supply and clock distribution are the most critical parts of any board layout. Because of this, it is advisable that these be completed before any other tracking is undertaken. After these, supply decoupling, analog signals and high speed digital signals should be addressed. Track widths for all signals, especially power rails, should be kept as wide as possible in order to reduce inductance.

The power and ground planes themselves can form a useful capacitor. Flood filling for either or both of these supply rails, therefore, should be used where possible. It is important to ensure that there are no floating copper areas remaining on the board: all such areas should be connected to the 0 V plane. The flood filling should be done on the outside layers of the board.

In applications where the USB bus supplies power to the board, care should be taken to ensure that suitable capacitive decoupling is provided close to the USB connector. The tracking to the on-board regulators should also be kept as short as possible.

It should also be remembered that the screen of the USB cable is not intended to be connected to the ground or 0 V supply of a remote device. It should either be left open circuit (being connected only at the host computer end) or decoupled with a suitable high voltage capacitor (typically 4.7 nF – 250 V) and a parallel resistor (typically 1 MΩ). Note that these components may not be required when the USB cabling is internal and permanently wired, and is routed away from the noisier parts of the system.

A.4 Digital and Analog Power Supply Decoupling

As a rule, a suitable decoupling capacitor should be placed on each and every supply pin on all digital devices. It is important that these capacitors are placed as close to the chip's supply pins as possible (less than 5 mm away). The ground connection of these capacitors should be tracked to 0 V by the shortest, heaviest traces possible.

Capacitors with a Type II dielectric, such as X5R or X7R and with a value of at least 100 nF, should be used for this purpose.

Note: When using the internal charge pump circuit of the mXT224S, no external capacitor should be connected to the XVDD pin.

In addition, at least one bulk tantalum decoupling capacitor, with a minimum value of 4.7 µF, should be placed on each power rail, close to where the supply enters the board.

Surface mounting capacitors are preferred to wire leaded types due to their lower ESR and ESL. It is often possible to fit these decoupling capacitors underneath and on the opposite side of the PCB to the digital ICs. This will provide the shortest tracking, and the most effective decoupling possible.

Refer to the Application Note *Selecting Decoupling Capacitors for Atmel's PLDs* (doc0484.pdf; available on Atmel's website) for further general information on decoupling capacitors.

A.5 Suggested Voltage Regulator Manufacturers

The AVdd supply stability is critical for the mXT224S because this supply interacts directly with the analog front end. Atmel therefore recommends that the supply for the analog section of the board be supplied by a regulator that is separate from the logic supply regulator. This reduces the amount of noise injected into the sensitive, low signal level parts of the design.

A low noise device should be chosen for the regulator. If possible this should have provision for adding a capacitor across the internal reference for further noise reduction. Reference should be made to the manufacturer's datasheet.

The voltage regulators listed in Table 6-1 have been tested and found to work well with the mXT224S. They have compatible footprints and pin-out specifications, and are available in the SOT23-5 package.

Table 6-1. Recommended Voltage Regulators

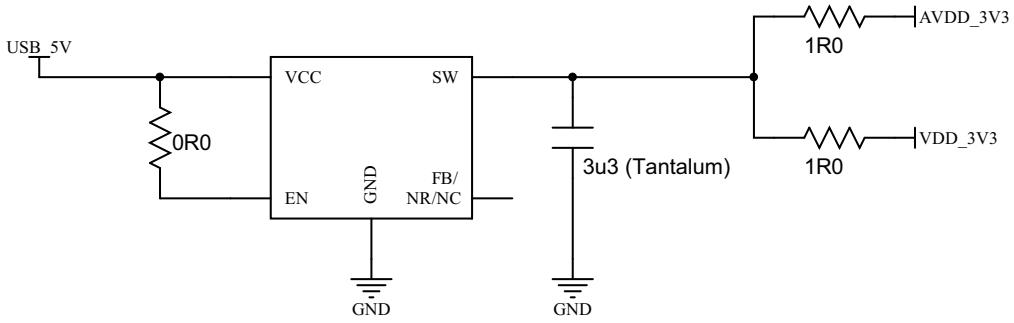
Manufacturer	Part Number
Linear Technology	LT1761
National Semiconductor	LP2981
TI/BB	REG102

Note that some manufacturers claim that minimal or no capacitance is required for correct regulator operation. However, in all cases, a minimum of a 1.0 µF ceramic, low ESR capacitor at the input and output of these devices should be used. The manufacturers' datasheets should always be referred to when selecting capacitors for these devices and the typical recommended values, types and dielectrics adhered to.

A.6 Using a Common Vdd/AVdd Supply

It is possible to use a single regulator for the Vdd and AVdd supplies if careful supply tracking is observed. The AVdd and Vdd supplies should each be sourced from the regulator by 1 Ω resistors. A Typical circuit is show in Figure 6-1.

Figure 6-1. Typical Circuit for AVdd and Vdd Common Supply



A.7 Analog I/O

In general, tracking for the analog I/O signals from the mXT224S device should be kept as short as possible. These normally go to a connector which interfaces directly to the touchscreen.

Ensure that adequate ground planes are used. An analog ground plane should be used in addition to a digital one. Care should be taken to ensure that both ground planes are kept separate and are connected together only at the point of entry for the power to the PCB. This is usually at the input connector.

A.8 Component Placement

It is important to orient all devices so that the tracking for important signals (such as power and clocks) are kept as short as possible. This simple point is often overlooked when initially planning a PCB layout and can save hours of work at a later stage.

A.9 Digital Signals

In general, when tracking digital signals, it is advisable to avoid sharp directional changes, sensitive signal tracks (such as analog I/O) and any clock or crystal tracking.

A good ground return path for all signals should be provided, where possible, to ensure that there are no discontinuities in the ground return path.

A.10 EMC and Other Observations

The following recommendations are not mandatory, but may help in situations where particularly difficult EMC or other problems are present:

- A small common mode choke is recommended on the differential USB data pair. This should be placed directly at the USB connector, between the connector and the relevant mXT224S pins. Tracking lengths for the USB data pair should be kept as short as possible.
- Try to keep as many signals as possible on the inside layers of the board. If suitable ground flood fills are used on the top and bottom layers, these will provide a good level of screening for noisy signals, both into and out of the PCB.

- Ensure that the on-board regulators have sufficient tracking around and underneath the devices to act as a heatsink. This heatsink will normally be connected to the 0 V or ground supply pin. Increasing the width of the copper tracking to any of the device pins will aid in removing heat. There should be no solder mask over the copper track underneath the body of the regulators.
- Ensure that the decoupling capacitors, especially tantalum, or high capacity ceramic types, have the requisite low ESR, ESL and good stability/temperature properties. Refer to the regulator manufacturer's datasheet for more information.

Appendix B. Reference Configuration

The values listed below are used in the reference unit to validate the interfaces and derive the characterization data provided in Section 6 on page 34.

The fields that are not listed have their values set to 0 (which is replaced by a default value). See *mXT224S Protocol Guide* for information about the individual objects and their fields.

The values for the user's application will depend on the circumstances of that particular project and will vary from those listed here. Further tuning will be required to achieve an optimal performance..

Field	Value
Power Configuration T7 – GEN_POWERCONFIG_T7 (Instance 0)	
IDLEACQINT	255
ACTVACQINT	255
ACTV2IDLETO	50
CFG	3
Acquisition Configuration T8 – GEN_ACQUISITIONCONFIG_T8 (Instance 0)	
CHRGTIME	25
TCHDRIFT	20
DRIFTST	20
ATCHCALST	50
Multiple Touch Touchscreen T9 – TOUCH_MULTITOUCHSCREEN_T9 (Instance 0)	
CTRL	143
XSIZE	18
YSIZE	12
BLEN	128
TCHTHR	50
TCHDI	1
ORIENT	4
MOVHYSTI	50
NUMTOUCH	10
MRGHYST	10
MRGTHR	10
AMPHYST	10
TCHHYST	10
XPITCH	50
YPITCH	50
CTE Configuration T46 – SPT_CTECONFIG_T46 (Instance 0)	
IDLESYNCSPERX	8
ACTVSYNCSPERX	16

Field	Value
XSLEW	3
XVOLTAGE	1
SlimSensor T56 – PROCI_SHIELDLESS_T56 (Instance 0)	
CTRL	3
OPTINT	1
INTTIME	24
INTDELAY[0]	5
INTDELAY[1]	5
INTDELAY[2]	5
INTDELAY[3]	5
INTDELAY[4]	5
INTDELAY[5]	5
INTDELAY[6]	5
INTDELAY[7]	5
INTDELAY[8]	5
INTDELAY[9]	5
INTDELAY[10]	5
INTDELAY[11]	5
INTDELAY[12]	5
INTDELAY[13]	5
INTDELAY[14]	5
INTDELAY[15]	5
INTDELAY[16]	5
INTDELAY[17]	5
MULTICUTGC	1
GCLIMIT	60
NCNCL	1
TOUCHBIAS	2
BASESCALE	6
SHIFTLIMIT	5
maXCharger T62 – PROCG_NOISESUPPRESSION_T62 (Instance 0)	
CTRL	3
CALCFG1	6
FREQ[1]	4
FREQ[2]	15
FREQ[3]	27
FREQ[4]	42

Field	Value
HOPCNT	5
HOPCNTPER	10
HOPEVALTO	5
HOPST	5
NLGAIN	128
MINNLTHR	30
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Appendix C. Glossary of Terms

Channel

One of the capacitive measurement points at which the sensor controller can detect capacitive change.

Jitter

The peak-to-peak variance in the reported location for an axis when a fixed touch is applied. Typically jitter is random in nature and has a Gaussian [1] distribution, therefore measurement of peak-to-peak jitter must be conducted over some period of time, typically a few seconds. Jitter is typically measured as a percentage of the axis in question.

For example a 100 x 100 mm touchscreen that shows ±0.5 percent jitter in X and ±1 percent jitter in Y would show a peak deviation from the average reported coordinate of ±0.5 mm in X and ±1 mm in Y. Note that by defining the jitter relative to the average reported coordinate, the effects of linearity are ignored.

Linearity

The measurement of the peak-to-peak deviation of the reported touch coordinate in one axis relative to the absolute position of touch on that axis. This is often referred to as the nonlinearity. Nonlinearities in either X or Y axes manifest themselves as regions where the perceived touch motion along that axis (alone) is not reflected correctly in the reported coordinate giving the sense of moving too fast or too slow. Linearity is measured as a percentage of the axis in question.

For each axis, a plot of the true coordinate versus the reported coordinate should be a perfect straight line at 45°. A non linearity makes this plot deviate from this ideal line. It is possible to correct modest nonlinearities using on-chip linearization tables, but this correction trades linearity for resolution in regions where stronger corrections are needed (because there is a stretching or compressing effect to correct the nonlinearity, so altering the resolution in these regions). Linearity is typically measured using data that has been sufficiently filtered to remove the effects of jitter. For example, a 100 mm slider with a nonlinearity of ±1 percent reports a position that is, at most, 1 mm away in either direction from the true position.

Resolution

The measure of the smallest movement on a slider or touchscreen in an axis that causes a change in the reported coordinate for that axis. Resolution is normally expressed in bits and tends to refer to resolution across the whole axis in question. For example, a resolution of 10 bits can resolve a movement of 0.0977 mm on a slider 100 mm long. Jitter in the reported position degrades usable resolution.

Touchscreen

A two-dimensional arrangement of electrodes whose capacitance changes when touched, allowing the location of touch to be computed in both X and Y axes. The output from the XY computation is a pair of numbers, typically 12-bits each, ranging from 0 to 4095, representing the extents of the touchscreen active region.

1. Sometimes called Bell-shaped or Normal distribution.

Appendix D. QMatrix Primer

D.1 Acquisition Technique

QMatrix capacitive acquisition uses a series of pulses to deposit charge into a sampling capacitor, Cs. The pulses are driven on X lines from the controller. The rising edge of the pulse causes current to flow in the mutual capacitance, Cx, formed between the X line and a neighboring receiver electrode or Y line. While one X line is being pulsed, all others are grounded. This leads to excellent isolation of the particular mutual capacitances being measured [1], a feature that makes for good inherent touchscreen performance.

After a fixed number of pulses (known as the burst length) the sampling capacitor's voltage is measured to determine how much charge has accumulated. This charge is directly proportional to Cx and therefore changes if Cx [2] changes. The transmit-receive charge transfer process between the X lines and Y lines causes an electric field to form that loops from X to Y. The field itself emanates from X and terminates on Y. If the X and Y electrodes are fixed directly [3] to a dielectric material like plastic or glass, then this field tends to channel through the dielectric with very little leakage of the field out into free-space (that is, above the panel). Some proportion of the field does escape the surface of the dielectric, however, and so can be influenced during a touch.

When a finger is placed in close proximity (a few millimeters) or directly onto the dielectric's surface, some of this stray field and some of the field that would otherwise have propagated via the dielectric and terminated onto the Y electrode, is diverted into the finger and is conducted back to the controller chip via the human body rather than via the Y line.

This means that less charge is accumulated in Cs, and hence the terminal voltage present on Cs, after all the charge transfer pulses are complete, becomes less. In this way, the controller can measure changes in Cx during touch. This means that the measured capacitance Cx goes down during touch, because the coupled field is partly diverted by the touching object.

The spatial separation between the X and Y electrodes is significant to make the electric field to propagate well in relation to the thickness of the dielectric panel.

D.2 Moisture Resistance

A useful side effect of the QMatrix acquisition method is that placing a floating conductive element between the X and Y lines tends to increase the field coupling and so increases the capacitance Cx. This is the opposite change direction to normal touch, and so can be quite easily ignored or compensated for by the controller. An example of such floating conductive elements is the water droplets caused by condensation.

As a result, QMatrix-based touchscreens tend not to go into false detect when they are covered in small non-coalesced water droplets. Once the droplets start to merge, however, they can become large enough to bridge the field across to nearby ground return paths (for example, other X lines not currently driven, or ground paths in mechanical chassis components). When this happens, the screen's behavior can become erratic.

1. A common problem with other types of capacitive acquisition technique when used for touchscreens, is that this isolation is not so pronounced. This means that when touching one region of the screen, the capacitive signals also tend to change slightly in nearby channels too, causing small but often significant errors in the reported touch position.
2. To a first approximation.
3. Air gaps in front of QMatrix sensors massively reduce this field propagation and kill sensitivity. Normal optically clear adhesives work well to attach QMatrix touchscreens to their dielectric front panel.

There are some measures used in these controllers to help with this situation, but in general there comes a point where the screen is so contaminated by moisture that false detections become inevitable. It should also be noted that uniform condensation soon becomes non-uniform once a finger has spread it around. Finger grease renders the water highly conductive, making the situation worse overall.

In general, QMatrix has industry-leading moisture tolerance but there comes a point when even the best capacitive touchscreen suffers due to moisture on the dielectric surface.

D.3 Interference Sources

D.3.1 Power Supply

The device can tolerate short-term power supply fluctuations. If the power supply fluctuates slowly with temperature, the device tracks and compensate for these changes automatically with only minor changes in sensitivity. If the supply voltage drifts or shifts quickly, the drift compensation mechanism is not able to keep up, causing sensitivity anomalies or false detections.

The device itself uses the AVdd power supply as an analog reference, so the power should be very clean and come from a separate regulator. A standard inexpensive Low Dropout (LDO) type regulator should be used that is not also used to power other loads, such as LEDs, relays, or other high current devices. Load shifts on the output of the LDO can cause AVdd to fluctuate enough to cause false detection or sensitivity shifts. The digital Vdd supply is far more tolerant to noise.

Noise on AVdd can appear directly in the measurement results. Vdd should be checked to ensure that it stays within specification in terms of noise, across a whole range of product operating conditions.

Ceramic bypass capacitors on AVdd and Vdd, placed very close (<5 mm) to the chip are recommended. A capacitor of between 100 nF and 1 mF is recommended. The capacitor must be either an X7R or X5R dielectric capacitor.

D.3.2 Other Noise Sources

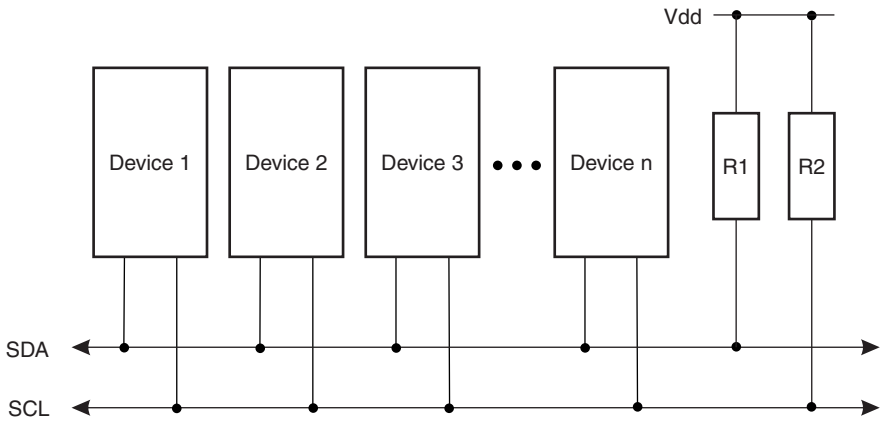
Refer to QTAN0079, *Buttons, Sliders and Wheels Sensor Design Guide*, for information (downloadable from the Touch Technology area of the Atmel website).

Appendix E. I²C-compatible Operation

E.1 Interface Bus

The device communicates with the host over an I²C-compatible bus. The following sections give an overview of the bus; more detailed information is available from www.i2C-bus.org. Devices are connected to the I²C-compatible bus as shown in Figure E-1. Both bus lines are connected to Vdd via pull-up resistors. The bus drivers of all I²C-compatible devices must be open-drain type. This implements a wired AND function that allows any and all devices to drive the bus, one at a time. A low level on the bus is generated when a device outputs a zero.

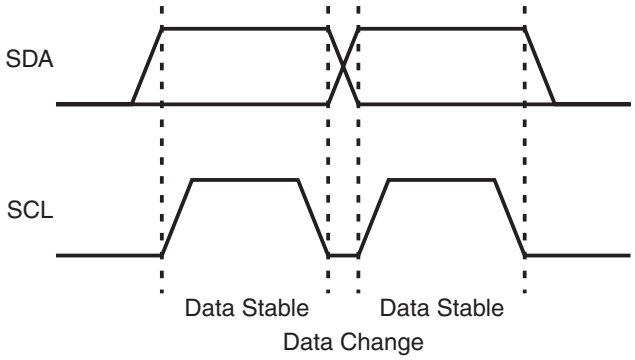
Figure E-1. I²C-compatible Interface Bus



E.2 Transferring Data Bits

Each data bit transferred on the bus is accompanied by a pulse on the clock line. The level of the data line must be stable when the clock line is high; the only exception to this rule is for generating START and STOP conditions.

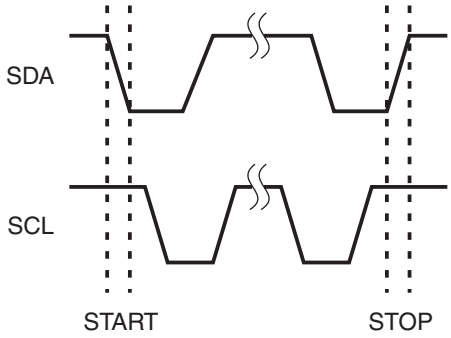
Figure E-2. Data Transfer



E.3 START and STOP Conditions

The host initiates and terminates a data transmission. The transmission is initiated when the host issues a START condition on the bus, and is terminated when the host issues a STOP condition. Between the START and STOP conditions, the bus is considered busy. As shown in Figure E-3, START and STOP conditions are signaled by changing the level of the SDA line when the SCL line is high.

Figure E-3. START and STOP Conditions

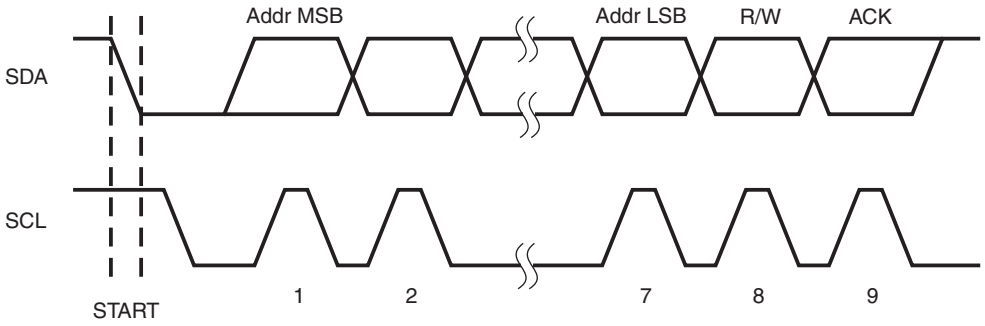


E.4 Address Byte Format

All address bytes are 9 bits long, consisting of 7 address bits, one READ/WRITE control bit and an acknowledge bit. If the READ/WRITE bit is set, a read operation is performed, otherwise a write operation is performed. When the device recognizes that it is being addressed, it will acknowledge by pulling SDA low in the ninth SCL (ACK) cycle. An address byte consisting of a slave address and a READ or a WRITE bit is called SLA+R or SLA+W, respectively.

The most significant bit of the address byte is transmitted first. The address sent by the host must be consistent with that selected with the option jumpers.

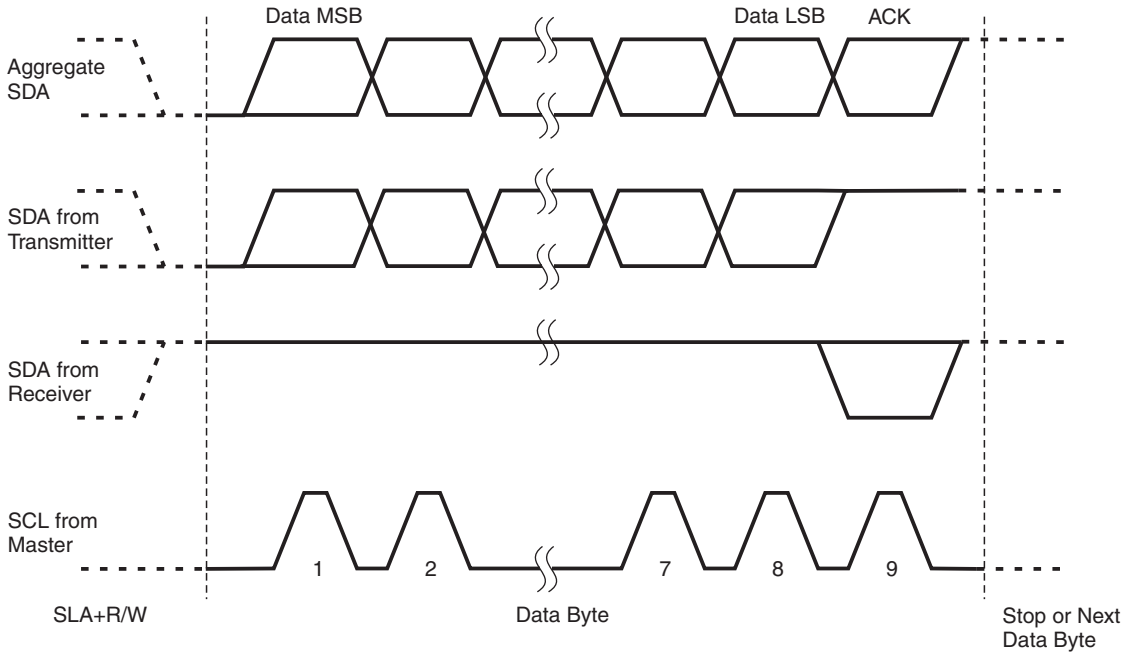
Figure E-4. Address Byte Format



E.5 Data Byte Format

All data bytes are 9 bits long, consisting of 8 data bits and an acknowledge bit. During a data transfer, the host generates the clock and the START and STOP conditions, while the receiver is responsible for acknowledging the reception. An acknowledge (ACK) is signaled by the receiver pulling the SDA line low during the ninth SCL cycle. If the receiver leaves the SDA line high, a NACK is signaled.

Figure E-5. Data Byte Format



E.6 Combining Address and Data Bytes into a Transmission

A transmission consists of a START condition, an SLA+R/W, one or more data bytes and a STOP condition. The wired “ANDing” of the SCL line is used to implement handshaking between the host and the device. The device extends the SCL low period by pulling the SCL line low whenever it needs extra time for processing between the data transmissions.

Note: Each write or read cycle must end with a stop condition. The device may not respond correctly if a cycle is terminated by a new start condition.

Figure E-6 shows a typical data transmission. Note that several data bytes can be transmitted between the SLA+R/W and the STOP.

Figure E-6. Byte Transmission

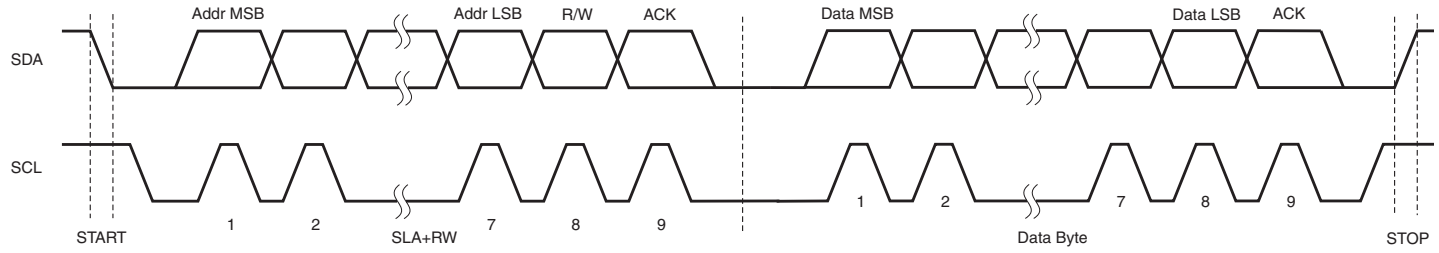


Table of Contents

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Revision Number	History
Revision AX – July 2012	Initial release for firmware revision 1.1

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