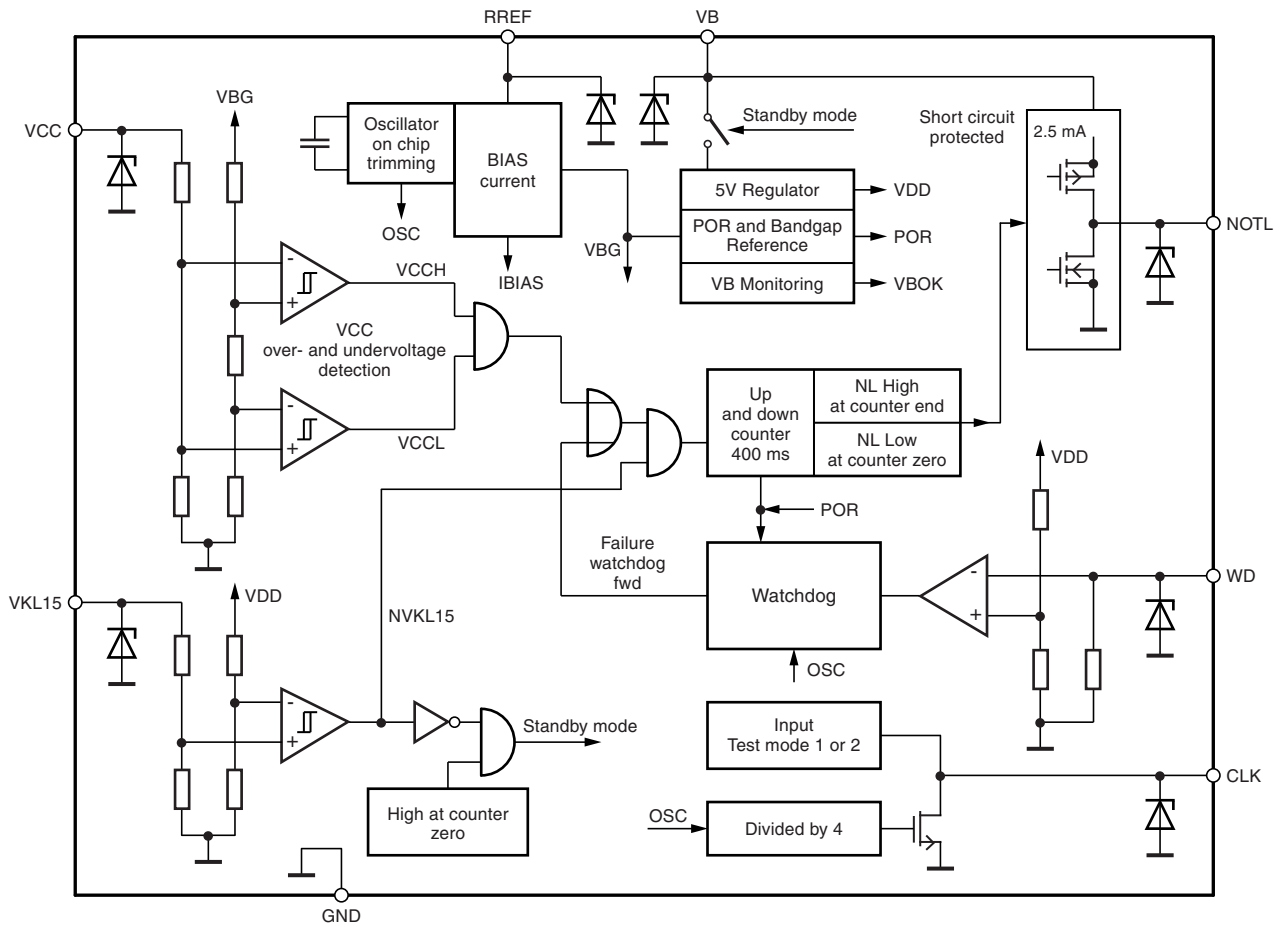


Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SO8

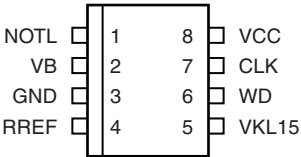


Table 2-1. Pin Description

Pin	Symbol	Function
1	NOTL	Push-pull output driver
2	VB	Voltage supply
3	GND	Ground
4	RREF	Reference voltage to adjust oscillator frequency via resistor Rset
5	VKL15	Input for standby modes on/of via ignition KL15
6	WD	Input for watchdog signal from microcontroller
7	CLK	Clock output signal, open drain
8	VCC	Input for monitoring 5V power supply

3. Functional Description

3.1 Voltage Supply

The IC can be supplied directly from V_{battery} . If the voltage at the VB pin is lower than the threshold of $V_{\text{VBlo}} = 5.76 \text{ V}$, the internal signal V_{BOK} is set to low. If V_{BOK} is low, the monitor function of the IC is completely disabled and the output NOTL is switched off in all cases (see [Figure 8-3 on page 11](#)).

If the voltage at pin VKL15 is low, the IC is in standby mode and reduces the current consumption at pin VB $< 100 \mu\text{A}$.

3.2 Oscillator

The frequency f_{CLK} of the internal oscillator is defined by the external resistor RSET and the internal capacitor. Thus, it is possible to vary the oscillator frequency between 4 kHz and 24 kHz.

3.3 VKL15 Monitoring

This input is used to monitor the battery voltage at ignition pin VKL15. If the voltage $V_{\text{KL15lo}} < 1.8\text{V}$, the internal signal NVKL15 is set to high (see [Figure 8-3 on page 11](#)). The IC switches to standby mode. During standby mode the monitor function is disabled and the output NOTL is switched off after the time delay t_{Delay} .

If the output NOTL is switched on and the voltage at VKL15 switches suddenly to low, the internal timer starts and switches the NOTL off after a time delay of $t_{\text{Delay}} = 400 \text{ ms}$.

3.4 VCC Over-/Undervoltage

Via the VCC input an external 5V voltage regulator is continuously monitored. If the voltage at pin VCC exceeds the voltage of $V_{\text{CC}_{\text{hon}}} > 6.3\text{V}$, the failure bit VCCH is set high. If the voltage at pin VCC decreases to a value below $V_{\text{CC}_{\text{lon}}} < 4\text{V}$, the internal failure bit VCCL will be set to high (see [Figure 8-1 on page 10](#)).

This failure bit starts the internal counter and switches the output NOTL on after the time delay of typically $t_{\text{Delay}} = 400 \text{ ms}$.

If the VCC voltage is inside the tolerance $V_{\text{CC}_{\text{loff}}} < V_{\text{VCC}} < V_{\text{CC}_{\text{hoff}}}$ the failure signal will be reset and the internal counter counts back to zero. After a time delay of typically $t_{\text{Delay}} = 400 \text{ ms}$, the output NOTL is switched off again.

3.5 Watchdog

A microcontroller can be monitored by a digital window watchdog which accepts an incoming trigger signal T_{WD} of a constant frequency at pin WD for correct operation. If the pulse width T_{WD} between two alternate edges exceeds the time window of $T_{\text{OWD}} > 8.9 \text{ ms}$ or if there is no watchdog signal, the failure signal fwd (failure watchdog) is set. In case the pulse width T_{WD} between two alternate edges falls below the time window of $T_{\text{UWD}} < 2.6 \text{ ms}$, the failure signal fwd (failure watchdog) is also set. With this fwd signal the internal up counter is activated and after a time delay of $t_{\text{Delay}} = 400 \text{ ms}$, the output NOTL is switched to high.

If NOTL is high, 16 successive correct watchdog signals T_{WD} within the pulse width of $T_{\text{UWD}} < T_{\text{WD}} < T_{\text{OWD}}$ are needed to create the internal signal nfwd (no failure watchdog) to start the down counter. After a time delay of $t_{\text{Delay}} = 400 \text{ ms}$, the output NOTL is switched to low (see [Figure 8-2 on page 10](#)).

3.6 Time Delay

The internal time delay is generated by an up/down counter. The clock for the counter is disabled if the voltage at the supply pin VB < 5.76V. In this case, the internal signal VBOK will be set to low and the output NOTL is directly switched to low.

The direction of counting is set by the watchdog or VCC over- and undervoltage detection. If the VCC monitoring detects an undervoltage condition, the failure signal VCCL (VCC low voltage) is set and starts the up counter. If the VCC monitoring detects an overvoltage condition, the failure signal VCCH (VCC high voltage) is set and starts the up counter.

A failure at the watchdog sets the internal fwd signal (failure watchdog) to high and starts the up counter. If the counter's final value is reached, a Flip Flop is set and switches the output NOTL to high. If no failure signal is set and the window watchdog has counted successive 16 alternate WDI edges then the down counter is started. If the counter reaches the zero value the Flip Flop receives a reset command and switches the output NOTL off.

The down counter is also started if the voltage at input VKL15 is low and switches the output NOTL after $t_{\text{Delay}} = 400 \text{ ms}$ to low (see [Figure 8-3 on page 11](#)).

3.7 Output NOTL

If the voltage at VKL15 is high and if a failure signal is set, the output NOTL switches to high after the internal time delay.

The output is short circuit protected with a current limitation of $ISC_{\text{NOTL}} = 15 \text{ mA}$.

The maximum output voltage is limited to $VC_{\text{NOTL}} = 22\text{V}$ (see [Figure 8-4 on page 11](#)).

3.8 Test Mode

The pin CLK is normally open or connected to GND. If the internal clock frequency is to be checked, the CLK pin has to be connected with an external resistor $R_{\text{ex}} = 5 \text{ k}\Omega$ to a 5V supply. The measured value is the clock frequency divided by four.

4. Truth Table

V_{VB}	V_{VCC}	WDI	VKL15	Mode
$V_{VB} < 5.76V$	Do not care	Do not care	Low	Standby, NOTL low
			High	NOTL low
$7.26V < V_{VB} < 17.5V$	$V_{VCC} < 4V$	Do not care	Low	Standby, NOTL low
			High	NOTL high
	$4.8V < V_{VCC} < 5.2V$	Do not care	Low	Standby, NOTL low
		No watchdog failure	High	NOTL low
		Watchdog failure	High	NOTL high
	$V_{VCC} > 6.3V$	Do not care	Low	Standby, NOTL low
	$V_{VCC} > 6.3V$		High	NOTL high
$22V < V_{VB} < 40V$	$V_{VCC} < 4V$	Do not care	Low	Standby, NOTL low
			High	NOTL high (maximum 22 V)
	$4.8V < V_{VCC} < 5.2V$	Do not care	Low	Standby, NOTL low
		No watchdog failure	High	NOTL low
		Watchdog failure	High	NOTL high (maximum 22 V)
	$V_{VCC} > 6.3V$	Do not care	Low	Standby, NOTL low
	$V_{VCC} > 6.3V$		High	NOTL high

5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_{VB}	-0.3	+40	V
Voltage at pins VCC, WD	V_{VCC}, V_{WDI}	-0.3	+30	V
Voltage at pins RREF, CLK	V_{RREF}, V_{CLK}	-0.5	+6	V
Voltage at pin NOTL	V_{NOTL}	-0.3	+22	V
Voltage at pin KL15 (in series with external resistor of 50 k Ω 1%)	V_{KL15}	-0.1	+40	V
Maximum current at pin VCC	I_{VCC}	-100	+0.1	mA
Maximum current at pin VB	I_{VB}	-10	+10	mA
Maximum current in pins CLK, RREF, VKL15, NOTL		-100	+100	mA
Maximum current at pin WD	I_{WD}	-1	+1	mA
ESD classification HBM ESD S.5.1	all pins	2000		V
ESD classification MM JEDEC A115A	all pins	200		V
Power dissipation	P_V		300	mW
Chip temperature	T_J	-40	+150	°C
Operating ambient temperature	T_{amb}	-40	+125	°C
Storage temperature	T_{Stg}	-55	+150	°C

6. Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance from junction to ambient	R_{thJA}	160	K/W

7. Electrical Characteristics

$V_{VB} = 7.2V$ to $17.5V$, $R_{KL15} = 50\text{ k}\Omega$ 1%, $R_{SET} = 22\text{ k}\Omega$ 1%, $T_{amb} = -40$ to $125^{\circ}C$, unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
0	Current Consumption and ESD Clamping								
0.1	Current consumption in normal mode	$V_{VKL15} > 4.5V$ $V_{VB} = 17.5V$ NOTL = high $I_{NOTL} = -2.5\text{ mA}$	2	I_{VB}			10	mA	A
0.2	Current consumption in standby mode	Standby: $V_{VKL15} < 1.8V$ $V_{VB} = 17.5V$ NOTL = low	2	I_{VBstby}			100	μA	A
0.3	Negative ESD clamping pin VB	to GND, $I_{VB} = -10\text{ mA}$	2	$V_{N_{VB}}$	-1.4		-0.3	V	A
0.4	Positive ESD clamping pin RREF	to GND, $I_{RREF} = 5\text{ mA}$	4	$V_{P_{RREF}}$	4		8	V	A
0.5	Positive ESD clamping pin CLK	to GND, $I_{CLK} = 20\text{ mA}$	7	$V_{P_{CLK}}$	6		10	V	A
0.6	Positive ESD clamping pin VB	to GND, $I_{VB} = 5\text{ mA}$	2	$V_{P_{VB}}$	41		65	V	A
0.7	Positive ESD clamping pin VKL15	to GND, $I_{VKL15} = 1.6\text{ mA}$	5	$V_{P_{VKL15}}$	41		65	V	A
0.8	Positive ESD clamping pin NOTL	to GND, $I_{NOTL} = 20\text{ mA}$	1	$V_{P_{NOTL}}$	31		55	V	A
0.9	Positive ESD clamping pin WD	to GND, $I_{WD} = 0.7\text{ mA}$	6	$V_{P_{WD}}$	35		55	V	A
0.10	Positive ESD clamping pin VCC	to GND, $I_{VCC} = 0.5\text{ mA}$	8	$V_{P_{VCC}}$	35		55	V	A
1	Reference Voltage								
1.1	Voltage at RREF		4	V_{RREF}	1.14	1.22	1.3	V	A
1.2	Possible values of resistor RREF		4	R_{RREF}	10	22	50	k Ω	A
2	Oscillator								
2.1	Oscillator frequency	$R_{SET} = 22\text{ k}\Omega \pm 1\%$ at pin CLK with pull-up-resistor to +5 V	7	f_{CLK}	9	10	11	kHz	A
2.2	Oscillator frequency is variable in a range	$R_{SE} = 10\text{ k}\Omega$ to $50\text{ k}\Omega \pm 1\%$	7	f_{CLK}	3.96		24.2	kHz	A
4	VB Monitoring								
4.1	High level threshold		2	V_{VBhi}	5.94		7.26	V	A
4.2	Low level threshold		2	V_{VBlo}	5.76		7.04	V	A
4.3	Hysteresis		2	V_{VBhys}	0.2			V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter



7. Electrical Characteristics (Continued)

$V_{VB} = 7.2V$ to $17.5V$, $R_{KL15} = 50\text{ k}\Omega \pm 1\%$, $R_{SET} = 22\text{ k}\Omega \pm 1\%$, $T_{amb} = -40$ to 125°C , unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5	VKL15 Monitoring								
5.1	Input resistor at VKL15		5	$R_{i_{KL15}}$	18		70	$\text{k}\Omega$	A
5.2	Low voltage threshold	$R_{KL15} = 50\text{ k}\Omega \pm 1\%$	5	$V_{KL15_{lo}}$	1.8			V	A
5.3	High voltage threshold	$R_{KL15} = 50\text{ k}\Omega \pm 1\%$	5	$V_{KL15_{hi}}$			4.5	V	A
5.4	Hysteresis		5	$V_{KL15_{hys}}$	0.2		1	V	A
6	VCC Monitoring								
6.1	Pull-down resistor to GND at pin VCC	$V_{VB} = 17.5V$ $V_{V_{KL15}} = 0V$ or $V_{V_{KL15}} = V_{VB}$ $V_{V_{CC}} = 5V$	8	$R_{pd_{VCC}}$	50		350	$\text{k}\Omega$	A
6.2	Undervoltage detection low level		8	$V_{CCI_{on}}$	4			V	A
6.3	Undervoltage detection high level		8	$V_{CCI_{off}}$			4.8	V	A
6.4	Overvoltage detection high level		8	$V_{CCI_{off}}$			6.3	V	A
6.5	Overvoltage detection low level		8	$V_{CC_{h_{off}}}$	5.2			V	A
6.6	Hysteresis of under- and overvoltage detection		8	$V_{CC_{hys}}$	0.2			V	A
9	Oscillator Test								
9.1	Pull-down-resistor	$CLK = \text{high}$, $V_{CLK} = 0V$ to $4.5V$	7	$R_{pd_{CLK}}$	6		15	$\text{k}\Omega$	A
9.2	Saturation voltage	$I_{CLK} = 1.6\text{ mA}$, $CLK = \text{low}$	7	$V_{s_{CLK}}$			0.4	V	A
9.3	Short current	$V_{CLK} = 5V$, $CLK = \text{low}$	7	$I_{sc_{CLK}}$			10	mA	A
10	Push-pull Output NOTL								
10.1	Saturation voltage NOTL switched off	$I_{NOTL} = 1.8\text{ mA}$ NOTL off	1	$V_{sat_{NOTL_{off}}}$			1	V	A
10.2	Short current NOTL if switched off	$V_{NOTL} = V_{VB}$ NOTL off	1	$I_{sc_{NOTL_{off}}}$			15	mA	A
10.3	Maximum output voltage NOTL	$17.5V < V_{VB} < 30V$ $I_{NOTL} = -2.5\text{ mA}$ NOTL on	1	$V_{NOTL_{max}}$	17.5		22	V	A
10.4	Saturation voltage NOTL switched on; guaranteed down to VB low level threshold	$V_{sat_{NOTL_{on}}} = V_{VB} - V_{NOTL}$ $V_{V_{KL15}} = V_{VB}$ $I_{NOTL} = -2.5\text{ mA}$ NOTL on	1	$V_{sat_{NOTL_{on}}}$			0.25	V	A
10.5	Short current NOTL if switched off	$V_{NOTL} = 0\text{ V}$ NOTL = on	1	$I_{sc_{NOTL_{on}}}$	-50			mA	A
10.7	Time delay of internal up and down counter		1	t_{Delay}	360	400	450	ms	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

7. Electrical Characteristics (Continued)

$V_{VB} = 7.2V$ to $17.5V$, $R_{KL15} = 50\text{ k}\Omega$ 1%, $R_{SET} = 22\text{ k}\Omega$ 1%, $T_{amb} = -40$ to 125°C , unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.8	Rise time at pin NOTL switch on	$C_{NOTL} \leq 200\text{ pF}$ V_{NOTL} from low = 10% to high = 90% V_{VB}	1	$t_{r_{NOTL}}$			5	μs	A
10.9	Fall time at pin NOTL switch off	$C_{NOTL} \leq 200\text{ pF}$ V_{NOTL} from high = 90% to low = 10% $V(VB)$	1	$t_{f_{NOTL}}$			5	μs	A
11	Watchdog								
11.1	Pull-down-resistor	$V_{VB} = V_{KL15} = 17.5V$	6	$R_{pd_{WD}}$	30		200	$\text{k}\Omega$	A
11.2	Voltage threshold low		6	$V_{low_{WD}}$	1			V	A
11.3	Voltage threshold high		6	$V_{high_{WD}}$			3.5	V	A
11.4	Hysteresis	$V_{hys_{WD}} = V_{high_{WD}} - V_{low_{WD}}$	6	$V_{hys_{WD}}$	0.5			V	A
11.5	Acceptable low WD pulse width for failure	Pulse = high or low $R_{SET} = 22\text{ k}\Omega \pm 1\%$	6	$T_{u_{WD}}$	2.6	3	3.3	ms	A
11.6	Acceptable high WD pulse width for failure	Pulse = high or low $R_{SET} = 22\text{ k}\Omega \pm 1\%$	6	$T_{o_{WD}}$	7.1	8	8.9	ms	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Diagrams

Figure 8-1. VCC Monitoring Diagram

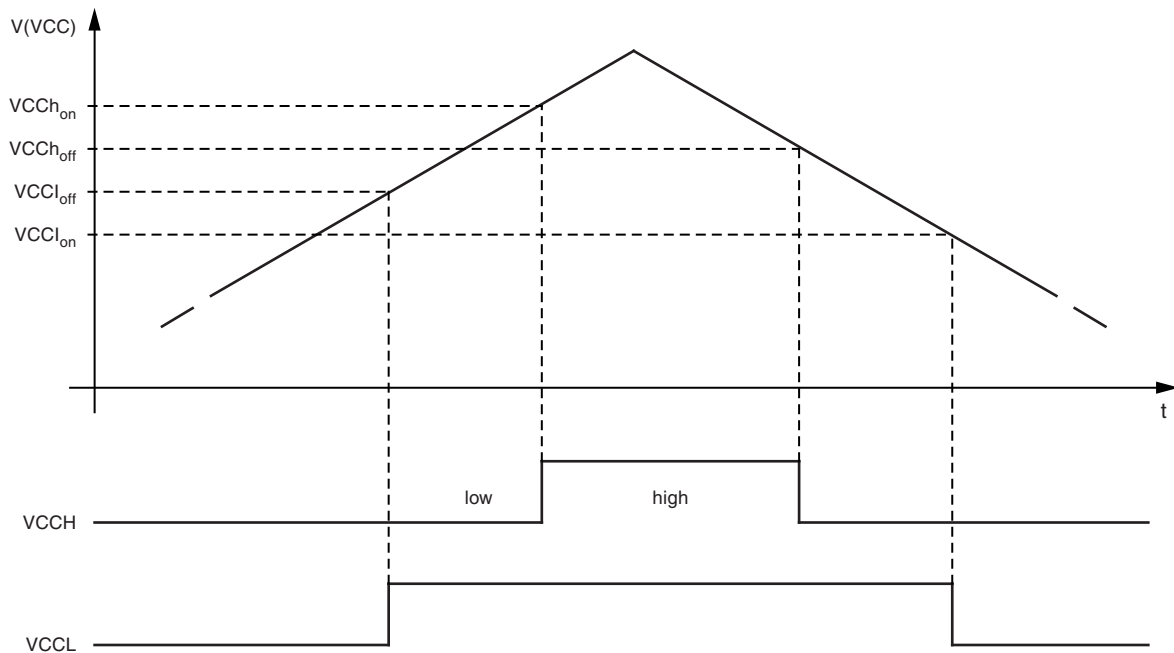


Figure 8-2. Watchdog Timing Diagram

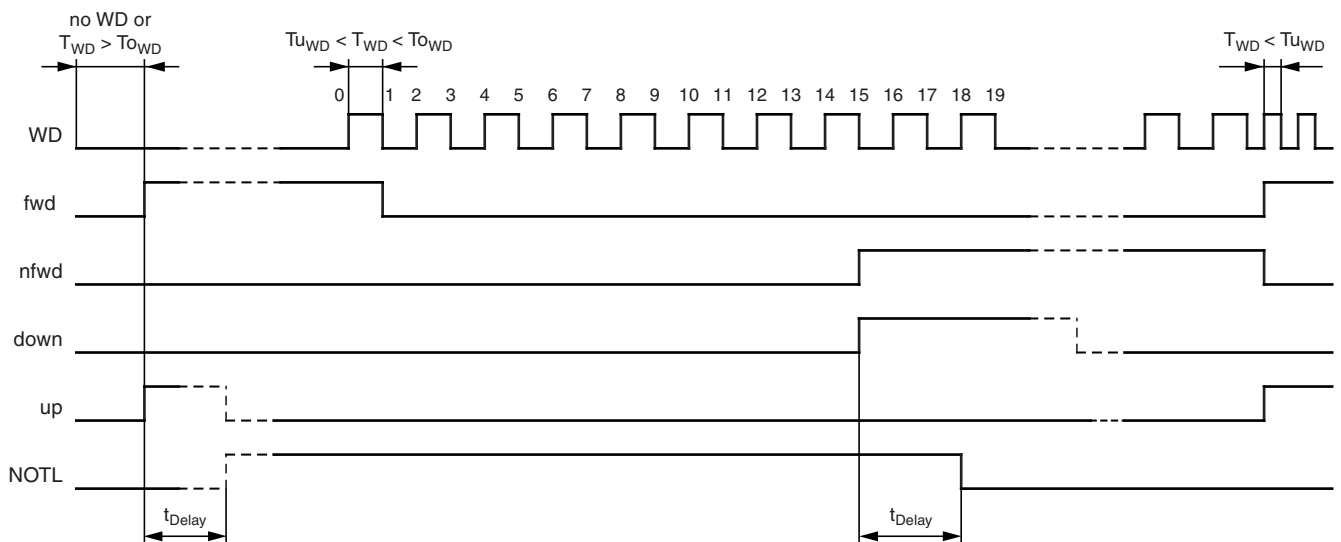


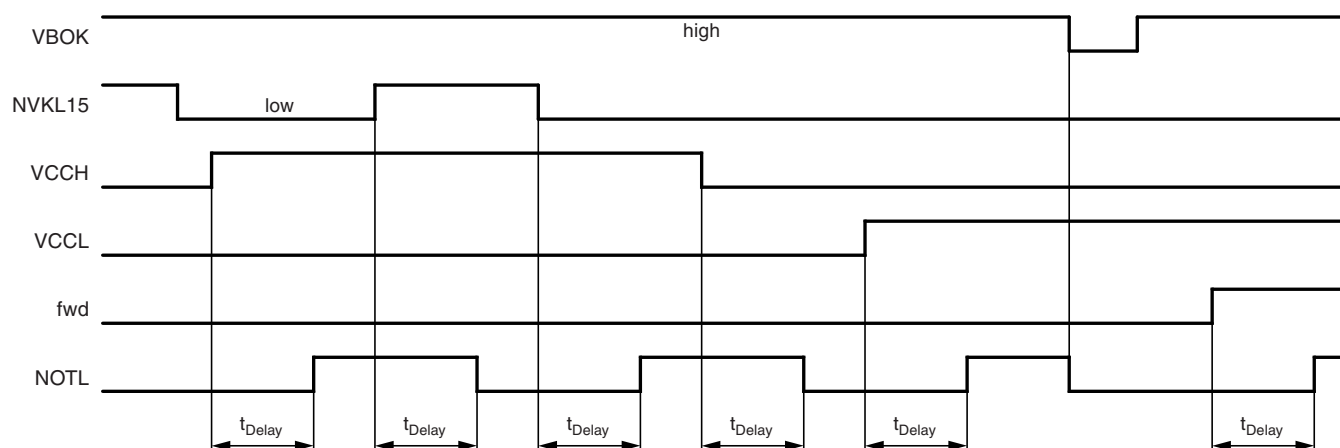
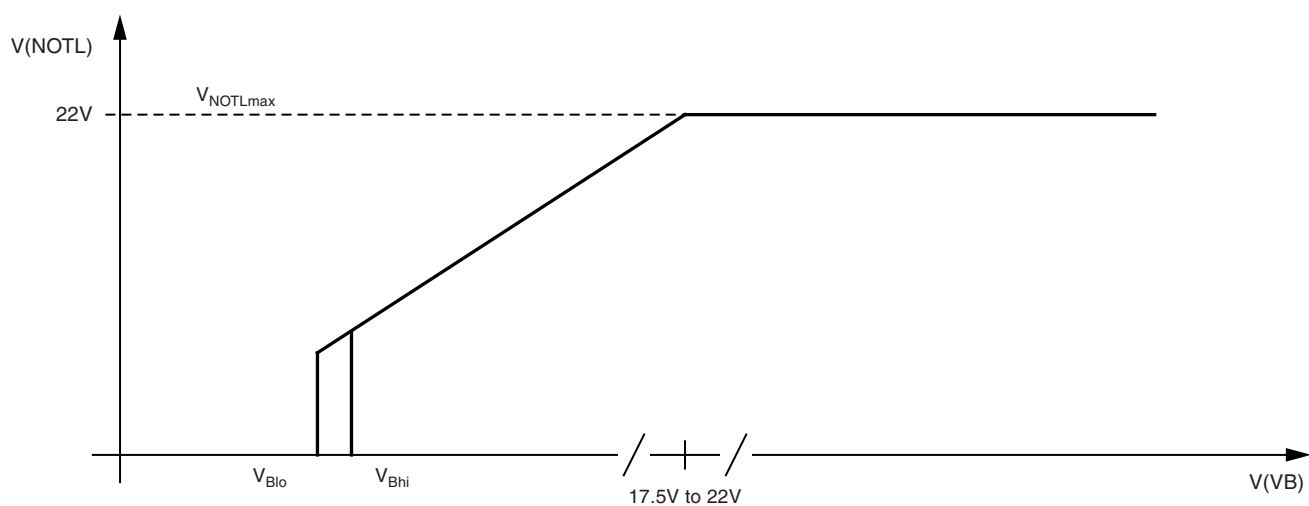
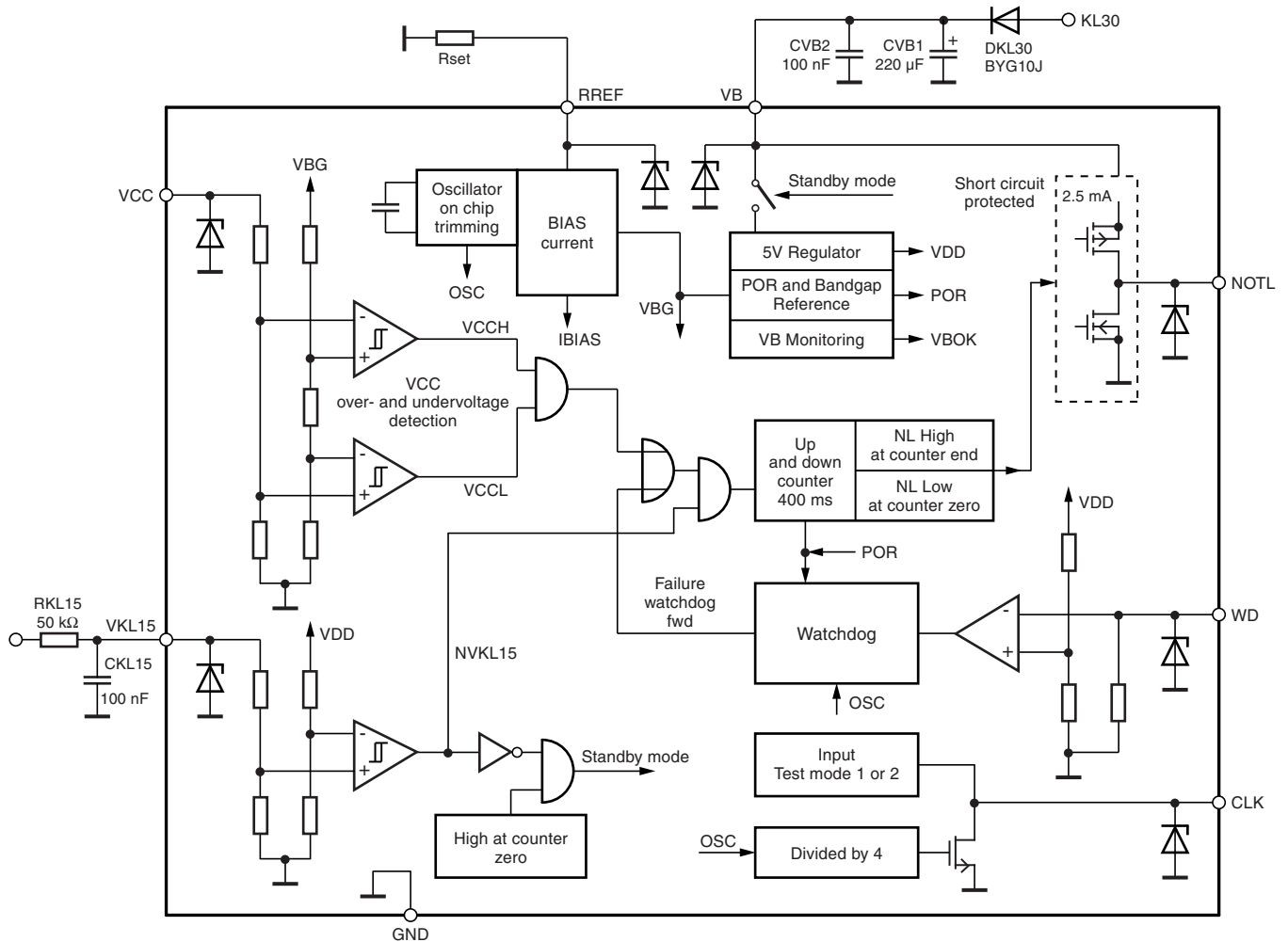
Figure 8-3. Time Delay Diagram**Figure 8-4.** Push-pull Output NOTL

Figure 8-5. Application Circuit



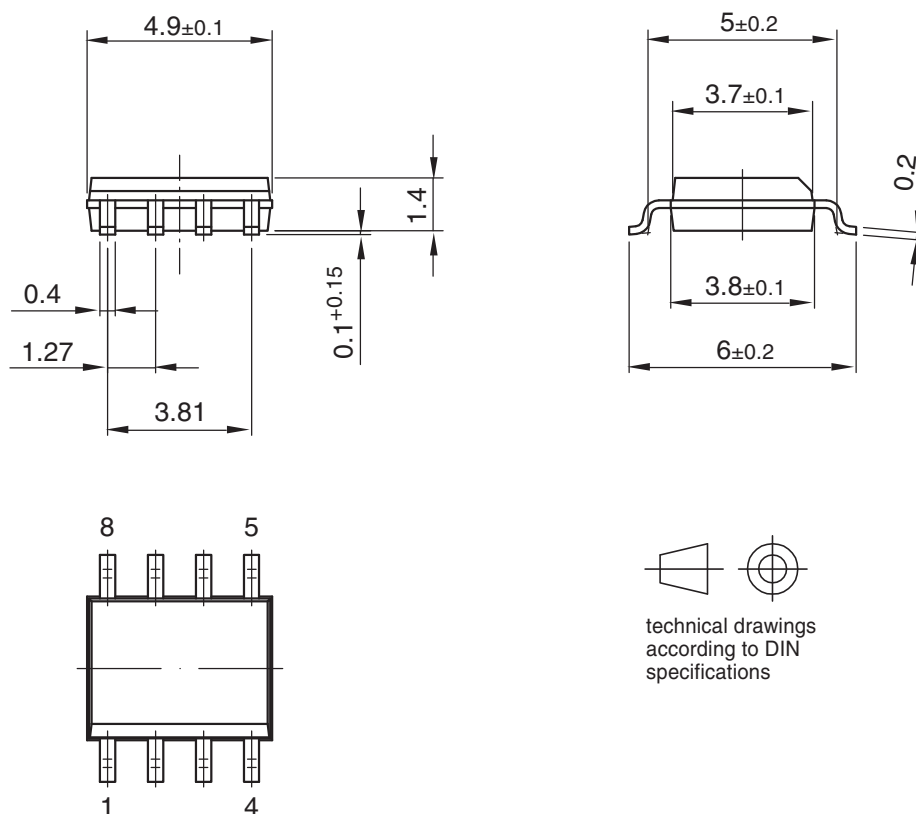
9. Ordering Information

Extended Type Number	Package	Remarks
ATA6025-TAQY	SO8	Taped and reeled, Pb-free

10. Package Information

Package: SO 8

Dimensions in mm



Drawing-No.: 6.541-5031.01-4

Issue: 1; 15.08.06

11. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4716C-AUTO-09/05	- Put datasheet in a new template - Pb-free logo on page 1 added - Heading rows on Table "Absolute Maximum Ratings" on page 6 added - Ordering Information on page 13 changed



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