Electrical Specifications

1. Small/Large -signal data measured in a fully de-embedded test fixture form TA = 25°C.
2. Pre-assembly into package performance verified 100% on-wafer.
3. This final package part performance is verified by a functional test correlated to actual performance at one or more frequencies.
4. Specifications are derived from measurements in a 50 Ω test environment. Aspects of the amplifier performance may be improved over a more narrow bandwidth by application of additional conjugate, linearity, or low noise (Γopt) matching.
5. All tested parameters guaranteed with measurement accuracy +/-1.5dB for Gain and P1dB +/-0.5 dB/ dBm for the 6 to 20 GHz, +/-0.75 dB/ dBm for the 20 to 33 GHz range and +/- 1.0dB/ dBm for the 33 to 50 GHz range

Table 1. RF Electrical Characteristics

TA = 25°C, Vd = 5V, Idq = 650mA, Zo = 50 Ω

	8 GHz			17 GHz				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Comment**
Operational Frequency, Freq	6					18	GHz	
Small Signal Gain, Gain	17.5	18		15.5	18		dB	
Output Power at 1dBGain Compression, P1dB	28	28.5		27	28.5		dBm	
Output Power at 3dBGain Compression, P3dB		29.5			29.5		dBm	
Output Third Order Intercept Point, OIP3; Δf = 100 MHz; Pin = -20 dBm		38			38		dBm	
Isolation, Iso		45			45		dB	
Input Return Loss, Rlin		3			3		dB	
Output Return Loss, RLout		9			9		dB	

Table 2. Recommended Operating Range

1. Ambient operational temperature TA = 25°C unless otherwise noted.
2. Channel-to-backside Thermal Resistance (Tchannel (Tc) = 34°C) as measured using infrared microscopy. Thermal Resistance at backside temperature (Tb) = 25°C calculated from measured data.

Description	Min.	Typical	Max.	Unit	Comments
Drain Supply Current, Id		650		mA	Vd = 3 V, Under any RF power drive and temperature
Drain Supply Voltage, Vd		-1.1		V	

Table 3. Thermal Properties

Parameter	Test Conditions	Value
Thermal Resistance (channel to baseplate), θjc		θjc = 20 °C/W
Maximum Power Dissipation	Tbaseplate = 85°C Pd = 3.5W Tch = 150°C	
Thermal Resistance (θjc)	Vd = 5V Id = 650mA Pd = 3.25W Tbaseplate = 75°C	θjc = 20°C/W Tch = 140°C
Thermal Resistance (θjc) Under RF Drive	Vd = 5V Id = 892mA Pout = 30dBm Pd = 3.47W Tbaseplate = 75°C	θjc = 20°C/W Tch = 145°C

Note:

1. Assume SnPb soldering to an evaluation RF board at 80°C base plate temperatures. Worst case for the channel temperature is under the quiescent operation. At saturated output power, DC power consumption rises to 4.26 W with 1.14 W RF power delivered to load. Power dissipation is 3.11 W and the temperature rise in the channel is 68.4°C. In this condition, the base plate temperature must be remained below 86.6°C to maintain maximum operating channel temperature below 155°C.

Absolute Minimum and Maximum Ratings

Table 4. Minimum and Maximum Ratings

Description	Min.	Max.	Unit	Comments
Drain to Ground Supply Voltage, Vd		6	V	
Gate Supply Voltage, Vg	-3	0.5	V	
Drain Current , Id		900	mA	
Power Dissipation, Pd		4.6	W	
RF CW Input Power, Pin		23	dBm	CW
Channel Temperature, Tch, max		+155	°C	
Storage Case Temperature, Tstg	-65	+155	°C	
Maximum Assembly Temperature, Tmax		260	°C	20 second maximum

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Dissipated power PD is in any combination of DC voltage, Drain Current, input power and power delivered to the load.
3. When operated at maximum PD with a base plate temperature of 85 C, the median time to failure (MTTF) is significantly reduced.
4. These ratings apply to each individual FET. The operating channel temperature will directly affect the device MTTF. For maximum life, it is recommended that junction temperatures (Tj) be maintained at the lowest possible levels. See MTTF vs. Tchannel Temperature Table.

Typical Performances

(Data Obtained from 3.5-mm Connector Based Test Fixture, and This Data is Including Connecter Loss, and Board Loss.)

(T_A = 25°C, V_d = 5 V, I_D = 650 mA, Z_{in} = Z_{out} = 50 Ω)

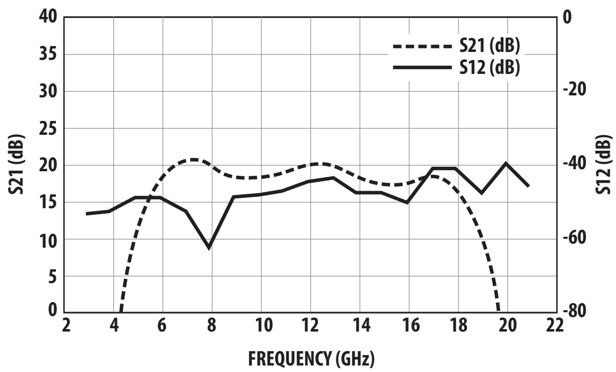


Figure 1. Typical gain and reverse isolation

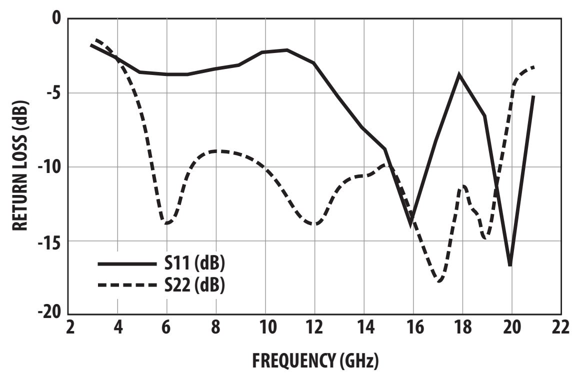


Figure 2. Typical return loss (input and output)

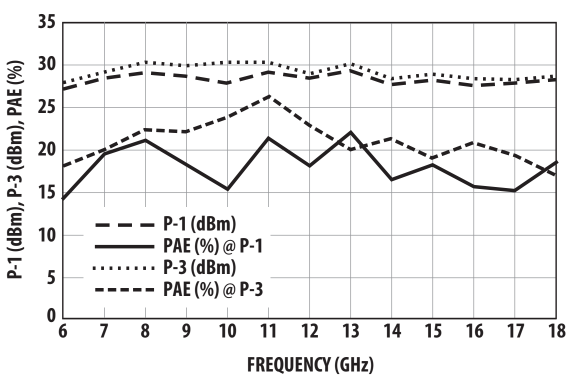


Figure 3. Typical output power (@P-1, P-3) and PAE and frequency

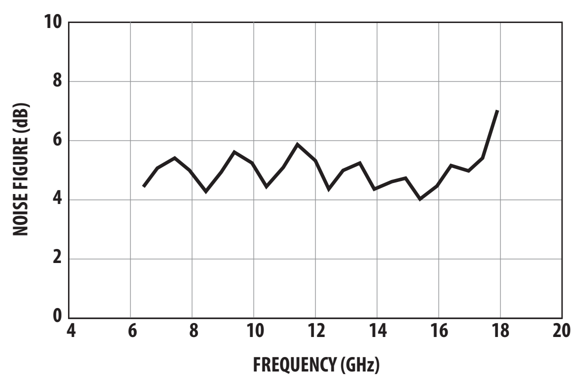


Figure 4. Typical noise figure

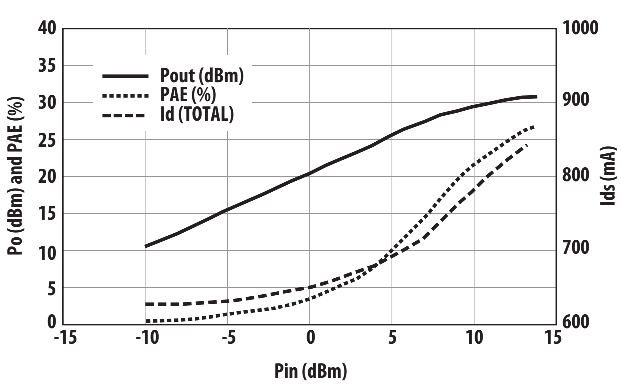


Figure 5. Typical output power, PAE, and total drain current versus input power at 8 GHz

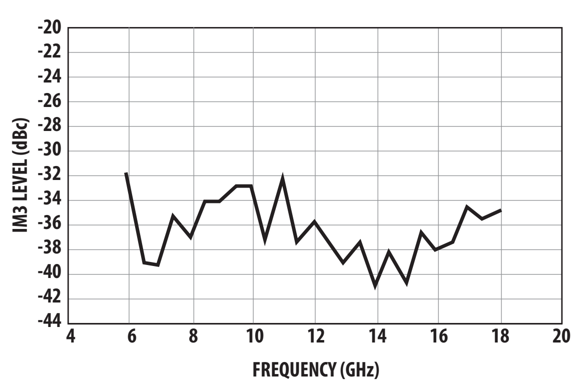


Figure 6. Typical IM3 level vs. frequency at +20 dBm output single carrier level (SCL)

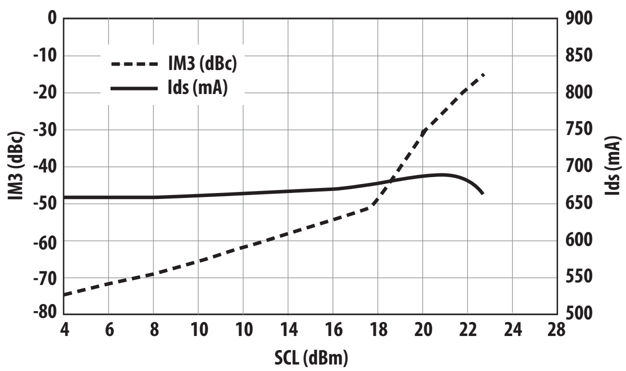


Figure 7. Typical IM3 level and Ids vs. single carrier output level at 6 GHz

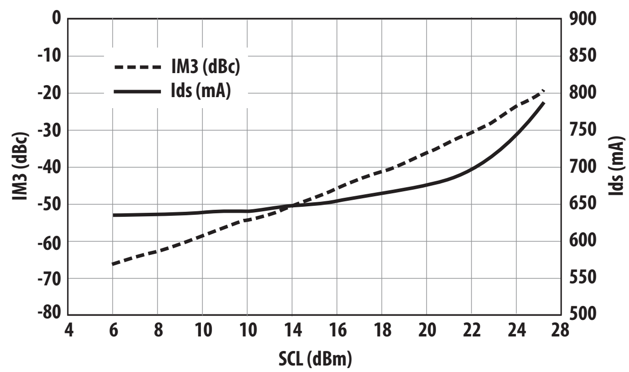


Figure 8. Typical IM3 level and Ids vs. single carrier output level at 8 GHz

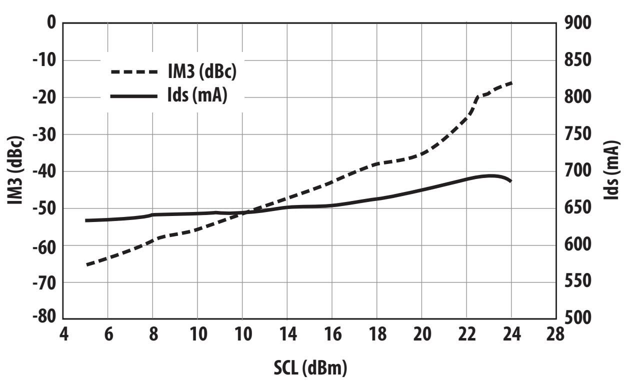


Figure 9. Typical IM3 level and Ids vs. single carrier output level at 12 GHz

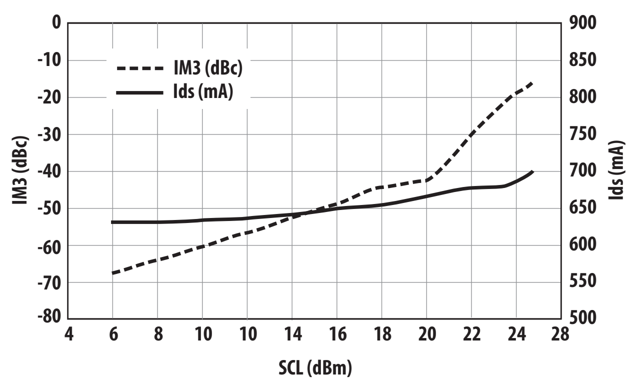


Figure 10. Typical IM3 level and Ids vs. single carrier output level at 14 GHz

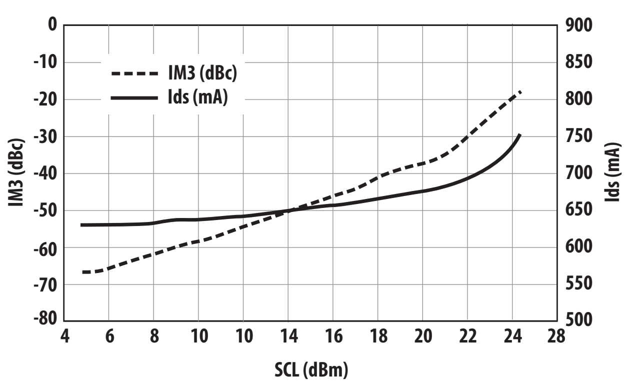


Figure 11. Typical IM3 level and Ids vs. single carrier output level at 16 GHz

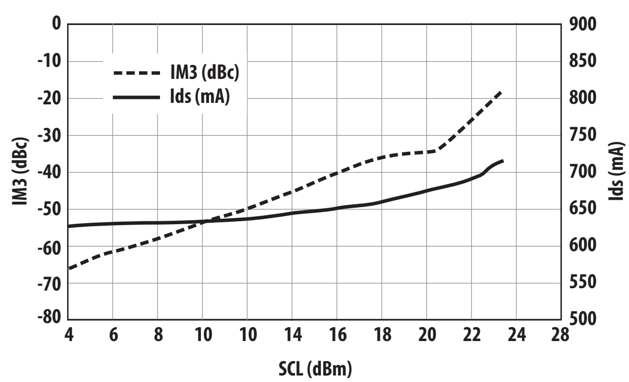


Figure 12. Typical IM3 level and Ids vs. single carrier output level at 18 GHz

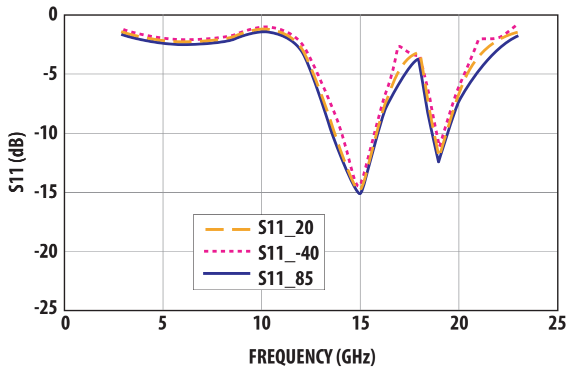


Figure 13. Typical S11 over temperature

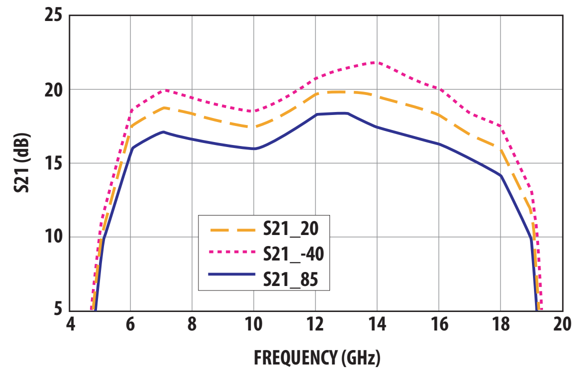


Figure 14. Typical gain over temperature

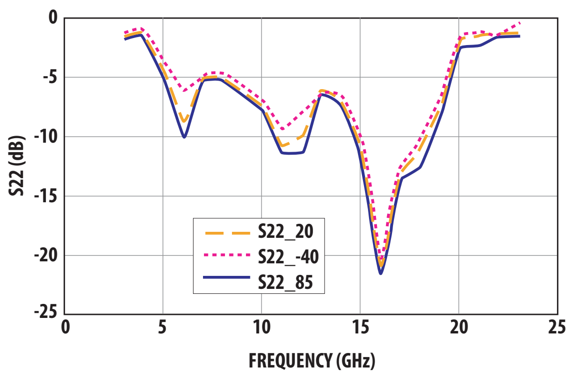


Figure 15. Typical S22 over temperature

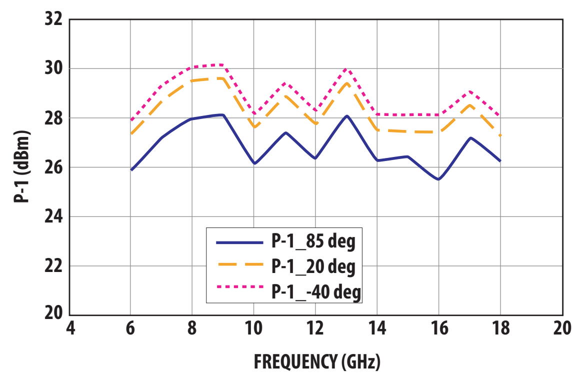


Figure 16. Typical P-1 over temperature

Biasing and Operation

The recommended quiescent DC bias condition for optimum efficiency, performance, and reliability is Vdd = 5 volts with Vg set for Idd = 650 mA. Minor improvements in performance are possible depending on the application. The drain bias voltage range is 3 to 5 V. A single DC gate supply connected to Vg will bias all gain stages. Muting can be accomplished by setting Vgg to the pinch-off voltage Vp.

A simplified schematic for the AMMP6408 MMIC die is shown in Figure 17. The MMIC die contains ESD and over voltage protection diodes for Vg, Vd1, and Vd2 terminals. In a finalized package form, Vd1 and Vd2 terminals are commonly connected to the Vdd terminal. The package diagram for the recommended assembly is shown in Figure 18. In finalized package form, ESD diodes protect all possible ESD or over voltage damages between Vgg and ground, Vgg and Vdd, Vdd and ground. Typical ESD diode current versus diode voltage for 11-connected diodes in series is shown in Figure 13. Under the recommended DC quiescent biasing condition at Vds = 5 V, Ids = 650 mA, Vgg = -1 V, typical gate terminal current is approximately 0.3mA. If an active biasing technique is selected for the AMMP6408 MMIC PA DC biasing, the active biasing circuit must have more than 10-times higher internal current that the gate terminal current.

An optional output power detector network is also provided. A typical measured detector voltage versus output power at 18 GHz is shown Figure 20. The differential voltage between the Det-Ref and Det-Out pads can be correlated with the RF power emerging from the RF output port. The detected voltage is given by,

$V = (V_{ref} - V_{det}) - V_{ofs}$

where V_{ref} is the voltage at the *DET _R* port, V_{det} is a voltage at the *DET _O* port, and V_{ofs} is the zero-input-power offset voltage. There are three methods to calculate V_{ofs}:

1. V_{ofs} can be measured before each detectore measurement (by removing or switching off the power source and measuring $V_{ref} - V_{det}$). This method gives an error due to temperature drift of less than 0.01 dB/50°C.
2. V_{ofs} can be measured at a single reference temperature. The drift error will be less than 0.25 dB.
3. V_{ofs} can either be characterized over temperature and stored in a lookup table, or it can be measured at two temperatures and a linear fit used to calculate V_{ofs} at any temperature. This method gives an error close to the method #1.

The RF ports are AC coupled at the RF input to the first stage and the RF output of the final stage. No ground wired are needed since ground connections are made with plated through-holes to the backside of the device.

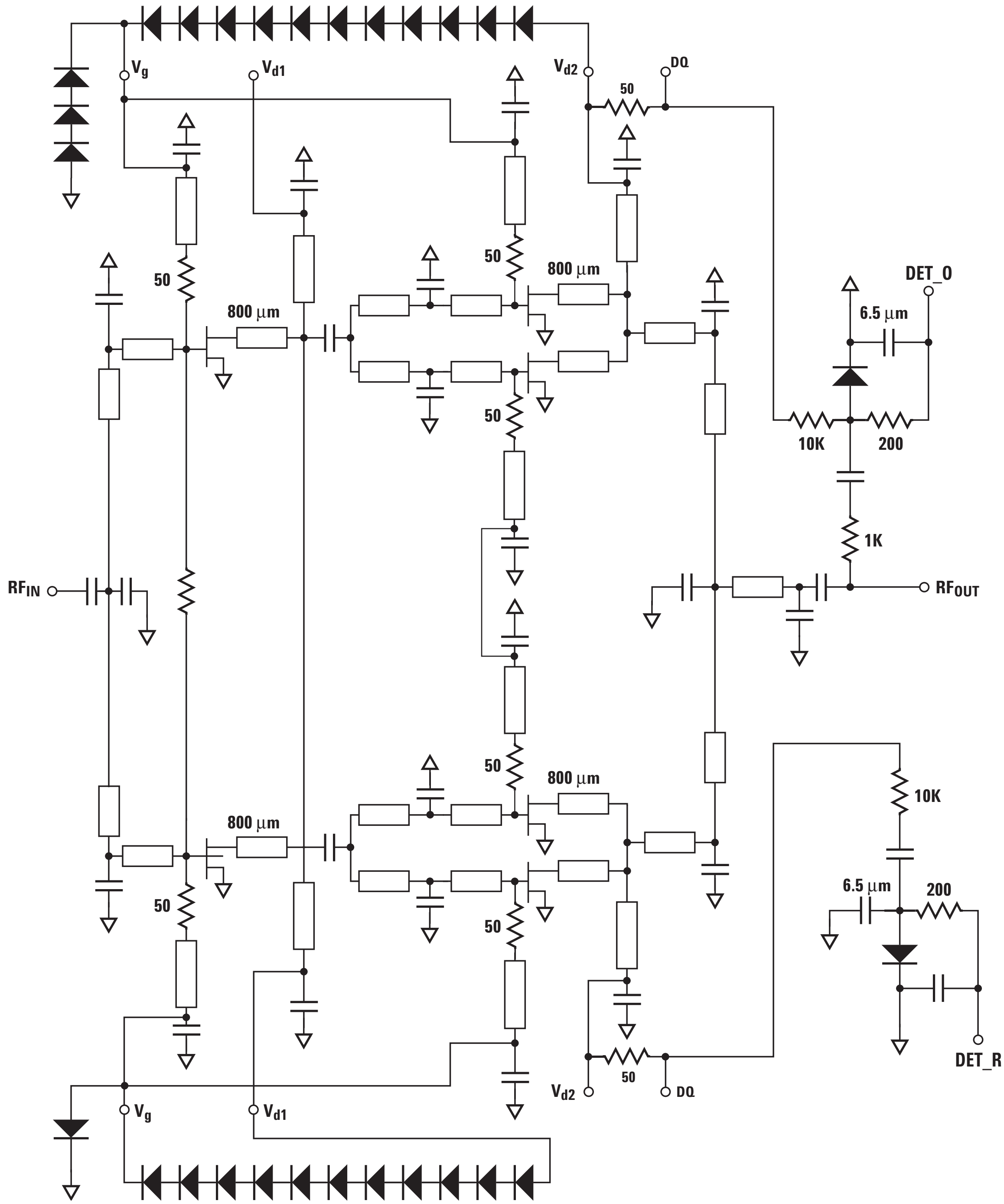
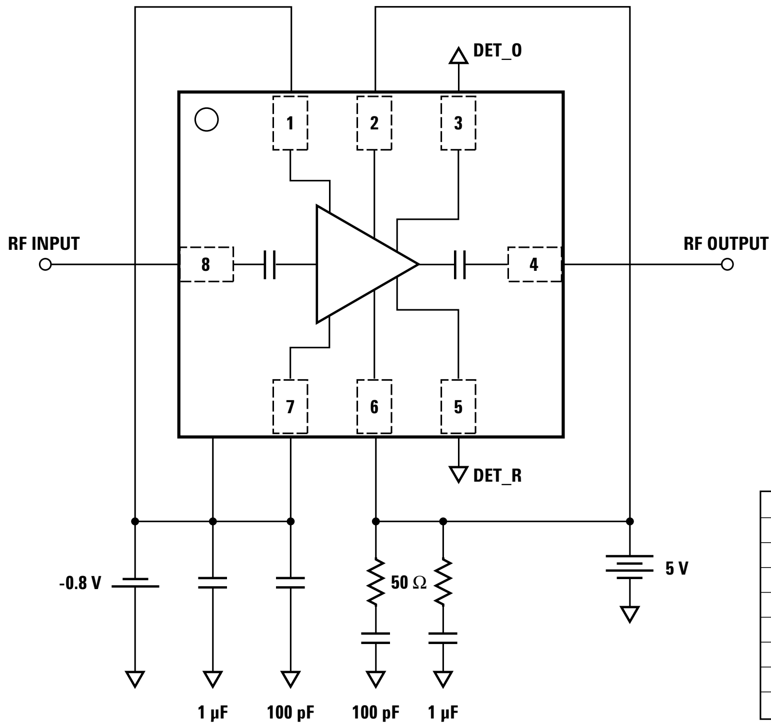


Figure 17. Simplified schematic for the MMIC die



PIN	FUNCTION
1	Vgg
2	Vdd
3	DET_O
4	RF_out
5	DER_R
6	Vdd
7	Vgg
8	RF_in

Note:
1. Vdd may be applied to either Pin 2 or Pin 6.
2. Vgg may be applied to either Pin 1 or Pin 7.

Figure 18. Schematic for recommended Bias circuitry

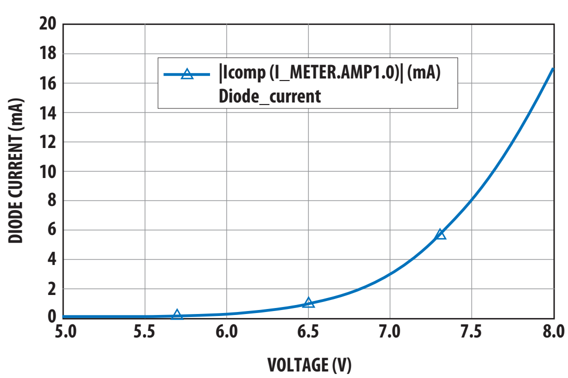


Figure 19. Typical ESD diode current versus diode voltage for 11-connected diodes in series

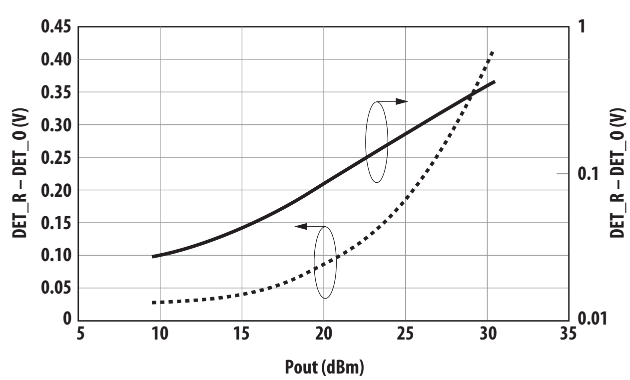


Figure 20. Typical detector voltage and output power, freq. = 18 GHz

Typical Scattering Parameters

Please refer to <http://www.avagotech.com> for typical scattering parameters data.

Package Dimension, PCB Layout and Tape and Reel information

Please refer to Avago Technologies Application Note 5520, AMxP-xxxx production Assembly Process (Land Pattern A).

Ordering Information

AMMP-6408 Part Number Ordering Information

Part Number	Devices per Container	Container
AMMP-6408-BLKG	10	Antistatic bag
AMMP-6408-TR1G	100	7" Reel
AMMP-6408-TR2G	500	7" Reel

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

AV02-2240EN - September 16, 2015