# TABLE OF CONTENTS

## REVISION HISTORY

**12/13—Rev. I to Rev. J**

Added $\theta_{JC}$ Values to Table 7 ..... 8
Changes to Ordering Guide ..... 23

**5/11—Rev. H to Rev. I**

Added Endnote 1 in Table 2 ..... 4
Added Endnote 1 in Table 3 ..... 5
Added Endnote 1 in Table 4 ..... 6
Added Endnote 1 in Table 5 ..... 7
Deleted A Negative Precision Reference Without Precision Resistors Section ..... 17
Deleted Figure 42; Renumbered Sequentially ..... 17
Updated Outline Dimensions ..... 21
Changes to Ordering Guide ..... 22

**6/07—Rev. G to Rev. H**

Changes to Table 2 ..... 3
Changes to Table 3 ..... 4
Changes to Table 4 ..... 5
Changes to Table 5 ..... 6
Updated Outline Dimensions ..... 21
Changes to Ordering Guide ..... 22

**6/05—Rev. F to Rev. G**

Changes to Table 1 ..... 1
Changes to Ordering Guide ..... 22

**2/05—Rev. E to Rev. F**

Updated Format ..... Universal
Updated Outline Dimensions ..... 21
Changes to Ordering Guide ..... 22

**7/04—Rev. D to Rev. E**

Changes to Ordering Guide ..... 5

**3/04—Rev. C to Rev. D**

Changes to Table I ..... 1
Changes to Ordering Guide ..... 4
Updated Outline Dimensions ..... 16

**1/03—Rev. B to Rev. C**

Changed Mini_SOIC to MSOP ..... Universal
Changes to Ordering Guide ..... 4
Corrections to Y-axis labels in TPCs 21 and 24 ..... 9
Enhancement to Figure 13 ..... 15
Updated Outline Dimensions ..... 16

**3/02—Rev. A to Rev. B**

Edits to Ordering Guide ..... 4
Deletion of Precision Voltage Regulator section ..... 15
Addition of Precision Boosted Output Regulator section ..... 15
Addition of Figure 13 ..... 15

**10/01—Rev. 0 to Rev. A**

Addition of ADR423 and ADR425 to ADR420/ADR421 ..... Universal

**5/01—Revision 0: Initial Version**

# SPECIFICATIONS

## ADR420 ELECTRICAL SPECIFICATIONS

$V_{IN}$ = 5.0 V to 15.0 V, $T_A$ = 25°C, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_{OUT}$ | | | | | |
| A Grade | | | 2.045 | 2.048 | 2.051 | V |
| B Grade | | | 2.047 | 2.048 | 2.049 | V |
| INITIAL ACCURACY[1] | $V_{OUTERR}$ | | | | | |
| A Grade | | | −3 | | +3 | mV |
| | | | −0.15 | | +0.15 | % |
| B Grade | | | −1 | | +1 | mV |
| | | | −0.05 | | +0.05 | % |
| TEMPERATURE COEFFICIENT | $TCV_{OUT}$ | −40°C < $T_A$ < +125°C | | | | |
| A Grade | | | | 2 | 10 | ppm°C |
| B Grade | | | | 1 | 3 | ppm/°C |
| SUPPLY VOLTAGE HEADROOM | $V_{IN} - V_{OUT}$ | | 2 | | | V |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | $V_{IN}$ = 5 V to 18 V, −40°C < $T_A$ < +125°C | | 10 | 35 | ppm/V |
| LOAD REGULATION | $\Delta V_{OUT}/\Delta I_L$ | $I_L$ = 0 mA to 10 mA, −40°C < $T_A$ < +125°C | | | 70 | ppm/mA |
| QUIESCENT CURRENT | $I_{IN}$ | No load | | 390 | 500 | µA |
| | | −40°C < $T_A$ < +125°C | | | 600 | µA |
| VOLTAGE NOISE | $e_N$ p-p | 0.1 Hz to 10 Hz | | 1.75 | | µV p-p |
| VOLTAGE NOISE DENSITY | $e_N$ | 1 kHz | | 60 | | nV/√Hz |
| TURN-ON SETTLING TIME | $t_R$ | | | 10 | | µs |
| LONG-TERM STABILITY | $\Delta V_{OUT}$ | 1000 hours | | 50 | | ppm |
| OUTPUT VOLTAGE HYSTERESIS | $V_{OUT\_HYS}$ | | | 40 | | ppm |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 1 kHz | | −75 | | dB |
| SHORT CIRCUIT TO GND | $I_{SC}$ | | | 27 | | mA |

[1] Initial accuracy does not include shift due to solder heat effect.

## ADR421 ELECTRICAL SPECIFICATIONS

$V_{IN}$ = 5.0 V to 15.0 V, $T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_{OUT}$ | | | | | |
| A Grade | | | 2.497 | 2.500 | 2.503 | V |
| B Grade | | | 2.499 | 2.500 | 2.501 | V |
| INITIAL ACCURACY[1] | $V_{OUTERR}$ | | | | | |
| A Grade | | | −3 | | +3 | mV |
| | | | −0.12 | | +0.12 | % |
| B Grade | | | −1 | | +1 | mV |
| | | | −0.04 | | +0.04 | % |
| TEMPERATURE COEFFICIENT | $TCV_{OUT}$ | −40°C < $T_A$ < +125°C | | | | |
| A Grade | | | | 2 | 10 | ppm/°C |
| B Grade | | | | 1 | 3 | ppm/°C |
| SUPPLY VOLTAGE HEADROOM | $V_{IN} - V_{OUT}$ | | 2 | | | V |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | $V_{IN}$ = 5 V to 18 V, −40°C < $T_A$ < +125°C | | 10 | 35 | ppm/V |
| LOAD REGULATION | $\Delta V_{OUT}/\Delta I_L$ | $I_L$ = 0 mA to 10 mA, −40°C < $T_A$ < +125°C | | | 70 | ppm/mA |
| QUIESCENT CURRENT | $I_{IN}$ | No load | | 390 | 500 | µA |
| | | −40°C < $T_A$ < +125°C | | | 600 | µA |
| VOLTAGE NOISE | $e_N$ p-p | 0.1 Hz to 10 Hz | | 1.75 | | µV p-p |
| VOLTAGE NOISE DENSITY | $e_N$ | 1 kHz | | 80 | | nV/√Hz |
| TURN-ON SETTLING TIME | $t_R$ | | | 10 | | µs |
| LONG-TERM STABILITY | $\Delta V_{OUT}$ | 1000 hours | | 50 | | ppm |
| OUTPUT VOLTAGE HYSTERESIS | $V_{OUT\_HYS}$ | | | 40 | | ppm |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 1 kHz | | −75 | | dB |
| SHORT CIRCUIT TO GND | $I_{SC}$ | | | 27 | | mA |

[1] Initial accuracy does not include shift due to solder heat effect.

## ADR423 ELECTRICAL SPECIFICATIONS

$V_{IN}$ = 5.0 V to 15.0 V, $T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_{OUT}$ | | | | | |
| A Grade | | | 2.996 | 3.000 | 3.004 | V |
| B Grade | | | 2.9985 | 3.000 | 3.0015 | V |
| INITIAL ACCURACY[1] | $V_{OUTERR}$ | | | | | |
| A Grade | | | −4 | | +4 | mV |
| | | | −0.13 | | +0.13 | % |
| B Grade | | | −1.5 | | +1.5 | mV |
| | | | −0.04 | | +0.04 | % |
| TEMPERATURE COEFFICIENT | $TCV_{OUT}$ | −40°C < $T_A$ < +125°C | | | | |
| A Grade | | | | 2 | 10 | ppm/°C |
| B Grade | | | | 1 | 3 | ppm/°C |
| SUPPLY VOLTAGE HEADROOM | $V_{IN} - V_{OUT}$ | | 2 | | | V |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | $V_{IN}$ = 5 V to 18 V, −40°C < $T_A$ < +125°C | | 10 | 35 | ppm/V |
| LOAD REGULATION | $\Delta V_{OUT}/\Delta I_L$ | $I_L$ = 0 mA to 10 mA, −40°C < $T_A$ < +125°C | | | 70 | ppm/mA |
| QUIESCENT CURRENT | $I_{IN}$ | No load | | 390 | 500 | µA |
| | | −40°C < $T_A$ < +125°C | | | 600 | µA |
| VOLTAGE NOISE | $e_N$ p-p | 0.1 Hz to 10 Hz | | 2 | | µV p-p |
| VOLTAGE NOISE DENSITY | $e_N$ | 1 kHz | | 90 | | nV/√Hz |
| TURN-ON SETTLING TIME | $t_R$ | | | 10 | | µs |
| LONG-TERM STABILITY | $\Delta V_{OUT}$ | 1000 hours | | 50 | | ppm |
| OUTPUT VOLTAGE HYSTERESIS | $V_{OUT\_HYS}$ | | | 40 | | ppm |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 1 kHz | | −75 | | dB |
| SHORT CIRCUIT TO GND | $I_{SC}$ | | | 27 | | mA |

[1] Initial accuracy does not include shift due to solder heat effect.

## ADR425 ELECTRICAL SPECIFICATIONS

$V_{IN}$ = 7.0 V to 15.0 V, $T_A$ = 25°C, unless otherwise noted.

**Table 5.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_{OUT}$ | | | | | |
| A Grade | | | 4.994 | 5.000 | 5.006 | V |
| B Grade | | | 4.998 | 5.000 | 5.002 | V |
| INITIAL ACCURACY[1] | $V_{OUTERR}$ | | | | | |
| A Grade | | | −6 | | +6 | mV |
| | | | −0.12 | | +0.12 | % |
| B Grade | | | −2 | | +2 | mV |
| | | | −0.04 | | +0.04 | % |
| TEMPERATURE COEFFICIENT | $TCV_{OUT}$ | | | | | |
| A Grade | | −40°C < $T_A$ < +125°C | | 2 | 10 | ppm/°C |
| B Grade | | | | 1 | 3 | ppm/°C |
| SUPPLY VOLTAGE HEADROOM | $V_{IN} - V_O$ | | 2 | | | V |
| LINE REGULATION | $\Delta V_O/\Delta V_{IN}$ | $V_{IN}$ = 7 V to 18 V, −40°C < $T_A$ < +125°C | | 10 | 35 | ppm/V |
| LOAD REGULATION | $\Delta V_O/\Delta I_L$ | $I_L$ = 0 mA to 10 mA, −40°C < $T_A$ < +125°C | | | 70 | ppm/mA |
| QUIESCENT CURRENT | $I_{IN}$ | No load | | 390 | 500 | µA |
| | | −40°C < $T_A$ < +125°C | | | 600 | µA |
| VOLTAGE NOISE | $e_N$ p-p | 0.1 Hz to 10 Hz | | 3.4 | | µV p-p |
| VOLTAGE NOISE DENSITY | $e_N$ | 1 kHz | | 110 | | nV/√Hz |
| TURN-ON SETTLING TIME | $t_R$ | | | 10 | | µs |
| LONG-TERM STABILITY | $\Delta V_O$ | 1000 hours | | 50 | | ppm |
| OUTPUT VOLTAGE HYSTERESIS | $V_{O\_HYS}$ | | | 40 | | ppm |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 1 kHz | | −75 | | dB |
| SHORT CIRCUIT TO GND | $I_{SC}$ | | | 27 | | mA |

[1] Initial accuracy does not include shift due to solder heat effect.

# ABSOLUTE MAXIMUM RATINGS

These ratings apply at 25°C, unless otherwise noted.

**Table 6.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 18 V |
| Output Short-Circuit Duration to GND | Indefinite |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +125°C |
| Junction Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 60 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, $\theta_{JA}$ is specified for devices soldered in the circuit board for surface-mount packages.

**Table 7.**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 8-Lead MSOP (RM) | 190 | 44 | °C/W |
| 8-Lead SOIC (R) | 130 | 43 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

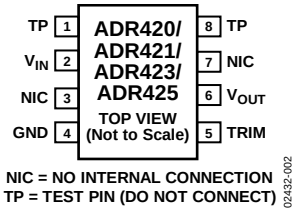



*Figure 2. 8-Lead SOIC, 8-Lead MSOP Pin Configuration*

**Table 8. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 8 | TP | Test Pin. There are actual connections in TP pins, but they are reserved for factory testing purposes. Users should not connect anything to TP pins; otherwise, the device may not function properly. |
| 2 | $V_{IN}$ | Input Voltage. |
| 3, 7 | NIC | No Internal Connect. NICs have no internal connections. |
| 4 | GND | Ground Pin = 0 V. |
| 5 | TRIM | Trim Terminal. It can be used to adjust the output voltage over a ±0.5% range without affecting the temperature coefficient. |
| 6 | $V_{OUT}$ | Output Voltage. |

# TYPICAL PERFORMANCE CHARACTERISTICS

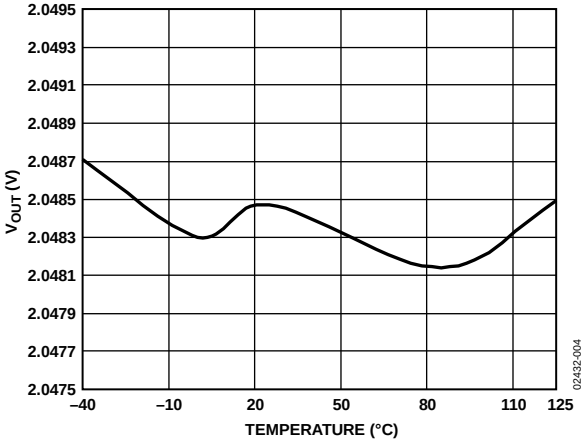



Figure 3. ADR420 Typical Output Voltage vs. Temperature

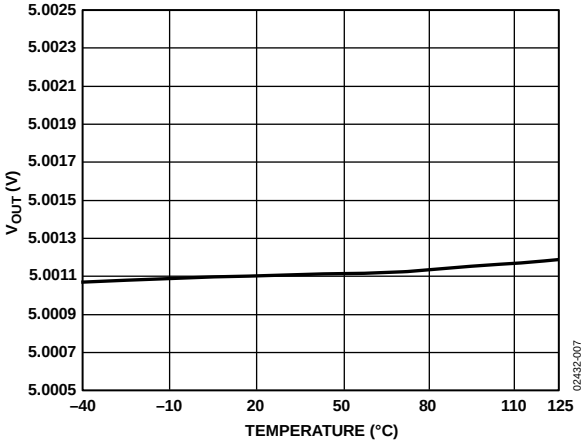



Figure 6. ADR425 Typical Output Voltage vs. Temperature

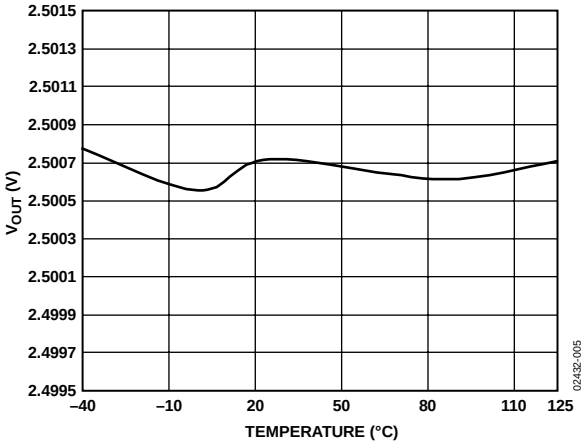



Figure 4. ADR421 Typical Output Voltage vs. Temperature

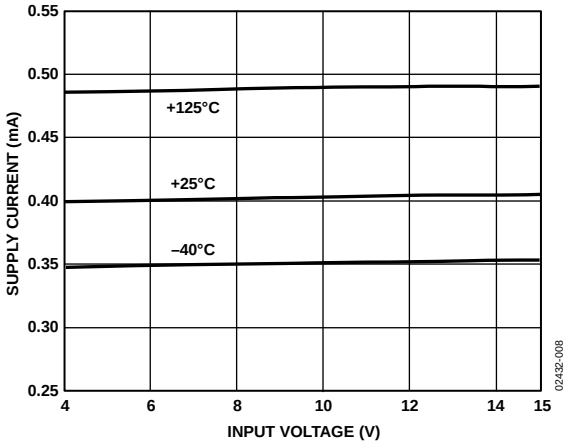



Figure 7. ADR420 Supply Current vs. Input Voltage

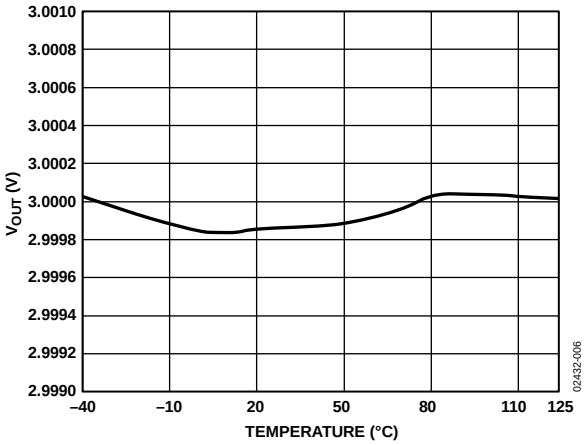



Figure 5. ADR423 Typical Output Voltage vs. Temperature

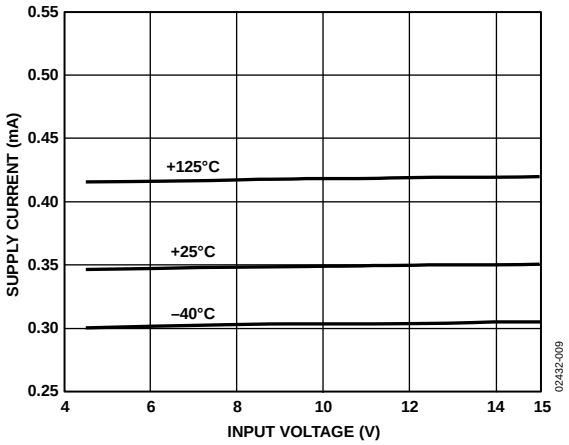



Figure 8. ADR421 Supply Current vs. Input Voltage

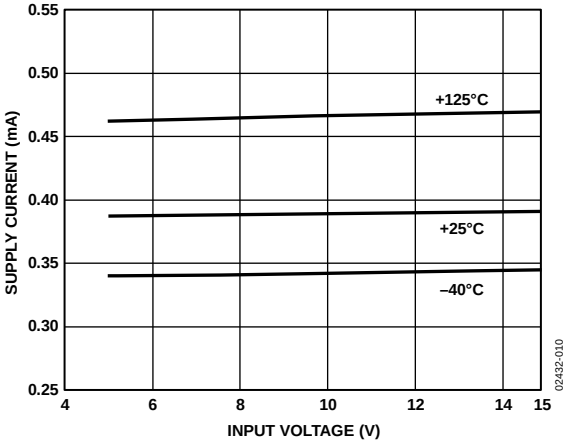



Figure 9. ADR423 Supply Current vs. Input Voltage

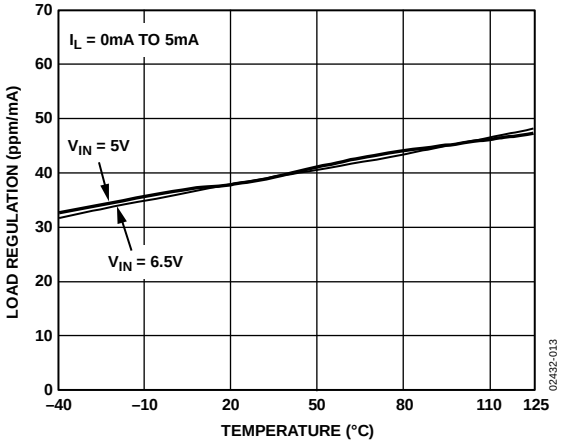



Figure 12. ADR421 Load Regulation vs. Temperature

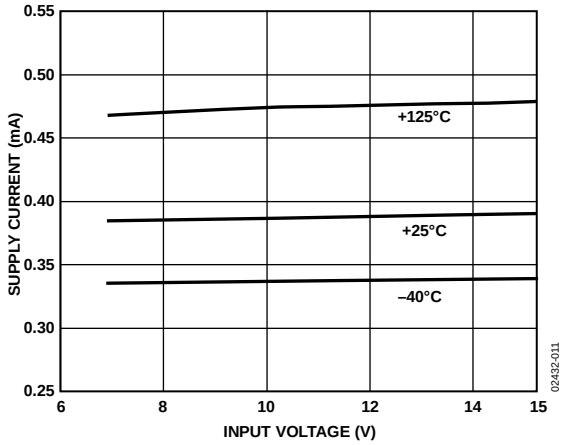



Figure 10. ADR425 Supply Current vs. Input Voltage

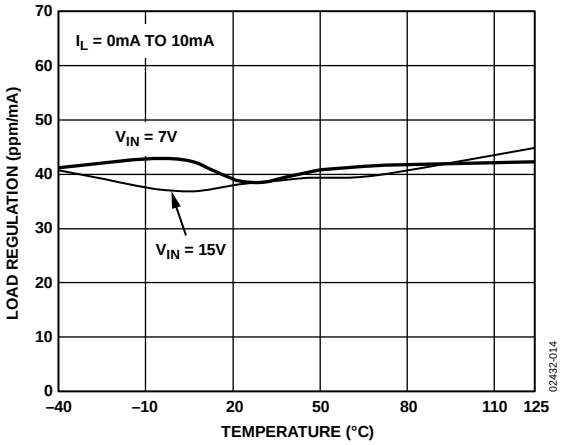



Figure 13. ADR423 Load Regulation vs. Temperature

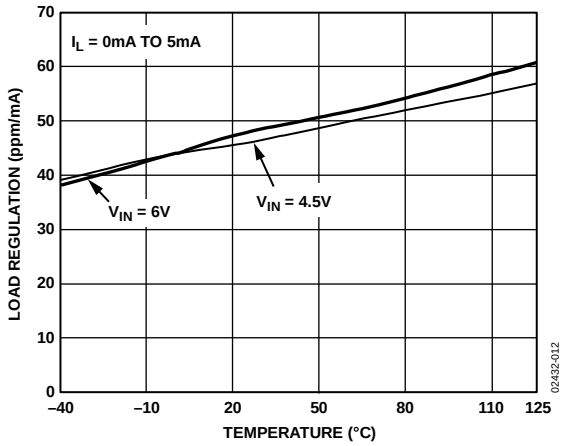



Figure 11. ADR420 Load Regulation vs. Temperature

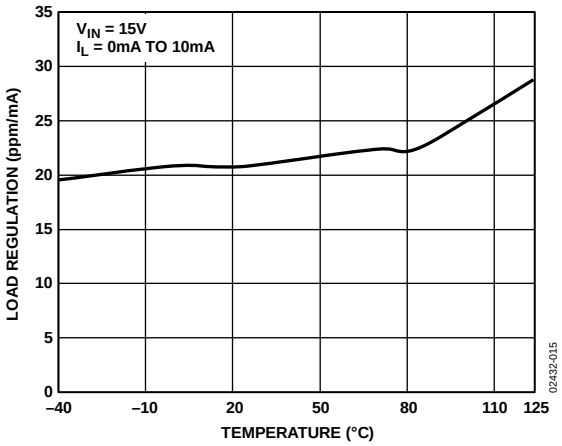



Figure 14. ADR425 Load Regulation vs. Temperature

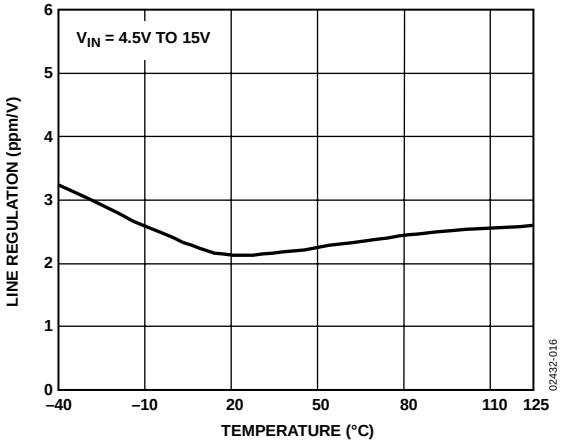



Figure 15. ADR420 Line Regulation vs. Temperature

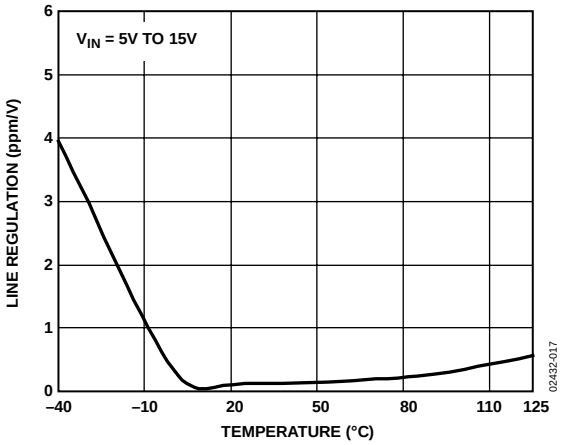



Figure 16. ADR421 Line Regulation vs. Temperature

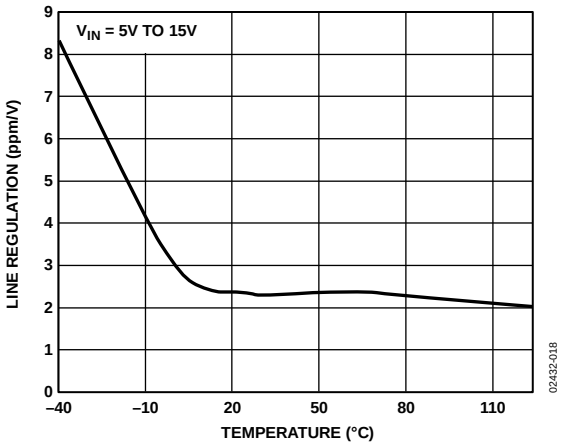



Figure 17. ADR423 Line Regulation vs. Temperature

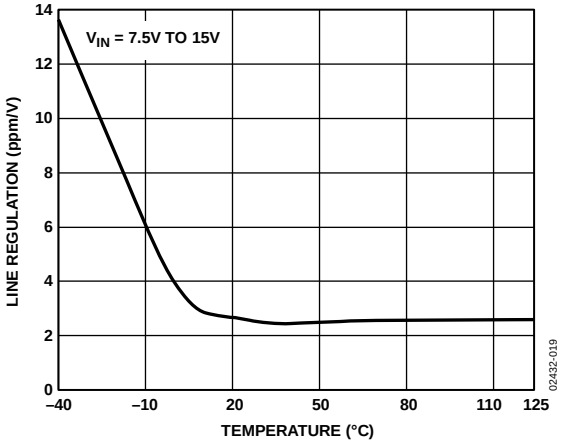



Figure 18. ADR425 Line Regulation vs. Temperature

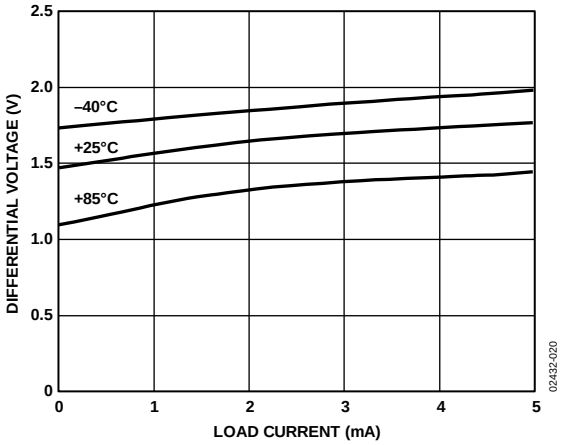



Figure 19. ADR420 Minimum Input/Output Voltage Differential vs. Load Current

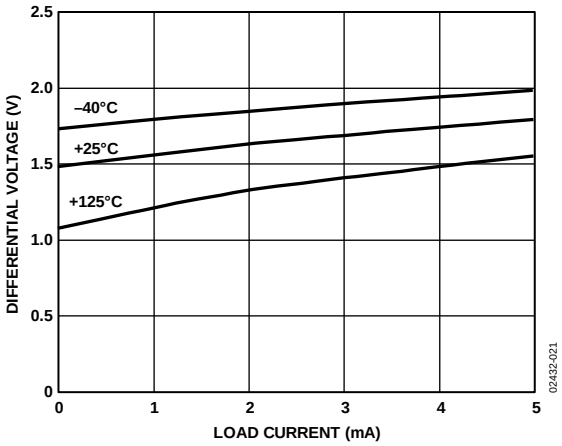



Figure 20. ADR421 Minimum Input/Output Voltage Differential vs. Load Current

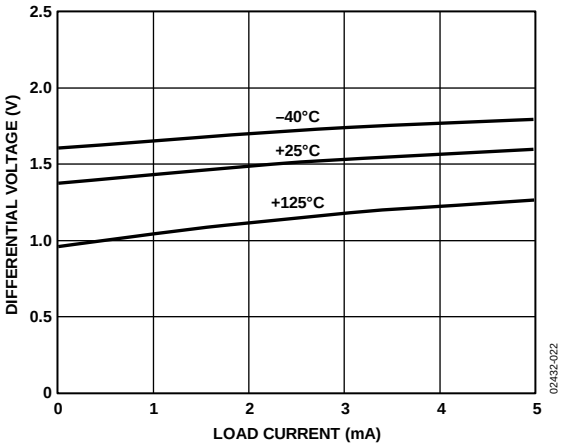



Figure 21. ADR423 Minimum Input/Output Voltage Differential vs. Load Current

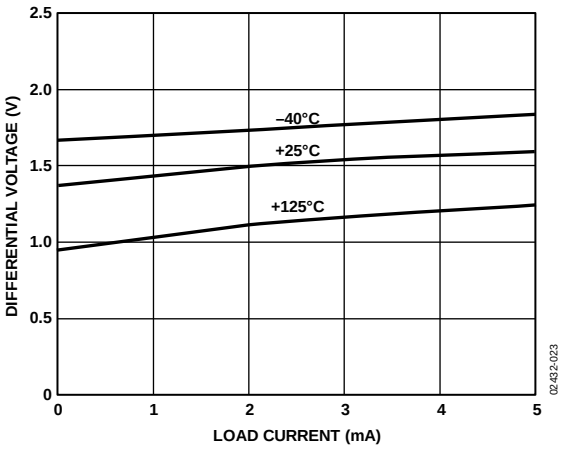



Figure 22. ADR425 Minimum Input/Output Voltage Differential vs. Load Current

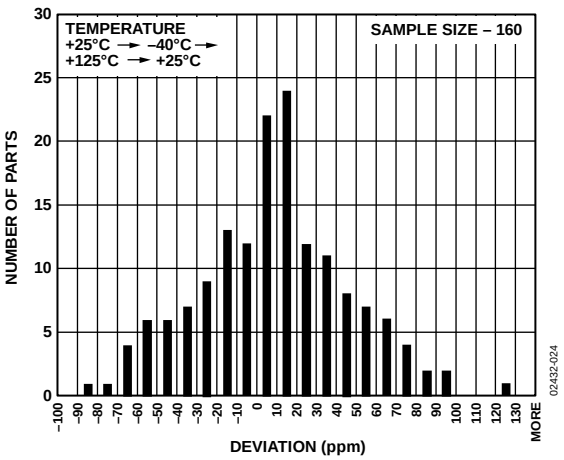



Figure 23. ADR421 Typical Hysteresis

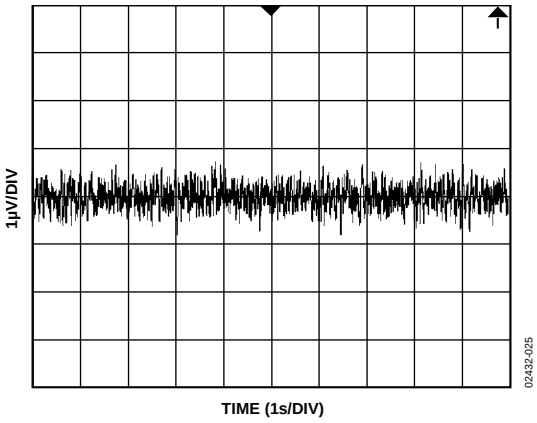



Figure 24. ADR421 Typical Noise Voltage 0.1 Hz to 10 Hz

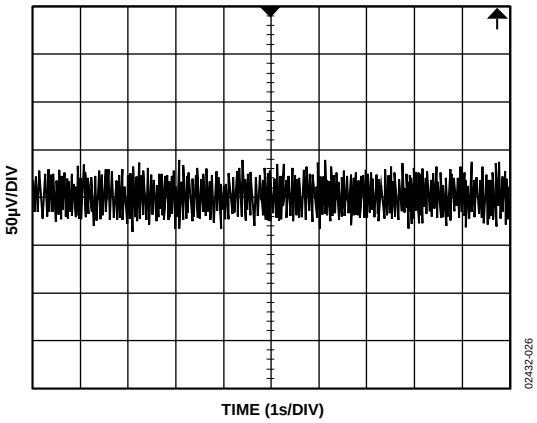



Figure 25. Typical Noise Voltage 10 Hz to 10 kHz

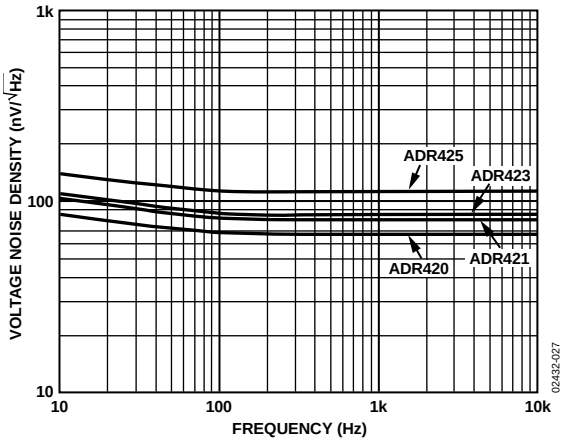



Figure 26. Voltage Noise Density vs. Frequency

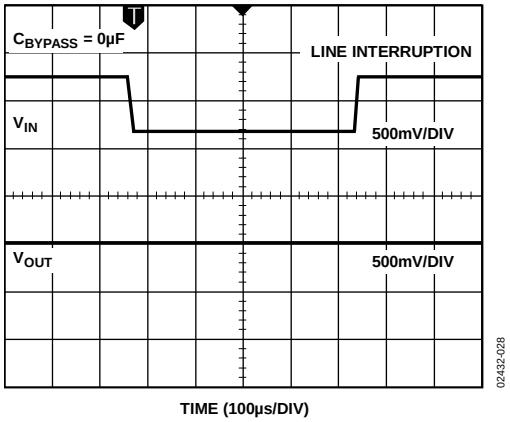



Figure 27. ADR421 Line Transient Response, no $C_{BYPASS}$

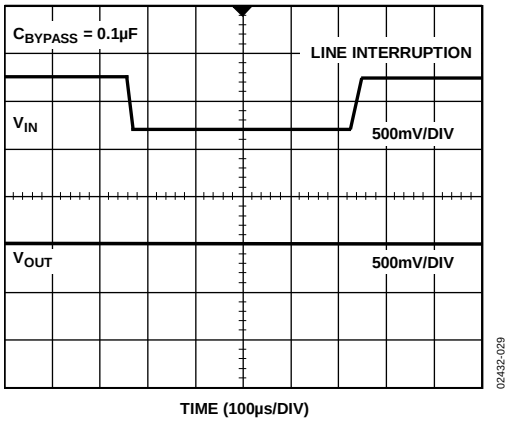



Figure 28. ADR421 Line Transient Response, $C_{BYPASS}$ = 0.1 µF

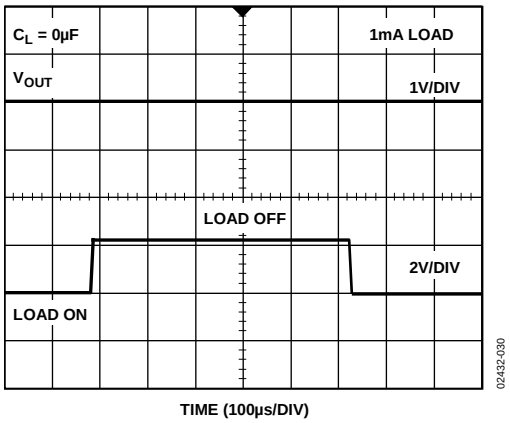



Figure 29. ADR421 Load Transient Response, no $C_L$

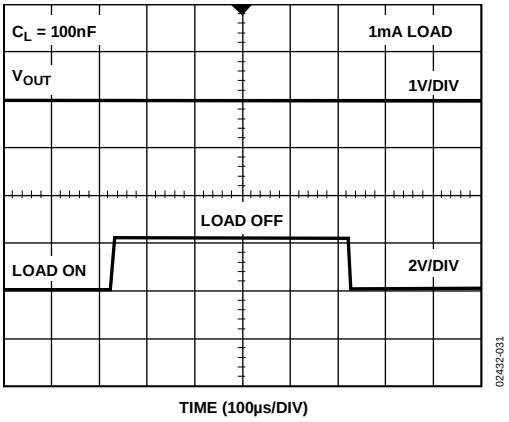



Figure 30. ADR421 Load Transient Response, $C_L$ = 100 nF

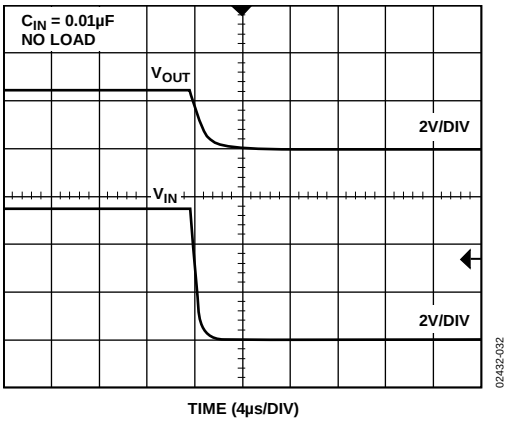



Figure 31. ADR421 Turn-Off Response

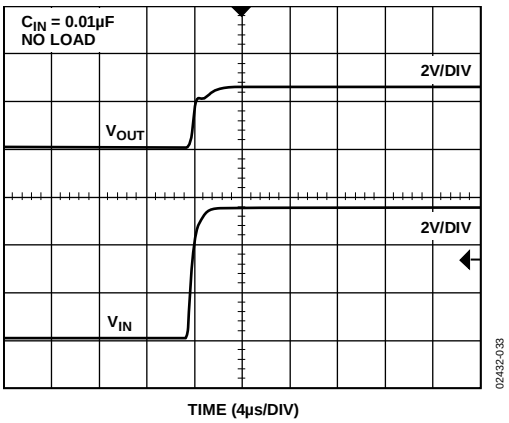



Figure 32. ADR421 Turn-On Response

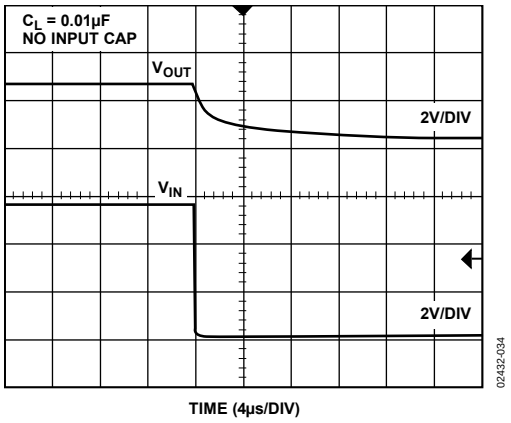



Figure 33. ADR421 Turn-Off Response

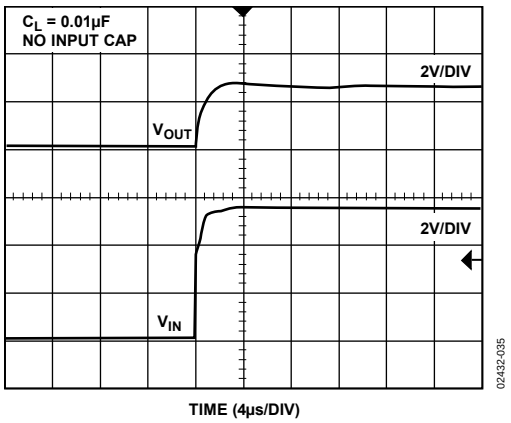



Figure 34. ADR421 Turn-On Response

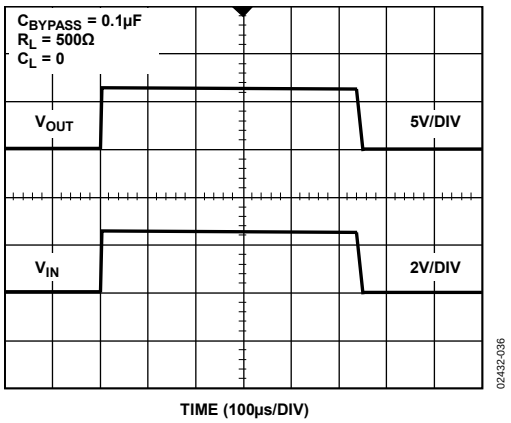



Figure 35. ADR421 Turn-On/Turn-Off Response

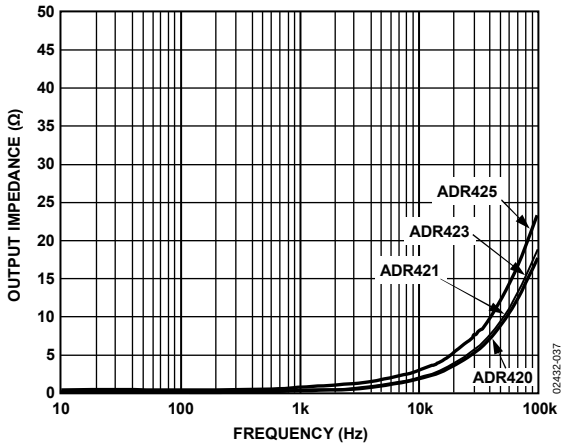



Figure 36. Output Impedance vs. Frequency

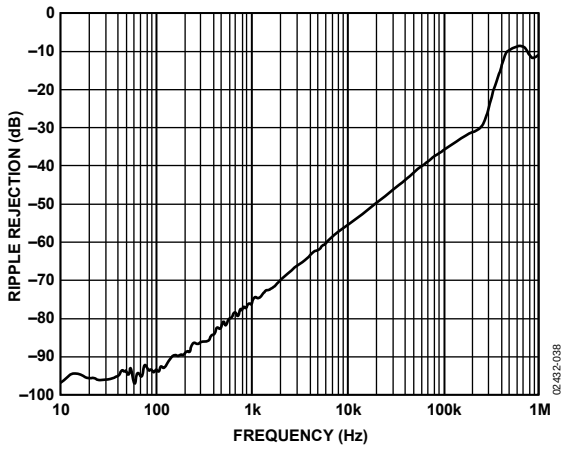



Figure 37. Ripple Rejection vs. Frequency

# TERMINOLOGY

**Temperature Coefficient**

The change of output voltage over the operating temperature range is normalized by the output voltage at 25°C, and expressed in ppm/°C as

$$TCV_{OUT}(ppm/°C) = \frac{V_{OUT}(T_2) - V_{OUT}(T_1)}{V_{OUT}(25°C) \times (T_2 - T_1)} \times 10^6$$

where:

$V_{OUT}$ (*25°C*) = $V_{OUT}$ at 25°C.

$V_{OUT}$ ($T_1$) = $V_{OUT}$ at Temperature 1.

$V_{OUT}$ ($T_2$) = $V_{OUT}$ at Temperature 2.

**Line Regulation**

The change in output voltage due to a specified change in input voltage. It includes the effects of self-heating. Line regulation is expressed in either percent per volt, parts per million per volt, or microvolts per volt change in input voltage.

**Load Regulation**

The change in output voltage due to a specified change in load current. It includes the effects of self-heating. Load regulation is expressed in either microvolts per milliampere, parts per million per milliampere, or ohms of dc output resistance.

**Long-Term Stability**

Typical shift of output voltage at 25°C on a sample of parts subjected to operation life test of 1000 hours at 125°C.

$$\Delta V_{OUT} = V_{OUT}(t_0) - V_{OUT}(t_1)$$

$$\Delta V_{OUT}(ppm) = \frac{V_{OUT}(t_0) - V_{OUT}(t_1)}{V_{OUT}(t_0)} \times 10^6$$

where:

$V_{OUT}$ ($t_0$) = $V_{OUT}$ at 25°C at Time 0.

$V_{OUT}$ ($t_1$) = $V_{OUT}$ at 25°C after 1000 hours operation at 125°C.

**Thermal Hysteresis**

The change of output voltage after the device is cycled through temperatures from +25°C to −40°C to +125°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle.

$$V_{OUT\_HYS} = V_{OUT}(25°C) - V_{OUT\_TC}$$

$$V_{OUT\_HYS}(ppm) = \frac{V_{OUT}(25°C) - V_{OUT\_TC}}{V_{OUT}(25°C)} \times 10^6$$

where:

$V_{OUT}$ (*25°C*) = $V_{OUT}$ at 25°C.

$V_{OUT\_TC}$ = $V_{OUT}$ at 25°C after temperature cycle at +25°C to −40°C to +125°C and back to +25°C.

**Input Capacitor**

Input capacitors are not required on the ADR42x. There is no limit for the value of the capacitor used on the input, but a 1 µF to 10 µF capacitor on the input improves transient response in applications where the supply suddenly changes. An additional 0.1 µF capacitor in parallel also helps to reduce noise from the supply.

**Output Capacitor**

The ADR42x do not need output capacitors for stability under any load condition. An output capacitor, typically 0.1 µF, filters out any low level noise voltage and does not affect the operation of the part. On the other hand, the load transient response can be improved with an additional 1 µF to 10 µF output capacitor in parallel. A capacitor here acts as a source of stored energy for sudden increase in load current. The only parameter that degrades by adding an output capacitor is the turn-on time, which depends on the size of the selected capacitor.

# THEORY OF OPERATION

The ADR42x series of references uses a reference generation technique known as XFET (eXtra implanted junction FET). This technique yields a reference with low supply current, good thermal hysteresis, and exceptionally low noise. The core of the XFET reference consists of two junction field-effect transistors (JFET), one having an extra channel implant to raise its pinch-off voltage. By running the two JFETs at the same drain current, the difference in pinch-off voltage can be amplified and used to form a highly stable voltage reference.

The intrinsic reference voltage is about 0.5 V with a negative temperature coefficient of about −120 ppm/°C. This slope is essentially constant to the dielectric constant of silicon and can be closely compensated by adding a correction term generated in the same fashion as the proportional-to-temperature (PTAT) term used to compensate band gap references. The primary advantage over a band gap reference is that the intrinsic temperature coefficient is approximately 30 times lower (therefore requiring less correction). This results in much lower noise because most of the noise of a band gap reference comes from the temperature compensation circuitry.

Figure 38 shows the basic topology of the ADR42x series. The temperature correction term is provided by a current source with a value designed to be proportional to absolute temperature. The general equation is

$$V_{OUT} = G \times (\Delta V_P - R1 \times I_{PTAT}) \quad (1)$$

where:
$G$ is the gain of the reciprocal of the divider ratio.
$\Delta V_P$ is the difference in pinch-off voltage between the two JFETs.
$I_{PTAT}$ is the positive temperature coefficient correction current.

Each ADR42x device is created by on-chip adjustment of R2 and R3 to achieve the specified reference output.

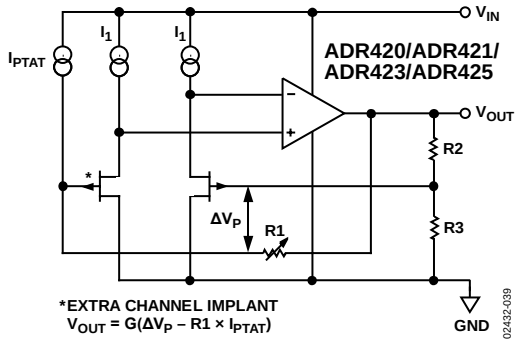



*Figure 38. Simplified Schematic*

## DEVICE POWER DISSIPATION CONSIDERATIONS

The ADR42x family of references is guaranteed to deliver load currents to 10 mA with an input voltage that ranges from 4.5 V to 18 V. When these devices are used in applications at higher currents, the following equation should be used to account for the temperature effects due to power dissipation increases:

$$T_J = P_D \times \theta_{JA} + T_A \quad (2)$$

where:
$T_J$ and $T_A$ are the junction temperature and the ambient temperature, respectively.
$P_D$ is the device power dissipation.
$\theta_{JA}$ is the device package thermal resistance.

## BASIC VOLTAGE REFERENCE CONNECTIONS

Voltage references, in general, require a bypass capacitor connected from $V_{OUT}$ to GND. The circuit in Figure 39 illustrates the basic configuration for the ADR42x family of references. Other than a 0.1 µF capacitor at the output to help improve noise suppression, a large output capacitor at the output is not required for circuit stability.

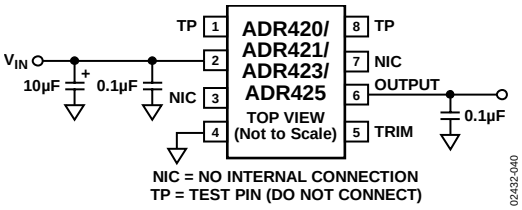



*Figure 39. Basic Voltage Reference Configuration*

## NOISE PERFORMANCE

The noise generated by ADR42x references is typically less than 2 µV p-p over the 0.1 Hz to 10 Hz band for the ADR420, ADR421, and ADR423. Figure 24 shows the 0.1 Hz to 10 Hz noise of the ADR421, which is only 1.75 µV p-p. The noise measurement is made with a band-pass filter made of a 2-pole high-pass filter with a corner frequency at 0.1 Hz and a 2-pole low-pass filter with a corner frequency at 10 Hz.

## TURN-ON TIME

At power-up (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components typically associated with this are the time for the active circuits to settle and the time for the thermal gradients on the chip to stabilize. Figure 31 to Figure 35 show the turn-on settling time for the ADR421.

# APPLICATIONS

## OUTPUT ADJUSTMENT

The ADR42x trim terminal can be used to adjust the output voltage over a ±0.5% range. This feature allows the system designer to trim system errors out by setting the reference to a voltage other than the nominal. This is also helpful if the part is used in a system at temperature to trim out any error. Adjustment of the output has a negligible effect on the temperature performance of the device. To avoid degrading temperature coefficients, both the trimming potentiometer and the two resistors need to be low temperature coefficient types, preferably <100 ppm/°C.

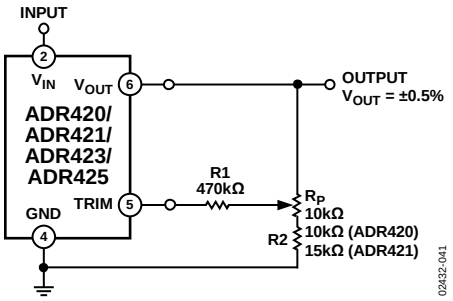



*Figure 40. Output Trim Adjustment*

## REFERENCE FOR CONVERTERS IN OPTICAL NETWORK CONTROL CIRCUITS

In the high capacity, all optical router network of Figure 41, arrays of micromirrors direct and route optical signals from fiber to fiber, without first converting them to electrical form, which reduces the communication speed. The tiny micro-mechanical mirrors are positioned so that each is illuminated by a single wavelength that carries unique information and can be passed to any desired input and output fiber. The mirrors are tilted by the dual-axis actuators controlled by precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) within the system. Due to the microscopic movement of the mirrors, not only is the precision of the converters important, but the noise associated with these controlling converters is extremely critical, because total noise within the system can be multiplied by the numbers of converters used. Consequently, the exceptional low noise of the ADR42x is necessary to maintain the stability of the control loop for this application.

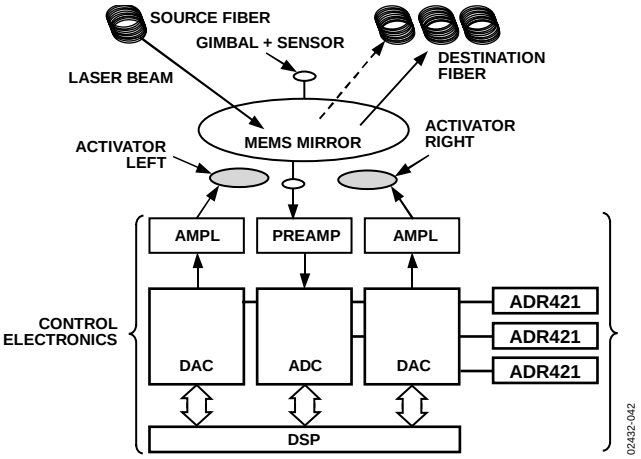



*Figure 41. All Optical Router Network*

## HIGH VOLTAGE FLOATING CURRENT SOURCE

The circuit in Figure 42 can be used to generate a floating current source with minimal self-heating. This particular configuration can operate on high supply voltages determined by the breakdown voltage of the N-channel JFET.

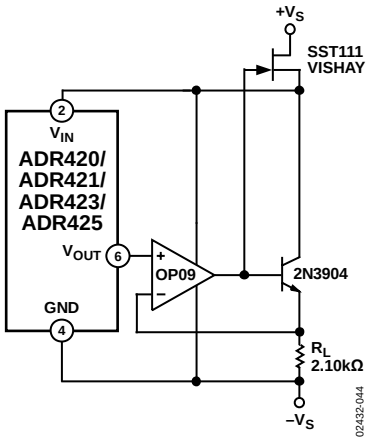



*Figure 42. High Voltage Floating Current Source*

## KELVIN CONNECTIONS

In many portable instrumentation applications where PC board cost and area are important considerations, circuit interconnects are often narrow. These narrow lines can cause large voltage drops if the voltage reference is required to provide load currents to various functions. In fact, a circuit's interconnects can exhibit a typical line resistance of 0.45 mΩ/square (1 oz. Cu, for example). Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. Load currents flowing through wiring resistance produce an error ($V_{ERROR} = R \times I_L$) at the load. However, the Kelvin connection in Figure 43 overcomes the problem by including the wiring resistance within the forcing loop of the op amp. Because the op amp senses the load voltage, op amp loop control forces the output to compensate for the wiring error and to produce the correct voltage at the load.

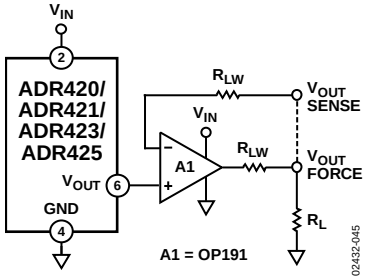



*Figure 43. Advantage of Kelvin Connection*

## DUAL-POLARITY REFERENCES

Dual-polarity references can easily be made with an op amp and a pair of resistors. In order not to defeat the accuracy obtained by the ADR42x, it is imperative to match the resistance tolerance and the temperature coefficient of all components.

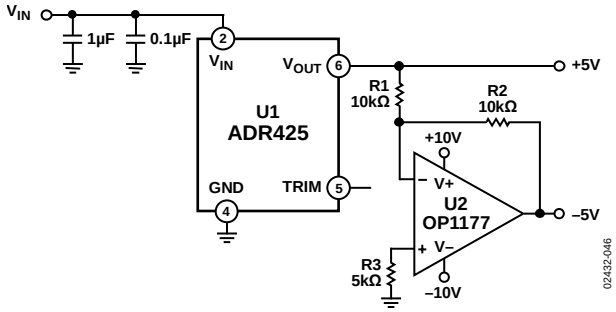



*Figure 44. +5 V and −5 V Reference Using ADR425*

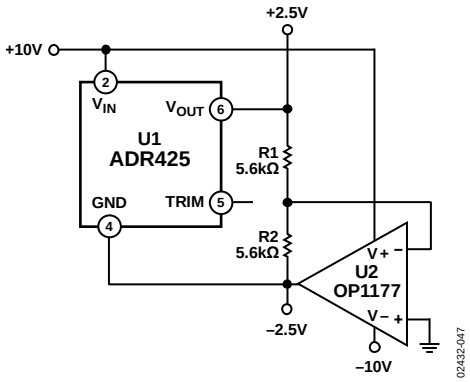



*Figure 45. +2.5 V and −2.5 V Reference Using ADR425*

## PROGRAMMABLE CURRENT SOURCE

Together with a digital potentiometer and a Howland current pump, the ADR425 forms the reference source for a programmable current as

$$I_L = \frac{\left(\frac{R2_A + R2_B}{R1}\right)}{R2_B} \times V_W \quad (3)$$

and

$$VW = \frac{D}{2^N} \times V_{REF} \quad (4)$$

where:
*D* is the decimal equivalent of the input code.
*N* is the number of bits.

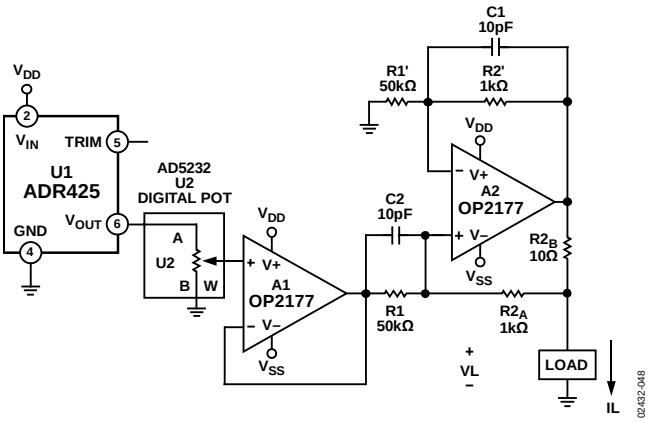



*Figure 46. Programmable Current Source*

R1' and R2' must be equal to R1 and $R2_A + R2_B$, respectively. Theoretically, $R2_B$ can be made as small as needed to achieve the current needed within A2 output current driving capability. In the example shown in Figure 46, OP2177 is able to deliver a maximum of 10 mA. Because the current pump uses both positive and negative feedback, capacitors C1 and C2 are needed to ensure that negative feedback prevails and, therefore, avoiding oscillation. This circuit also allows bidirectional current flow if the inputs $V_A$ and $V_B$ of the digital potentiometer are supplied with the dual-polarity references as previously shown.

## PROGRAMMABLE DAC REFERENCE VOLTAGE

With a multichannel DAC, such as the quad, 12-bit voltage output AD7398, one of its internal DACs, and an ADR42x voltage reference can be used as a common programmable $V_{REF}x$ for the rest of the DACs. The circuit configuration is shown in Figure 47. The relationship of $V_{REF}x$ to $V_{REF}$ depends on the digital code and the ratio of R1 and R, and is given by

$$V_{REF}x = \frac{V_{REF} \times \left(1 + \frac{R2}{R1}\right)}{\left(1 + \frac{D}{2^N} \times \frac{R2}{R1}\right)} \quad (5)$$

where:
*D* is the decimal equivalent of input code.
*N* is the number of bits.
$V_{REF}$ is the applied external reference.
$V_{REF}x$ is the reference voltage for DACs A to D.

**Table 9. $V_{REF}x$ vs. R1 and R2**

| R1, R2 | Digital Code | $V_{REF}$ |
|---|---|---|
| R1 = R2 | 0000 0000 0000 | 2 $V_{REF}$ |
| R1 = R2 | 1000 0000 0000 | 1.3 $V_{REF}$ |
| R1 = R2 | 1111 1111 1111 | $V_{REF}$ |
| R1 = 3R2 | 0000 0000 0000 | 4 $V_{REF}$ |
| R1 = 3R2 | 1000 0000 0000 | 1.6 $V_{REF}$ |
| R1 = 3R2 | 1111 1111 1111 | $V_{REF}$ |

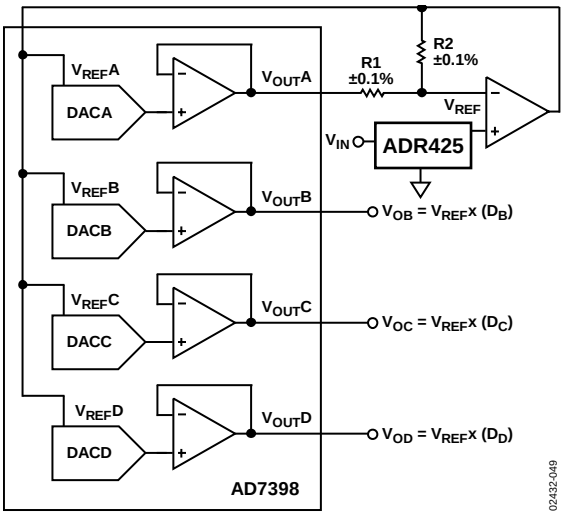



*Figure 47. Programmable DAC Reference*

## PRECISION VOLTAGE REFERENCE FOR DATA CONVERTERS

The ADR42x family has a number of features that make it ideal for use with ADCs and DACs. The exceptionally low noise, tight temperature coefficient, and high accuracy characteristics make the ADR42x ideal for low noise applications such as cellular base station applications.

AD7701 is an example of an ADC that is well suited for the ADR42x. The ADR421 is used as the precision reference for the converter in Figure 48. The AD7701 is a 16-bit ADC with on-chip digital filtering intended for measuring wide dynamic range and low frequency signals, such as those representing chemical, physical, or biological processes. It contains a charge-balancing (Σ-Δ) ADC, calibration microcontroller with on-chip static RAM, clock oscillator, and serial communications port.

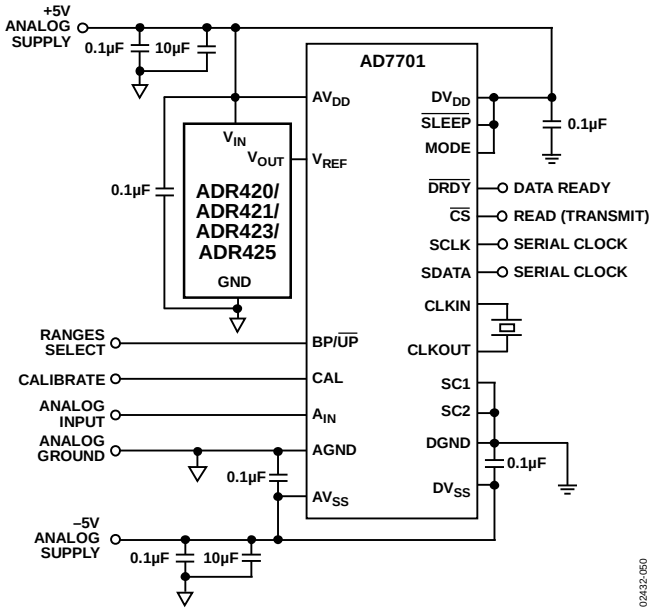



*Figure 48. Voltage Reference for 16-Bit ADC AD7701*

## PRECISION BOOSTED OUTPUT REGULATOR

A precision voltage output with boosted current capability can be realized with the circuit shown in Figure 49. In this circuit, U2 forces $V_{OUT}$ to be equal to $V_{REF}$ by regulating the turn on of N1. Therefore, the load current is furnished by $V_{IN}$. In this configuration, a 50 mA load is achievable at $V_{IN}$ of 5 V. Moderate heat is generated on the MOSFET, and higher current can be achieved by replacing the larger device. In addition, for a heavy capacitive load with step input, a buffer may be added at the output to enhance the transient response.

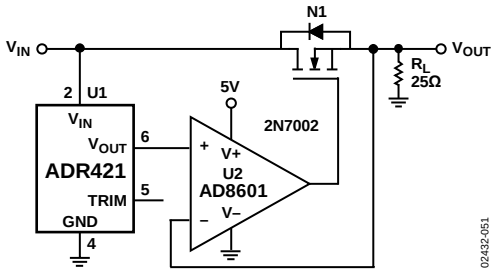
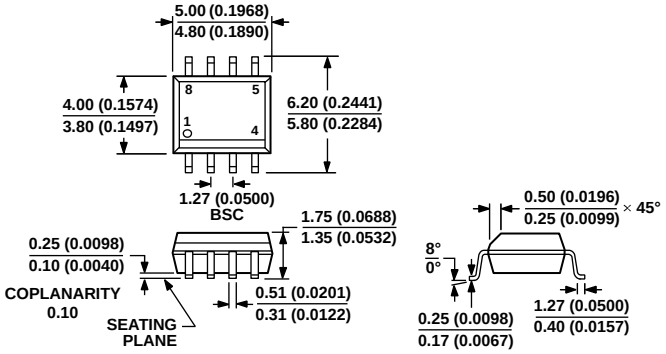


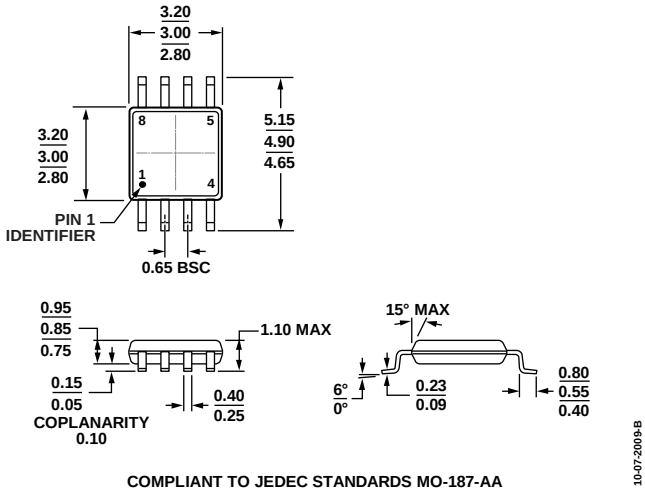

*Figure 49. Precision Boosted Output Regulator*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

*Figure 50. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*




COMPLIANT TO JEDEC STANDARDS MO-187-AA

*Figure 51. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Output Voltage, $V_{OUT}$ (V) | Initial Accuracy | | Temperature Coefficient (ppm/°C) | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|---|---|---|---|
| | | mV | % | | | | | |
| ADR420ARZ | 2.048 | 3 | 0.15 | 10 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR420ARZ-REEL7 | 2.048 | 3 | 0.15 | 10 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR420ARMZ | 2.048 | 3 | 0.15 | 10 | −40°C to +125°C | 8-Lead MSOP | RM-8 | L0C |
| ADR420ARMZ-REEL7 | 2.048 | 3 | 0.15 | 10 | −40°C to +125°C | 8-Lead MSOP | RM-8 | L0C |
| ADR420BRZ | 2.048 | 1 | 0.05 | 3 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR420BRZ-REEL7 | 2.048 | 1 | 0.05 | 3 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR421ARZ | 2.50 | 3 | 0.12 | 10 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR421ARZ-REEL7 | 2.50 | 3 | 0.12 | 10 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR421ARMZ | 2.50 | 3 | 0.12 | 10 | −40°C to +125°C | 8-Lead MSOP | RM-8 | R06 |
| ADR421ARMZ-REEL7 | 2.50 | 3 | 0.12 | 10 | −40°C to +125°C | 8-Lead MSOP | RM-8 | R06 |
| ADR421BR | 2.50 | 1 | 0.04 | 3 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR421BR-REEL7 | 2.50 | 1 | 0.04 | 3 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR421BRZ | 2.50 | 1 | 0.04 | 3 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR421BRZ-REEL7 | 2.50 | 1 | 0.04 | 3 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR423ARZ | 3.00 | 4 | 0.13 | 10 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR423ARZ-REEL7 | 3.00 | 4 | 0.13 | 10 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR423ARMZ | 3.00 | 4 | 0.13 | 10 | −40°C to +125°C | 8-Lead MSOP | RM-8 | R0U |
| ADR423ARMZ-REEL7 | 3.00 | 4 | 0.13 | 10 | −40°C to +125°C | 8-Lead MSOP | RM-8 | R0U |
| ADR423BRZ | 3.00 | 1.5 | 0.04 | 3 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR423BRZ-REEL7 | 3.00 | 1.5 | 0.04 | 3 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR425ARZ | 5.00 | 6 | 0.12 | 10 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR425ARZ-REEL7 | 5.00 | 6 | 0.12 | 10 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR425ARMZ | 5.00 | 6 | 0.12 | 10 | −40°C to +125°C | 8-Lead MSOP | RM-8 | R7A# |
| ADR425ARMZ-REEL7 | 5.00 | 6 | 0.12 | 10 | −40°C to +125°C | 8-Lead MSOP | RM-8 | R7A# |
| ADR425BRZ | 5.00 | 2 | 0.04 | 3 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADR425BRZ-REEL7 | 5.00 | 2 | 0.04 | 3 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |

[1] Z = RoHS Compliant Part. # denotes RoHS-compliant product may be top or bottom marked.

# NOTES


D02432-0-12/13(J)