

TABLE OF CONTENTS

| | |
|--|---|
| Features | 1 |
| Applications | 1 |
| General Description | 1 |
| Functional Block Diagram | 1 |
| Revision History | 2 |
| Specifications..... | 3 |
| Timing Characteristics | 4 |
| Absolute Maximum Ratings..... | 5 |
| ESD Caution..... | 5 |
| Pin Configuration and Function Descriptions..... | 6 |
| Typical Performance Characteristics | 7 |
| PCB Land Pattern Layout | 8 |
| Alternate PCB Land Patterns | 9 |

REVISION HISTORY

11/11—Rev. C to Rev. D

| | |
|---|-----------|
| Changed PSRR to PSR | Universal |
| Changed Pb-Free Temperature from 245°C to 260°C, Table 4 .. | 5 |
| Changes to Figure 8 and Figure 9..... | 8 |
| Added Alternate PCB Land Patterns Section | 9 |
| Changes to Temperature Humidity Bias (THB) Description, Table 6 | 12 |

8/11—Rev. B to Rev. C

| | |
|---|----|
| Changes to Clock Frequency and Supply Voltage Parameters, Table 1 | 3 |
| Changes to Table 3 and Table 4..... | 5 |
| Deleted Power-Saving Features Section | 8 |
| Changes to Figure 9 | 8 |
| Added Applications Information Section | 9 |
| Added Supporting Documents, Evaluation Board User Guides, Circuit Note, and Application Notes Sections | 9 |
| Changes to Interfacing with Analog Devices Codecs Section..... | 9 |
| Moved Sleep Mode Section and Power Savings When Disabling One Microphone in a Multimicrophone Application Section ... | 9 |
| Changes to Figure 10..... | 9 |
| Change to Pick-and-Place Equipment Section..... | 10 |
| Deleted Evaluation Board Section..... | 10 |
| Deleted Figure 10 and Figure 11; Renumbered Sequentially ... | 10 |
| Deleted Table 6; Renumbered Sequentially..... | 10 |
| Deleted Figure 12..... | 11 |
| Change to Temperature Cycle Description, Table 6 | 11 |
| Changes to Ordering Guide | 12 |

| | |
|---|----|
| Applications Information | 10 |
| Interfacing with Analog Devices Codecs..... | 10 |
| Sleep Mode | 10 |
| Power Savings When Disabling One Microphone in a Multimicrophone Application..... | 10 |
| Supporting Documents | 10 |
| Handling Instructions..... | 11 |
| Pick-and-Place Equipment | 11 |
| Reflow Solder..... | 11 |
| Board Wash | 11 |
| Reliability Specifications..... | 12 |
| Outline Dimensions | 13 |
| Ordering Guide | 13 |

6/11—Rev. A to Rev. B

| | |
|--------------------------|---|
| Changes to Figure 1..... | 1 |
| Changes to Figure 5..... | 7 |

2/11—Rev. 0 to Rev. A

| | |
|---|----|
| Changes to Features Section, Applications Section, and General Description Section | 1 |
| Added Dynamic Range Parameter, Changes to Input Characteristics Parameter and Output Characteristics Parameter, Deleted Polarity Parameter, Table 1 | 3 |
| Changes to Table 3..... | 5 |
| Changes to Table 5..... | 6 |
| Added Power-Saving Features Section | 8 |
| Updated Outline Dimensions | 13 |
| Changes to Ordering Guide | 13 |

4/10—Revision 0: Initial Version

SPECIFICATIONS

$T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$, $\text{CLK} = 2.4\text{ MHz}$, unless otherwise noted. All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.

Table 1.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---------------------------------|----------|--|----------------------|------------------|----------------------|---------------|
| PERFORMANCE | | | | | | |
| Directionality | | | | Omni | | |
| Sensitivity ¹ | | 1 kHz, 94 dB SPL | -29 | -26 | -23 | dBFS |
| Signal-to-Noise Ratio | SNR | 20 kHz bandwidth, A-weighted | | 61 | | dBA |
| Equivalent Input Noise | EIN | 20 kHz bandwidth, A-weighted | | 33 | | dBA SPL |
| Dynamic Range | | Derived from EIN and maximum acoustic input | | 87 | | dB |
| Frequency Response ² | | Low frequency -3 dB point | | 100 | | Hz |
| | | High frequency -3 dB point | | 15 | | kHz |
| | | Deviation limits from flat response within pass band | | -3/+2 | | dB |
| Total Harmonic Distortion | THD | 105 dB SPL | | | 3 | % |
| Power Supply Rejection | PSR | 217 Hz, 100 mV p-p square wave superimposed on $V_{DD} = 1.8\text{ V}$ | | 80 | | dBFS |
| Maximum Acoustic Input | | Peak | | 120 | | dB SPL |
| INPUT CHARACTERISTICS | | | | | | |
| Clock Frequency | CLK | | 1.0 | 2.4 ³ | 3.3 | MHz |
| Clock Duty Ratio | | Clock frequency of 2.4 MHz or less | 40 | | 60 | % |
| Input Voltage High | V_{IH} | | 0.65 $\times V_{DD}$ | | | V |
| Input Voltage Low | V_{IL} | | | | 0.35 $\times V_{DD}$ | V |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | V_{OH} | $I_{LOAD} = 0.5\text{ mA}$ | 0.7 $\times V_{DD}$ | V_{DD} | | V |
| Output Voltage Low | V_{OL} | $I_{LOAD} = 0.5\text{ mA}$ | | 0 | 0.3 $\times V_{DD}$ | V |
| Latency | | | | | <30 | μs |
| Wake-Up Time | | From sleep mode, power on | | | 10 | ms |
| POWER SUPPLY | | | | | | |
| Supply Voltage | V_{DD} | | 1.8 | | 3.3 | V |
| Supply Current | I_S | Normal mode Sleep mode ⁴ | | | 650 50 | μA |

¹ Relative to the rms level of a sine wave with positive amplitude equal to 100% 1s density and negative amplitude equal to 0% 1s density.

² See Figure 5 and Figure 6.

³ The microphone operates at any clock frequency between 1.0 MHz and 3.3 MHz. Some specifications may not be guaranteed at frequencies other than 2.4 MHz.

⁴ The microphone enters sleep mode when the clock is turned off or the clock frequency is less than 1 kHz.

TIMING CHARACTERISTICS

Table 2.

| Parameter | Description | Min | Max | Unit |
|---------------|---|-----|------|------|
| Input | | | | |
| t_{CLKIN} | Input clock period | 310 | 1000 | ns |
| Output | | | | |
| t_{1OUTEN} | DATA1 driven after falling clock edge | 30 | | ns |
| $t_{1OUTDIS}$ | DATA1 disabled after rising clock edge | | 20 | ns |
| t_{2OUTEN} | DATA2 driven after rising clock edge | 30 | | ns |
| $t_{2OUTDIS}$ | DATA2 disabled after falling clock edge | | 20 | ns |

Timing Diagram

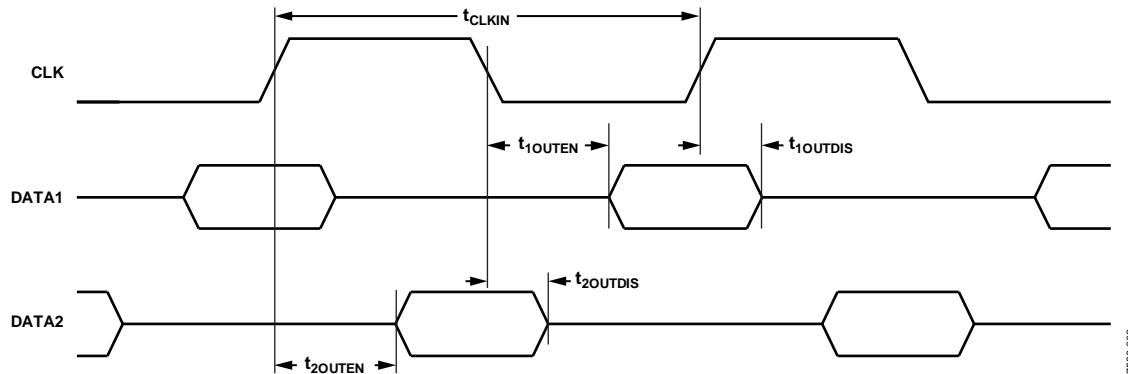


Figure 2. Pulse Density Modulated Output Timing

0796-002

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|----------------------------|--|
| Supply Voltage | -0.3 V to 3.6 V |
| Digital Pin Input Voltage | -0.3 V to $V_{DD} + 0.3$ V or 3.6 V, whichever is less |
| Sound Pressure Level (SPL) | 160 dB |
| Mechanical Shock | 10,000 g |
| Vibration | Per MIL-STD-883 Method 2007, Test Condition B |
| Temperature Range | -40°C to +85°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

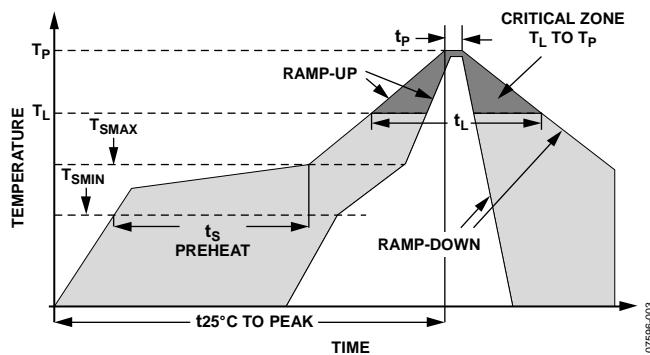


Figure 3. Recommended Soldering Profile Limits

Table 4. Recommended Soldering Profile Limits

| Profile Feature | Sn63/Pb37 | Pb Free |
|--|------------------|------------------|
| Average Ramp Rate (T_L to T_P) | 1.25°C/sec max | 1.25°C/sec max |
| Preheat | | |
| Minimum Temperature (T_{SMIN}) | 100°C | 100°C |
| Maximum Temperature (T_{SMAX}) | 150°C | 200°C |
| Time (T_{SMIN} to T_{SMAX}), t_s | 60 sec to 75 sec | 60 sec to 75 sec |
| Ramp-Up Rate (T_{SMAX} to T_L) | 1.25°C/sec | 1.25°C/sec |
| Time Maintained Above Liquidous (t_L) | 45 sec to 75 sec | ~50 sec |
| Liquidous Temperature (T_L) | 183°C | 217°C |
| Peak Temperature (T_P) | 215°C +3°C/-3°C | 260°C +0°C/-5°C |
| Time Within 5°C of Actual Peak Temperature (t_P) | 20 sec to 30 sec | 20 sec to 30 sec |
| Ramp-Down Rate | 3°C/sec max | 3°C/sec max |
| Time 25°C ($t_{25°C}$) to Peak Temperature | 5 minute max | 5 minute max |

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

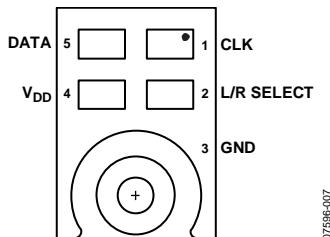


Figure 4. Pin Configuration (Bottom View)

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------------|--|
| 1 | CLK | Clock Input to Microphone. |
| 2 | L/R SELECT | Left Channel or Right Channel Select. DATA1 (right): L/R SELECT tied to GND. DATA2 (left): L/R SELECT pulled to V _{DD} . |
| 3 | GND | Ground. |
| 4 | V _{DD} | Power Supply. Placing a 0.1 μ F (100 nF) ceramic type X7R capacitor between Pin 4 (V _{DD}) and ground is strongly recommended for best performance and to avoid potential parasitic artifacts. The capacitor should be placed as close to Pin 4 as possible. |
| 5 | DATA | Digital Output Signal (DATA1, DATA2). |

TYPICAL PERFORMANCE CHARACTERISTICS

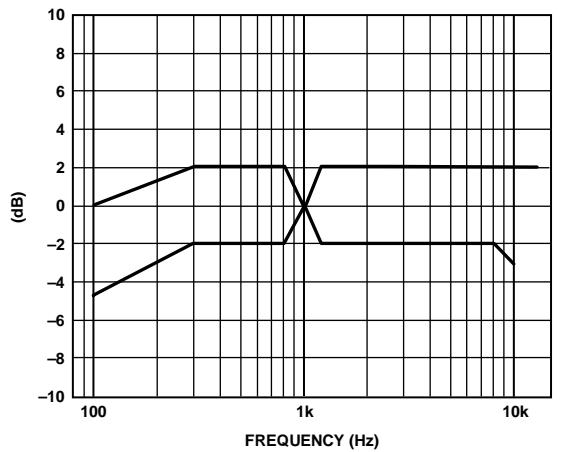


Figure 5. Frequency Response Mask

07598-004

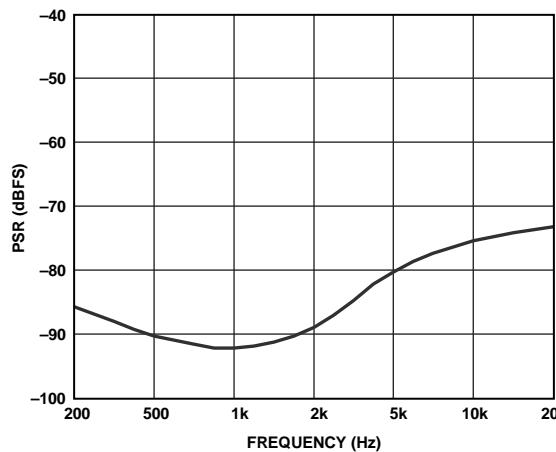


Figure 7. Typical Power Supply Rejection vs. Frequency

07598-006

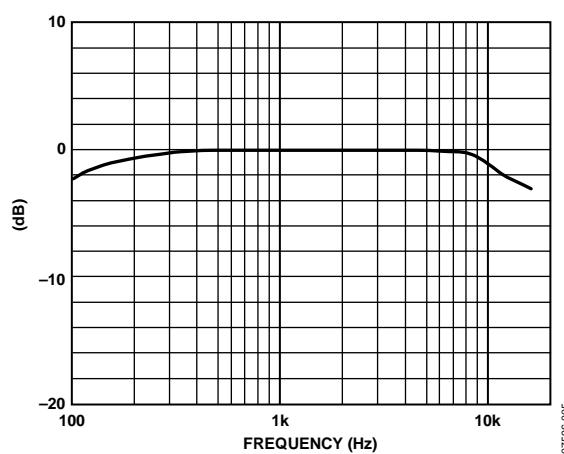


Figure 6. Typical Frequency Response (Measured)

07598-005

PCB LAND PATTERN LAYOUT

The recommended PCB land pattern for the ADMP421 should be laid out to a 1:1 ratio to the solder pads on the microphone package, as shown in Figure 8. Care should be taken to avoid applying solder paste to the sound hole in the PCB. A suggested

solder paste stencil pattern layout is shown in Figure 9. The diameter of the sound hole in the PCB should be larger than the diameter of the sound port of the microphone. A minimum diameter of 0.5 mm is recommended.

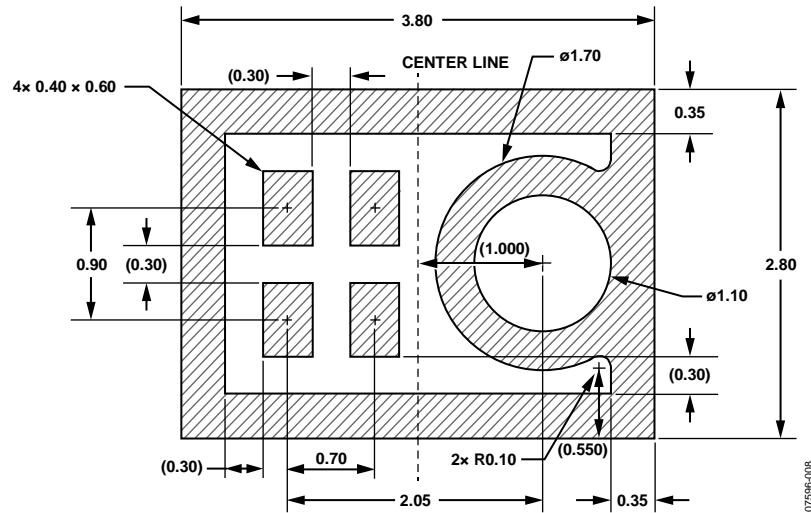


Figure 8. Suggested PCB Land Pattern Layout

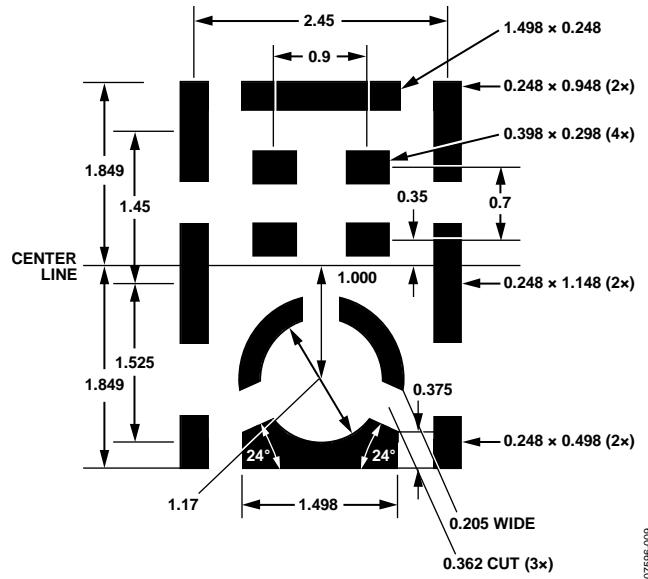


Figure 9. Suggested Solder Paste Stencil Pattern Layout

ALTERNATE PCB LAND PATTERNS

The ADMP421's standard PCB land pattern has a solid ring around the edge of the footprint, which may make routing the microphone signals more difficult in some board designs. This ring is used to improve the RF immunity performance of the ADMP421, but it is not necessary to have this full ring connected for electrical functionality. If a design can tolerate reduced RF immunity then this ring can either be broken or removed completely from the PCB footprint. Figure 10 shows an example land pattern with no enclosing ring around the edge of the part, and Figure 11 shows an example pattern with the ring broken on two sides so that the inner pads can be more easily routed on the PCB.

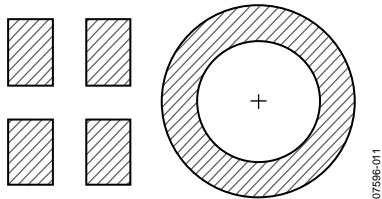


Figure 10. Example PCB Land Pattern with No Enclosing Ring

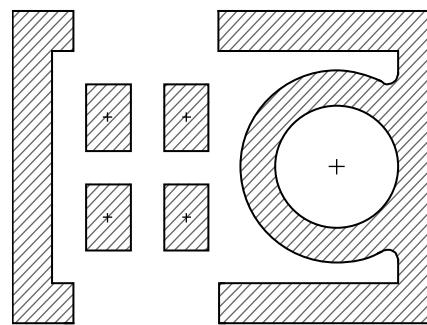


Figure 11. Example PCB Land Pattern with Broken Enclosing Ring

Note that in both of these patterns, the solid ring around the sound port is still present; this ring is needed to ground the microphone and for acoustic performance. The pad on the package connected to this ring is ground and still needs a solid electrical connection to the PCB ground. If a pattern like one of these two examples is used on a PCB, take care that the unconnected ring on the bottom of the ADMP421 is not placed directly over any exposed copper. This ring on the microphone is still at ground and any PCB traces routed underneath it need to be properly masked to avoid short circuits.

APPLICATIONS INFORMATION

INTERFACING WITH ANALOG DEVICES CODECS

Analog Devices ADAU1361, ADAU1761, and ADAU1781 codecs feature digital microphone inputs that support the ADMP421 PDM output data format. See the connection diagrams shown in Figure 12, and refer to the [AN-1003 Application Note](#) and the codecs' respective data sheets for more details on the digital microphone interface.

SLEEP MODE

The microphone enters sleep mode when the clock is turned off or the clock frequency falls below 1 kHz. In sleep mode, the microphone data output is in high impedance state and the current consumption is less than 50 μ A.

POWER SAVINGS WHEN DISABLING ONE MICROPHONE IN A MULTIMICROPHONE APPLICATION

The ADMP421 has a unique power-saving feature when used in systems where two or more microphones share the same clock and/or data lines. The microphone is designed to present high impedance on both the clock and data pins when the power supply (V_{DD}) pin is at 0 V or floating. This disabled microphone presents no load to and consumes no power from other active microphones.

SUPPORTING DOCUMENTS

Evaluation Board User Guides

UG-118, EVAL-ADMP421Z Bottom Port Digital Output MEMS Microphone Evaluation Board

UG-183, EVAL-ADMP421Z-FLEX: Bottom-Ported Digital Output MEMS Microphone Evaluation Board

Circuit Note

CN-0078, iMEMS Digital Microphone Simplifies the Interface to a SigmaDSP Audio Codec

Application Notes

AN-1003, Recommendations for Mounting and Connecting Analog Devices, Inc., Bottom-Ported MEMS Microphones

AN-1068, Reflow Soldering of the MEMS Microphone

[AN-1112](#), Microphone Specifications Explained

[AN-1124, Recommendations for Sealing Analog Devices, Inc.,
Bottom-Port MEMS Microphones from Dust and Liquid Ingress](#)

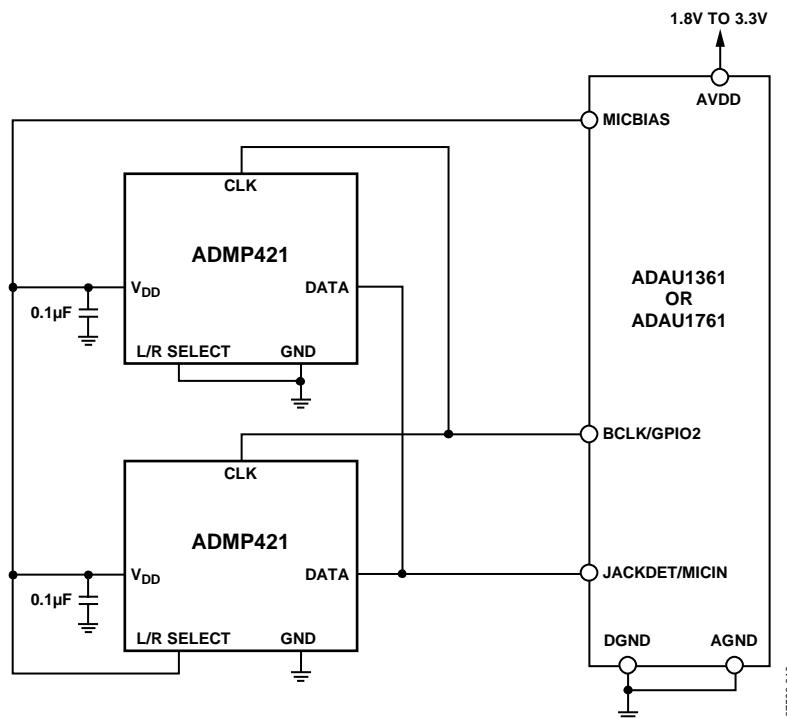


Figure 12. ADAU1361 and ADAU1761 Stereo Interface Block Diagram

HANDLING INSTRUCTIONS

PICK-AND-PLACE EQUIPMENT

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Care should be taken to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the bottom of the package, the pickup tool can make contact with any part of the lid surface.
- Use care during pick-and-place to ensure that no high shock events above 10 kg are experienced because such events may cause damage to the microphone.
- Do not pick up the microphone with a vacuum tool that makes contact with the bottom side of the microphone. Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

REFLOW SOLDER

For best results, the soldering profile should be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 3 and Table 4.

BOARD WASH

When washing the PCB, ensure that water does not make contact with the microphone port. Blow-off procedures and ultrasonic cleaning must not be used.

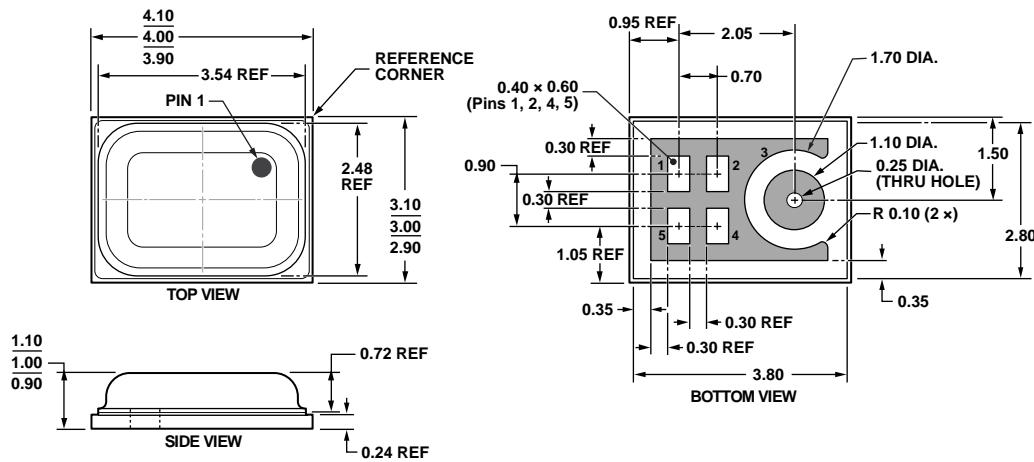
RELIABILITY SPECIFICATIONS

The microphone sensitivity after stress must deviate by no more than 3 dB from the initial value.

Table 6.

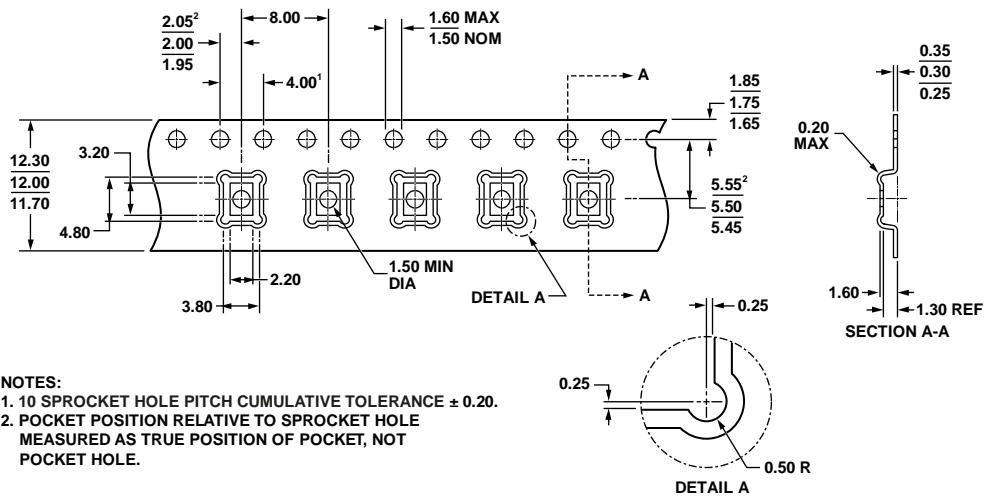
| Stress Test | Description |
|---------------------------------|--|
| Low Temperature Operating Life | -40°C, 500 hours, powered |
| High Temperature Operating Life | +125°C, 500 hours, powered |
| Temperature Humidity Bias (THB) | +85°C/85% relative humidity (RH), 500 hours, powered |
| Temperature Cycle | -40°C/+125°C, one cycle per hour, 1000 cycles |
| High Temperature Storage | +150°C, 500 hours |
| Low Temperature Storage | -40°C, 500 hours |
| Component CDM ESD | All pins, 0.5 kV |
| Component HBM ESD | All pins, 1.5 kV |
| Component MM ESD | All pins, 0.2 kV |

OUTLINE DIMENSIONS



06-16-2010-G

Figure 13. 5-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
4 mm x 3 mm Body
(CE-5-1)
Dimensions shown in millimeters



062408-A

Figure 14. LGA_CAV Tape and Reel Outline Dimensions
Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option ² | Ordering Quantity |
|--------------------|-------------------|---------------------------------------|-----------------------------|-------------------|
| ADMP421BCEZ-RL | -40°C to +85°C | 5-Terminal LGA_CAV, 13" Tape and Reel | CE-5-1 | 5,000 |
| ADMP421BCEZ-RL7 | -40°C to +85°C | 5-Terminal LGA_CAV, 7" Tape and Reel | CE-5-1 | 1,000 |
| EVAL-ADMP421Z | | Evaluation Board | | |
| EVAL-ADMP421Z-FLEX | | Flex Evaluation Board | | |

¹ Z = RoHS Compliant Part.

² This package option is halide free.

NOTES

NOTES

NOTES

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