TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
5 V Performance ... 4
3.3 V Performance ... 4
Absolute Maximum Ratings ... 5
ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
Typical Performance Characteristics ... 7
5 V Performance ... 7
3.3 V Performance ... 14
Upconversion ... 15
Spurious Performance ... 16
Circuit Description ... 17
RF Subsystem ... 17
LO Subsystem ... 17
Applications Information ... 19
Basic Connections ... 19
IF Port ... 19
Mixer VGS Control DAC ... 19
Evaluation Board ... 20
Outline Dimensions ... 23
Ordering Guide ... 23

REVISION HISTORY

3/16—Rev. B to Rev. C

Added Thermal Resistance Section and Junction to Board Thermal Impedance Section ... 5
Changes to Figure 2 ... 6
Change to Evaluation Board Section and Figure 49 ... 20

2/15—Rev. A to Rev. B

Changes to Table 1 ... 1
Deleted Figure 37 and Figure 39; Renumbered Sequentially ... 13
Deleted Bias Resistor Selection Section ... 19
Changes to Figure 49 ... 20
Changes to Table 7 ... 21
Updated Outline Dimensions ... 23
Changes to Ordering Guide ... 23

8/14—Rev. 0 to Rev. A

Changes to General Description Section ... 1
Changes to Table 7 ... 21
Updated Outline Dimensions ... 23

10/09—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, I_S = 95 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, Z_O = 50 Ω, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20 dB over a limited bandwidth		16		dB
Input Impedance			50		Ω
RF Frequency Range		1500		2700	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		36||2		Ω||pF
IF Frequency Range		dc		450	MHz
DC Bias Voltage[1]	Externally generated	3.3	5.0	5.5	V
LO INTERFACE					
LO Power		−6	0	+10	dBm
Return Loss			17		dB
Input Impedance			50		Ω
LO Frequency Range		1230		2470	MHz
POWER-DOWN (PWDN) INTERFACE[2]					
PWDN Threshold			1.0		V
Logic 0 Level				0.4	V
Logic 1 Level		1.4			V
PWDN Response Time	Device enabled, IF output to 90% of its final level		160		ns
	Device disabled, supply current < 5 mA		220		ns
PWDN Input Bias Current	Device enabled		0.0		µA
	Device disabled		70		µA

[1] Apply the supply voltage from the external circuit through the choke inductors.
[2] PWDN function is intended for use with $V_S \leq 3.6$ V only.

5 V PERFORMANCE

V_S = 5 V, I_S = 95 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

Table 3.

Parameter	Test Conditions\Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Power Conversion Loss	Including 1:1 IF port transformer and printed circuit board (PCB) loss	6.5	7.3	8.4	dB
Voltage Conversion Loss	Z_{SOURCE} = 50 Ω, differential Z_{LOAD} = 50 Ω differential				dB
SSB Noise Figure			8.3		dB
SSB Noise Figure Under Blocking	5 dBm blocker present ±10 MHz from wanted RF input, LO source filtered		18.5		dB
Input Third-Order Intercept (IIP3)	f_{RF1} = 1899.5 MHz, f_{RF2} = 1900.5 MHz, f_{LO} = 1697 MHz, each RF tone at 0 dBm	27	36		dBm
Input Second-Order Intercept (IIP2)	f_{RF1} = 1950 MHz, f_{RF2} = 1900 MHz, f_{LO} = 1697 MHz, each RF tone at 0 dBm		67		dBm
Input 1 dB Compression Point (IP1dB)[1]	Exceeding 20 dBm RF power results in damage to the device		25		dBm
LO to IF Leakage	Unfiltered IF output		−18		dBm
LO to RF Leakage			−33		dBm
RF to IF Isolation			−50		dBc
IF/2 Spurious	0 dBm input power		−65		dBc
IF/3 Spurious	0 dBm input power		−71		dBc
POWER SUPPLY					
Positive Supply Voltage		4.5	5	5.5	V
Quiescent Current	Resistor programmable		95		mA

[1] Exceeding 20 dBm RF power results in damage to the device.

3.3 V PERFORMANCE

V_S = 3.3 V, I_S = 56 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, R9 = 226 Ω, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Power Conversion Loss	Including 1:1 IF port transformer and PCB loss		7.4		dB
Voltage Conversion Loss	Z_{SOURCE} = 50 Ω, differential Z_{LOAD} = 50 Ω differential		7.1		dB
SSB Noise Figure			8.4		dB
Input Third-Order Intercept (IIP3)	f_{RF1} = 1899.5 MHz, f_{RF2} = 1900.5 MHz, f_{LO} = 1697 MHz, each RF tone at 0 dBm		32		dBm
Input Second-Order Intercept (IIP2)	f_{RF1} = 1950 MHz, f_{RF2} = 1900 MHz, f_{LO} = 1697 MHz, each RF tone at 0 dBm		58		dBm
POWER INTERFACE					
Supply Voltage		3.0	3.3	3.6	V
Quiescent Current	Resistor programmable		56		mA
Power-Down Current	Device disabled		150		µA

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage, V_S	5.5 V
RF Input Level	20 dBm
LO Input Level	13 dBm
IFOP, IFON Bias Voltage	6.0 V
VGS0, VGS1, LOSW, PWDN	5.5 V
Internal Power Dissipation	1.2 W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is thermal resistance, junction to ambient (°C/W), and θ_{JB} is thermal impedance, junction to board (°C/W).

Table 6. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JB}[1]	Unit
20-Lead LFCSP	25	14.74	°C/W

[1] See the JEDEC standard, JESD51-2, for information on optimizing thermal impedance (PCB with 3 × 3 vias).

Junction to Board Thermal Impedance

The junction to board thermal impedance (θ_{JB}) is the thermal impedance from the die to or near the component lead of the ADL5365. For the ADL5365, θ_{JB} is determined experimentally to 14.74°C/W with the device mounted on a 4-layer circuit board with two layers as ground planes in a configuration similar to the ADL5365-EVALZ evaluation board. Board size and complexity (number of layers) affect θ_{JB}; more layers tend to reduce the thermal impedance slightly.

If the board temperature is known, use the junction to board thermal impedance to calculate die temperature (also known as junction temperature) to ensure it does not exceed the specified limit of 150°C. For example if the board temperature is 85°C, the die temperature is given by the equation

$$T_J = T_B + (P_{DISS} \times \theta_{JB})$$

where T_J is the junction temperature.
T_B is the board temperature measured at or near the component lead.
P_{DISS} is the power dissipated from the part.

The typical worst case power dissipation for the ADL5365 is 523 mW (5.5V × 97mA). Therefore T_J is

$$T_J = 85°C + (0.523\ W \times 14.74°C/W) = 92.9°C$$

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

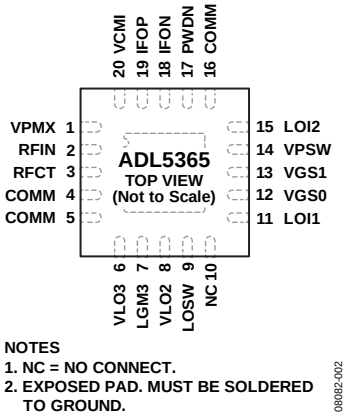

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VPMX	Positive Supply Voltage.
2	RFIN	RF Input. Must be ac-coupled.
3	RFCT	RF Balun Center Tap (AC Ground).
4, 5, 16	COMM	Device Common (DC Ground).
6, 8	VLO3, VLO2	Positive Supply Voltages for LO Amplifier.
7	LGM3	LO Amplifier Bias Control.
9	LOSW	LO Switch. LOI1 selected for 0 V, or LOI2 selected for 3 V.
10	NC	No Connect.
11, 15	LOI1, LOI2	LO Inputs. These pins must be ac-coupled.
12, 13	VGS0, VGS1	Mixer Gate Bias Controls. 3 V logic. Ground these pins for nominal setting.
14	VPSW	Positive Supply Voltage for LO Switch.
17	PWDN	Power-Down. Connect this pin to ground for normal operation or connect this pin to 3.0 V for disable mode.
18, 19	IFON, IFOP	Differential IF Outputs.
20	VCMI	No Connect. This pin can be grounded.
	EPAD (EP)	Exposed pad must be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

5 V PERFORMANCE

V_S = 5 V, I_S = 95 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

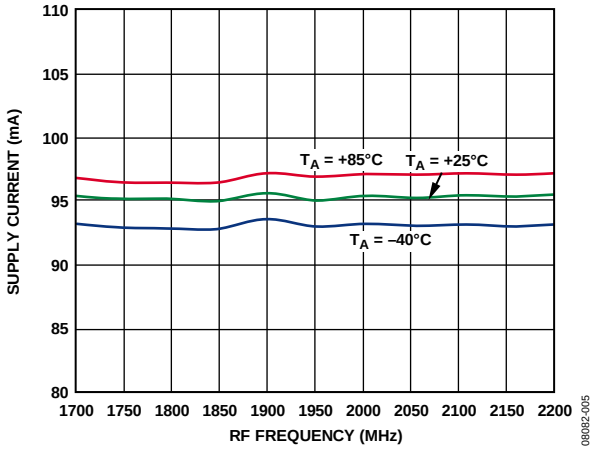

Figure 3. Supply Current vs. RF Frequency

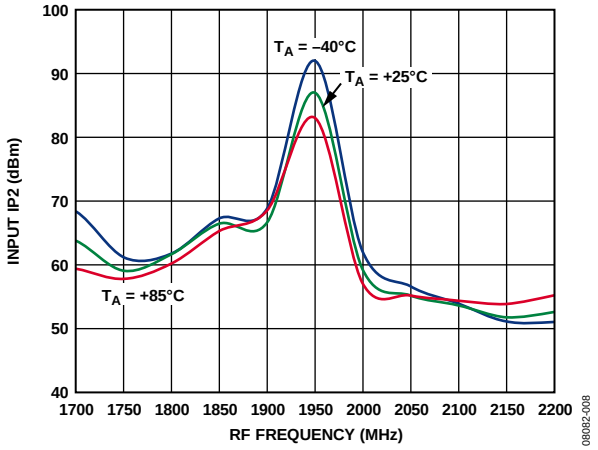

Figure 6. Input IP2 vs. RF Frequency

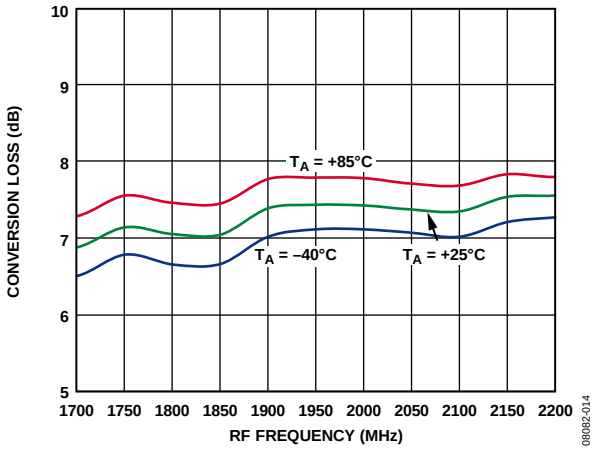

Figure 4. Power Conversion Loss vs. RF Frequency

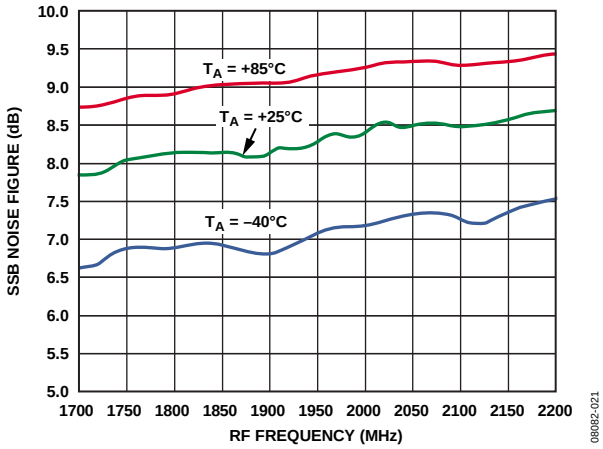

Figure 7. SSB Noise Figure vs. RF Frequency

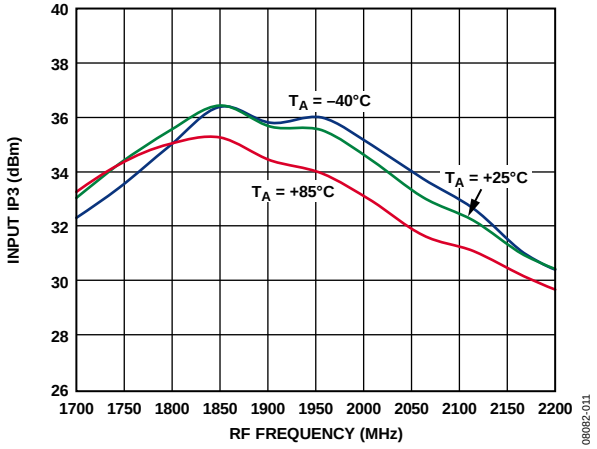

Figure 5. Input IP3 vs. RF Frequency

V_S = 5 V, I_S = 95 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

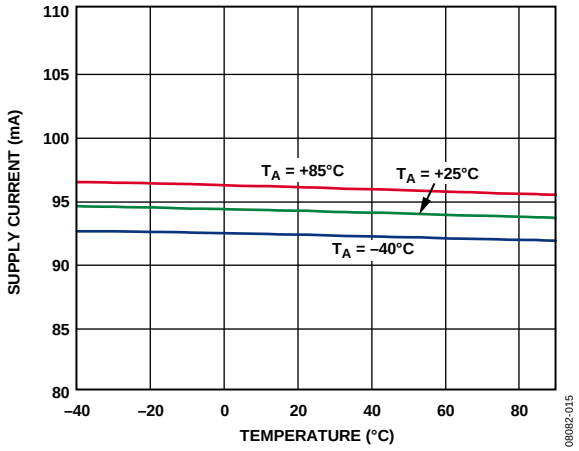

Figure 8. Supply Current vs. Temperature

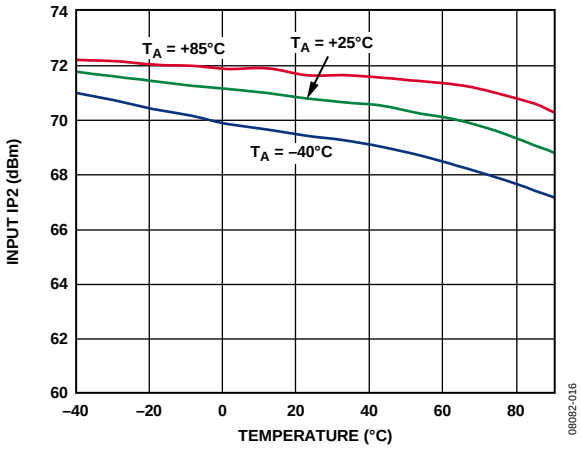

Figure 11. Input IP2 vs. Temperature

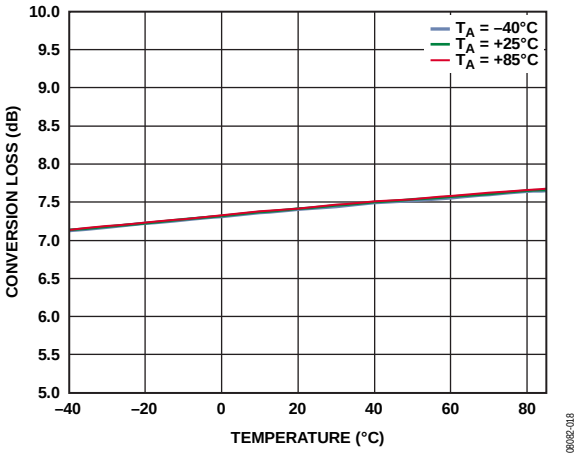

Figure 9. Power Conversion Loss vs. Temperature

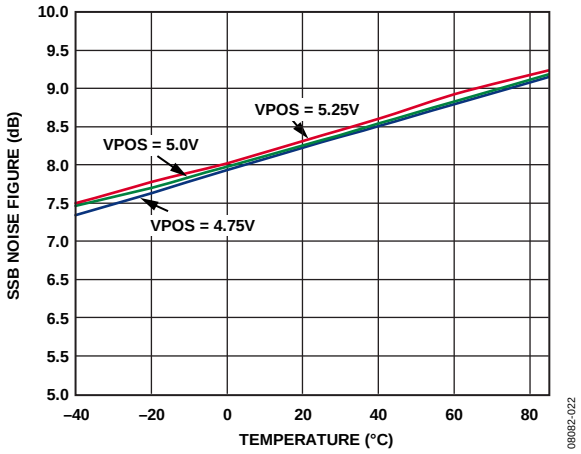

Figure 12. SSB Noise Figure vs. Temperature

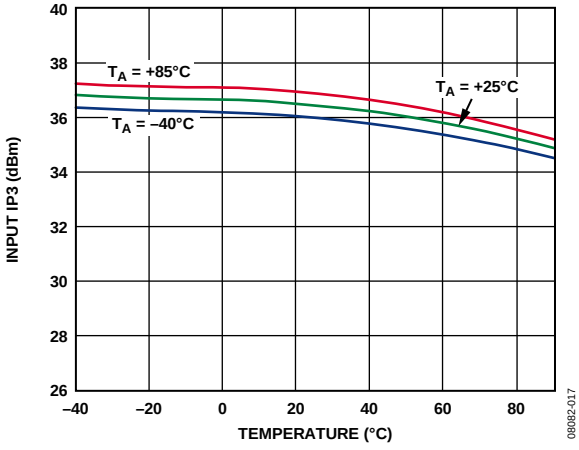

Figure 10. Input IP3 vs. Temperature

V_S = 5 V, I_S = 95 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

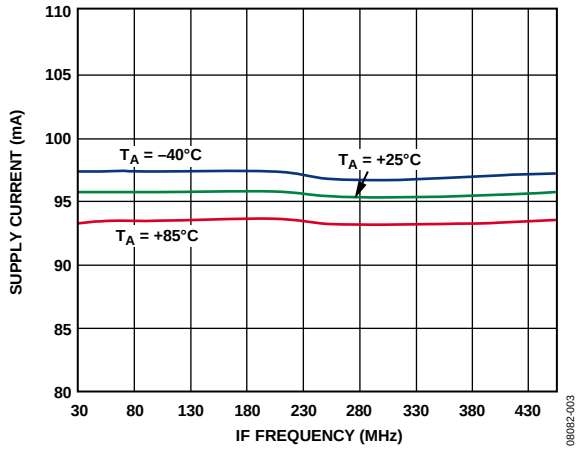

Figure 13. Supply Current vs. IF Frequency

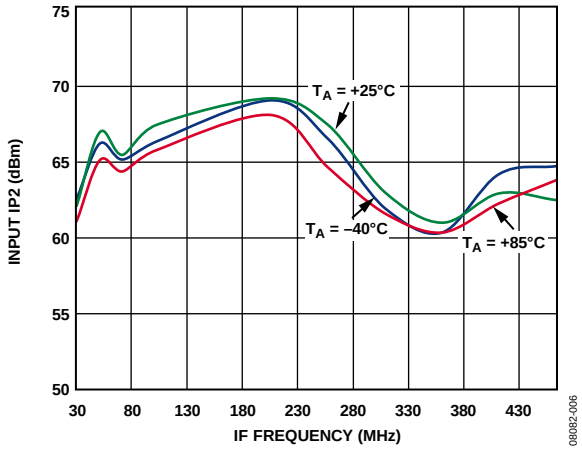

Figure 16. Input IP2 vs. IF Frequency

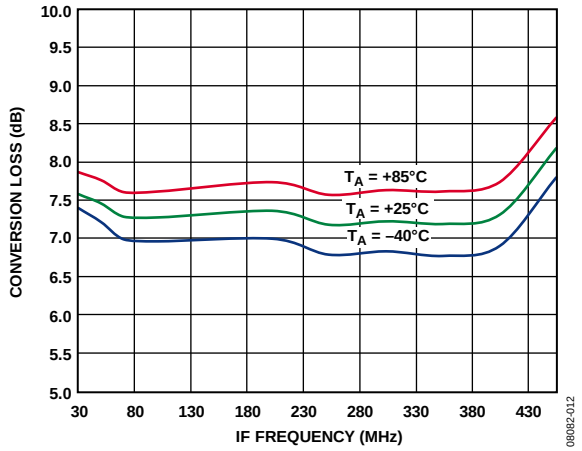

Figure 14. Power Conversion Loss vs. IF Frequency

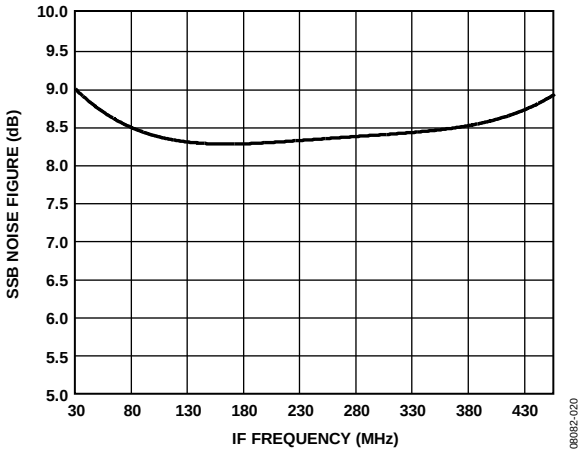

Figure 17. SSB Noise Figure vs. IF Frequency

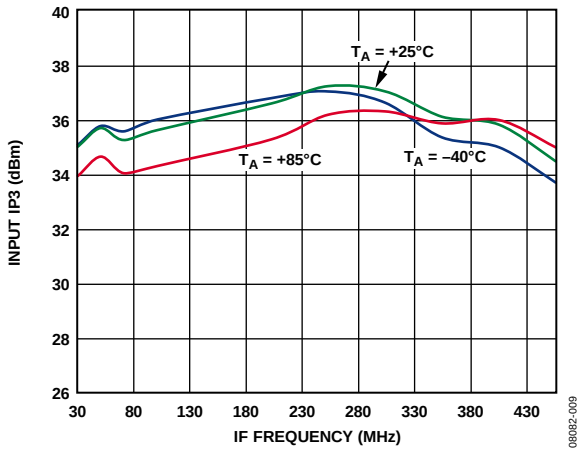

Figure 15. Input IP3 vs. IF Frequency

V_S = 5 V, I_S = 95 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

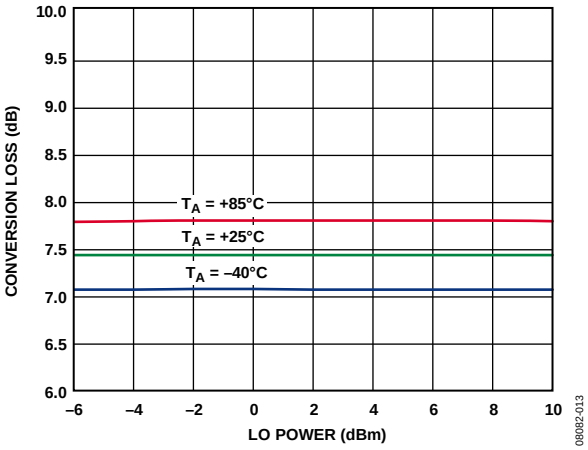

Figure 18. Power Conversion Loss vs. LO Power

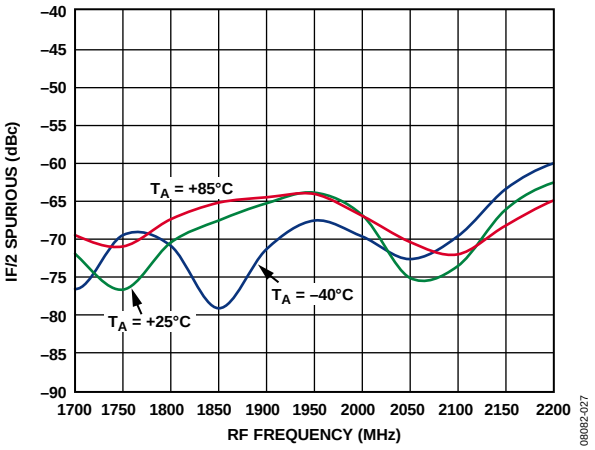

Figure 21. IF/2 Spurious vs. RF Frequency

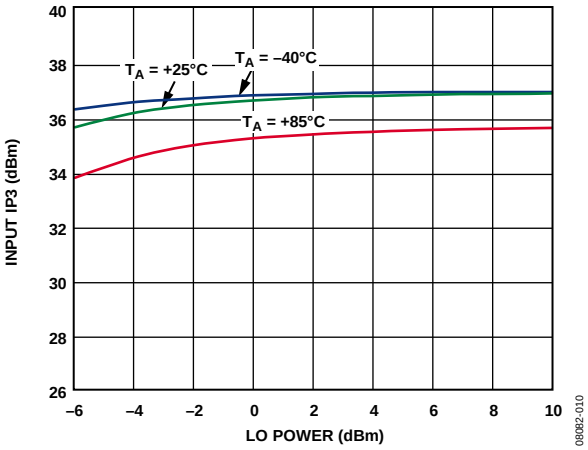

Figure 19. Input IP3 vs. LO Power

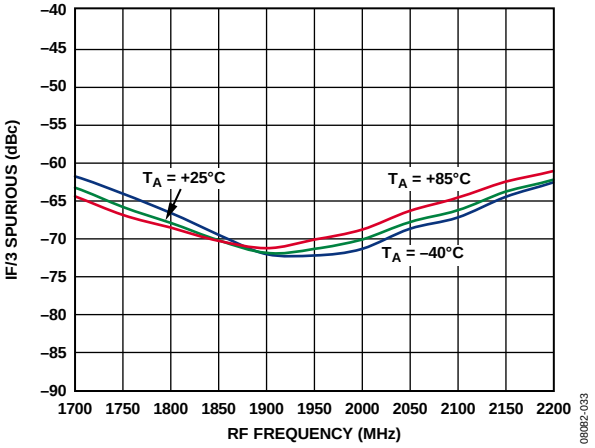

Figure 22. IF/3 Spurious vs. RF Frequency

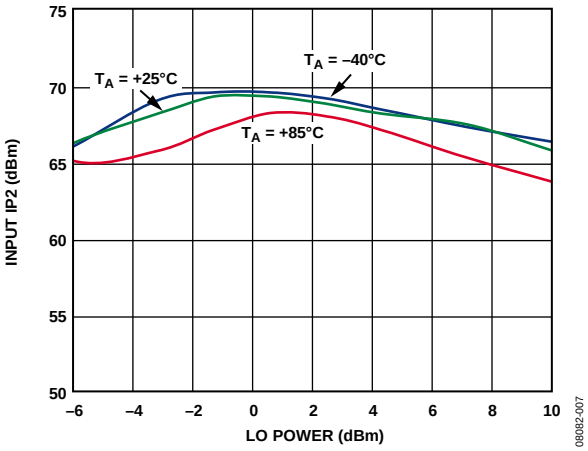

Figure 20. Input IP2 vs. LO Power

V_S = 5 V, I_S = 95 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

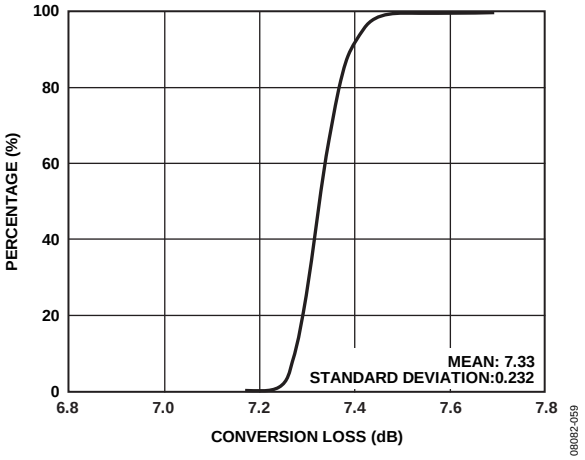

Figure 23. Conversion Loss Distribution

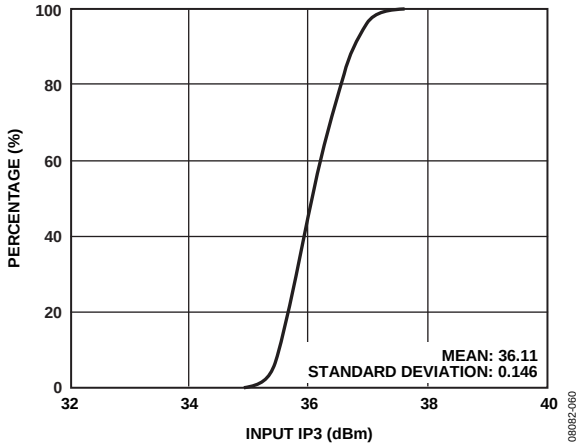

Figure 24. Input IP3 Distribution

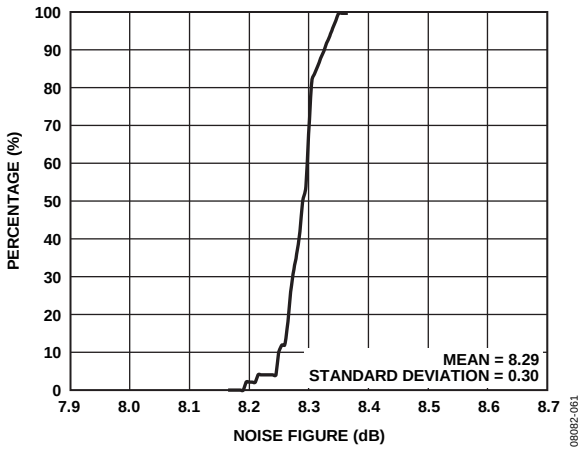

Figure 25. SSB Noise Figure Distribution

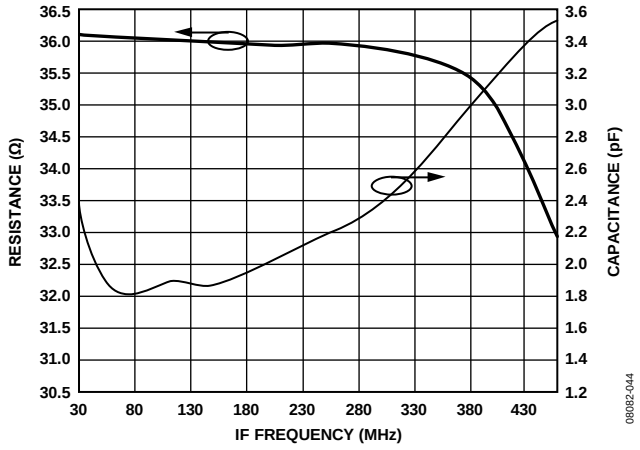

Figure 26. IF Output Impedance (R Parallel, C Equivalent)

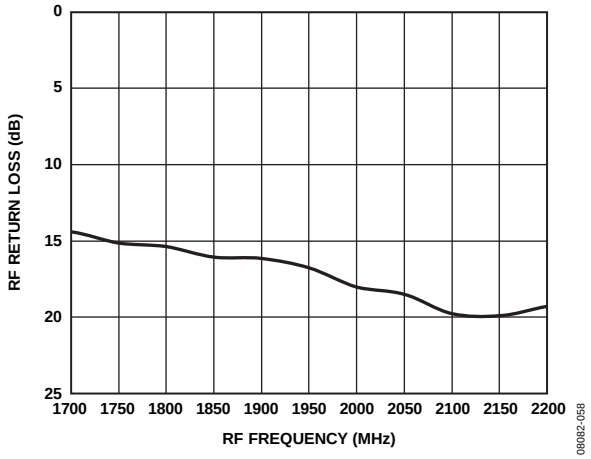

Figure 27. RF Port Return Loss, Fixed IF

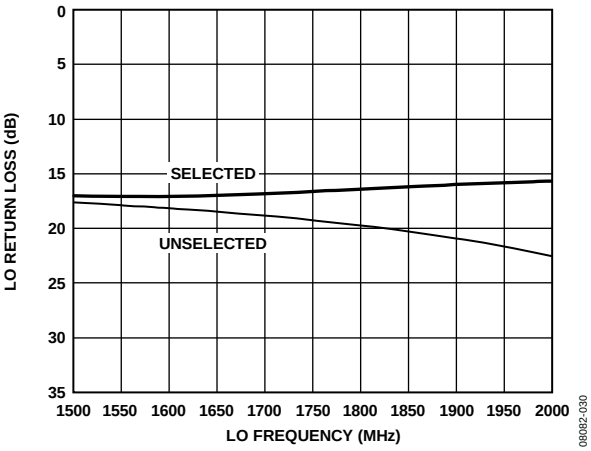

Figure 28. LO Return Loss, Selected and Unselected

V_S = 5 V, I_S = 95 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

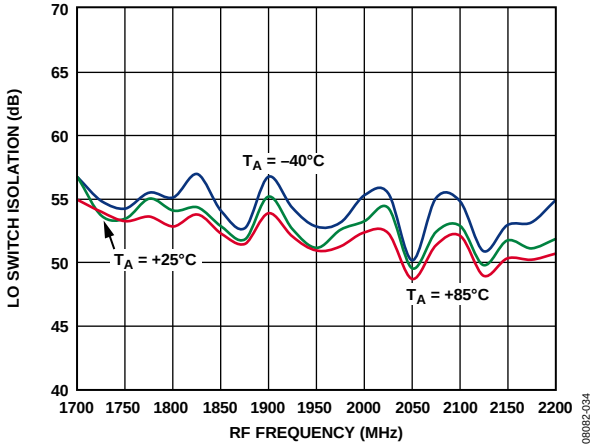

Figure 29. LO Switch Isolation vs. RF Frequency

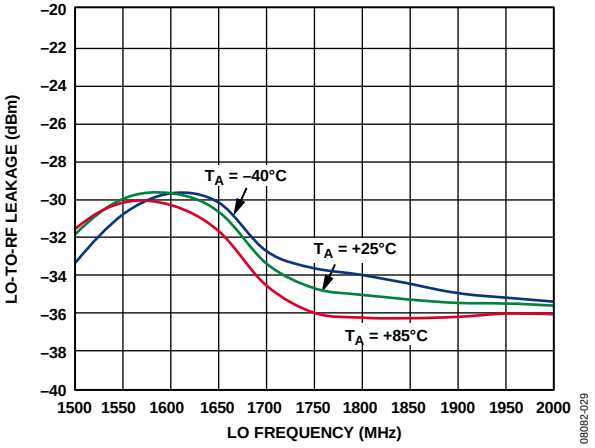

Figure 32. LO to RF Leakage vs. LO Frequency

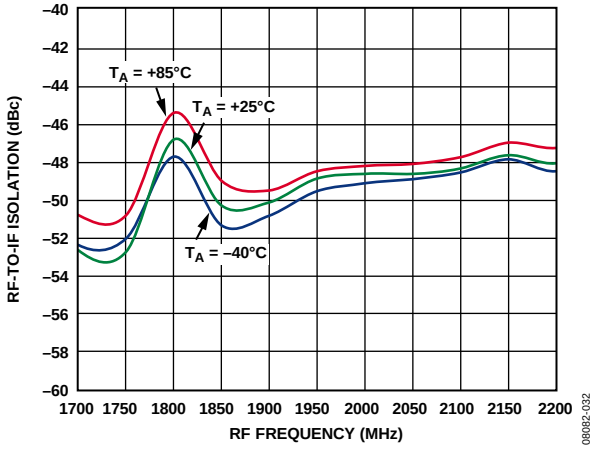

Figure 30. RF to IF Isolation vs. RF Frequency

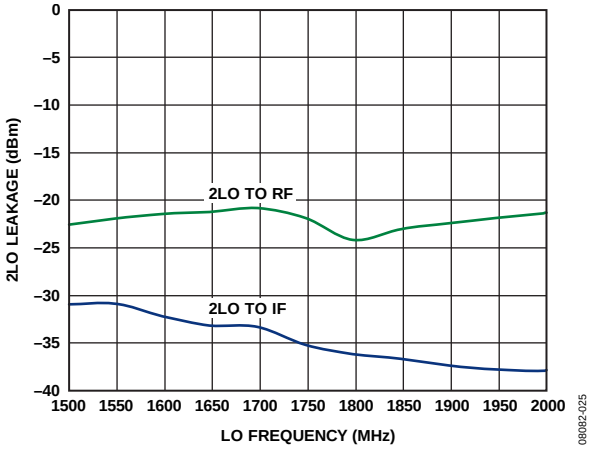

Figure 33. 2LO Leakage vs. LO Frequency

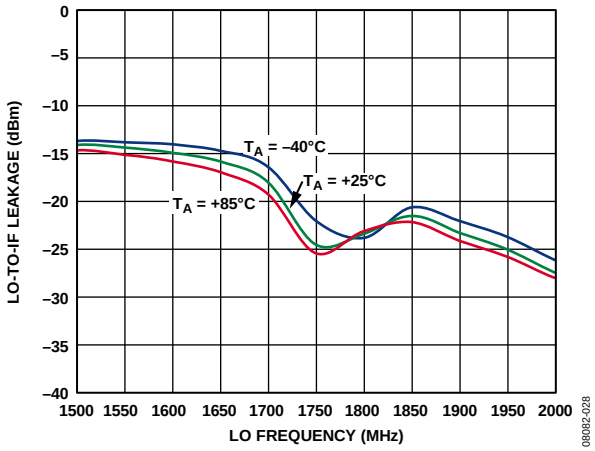

Figure 31. LO to IF Leakage vs. LO Frequency

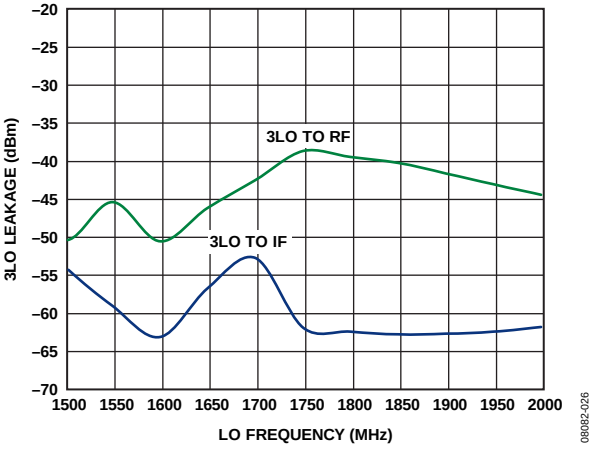

Figure 34. 3LO Leakage vs. LO Frequency

V_S = 5 V, I_S = 95 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

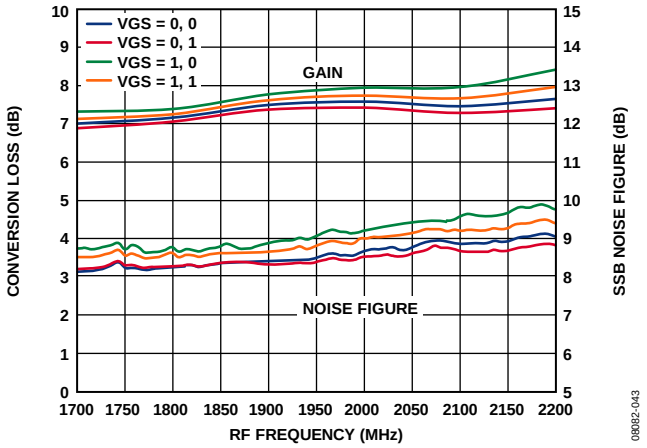

Figure 35. Power Conversion Loss and SSB Noise Figure vs. RF Frequency

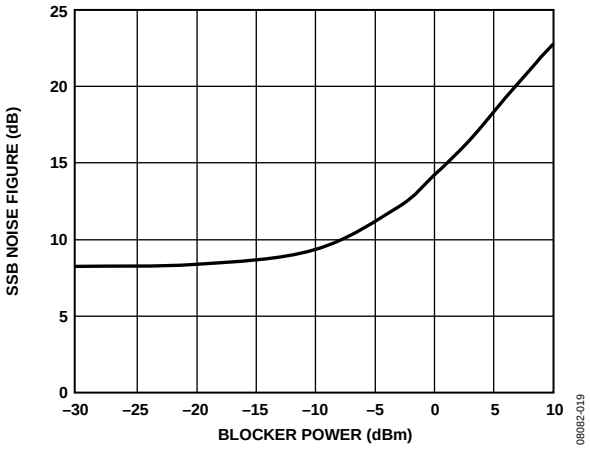

Figure 37. SSB Noise Figure vs.10 MHz Offset Blocker Power

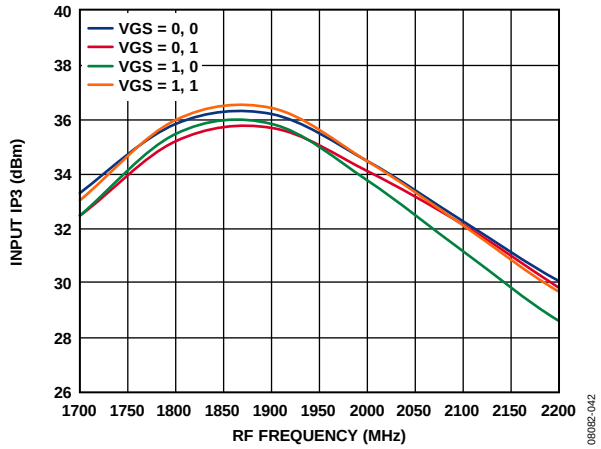

Figure 36. Input IP3 vs. RF Frequency

3.3 V PERFORMANCE

V_S = 3.3 V, I_S = 56 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, RF power = 0 dBm, R9 = 226 Ω, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

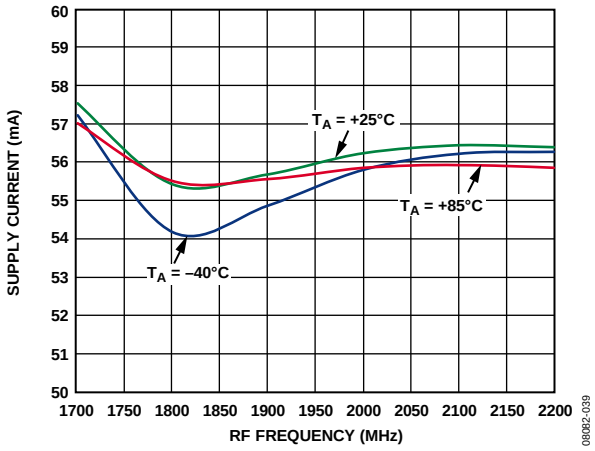

Figure 38. Supply Current vs. RF Frequency at 3.3 V

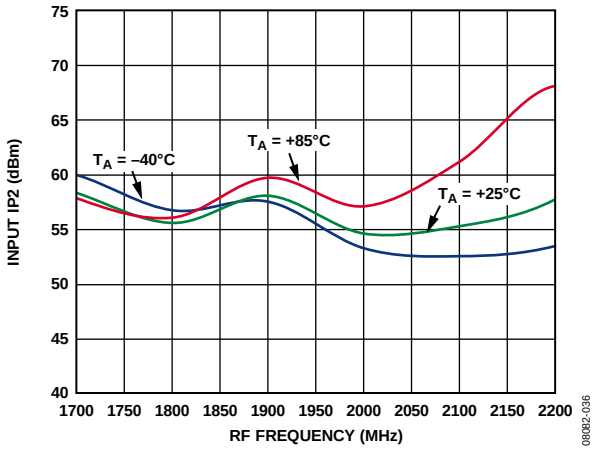

Figure 41. Input IP2 vs. RF Frequency at 3.3 V

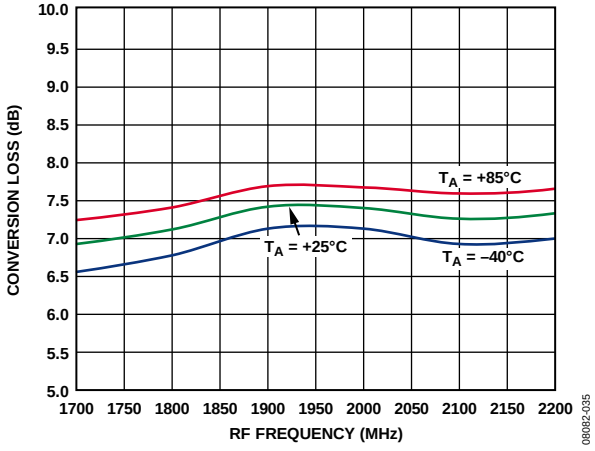

Figure 39. Power Conversion Loss vs. RF Frequency at 3.3 V

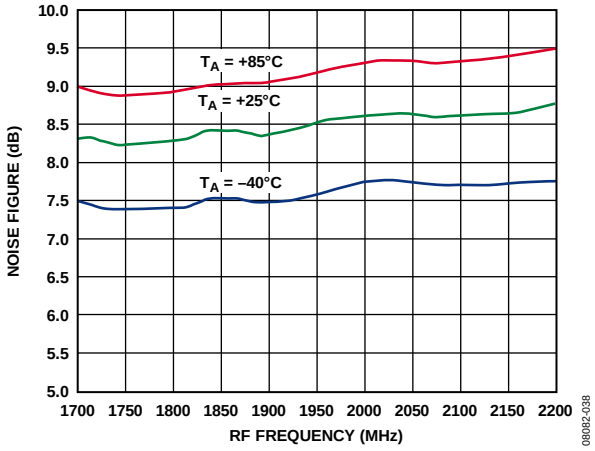

Figure 42. SSB Noise Figure vs. RF Frequency at 3.3 V

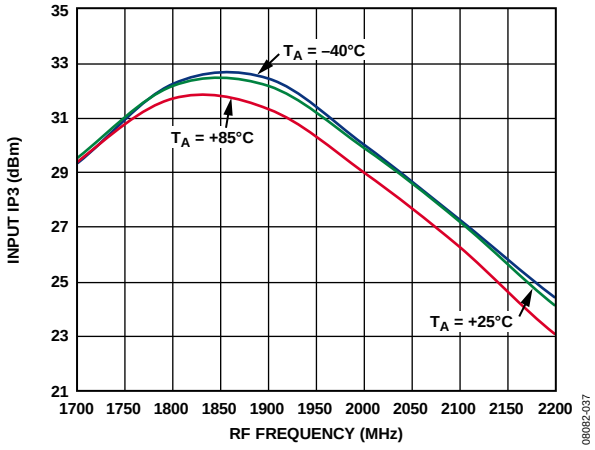

Figure 40. Input IP3 vs. RF Frequency at 3.3 V

UPCONVERSION

T_A = 25°C, f_{IF} = 153 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

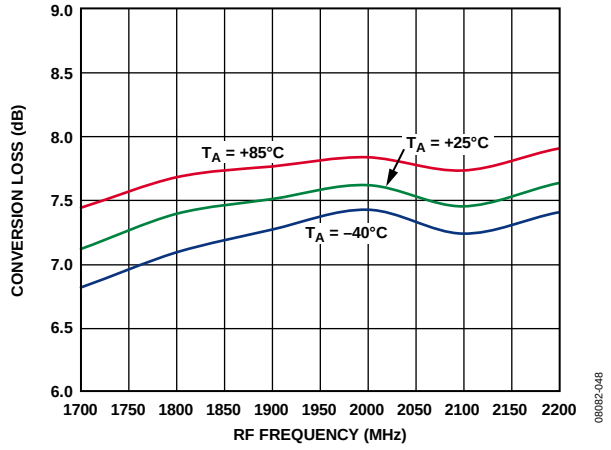

Figure 43. Power Conversion Loss vs. RF Frequency, V_S = 5 V, Upconversion

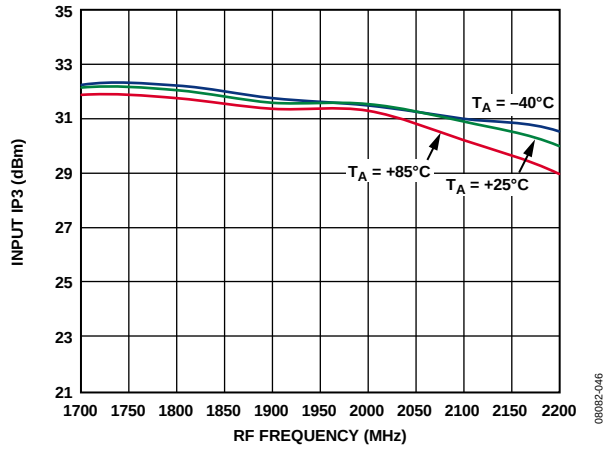

Figure 44. Input IP3 vs. RF Frequency, V_S = 5 V, Upconversion

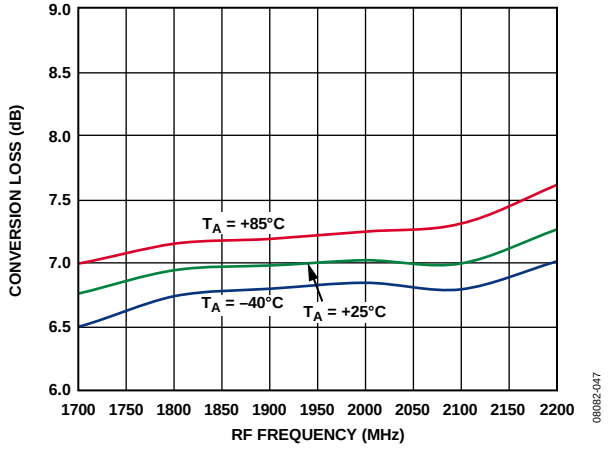

Figure 45. Power Conversion Loss vs. RF Frequency at 3.3 V, Upconversion

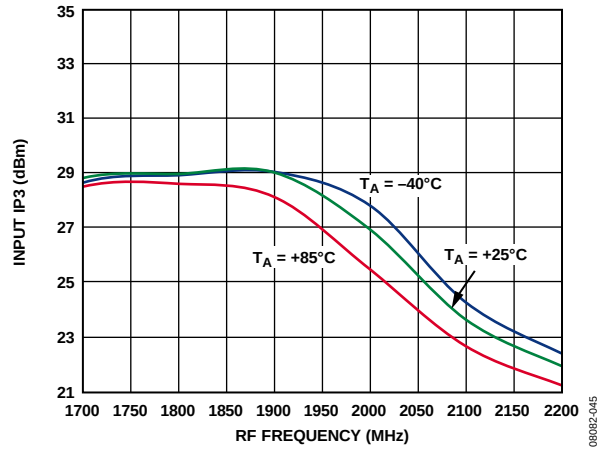

Figure 46. Input IP3 vs. RF Frequency at 3.3 V, Upconversion

SPURIOUS PERFORMANCE

(N × f_{RF}) − (M × f_{LO}) spur measurements were made using the standard evaluation board. Mixer spurious products are measured in dBc from the IF output power level. Data was measured only for frequencies less than 6 GHz. Typical noise floor of the measurement system = −100 dBm.

5 V Performance

V_S = 5 V, I_S = 95 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, RF power = 0 dBm, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0		−10.9	−28.3	−44.5												
	1	−42.2	0.0	−49.3	−31.2	−49.8											
	2	−75.8	−76.5	−64.6	−78.4	−78.5	−94.7										
	3	<−100	−83.0	<−100	−73.5	−90.9	−89.8	<−100									
	4		<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100							
	5				<−100	<−100	<−100	<−100	<−100	<−100	<−100						
	6					<−100	<−100	<−100	<−100	<−100	<−100	<−100					
	7						<−100	<−100	<−100	<−100	<−100	<−100	<−100				
	8							<−100	<−100	<−100	<−100	<−100	<−100	<−100			
	9								<−100	<−100	<−100	<−100	<−100	<−100	<−100		
	10									<−100	<−100	<−100	<−100	<−100	<−100	<−100	
	11										<−100	<−100	<−100	<−100	<−100	<−100	<−100
	12											<−100	<−100	<−100	<−100	<−100	<−100
	13													<−100	<−100	<−100	<−100
	14														<−100	<−100	<−100
	15															<−100	<−100

3.3 V Performance

V_S = 3.3 V, I_S = 56 mA, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, RF power = 0 dBm, R9 = 226 Ω, VGS0 = VGS1 = 0 V, and Z_O = 50 Ω, unless otherwise noted.

		M															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
N	0		−16.9	−35.1	−61.4												
	1	−41.9	0.0	−49.1	−30.4	−52.6											
	2	−72.3	−80.3	−62.7	−68.5	−71.9	<−100										
	3	−94.6	−71.6	<−100	−61.2	−92.7	−75.1	<−100									
	4		<−100	<−100	<−100	<−100	<−100	<−100	<−100	<−100							
	5				<−100	<−100	<−100	<−100	<−100	<−100	<−100						
	6					<−100	<−100	<−100	<−100	<−100	<−100	<−100					
	7						<−100	<−100	<−100	<−100	<−100	<−100	<−100				
	8							<−100	<−100	<−100	<−100	<−100	<−100	<−100			
	9								<−100	<−100	<−100	<−100	<−100	<−100	<−100		
	10									<−100	<−100	<−100	<−100	<−100	<−100	<−100	
	11										<−100	<−100	<−100	<−100	<−100	<−100	<−100
	12											<−100	<−100	<−100	<−100	<−100	<−100
	13													<−100	<−100	<−100	<−100
	14														<−100	<−100	<−100
	15															<−100	<−100

CIRCUIT DESCRIPTION

The ADL5365 consists of two primary components: the radio frequency (RF) subsystem and the local oscillator (LO) subsystem. The combination of design, process, and packaging technology allows the functions of these subsystems to be integrated into a single die, using mature packaging and interconnection technologies to provide a high performance, low cost design with excellent electrical, mechanical, and thermal properties. In addition, the need for external components is minimized, optimizing cost and size.

The RF subsystem consists of an integrated, low loss RF balun, passive MOSFET mixer, and a sum termination network.

The LO subsystem consists of an SPDT terminated FET switch and a three-stage limiting LO amplifier. The purpose of the LO subsystem is to provide a large, fixed amplitude, balanced signal to drive the mixer independent of the level of the LO input.

A block diagram of the device is shown in Figure 47.

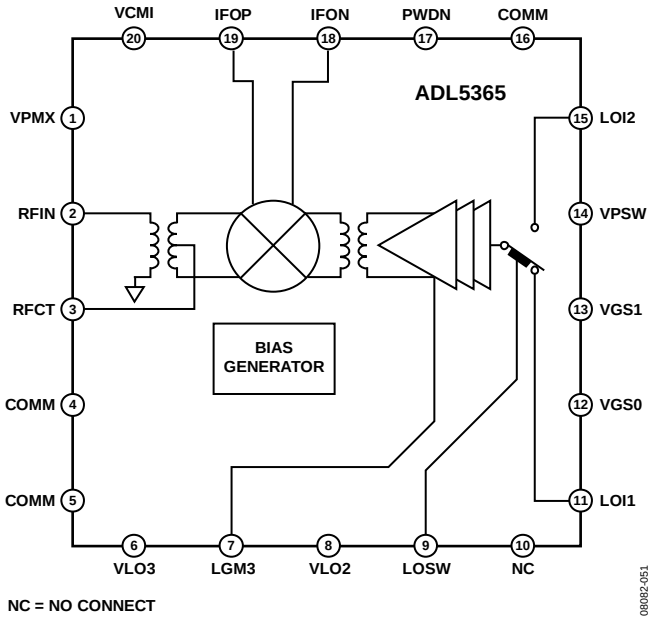

Figure 47. Simplified Schematic

RF SUBSYSTEM

The single-ended, 50 Ω RF input is internally transformed to a balanced signal using a low loss (<1 dB) unbalanced to balanced (balun) transformer. This transformer is made possible by an extremely low loss metal stack, which provides both excellent balance and dc isolation for the RF port. Although the port can be dc connected, it is recommended that a blocking capacitor be used to avoid running excessive dc current through the part. The RF balun can easily support an RF input frequency range of 1200 MHz to 2500 MHz.

The resulting balanced RF signal is applied to a passive mixer that commutates the RF input with the output of the LO subsystem. The passive mixer is essentially a balanced, low loss switch that adds minimum noise to the frequency translation. The only noise contribution from the mixer is due to the resistive loss of the switches, which is in the order of a few ohms.

As the mixer is inherently broadband and bidirectional, it is necessary to properly terminate all the idler (M × N product) frequencies generated by the mixing process. Terminating the mixer avoids the generation of unwanted intermodulation products and reduces the level of unwanted signals at the IF output. This termination is accomplished by the addition of a sum network between the IF output and the mixer.

Additionally, dc current can be saved by reducing the dc supply voltage to as low as 3.3 V, further reducing the dissipated power of the part. (Note that no performance enhancement is obtained by reducing the value of these resistors and excessive dc power dissipation may result.)

LO SUBSYSTEM

The LO amplifier is designed to provide a large signal level to the mixer to obtain optimum intermodulation performance. The resulting amplifier provides extremely high performance centered on an operating frequency of 1700 MHz. The best operation is achieved with either high-side LO injection for RF signals in the 1200 MHz to 1700 MHz range or low-side injection for RF signals in the 1700 MHz to 2500 MHz range. Operation outside these ranges is permissible, and conversion gain is extremely wideband, easily spanning 1200 MHz to 2500 MHz, but intermodulation is optimal over the aforementioned ranges.

The ADL5365 has two LO inputs permitting multiple synthesizers to be rapidly switched with extremely short switching times (<40 ns) for frequency agile applications. The two inputs are applied to a high isolation SPDT switch that provides a constant input impedance, regardless of whether the port is selected, to avoid pulling the LO sources. This multiple section switch also ensures high isolation to the off input, minimizing any leakage from the unwanted LO input that may result in undesired IF responses.

The single-ended LO input is converted to a fixed amplitude differential signal using a multistage, limiting LO amplifier. This results in consistent performance over a range of LO input power. Optimum performance is achieved from −6 dBm to +10 dBm, but the circuit continues to function at considerably lower levels of LO input power.

The performance of this amplifier is critical in achieving a high intercept passive mixer without degrading the noise floor of the system. This is a critical requirement in an interferer rich environment, such as cellular infrastructure, where blocking interferers can limit mixer performance. The bandwidth of the intermodulation performance is somewhat influenced by the current in the LO amplifier chain. For dc current sensitive applications, it is permissible to reduce the current in the LO amplifier by raising the value of the external bias control resistor. For dc current critical applications, the LO chain can operate with a supply voltage as low as 3.3 V, resulting in substantial dc power savings.

In addition, when operating with supply voltages below 3.6 V, the ADL5365 has a power-down mode that permits the dc current to drop to <200 μA.

All of the logic inputs are designed to work with any logic family that provides a Logic 0 input level of less than 0.4 V and a Logic 1 input level that exceeds 1.4 V. All logic inputs are high impedance up to Logic 1 levels of 3.3 V. At levels exceeding 3.3 V, protection circuitry permits operation up to 5.5 V, although a small bias current is drawn.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The ADL5365 mixer is designed to up or downconvert between radio frequencies (RF) from 1200 MHz to 2500 MHz and intermediate frequencies (IF) from dc to 450 MHz. Figure 48 depicts the basic connections of the mixer. It is recommended to ac-couple RF and LO input ports to prevent nonzero dc voltages from damaging the RF balun or LO input circuit. The RFIN capacitor value of 3 pF is recommended to provide the optimized RF input return loss for the desired frequency band.

For upconversion, the IF input, Pin 18 (IFON) and Pin 19 (IFOP), must be driven differentially or by using a 1:1 ratio transformer for single-ended operation. A 3 pF capacitor is recommended for the RF output, Pin 2 (RFIN).

IF PORT

The real part of the output impedance is approximately 50 Ω, as seen in Figure 26, which matches many commonly used SAW filters without the need for a transformer. This results in a voltage conversion loss that is approximately the same as the power conversion loss, as shown in Table 3.

MIXER VGS CONTROL DAC

The ADL5365 features two logic control pins, Pin 12 (VGS0) and Pin 13 (VGS1), that allow programmability for internal gate to source voltages for optimizing mixer performance over desired frequency bands. The evaluation board defaults both VGS0 and VGS1 to ground. Power conversion loss, NF, and IIP3 can be optimized, as shown in Figure 35 and Figure 36.

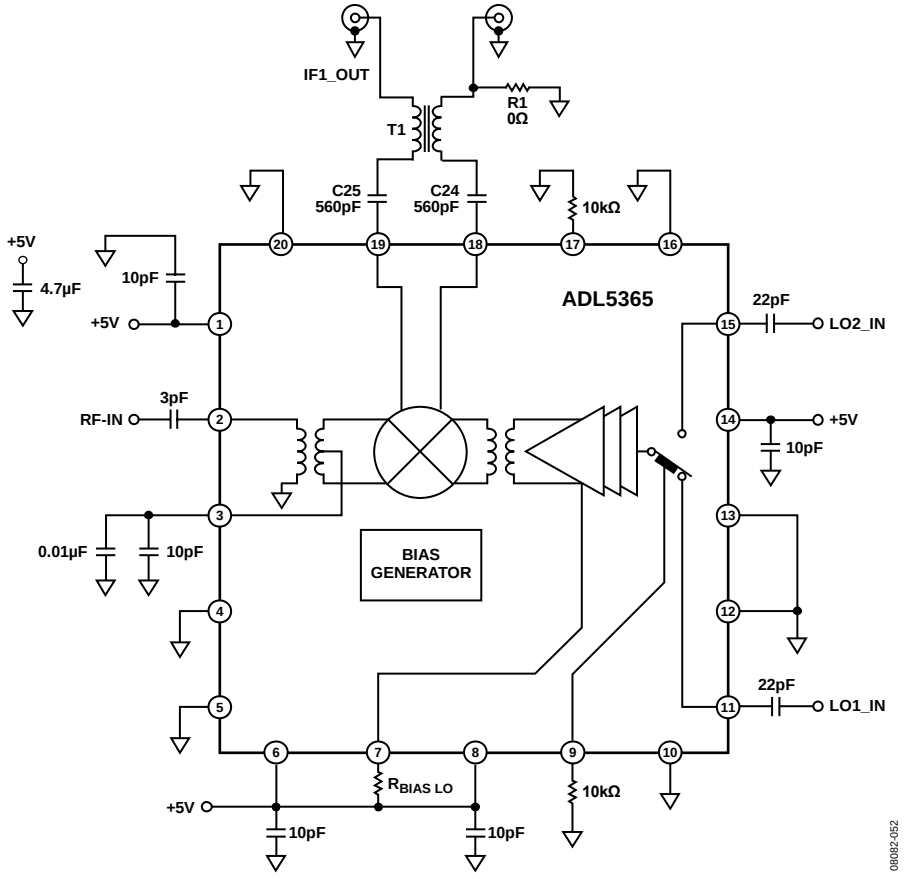

Figure 48. Typical Application Circuit

EVALUATION BOARD

An evaluation board is available for the family of double balanced mixers. The standard evaluation board schematic is shown in Figure 49. The evaluation board, ADL5365-EVALZ, is fabricated using Rogers® RO3003 material.

Table 8 describes the various configuration options of the evaluation board. The evaluation board layout is shown in Figure 50 to Figure 53.

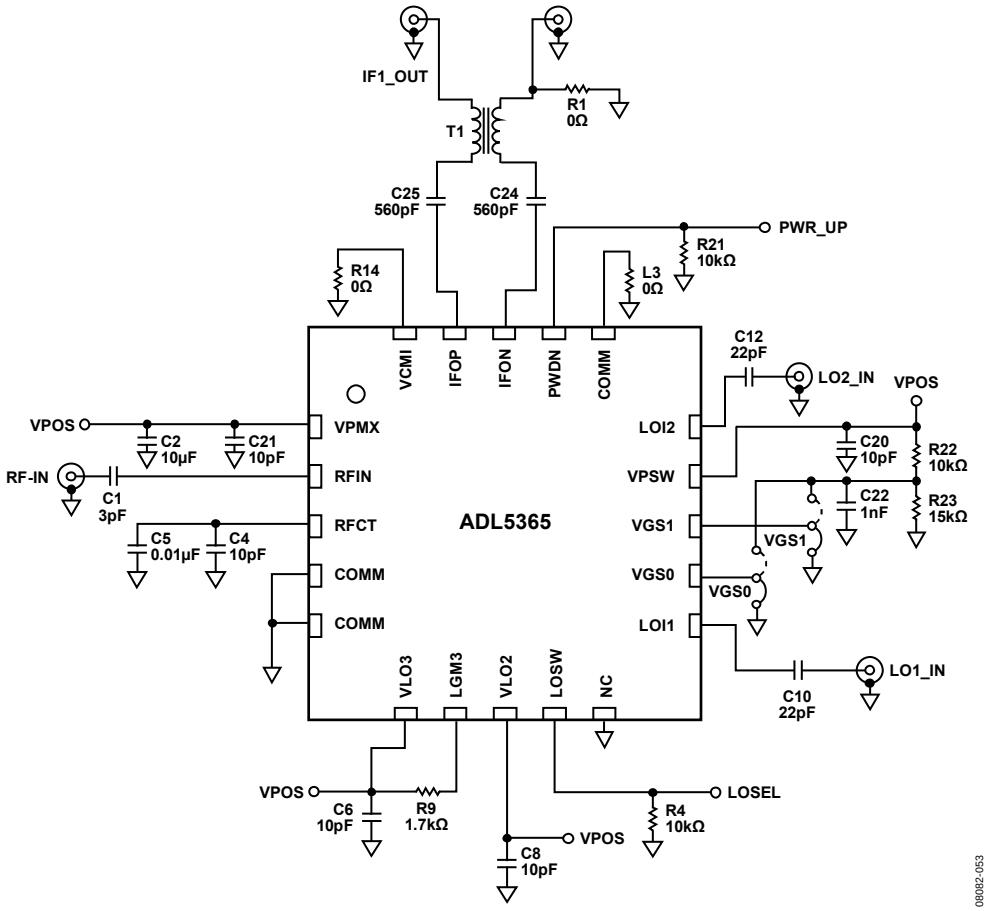

Figure 49. Evaluation Board Schematic

Table 8. Evaluation Board Configuration

Components	Description	Default Conditions
C2, C6, C8, C20, C21	Power Supply Decoupling. Nominal supply decoupling consists ofa 10 µF capacitor to ground in parallel with a 10 pF capacitor to ground positioned as close to the device as possible.	C2 = 10 µF (Size 0603), C6, C8, C20, C21 = 10 pF (Size 0402)
C1, C4, C5	RF Input Interface. The input channels are ac-coupled through C1. C4 and C5 provide bypassing for the center taps of the RF input baluns.	C1 = 3 pF (Size 0402), C4 = 10 pF (Size 0402), C5 = 0.01 µF (Size 0402)
T1, R1, C24 (R24), C25 (R25)	IF Output Interface. T1 is a 1:1 impedance transformer used to provide a single-ended IF output interface. Remove R1 for balanced output operation. C24 (R24) and C25 (R25) are capacitors (resistors) used to block the dc bias at the IF ports.	T1 = TC1-1-13M+ (Mini-Circuits), R1 = 0 Ω (Size 0402), C24 (R24), C25 (R25) = 560 pF (Size 0402)
C10, C12, R4	LO Interface. C10 and C12 provide ac coupling for the LO1_IN and LO2_IN local oscillator inputs. LOSEL selects the appropriate LO inputfor both mixer cores. R4 provides a pull-down to ensure that LO1_IN is enabled when the LOSEL test point is logic low. LO2_IN is enabled when LOSEL is pulled to logic high.	C10, C12 = 22 pF (Size 0402), R4 = 10 kΩ (Size 0402)
R21	PWDN Interface. R21 pulls the PWDN logic low and enables the device. The PWR_UP test point allows the PWDN interface to be exercised using an external logic generator. Grounding the PWDN pin for nominal operation is allowed. Using the PWDN pin when supply voltages exceed 3.3 V is not allowed.	R21 = 10 kΩ (Size 0402)
C22, L3, R9, R14, R22, R23, VGS0, VGS1	Bias Control. R22 and R23 form a voltage divider to provide 3 V for logic control, bypassed to ground through C22. VGS0 and VGS1 jumpers provide programmability at the VGS0 and VGS1 pins. It is recommended to pull these two pins to ground for nominal operation. R9 sets the bias point for the internal LO buffers. R14 sets the bias point for the internal IF amplifier.	C22 = 1 nF (Size 0402), L3 = 0 Ω (Size 0603), R9 = 1.7 kΩ (Size 0402), R14 = 0 Ω (Size 0402), R22 = 10 kΩ (Size 0402), R23 = 15 kΩ (Size 0402), VGS0 = VGS1 = 3-pin shunt

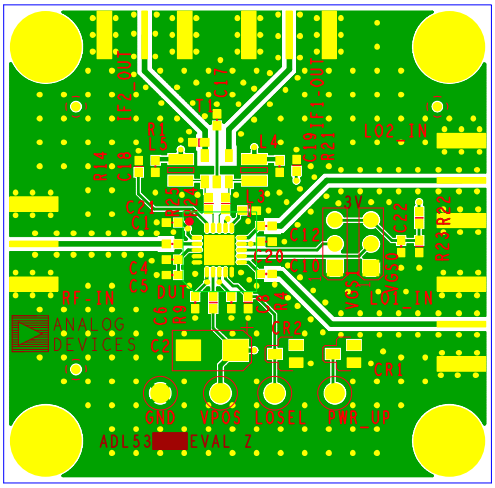

Figure 50. Evaluation Board Top Layer

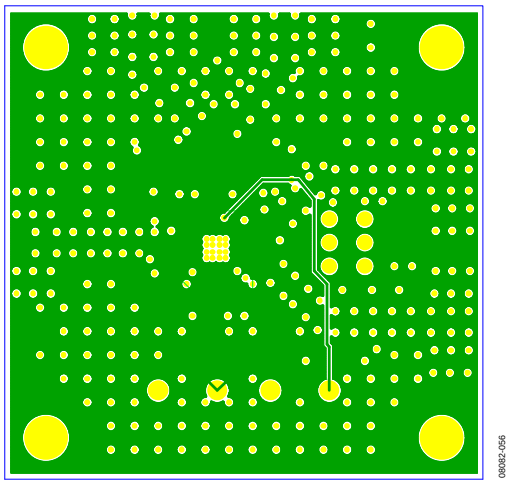

Figure 52. Evaluation Board Power Plane, Internal Layer 2

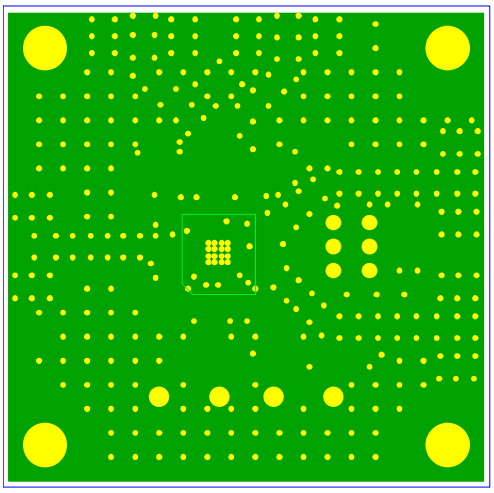

Figure 51. Evaluation Board Ground Plane, Internal Layer 1

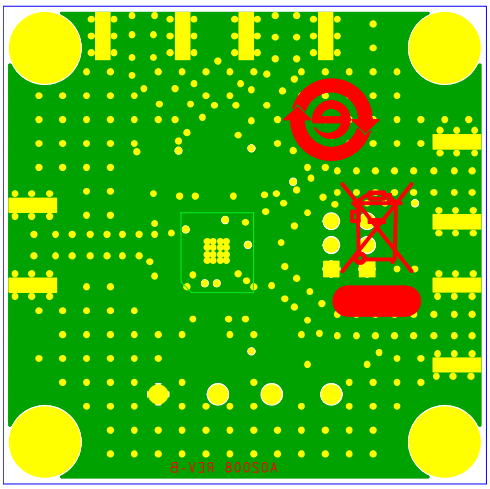

Figure 53. Evaluation Board Bottom Layer

OUTLINE DIMENSIONS

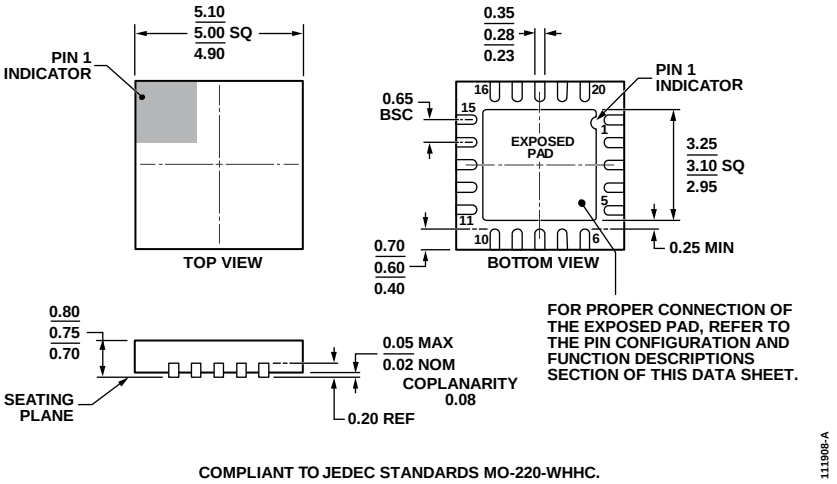

Figure 54. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-20-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5365ACPZ-R7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 7″Tape and Reel	CP-20-9	1,500
ADL5365-EVALZ		Evaluation Board		1

[1] Z = RoHS Compliant Part.

NOTES

D08082-0-3/16(C)