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REVISION HISTORY

1/09—Rev. 0 to Rev. A

Change to I_{DD} Parameter, Table 1 4
Change to I_{DD} Parameter, Table 2 5
Updated Outline Dimensions 14

4/06—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.[1]

Table 1.

Parameter	+25°C	−40°C to +105°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance, R_{ON}	130		Ω typ	V_S = ±10 V, I_S = −1 mA; see Figure 13
	210	300	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels, ΔR_{ON}	5		Ω typ	V_S = ±10 V, I_S = −1 mA
	10		Ω max	
On Resistance Flatness, R_{FLAT} (On)	25		Ω typ	V_S = −5 V, 0 V, +5 V, I_S = −1 mA
	70		Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	±1		nA typ	V_D = ±10 V, V_S = −10 V; see Figure 14
		±50	nA max	
Drain Off Leakage, I_D (Off)	±1		nA typ	V_S = 1 V, 10 V; V_D = 10 V, 1 V; see Figure 14
		±50	nA max	
Channel On Leakage, I_D, I_S (On)	±1		nA typ	V_S = V_D = ±10 V; see Figure 15
		±50	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.005		μA max	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
Transition Time, $t_{TRANSITION}$	80		ns typ	R_L = 300 Ω, C_L = 35 pF
	130	190	ns max	V_S = 10 V; see Figure 16
t_{ON} (EN)	80		ns typ	R_L = 300 Ω, C_L = 35 pF
	100	120	ns max	V_S = 10 V; see Figure 18
t_{OFF} (EN)	85		ns typ	R_L = 300 Ω, C_L = 35 pF
	100	150	ns max	V_S = 10 V; see Figure 18
Break-Before-Make Time Delay, t_{BBM}	25		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = 10 V; see Figure 17
Charge Injection	2		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 19
Off Isolation	80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 20
Channel-to-Channel Crosstalk	80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 21
−3 dB Bandwidth	500		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 22
C_S (Off)	5		pF typ	f = 1 MHz, V_S = 0 V
C_D (Off)				
ADG1308	15		pF typ	f = 1 MHz, V_S = 0 V
ADG1309	10		pF typ	f = 1 MHz, V_S = 0 V
C_D, C_S (On)				
ADG1308	20		pF typ	f = 1 MHz, V_S = 0 V
ADG1309	15		pF typ	f = 1 MHz, V_S = 0 V

Parameter	+25°C	−40°C to +105°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS				V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.002		µA typ	Digital inputs = 0 V or V_{DD}
		1.0	µA max	
I_{DD}	220		µA typ	Digital inputs = 5 V
		380	µA max	
I_{SS}	0.002		µA typ	Digital inputs = 0 V or V_{DD} or 5 V
		1.0	µA max	
V_{DD}/V_{SS}		±5/±16.5	V min/V max	$\|V_{DD}\| = \|V_{SS}\|$

[1] Temperature range for B version is –40°C to +105°C.
[2] Guaranteed by design; not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V, V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.[1]

Table 2.

Parameter	+25°C	−40°C to +105°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	325		Ω typ	V_S = 0 V to 10 V, I_S = −1 mA; see Figure 13
	500	660	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels, ΔR_{ON}	10		Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	20		Ω max	
On Resistance Flatness, R_{FLAT} (On)	65		Ω typ	V_S = 3 V, 6 V, 9 V, I_S = −1 mA
LEAKAGE CURRENTS				V_{DD} = 13.2 V
Source Off Leakage, I_S (Off)	±1		nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 14
		±50	nA max	
Drain Off Leakage, I_D (Off)	±1		nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 14
		±50	nA max	
Channel On Leakage, I_D, I_S (On)	±1		nA typ	V_S = V_D = 1 V or 10 V; see Figure 15
		±50	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.001			
		±0.1	μA max	V_{IN} = V_{INL} or V_{INH}
Digital Input Capacitance, C_{IN}	3		pF typ	
DYNAMIC CHARACTERISTICS[2]				
Transition Time, $t_{TRANSITION}$	100		ns typ	R_L = 300 Ω, C_L = 35 pF
	170	240		V_S = 8 V; see Figure 16
t_{ON} (EN)	90		ns typ	R_L = 300 Ω, C_L = 35 pF
	110	170		V_S = 8 V; see Figure 18
t_{OFF} (EN)	105		ns typ	R_L = 300 Ω, C_L = 35 pF
	130	180		V_S = 8 V; see Figure 18
Break-Before-Make Time Delay, t_{BBM}	45		ns typ	R_L = 300 Ω, C_L = 35 pF
		20	ns min	V_{S1} = V_{S2} = 8 V; see Figure 17
Charge Injection	2		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 19
Off Isolation	80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 20
Channel-to-Channel Crosstalk	80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 21
−3 dB Bandwidth	500		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 22
C_S (Off)	5		pF typ	f = 1 MHz, V_S = 6 V
C_D (Off)				
ADG1308	10		pF typ	f = 1 MHz, V_S = 6 V
ADG1309	15		pF typ	f = 1 MHz, V_S = 6 V
C_D, C_S (On)				
ADG1308	20		pF typ	f = 1 MHz, V_S = 6 V
ADG1309	15		pF typ	f = 1 MHz, V_S = 6 V
POWER REQUIREMENTS				V_{DD} = 13.2 V
I_{DD}	0.002		μA typ	Digital inputs = 0 V or V_{DD}
		1.0	μA max	
I_{DD}	220		μA typ	Digital inputs = 5
		380	μA max	
V_{DD}		5/16.5	V min/V max	V_{SS} = 0 V, GND = 0 V

[1] Temperature range for the B version is −40°C to +105°C.
[2] Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog, Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA (whichever occurs first)
Continuous Current, S or D pins	30 mA
Peak Current, S or D pins (Pulsed at 1 ms, 10% Duty Cycle Maximum)	100 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP, θ_{JA}, Thermal Impedance	112°C/W
16-Lead SOIC, θ_{JA}, Thermal Impedance	77°C/W
Reflow Soldering Peak Temperature (Pb-free)	260 (+0/−5)°C

[1] Overvoltages at A, EN, S, or D pins are clamped by internal diodes. Current should be limited to the maximum ratings provided.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

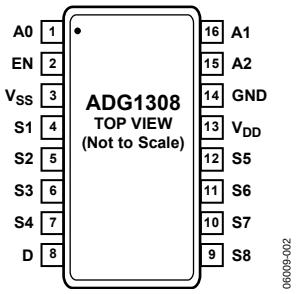


Figure 2. ADG1308 Pin Configuration (TSSOP and SOIC_N)

Table 4. ADG1308 Pin Function Descriptions

Pin Number	Mnemonic	Description
1	A0	Logic Control Input A0.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	V_{SS}	Most Negative Power Supply Potential. In single supply applications, this pin can be connected to ground.
4	S1	Source Terminal 1. Can be an input or an output.
5	S2	Source Terminal 2. Can be an input or an output.
6	S3	Source Terminal 3. Can be an input or an output.
7	S4	Source Terminal 4. Can be an input or an output.
8	D	Drain Terminal. Can be an input or an output.
9	S8	Source Terminal 8. Can be an input or an output.
10	S7	Source Terminal 7. Can be an input or an output.
11	S6	Source Terminal 6. Can be an input or an output.
12	S5	Source Terminal 5. Can be an input or an output.
13	V_{DD}	Most Positive Power Supply Potential.
14	GND	Ground (0 V) Reference.
15	A2	Logic Control Input A2.
16	A1	Logic Control Input A1.

ADG1308 TRUTH TABLE

Table 5.

A2	A1	A0	EN	ON SWITCH
X[1]	X[1]	X[1]	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

[1] X = Don't care.

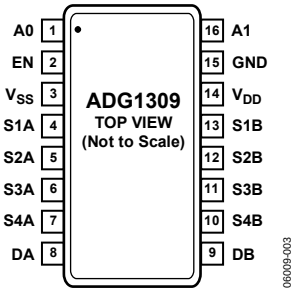


Figure 3. ADG1309 Pin Configuration (TSSOP and SOIC_N)

Table 6. ADG1309 Pin Function Descriptions

Pin Number SOIC/TSSOP	Mnemonic	Description
1	A0	Logic Control Input A0.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	V_{SS}	Most Negative Power Supply Potential. In single supply applications, this pin can be connected to ground.
4	S1A	Source Terminal 1A. Can be an input or an output.
5	S2A	Source Terminal 2A. Can be an input or an output.
6	S3A	Source Terminal 3A. Can be an input or an output.
7	S4A	Source Terminal 4A. Can be an input or an output.
8	DA	Drain Terminal A. Can be an input or an output.
9	DB	Drain Terminal B. Can be an input or an output.
10	S4B	Source Terminal 4B. Can be an input or an output.
11	S3B	Source Terminal 3B. Can be an input or an output.
12	S2B	Source Terminal 2B. Can be an input or an output.
13	S1B	Source Terminal 1B. Can be an input or an output.
14	V_{DD}	Most Positive Power Supply Potential.
15	GND	Ground (0 V) Reference.
16	A1	Logic Control Input A1.

ADG1309 TRUTH TABLE

Table 7.

AI	A0	EN	ON SWITCH PAIR
X[1]	X[1]	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

[1] X = Don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

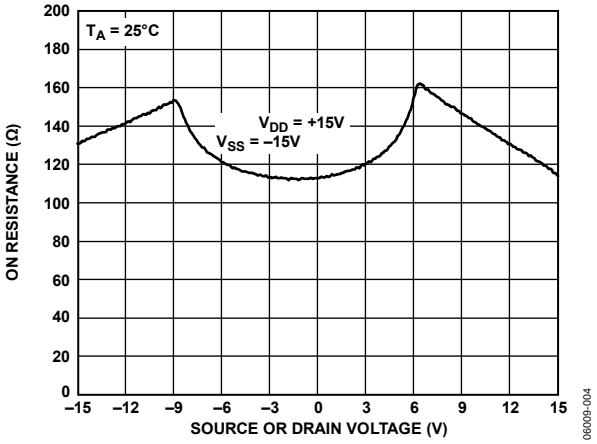


Figure 4. On Resistance as a Function of V_D (V_S) for Dual Supply

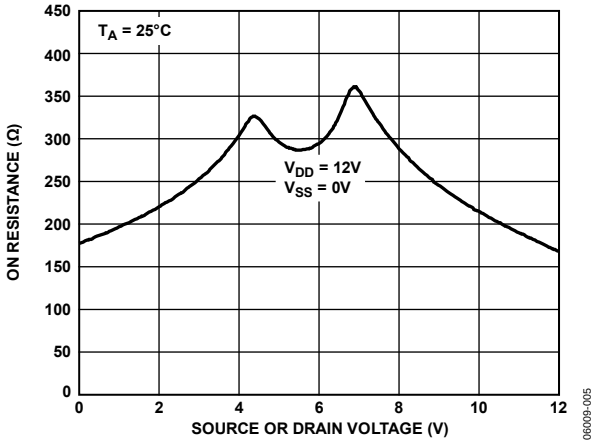


Figure 5. On Resistance as a Function of V_D (V_S) for Single Supply

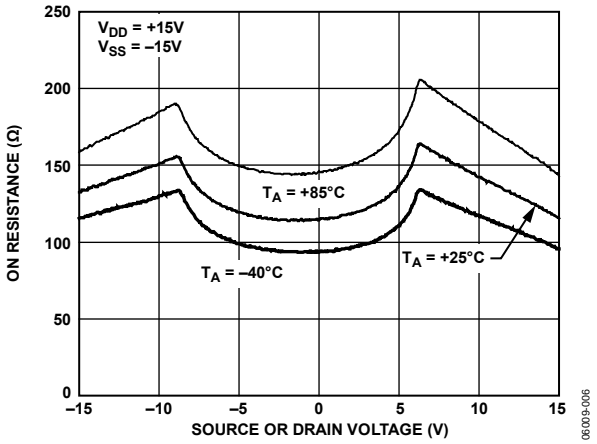


Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

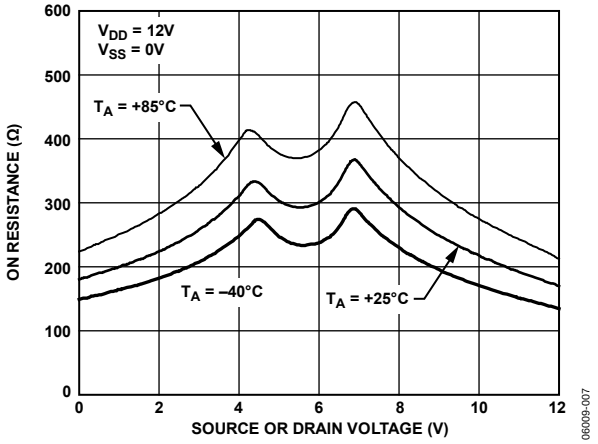


Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

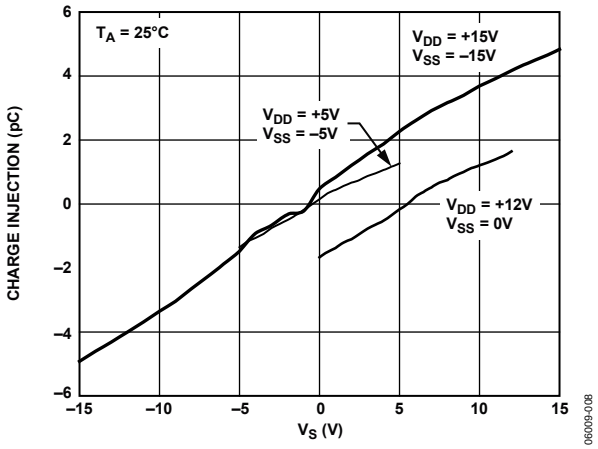


Figure 8. Charge Injection vs. Source Voltage

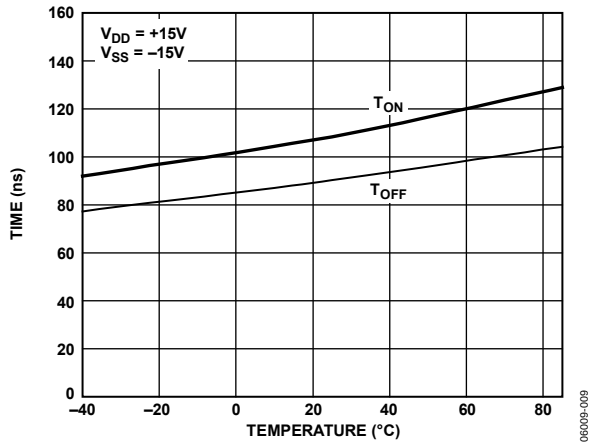


Figure 9. T_{ON}/T_{OFF} Time vs. Temperature

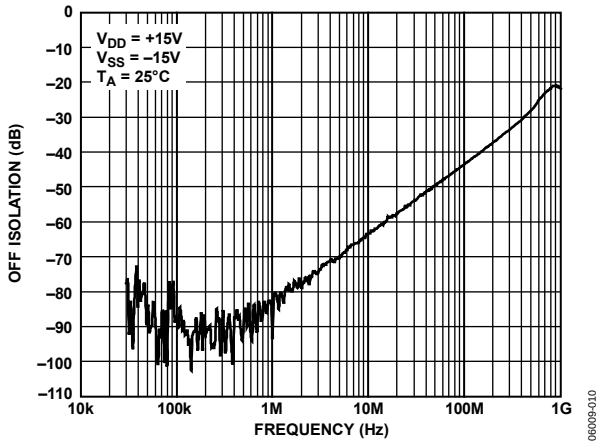


Figure 10. Off Isolation vs. Frequency

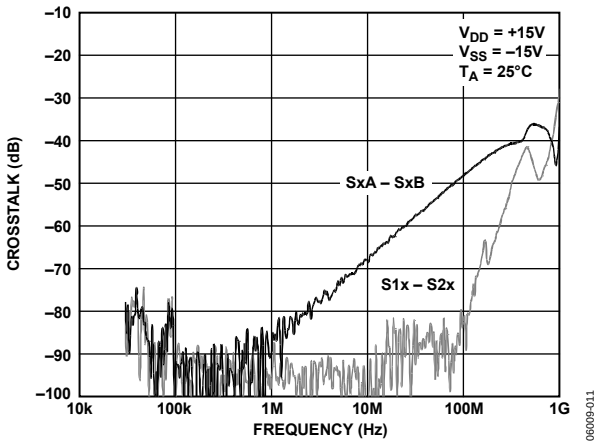


Figure 12. Crosstalk vs. Frequency

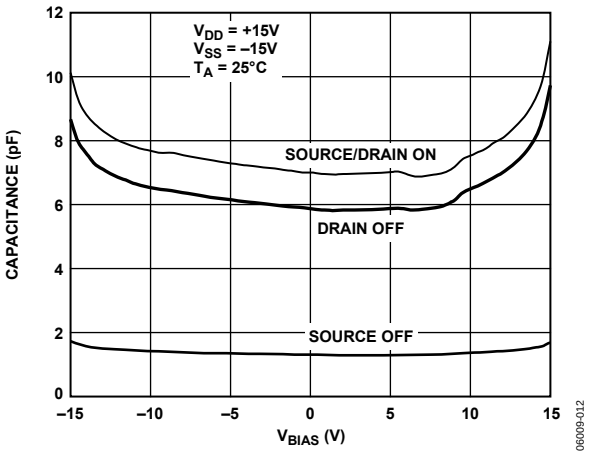


Figure 11. ADG1308 Capacitance vs. Source Voltage, ±15 V Dual Supply

TEST CIRCUITS

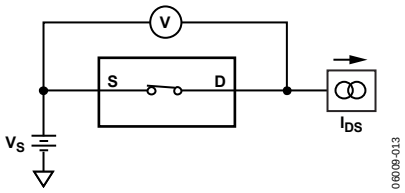


Figure 13. On Resistance

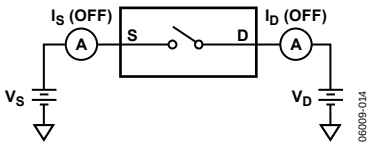


Figure 14. Off Leakage

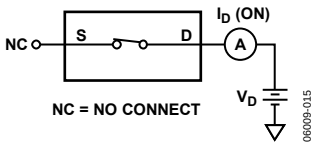


Figure 15. On Leakage

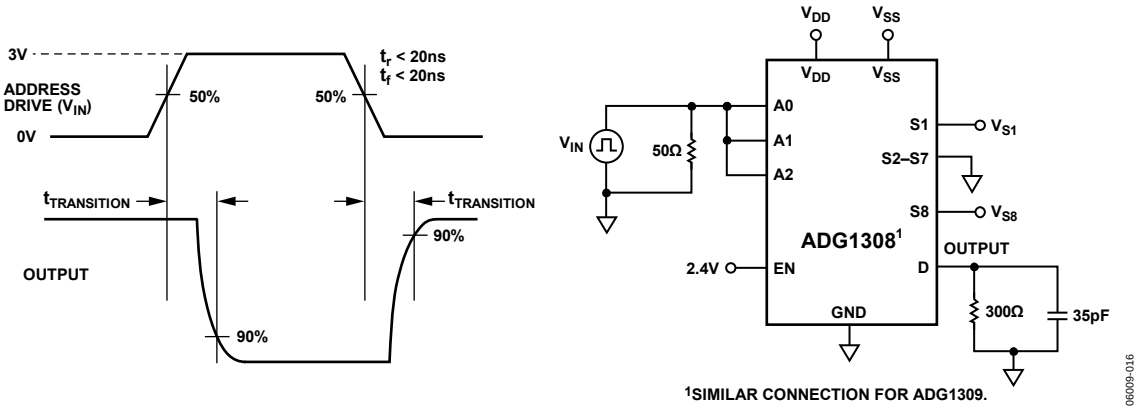


Figure 16. Address to Output Switching Times, $t_{TRANSITION}$

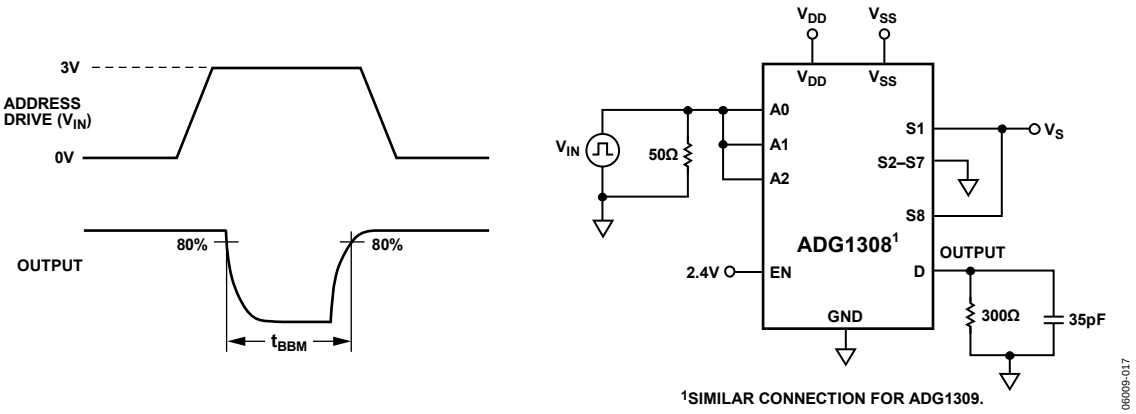


Figure 17. Break-Before-Make Delay, t_{BBM}

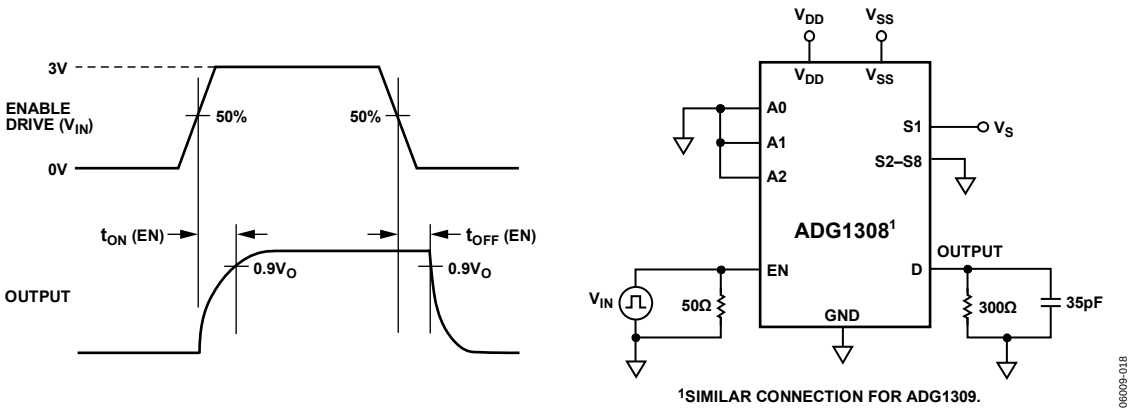


Figure 18. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

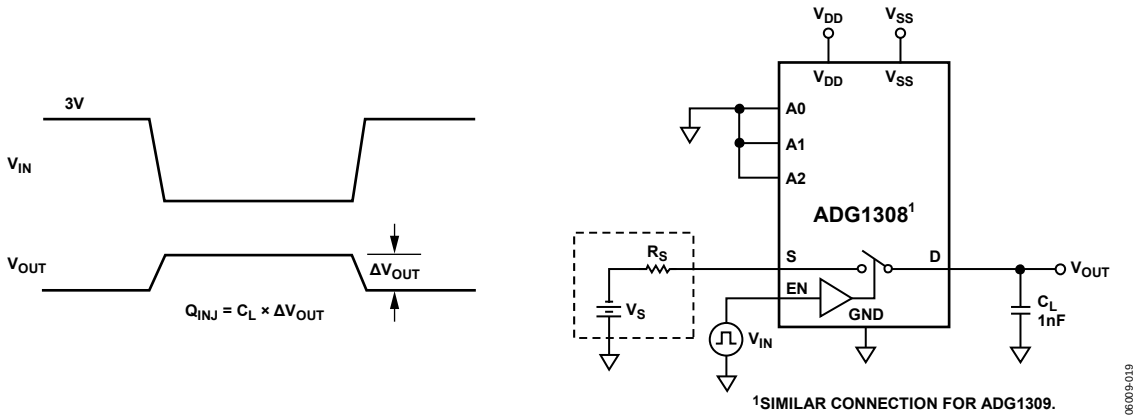


Figure 19. Charge Injection

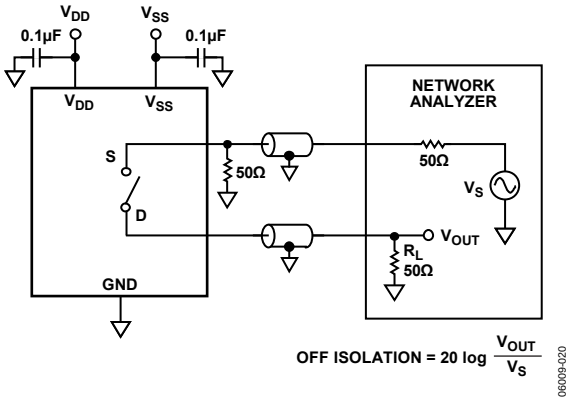


Figure 20. Off Isolation

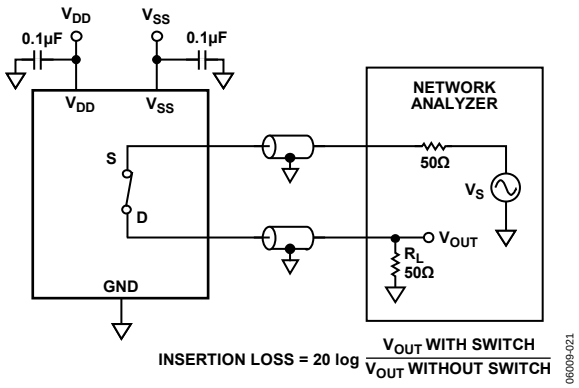


Figure 22. Bandwidth

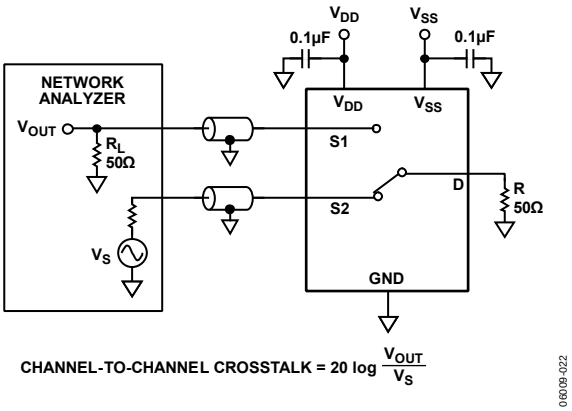


Figure 21. Channel-to-Channel Crosstalk

TERMINOLOGY

R_{ON}

Ohmic resistance between D and S.

ΔR_{ON}
Difference between the R_{ON} of any two channels.

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

V_D (V_S)
Analog voltage on Terminal D and Terminal S.

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_D, C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

T_{BBM}
Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

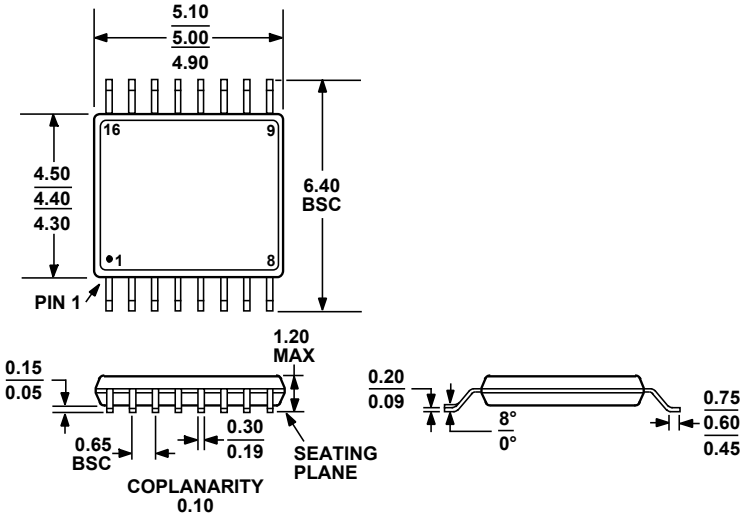
Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

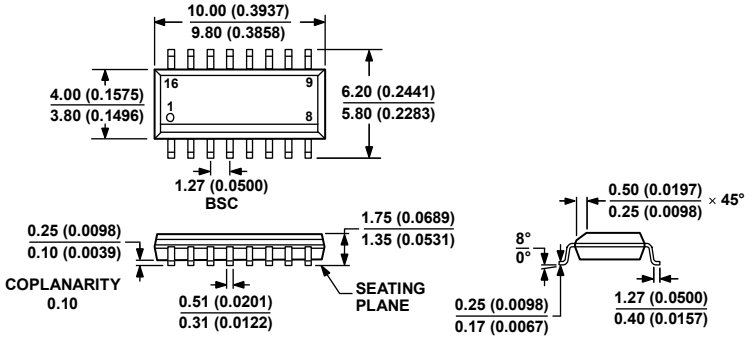
On Response
The frequency response of the on switch.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 23. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

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Figure 24. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1308BRUZ[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1308BRUZ-REEL7[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1308BRZ[1]	−40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1308BRZ-REEL7[1]	−40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1309BRUZ[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1309BRUZ-REEL7[1]	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1309BRZ[1]	−40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1309BRZ-REEL7[1]	−40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16

[1] Z = RoHS Compliant Part.

NOTES

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