

ADA4960-1* PRODUCT PAGE QUICK LINKS

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DOCUMENTATION

Application Notes

- AN-1026: High Speed Differential ADC Driver Design Considerations
- AN-1363: Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers

Data Sheet

- ADA4960-1: 5 GHz, Low Distortion ADC Driver/Line Driver Data Sheet

TOOLS AND SIMULATIONS

- ADI DiffAmpCalc™
- ADA4960 SPICE Macro Model
- spice_ADA4960

REFERENCE DESIGNS

- CN0238

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Test & Instrumentation Solutions Bulletin, Volume 10, Issue 3

Tutorials

- MT-218: Multiple Feedback Band-Pass Design Example

DESIGN RESOURCES

- ADA4960-1 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

3/2017—Rev. 0 to Rev. A

Changed LFCSP_WQ to LFCSP	Throughout
Updated Outline Dimensions	19
Changes to Ordering Guide	19

4/2010—Revision 0: Initial Version

SPECIFICATIONS

VCC = 5 V, V_{OCM} = 2.5 V, R_L = 100 Ω differential, A_V = 6 dB, C_L = 1 pF differential, f = 140 MHz, T = 25°C. Inputs and outputs are ac-coupled.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	A _V = 6 dB, V _{OUT} ≤ 1.0 V p-p		5000		MHz
	A _V = 12 dB, V _{OUT} ≤ 1.0 V p-p		2000		MHz
	A _V = 18 dB, V _{OUT} ≤ 1.0 V p-p		1200		MHz
Bandwidth for 0.1 dB Flatness	V _{OUT} ≤ 1.0 V p-p		300		MHz
Gain Accuracy	R _G = 95.3 Ω		0.5		dB
Gain Supply Sensitivity	V _S ± 5%		0.2		dB/V
Gain Temperature Sensitivity	–40°C to +85°C		2.5		mdB/°C
Slew Rate	A _V = 6 dB, V _{OUT} = 2 V step, 20% to 80%		8700		V/ μ s
	A _V = 12 dB, V _{OUT} = 2 V step, 20% to 80%		7700		V/ μ s
	A _V = 18 dB, V _{OUT} = 2 V step, 20% to 80%		6600		V/ μ s
	A _V = 6 dB, V _{OUT} = 1 V step, 20% to 80%		7200		V/ μ s
	A _V = 12 dB, V _{OUT} = 1 V step, 20% to 80%		4900		V/ μ s
	A _V = 18 dB, V _{OUT} = 1 V step, 20% to 80%		3700		V/ μ s
Settling Time	1 V step to 1%		1		ns
	1 V step to 0.1%		1.4		ns
Overdrive Recovery Time	V _{IN} = 1 V to 0 V step, A _V = 12 dB, V _{OUT} ≤ 1%		6.7		ns
	V _{IN} = 1 V to 0 V step, A _V = 12 dB, V _{OUT} ≤ 0.5%		9.3		ns
Reverse Isolation (S12)	f = ≤1 GHz		68		dB
INPUT/OUTPUT CHARACTERISTICS					
Output Common Mode			V _S /2		V
VOCM Adjustment Range		1		2.75	V
Input Common-Mode Range		2.25		2.75	V
Maximum Output Voltage Swing	1 dB compressed		3.5		V p-p
Output Common-Mode Offset	Referenced to VCC/2	–20		+10	mV
Output Common-Mode Drift	–40°C to +85°C		0.05		mV/°C
Output Differential Offset Voltage		–36		+22	mV
Common-Mode Rejection Ratio (CMRR)			60		dB
Output Differential Offset Drift	–40°C to +85°C		0.05		mV/°C
Input Bias Current	–40°C to +85°C		–20		μ A
Input Resistance (Differential)	A _V = all gains		10		k Ω
Input Capacitance (Differential)	A _V = all gains		0.4		pF
Input Resistance (Single-Ended)	A _V = all gains		5		k Ω
Input Capacitance (Single-Ended)	A _V = all gains		0.8		pF
Output Resistance (Differential)			150		Ω
Output Capacitance (Differential)			1.2		pF
POWER INTERFACE					
Supply Voltage		4.75	5.0	5.25	V
ENB Threshold	Low to high	2.2			V
	High to low			1.3	V
ENB Input Bias Current	ENB high		30		μ A
	ENBL low		–180		μ A
Quiescent Current	ENB high	56	60	64	mA
	ENBL low		2.9		mA

Parameter	Conditions	Min	Typ	Max	Unit
NOISE/HARMONIC PERFORMANCE					
140 MHz					
Second/Third Harmonic Distortion	$A_V = 6 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-91/-73		dBc
	$A_V = 12 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-86/-73		dBc
	$A_V = 18 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-82/-72		dBc
OIP3/IMD3	$A_V = 6 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+33.2/-79		dBm/dBc
	$A_V = 12 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+33.4/-78		dBm/dBc
	$A_V = 18 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+33.3/-78		dBm/dBc
Noise Spectral Density (RTI)	$A_V = 6 \text{ dB}$		5.4		nV/ $\sqrt{\text{Hz}}$
	$A_V = 12 \text{ dB}$		3.2		nV/ $\sqrt{\text{Hz}}$
	$A_V = 18 \text{ dB}$		2.1		nV/ $\sqrt{\text{Hz}}$
1 dB Compression Point (RTO)	$A_V = 6 \text{ dB}$		12.0		dBm
	$A_V = 12 \text{ dB}$		12.0		dBm
	$A_V = 18 \text{ dB}$		11.9		dBm
250 MHz					
Second/Third Harmonic Distortion	$A_V = 6 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-88/-69		dBc
	$A_V = 12 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-81/-68		dBc
	$A_V = 18 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-77/-68		dBc
OIP3/IMD3	$A_V = 6 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+32.5/-77		dBm/dBc
	$A_V = 12 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+32.6/-77		dBm/dBc
	$A_V = 18 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+32.1/-76		dBm/dBc
Noise Spectral Density (RTI)	$A_V = 6 \text{ dB}$		5.4		nV/ $\sqrt{\text{Hz}}$
	$A_V = 12 \text{ dB}$		3.1		nV/ $\sqrt{\text{Hz}}$
	$A_V = 18 \text{ dB}$		2.0		nV/ $\sqrt{\text{Hz}}$
1 dB Compression Point (RTO)	$A_V = 6 \text{ dB}$		12.0		dBm
	$A_V = 12 \text{ dB}$		11.9		dBm
	$A_V = 18 \text{ dB}$		11.7		dBm
500 MHz					
Second/Third Harmonic Distortion	$A_V = 6 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-77/-66		dBc
	$A_V = 12 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-71/-66		dBc
	$A_V = 18 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-68/-65		dBc
OIP3/IMD3	$A_V = 6 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+30.2/-72		dBm/dBc
	$A_V = 12 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+29.9/-71		dBm/dBc
	$A_V = 18 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+29.1/-70		dBm/dBc
Noise Spectral Density (RTI)	$A_V = 6 \text{ dB}$		5.2		nV/ $\sqrt{\text{Hz}}$
	$A_V = 12 \text{ dB}$		3.0		nV/ $\sqrt{\text{Hz}}$
	$A_V = 18 \text{ dB}$		1.9		nV/ $\sqrt{\text{Hz}}$
1 dB Compression Point (RTO)	$A_V = 6 \text{ dB}$		11.6		dBm
	$A_V = 12 \text{ dB}$		11.4		dBm
	$A_V = 18 \text{ dB}$		11.0		dBm
750 MHz					
Second/Third Harmonic Distortion	$A_V = 6 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-70/-68		dBc
	$A_V = 12 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-67/-69		dBc
	$A_V = 18 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p}$		-64/-69		dBc
OIP3/IMD3	$A_V = 6 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+28.3/-67		dBm/dBc
	$A_V = 12 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+27.7/-67		dBm/dBc
	$A_V = 18 \text{ dB}, V_{OUT} = 0.9 \text{ V p-p composite (2 MHz spacing)}$		+26.9/-65		dBm/dBc
Noise Spectral Density (RTI)	$A_V = 6 \text{ dB}$		5.0		nV/ $\sqrt{\text{Hz}}$
	$A_V = 12 \text{ dB}$		3.0		nV/ $\sqrt{\text{Hz}}$
	$A_V = 18 \text{ dB}$		1.8		nV/ $\sqrt{\text{Hz}}$
1 dB Compression Point (RTO)	$A_V = 6 \text{ dB}$		9.7		dBm
	$A_V = 12 \text{ dB}$		9.5		dBm
	$A_V = 18 \text{ dB}$		9.5		dBm

Parameter	Conditions	Min	Typ	Max	Unit
1000 MHz					
Second/Third Harmonic Distortion	$A_V = 6 \text{ dB}$, $V_{OUT} = 0.9 \text{ V p-p}$		-73/-72		dBc
	$A_V = 12 \text{ dB}$, $V_{OUT} = 0.9 \text{ V p-p}$		-69/-78		dBc
	$A_V = 18 \text{ dB}$, $V_{OUT} = 0.9 \text{ V p-p}$		-67/-85		dBc
OIP3/IMD3	$A_V = 6 \text{ dB}$, $V_{OUT} = 0.9 \text{ V p-p}$ composite (2 MHz spacing)		+26.2/-63		dBm/dBc
	$A_V = 12 \text{ dB}$, $V_{OUT} = 0.9 \text{ V p-p}$ composite (2 MHz spacing)		+26.0/-63		dBm/dBc
	$A_V = 18 \text{ dB}$, $V_{OUT} = 0.9 \text{ V p-p}$ composite (2 MHz spacing)		+25.0/-61		dBm/dBc
Noise Spectral Density (RTI)	$A_V = 6 \text{ dB}$		4.8		nV/ $\sqrt{\text{Hz}}$
	$A_V = 12 \text{ dB}$		2.7		nV/ $\sqrt{\text{Hz}}$
	$A_V = 18 \text{ dB}$		1.6		nV/ $\sqrt{\text{Hz}}$
1 dB Compression Point (RTO)	$A_V = 6 \text{ dB}$		8.0		dBm
	$A_V = 12 \text{ dB}$		7.7		dBm
	$A_V = 18 \text{ dB}$		7.6		dBm

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VCC	5.25 V
VIP, VIN	VCC + 0.5 V
Internal Power Dissipation	See Figure 3
Maximum Junction Temperature	150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device (including the exposed pad) soldered to a high thermal conductivity, 4-layer circuit board, as described in EIA/JESD 51-7.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP (Exposed Pad)	89.5	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4960-1 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4960-1. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA} . In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through holes, ground, and power planes reduce θ_{JA} .

Figure 3 shows the maximum safe power dissipation of the ADA4960-1 vs. the ambient temperature on a JEDEC standard 4-layer board.

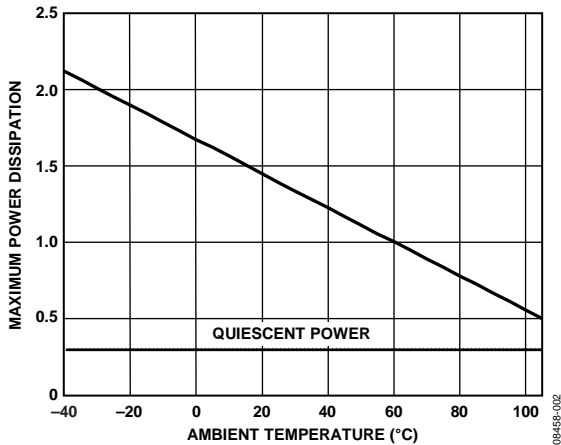


Figure 3. Maximum Power Dissipation vs. Ambient Temperature for 4-Layer Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

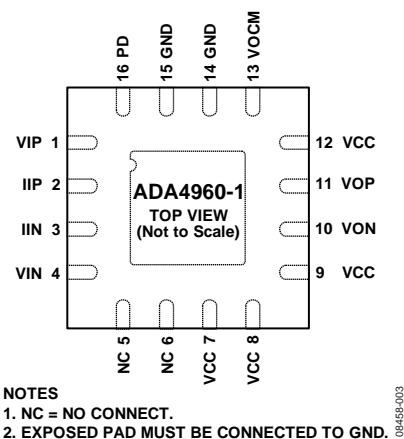


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIP	Balanced Differential Input. This pin is internally biased to $VCC/2$.
2	IIP	Gain Setting Resistor. Connect R_G between this pin and IIN.
3	IIN	Gain Setting Resistor. Connect R_G between this pin and IIP.
4	VIN	Balanced Differential Input. This pin is internally biased to $VCC/2$.
5, 6	NC	Leave these pins unconnected.
7, 8, 9, 12	VCC	Positive 5 V Supply Pins.
10	VON	Balanced Differential Output. This pin is biased to the VOCM input voltage.
11	VOP	Balanced Differential Output. This pin is biased to the VOCM input voltage.
13	VOCM	This pin is internally biased at $VCC/2$. As an input, this pin sets the dc VOP and VON voltages.
14, 15	GND	Ground. Connect this pin to a low impedance ground.
16	PD	This pin grounded disables the part, and at 5 V, this pin turns the part on.
	EPAD	The exposed pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $V_{OCM} = 2.5\text{ V}$, $R_L = 100\ \Omega$ differential, $A_V = 6\text{ dB}$, $C_L = 1\text{ pF}$ differential, $f = 140\text{ MHz}$, $T = 25^\circ\text{C}$.

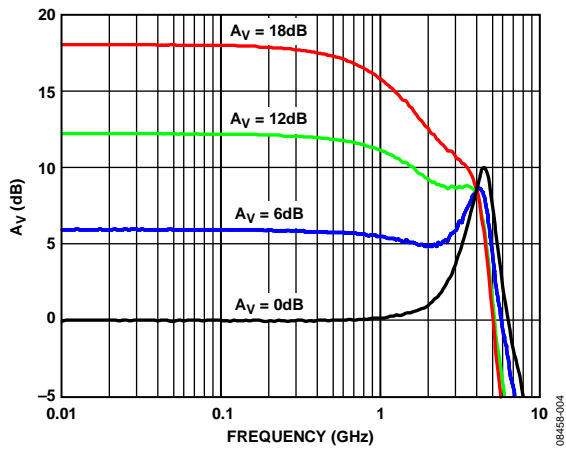


Figure 5. Small Signal Frequency Response, Gain vs. Frequency at $A_V = 0\text{ dB}$, $A_V = 6\text{ dB}$, $A_V = 12\text{ dB}$, and $A_V = 18\text{ dB}$

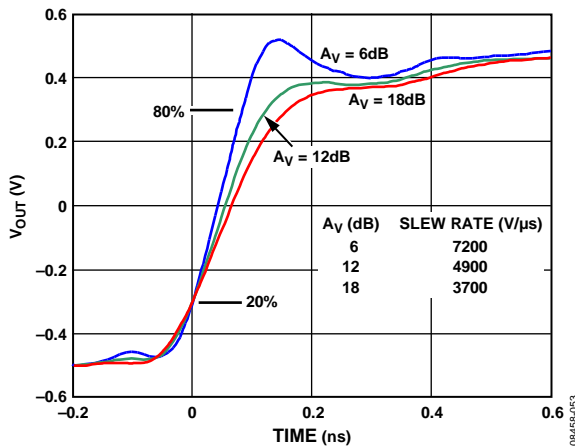


Figure 6. Rise Time, V_{OUT} vs. Time, $V_{OUT} = 1\text{ V p-p}$

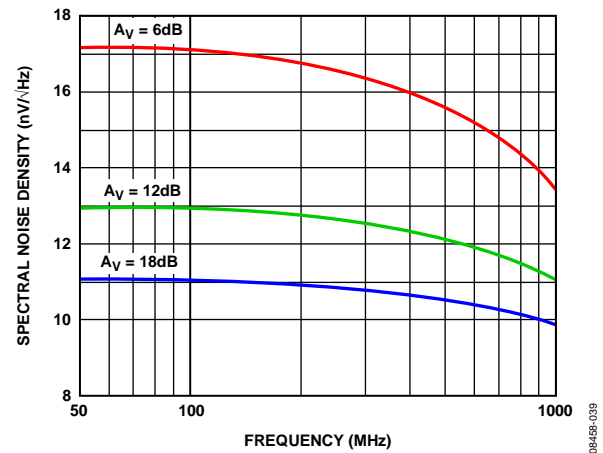


Figure 8. RTO Noise Spectral Density vs. Frequency at $A_V = 6\text{ dB}$, $A_V = 12\text{ dB}$, and $A_V = 18\text{ dB}$

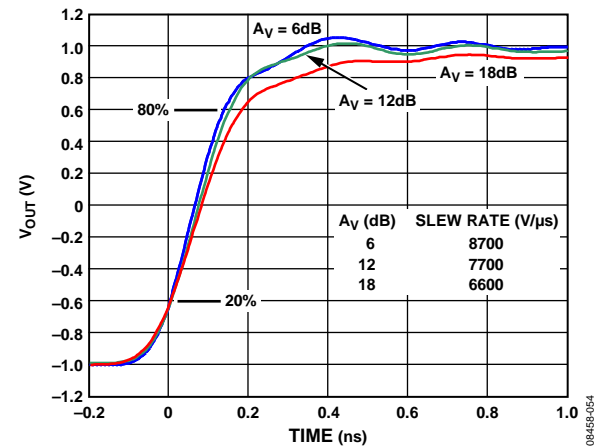


Figure 9. Rise Time, V_{OUT} vs. Time, $V_{OUT} = 2\text{ V p-p}$

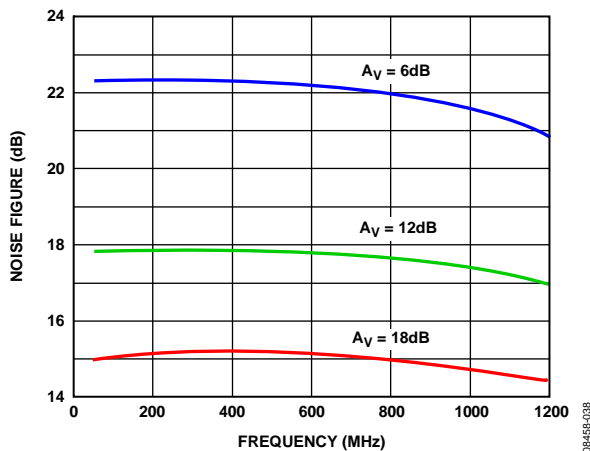


Figure 7. Noise Figure vs. Frequency at $A_V = 6\text{ dB}$, $A_V = 12\text{ dB}$, and $A_V = 18\text{ dB}$

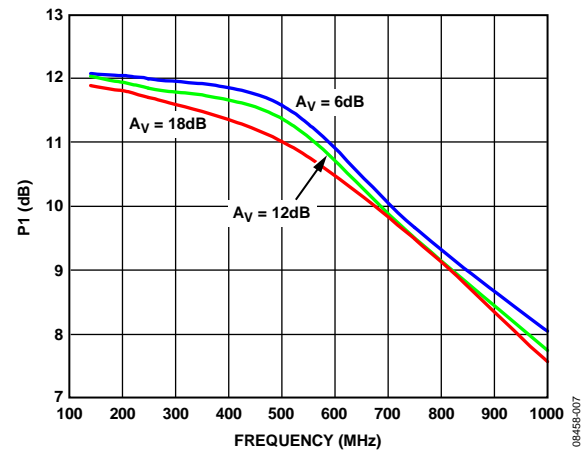


Figure 10. P_1 vs. Frequency at $A_V = 6\text{ dB}$, $A_V = 12\text{ dB}$, and $A_V = 18\text{ dB}$

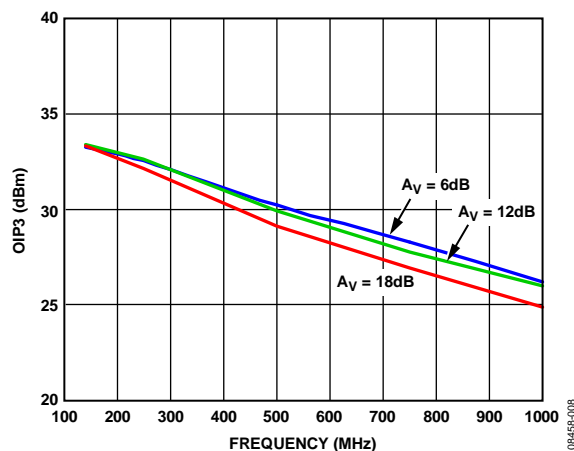


Figure 11. OIP3 vs. Frequency at $A_V = 6$ dB, $A_V = 12$ dB, and $A_V = 18$ dB, $V_{OUT} = 0.45$ V p-p/Tone, 2 MHz Spacing

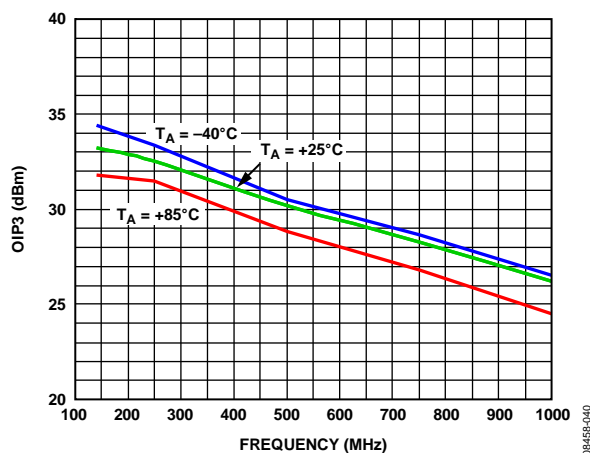


Figure 12. OIP3 vs. Frequency at $A_V = 6$ dB, $T_A = -40^\circ\text{C}$, $T_A = +25^\circ\text{C}$, and $T_A = +85^\circ\text{C}$, $V_{OUT} = 0.45$ V p-p/Tone, 2 MHz Spacing

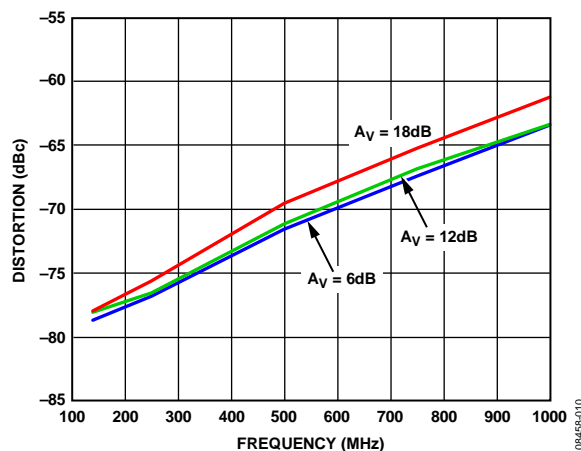


Figure 13. Two Tone IMD3 vs. Frequency, $A_V = 6$ dB, $A_V = 12$ dB, and $A_V = 18$ dB, $V_{OUT} = 0.9$ V p-p/Tone, 2 MHz Spacing

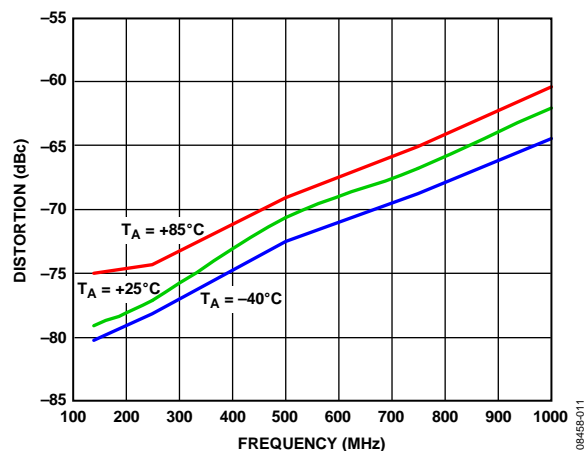


Figure 14. Two Tone IMD3 vs. Frequency at $T_A = -40^\circ\text{C}$, $T_A = +25^\circ\text{C}$, and $T_A = +85^\circ\text{C}$, $A_V = 6$ dB, $V_{OUT} = 0.45$ V p-p/Tone, 2 MHz Spacing

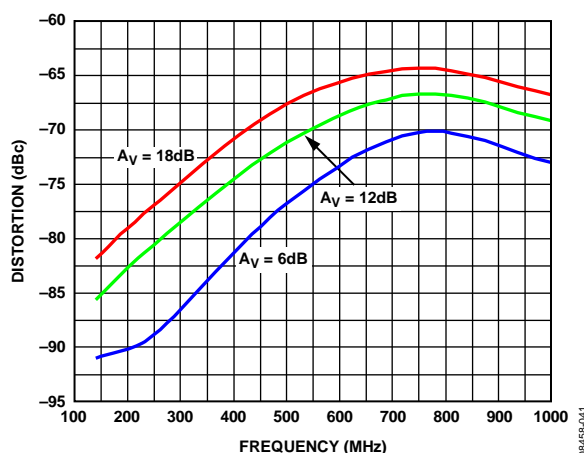


Figure 15. HD2 vs. Frequency at $A_V = 6$ dB, $A_V = 12$ dB, and $A_V = 18$ dB, $V_{OUT} = 0.9$ V p-p

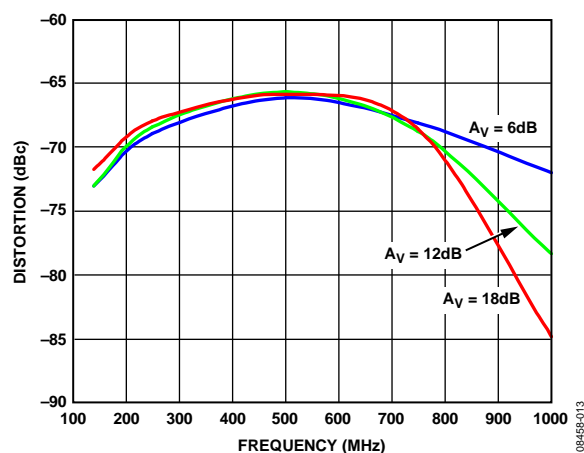


Figure 16. HD3 vs. Frequency at $A_V = 6$ dB, $A_V = 12$ dB, and $A_V = 18$ dB, $V_{OUT} = 0.9$ V p-p

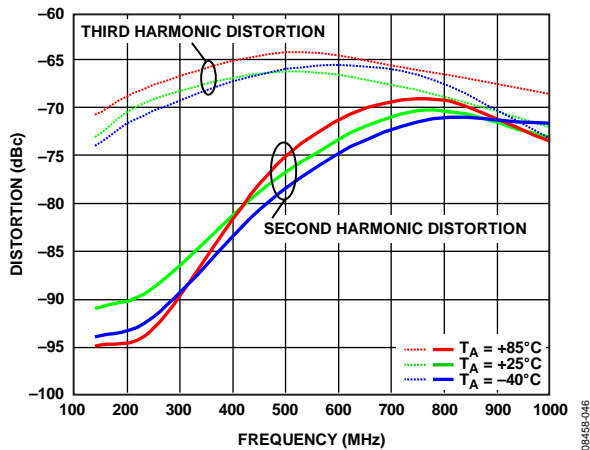


Figure 17. HD2 and HD3 vs. Frequency at $T_A = -40^\circ\text{C}$, $+25^\circ\text{C}$, $+85^\circ\text{C}$, $A_V = 6\text{ dB}$, $V_{OUT} = 0.9\text{ V p-p}$

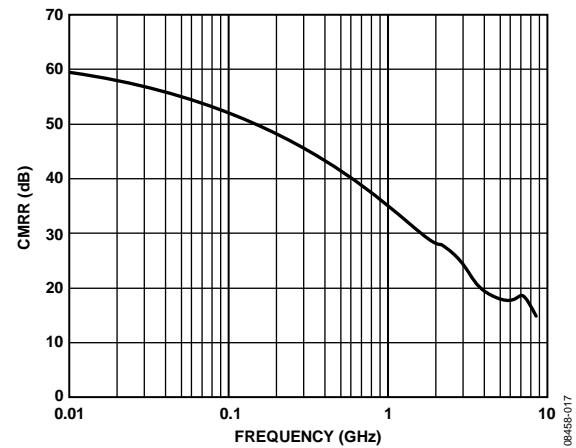


Figure 20. CMRR vs. Frequency, $A_V = 6\text{ dB}$, $V_{OUT} = 0.9\text{ V p-p}$

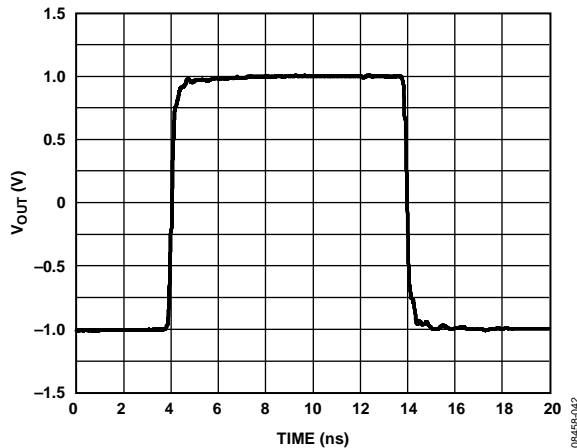


Figure 18. Large Signal Pulse Response, $A_V = 18\text{ dB}$

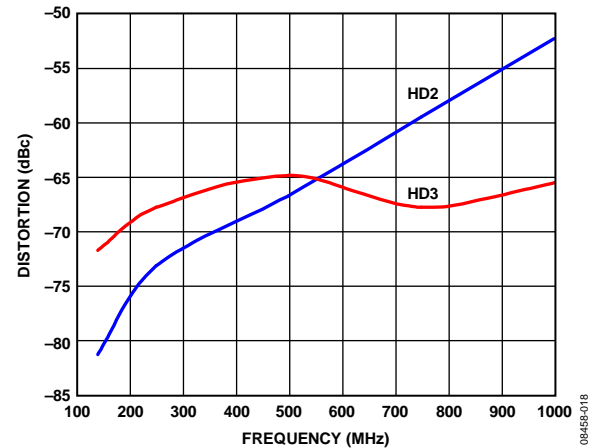


Figure 21. HD2/HD3 vs. Frequency, Single-Ended Input, $A_V = 6\text{ dB}$, $V_{OUT} = 0.9\text{ V p-p}$

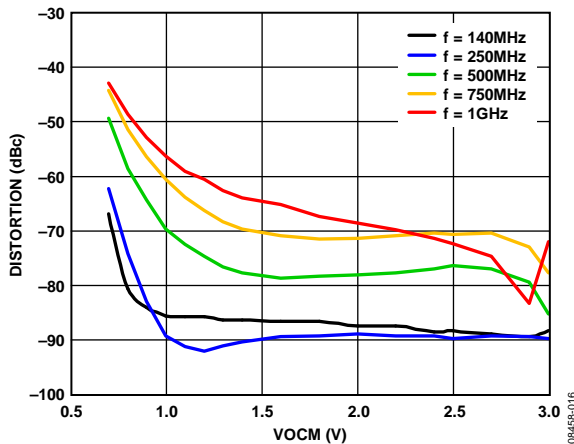


Figure 19. HD2 vs. VOCM, $A_V = 6\text{ dB}$, $V_{OUT} = 0.9\text{ V p-p}$, $f = 140\text{ MHz}$, $f = 250\text{ MHz}$, $f = 500\text{ MHz}$, $f = 750\text{ MHz}$, $f = 1\text{ GHz}$

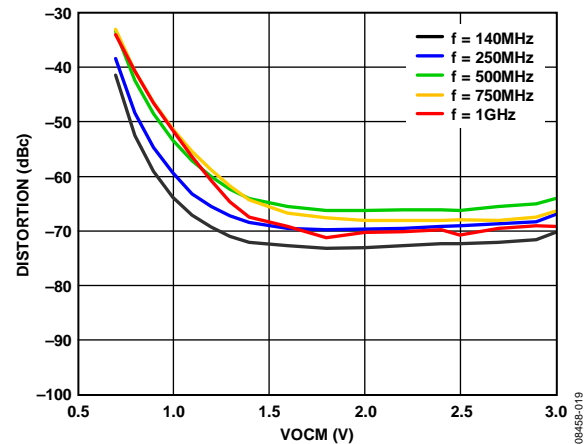


Figure 22. HD3 vs. VOCM, $A_V = 6\text{ dB}$, $V_{OUT} = 0.9\text{ V p-p}$, $f = 140\text{ MHz}$, $f = 250\text{ MHz}$, $f = 500\text{ MHz}$, $f = 750\text{ MHz}$, $f = 1\text{ GHz}$

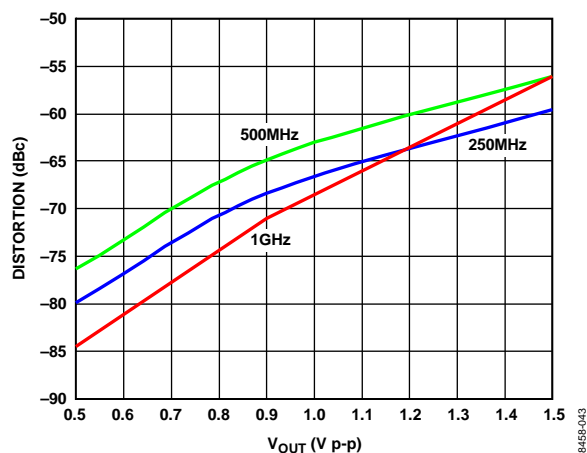


Figure 23. HD3 vs. Output Amplitude @ 250 MHz, 500 MHz, 1 GHz,
 $A_V = 6$ dB, $V_{OUT} = 0.9$ V p-p

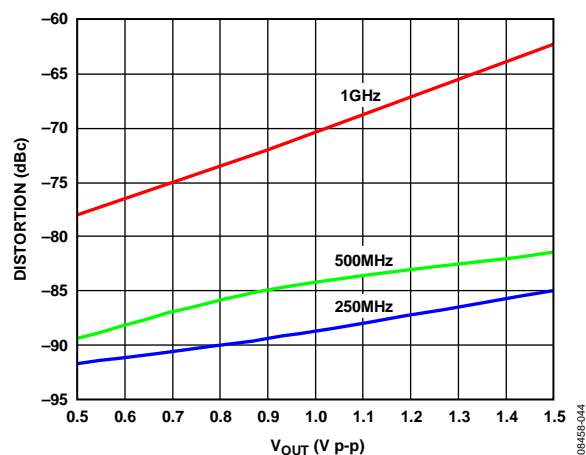


Figure 25. HD2 vs. V_{OUT} @ 250 MHz, 500 MHz, and 1 GHz,
 $A_V = 6$ dB, $V_{OUT} = 0.9$ V p-p

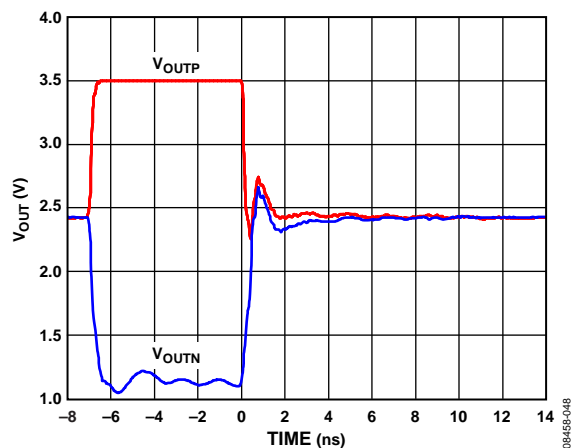


Figure 24. Output Overdrive, V_{OUT} vs. Time, $V_{IN} = 1$ V p-p, $A_V = 12$ dB

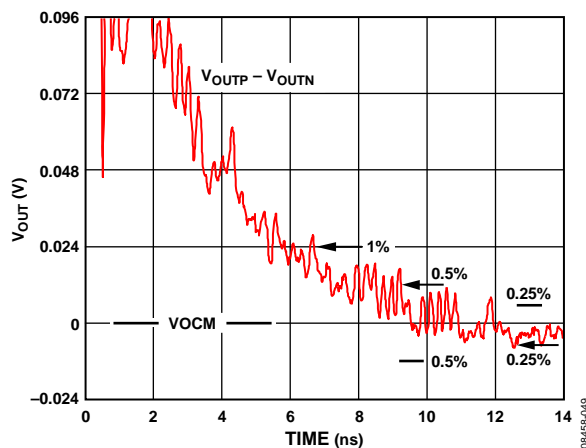


Figure 26. Output Overdrive Recovery, V_{OUT} vs. Time,
 $V_{IN} = 1$ V p-p, $A_V = 12$ dB, $V_{OCM} = 2.4$ V

TEST CIRCUITS

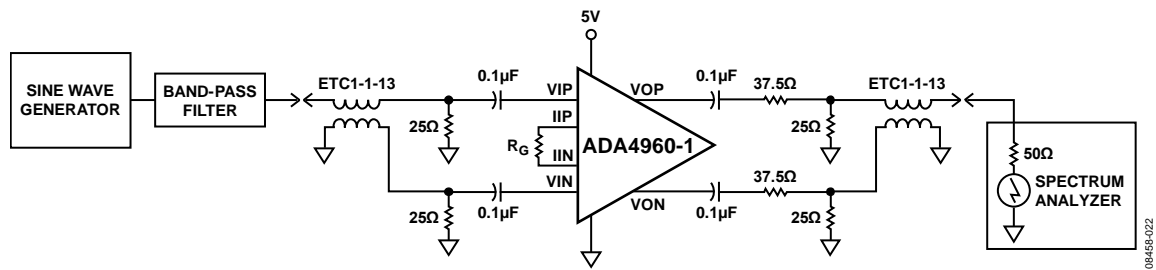


Figure 27. Distortion Test Circuit

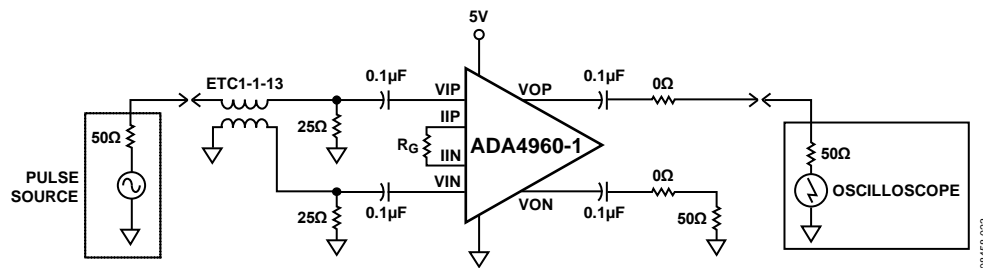


Figure 28. Time Domain Test Circuit

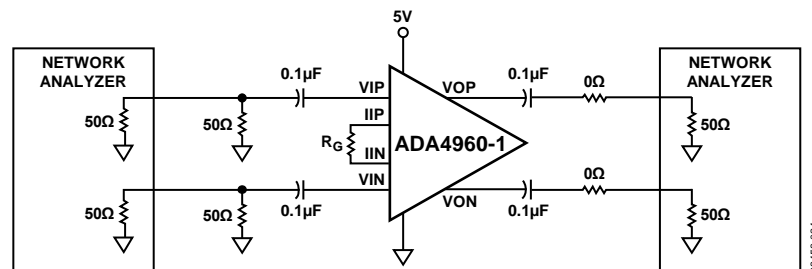


Figure 29. S-Parameter Test Circuit

CIRCUIT DESCRIPTION

BASIC STRUCTURE

The ADA4960-1 is a low noise, fully differential amplifier/ADC driver that uses a single 5 V supply at 60 mA. This amplifier has buffered inputs that isolate the gain-setting resistor (R_G) from the input signals, keeping a constant 10 k Ω differential input impedance for all gains.

The differential output impedance is 150 Ω . The gain range is 0 dB to 18 dB and is set using a single resistor (R_G).

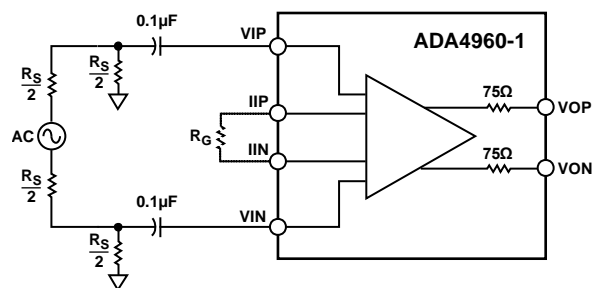


Figure 30. Basic Structure of the ADA4960-1

The ADA4960-1 can be ac-coupled or dc-coupled at the inputs and/or outputs within the specified input and output common-mode range.

The inputs, VIP and VIN, have a common-mode voltage range of 2.25 V to 2.75 V and are internally set at $V_{CC}/2$. The outputs, VOP and VON, have a common-mode voltage range of 1.0 V to 2.75 V that can be set externally using the V_{OCM} pin. The V_{OCM} pin is internally set to $V_{CC}/2$ with no external connection.

The input of the device can be configured as single-ended or differential with similar HD3 distortion results.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The basic connections for operating the ADA4960-1 are shown in Figure 33. Connect VCC to 5 V and decouple each supply pin with a low inductance surface-mount ceramic capacitor of 0.1 μ F placed as close to the device as possible.

In addition, decouple the VOCM pin and the VCI pin by using a 0.1 μ F capacitor, whether or not they are used as inputs.

For normal operation, the enable pin (PD) should be tied to VCC. When the ADA4960-1 is pulled low, it goes into power-down mode. The VOP and VON outputs are internally biased at VCC/2 with no external source. The output common-mode range can be adjusted in the range of 1 V to 2.75 V by applying an external source voltage to the VCOM pin.

INPUT AND OUTPUT INTERFACING

The ADA4960-1 can be configured as a differential-input-to-differential-output driver, as shown in Figure 31.

The differential broadband input is provided by the ETC1-1-13 balun transformer. The two 25 Ω resistors, R1 and R2, provide the 50 Ω match to the 50 Ω ac source. The 0.1 μ F capacitors, connected in series with the inputs and outputs, isolate the source and balanced load from the internal bias. R_G is the gain-setting resistor. Load R_L should equal 100 Ω to provide the expected ac performance (see the Specifications section). Different loads can be applied with the gain value described by the gain adjust equation (see the Gain Adjust section).

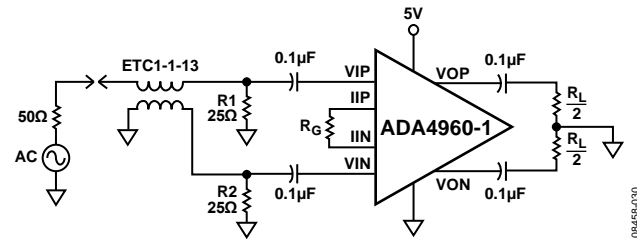


Figure 31. Differential-Input-to-Differential-Output Configuration

The ADA4960-1 can also be configured as a single-ended-input-to-differential-output driver, as shown in Figure 32. R1 provides the input source match, and R2 balances the input source impedances. The 0.1 μ F capacitors, connected in series with the inputs and outputs, isolate the source and balanced load from the internal bias. R_G is the gain-setting resistor. R_L should equal 100 Ω to provide the expected ac performance (see the Specifications section).

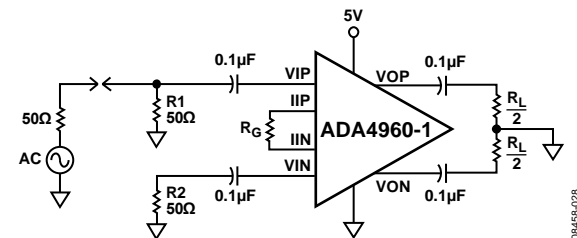


Figure 32. Single-Ended-Input-to-Differential-Output Configuration

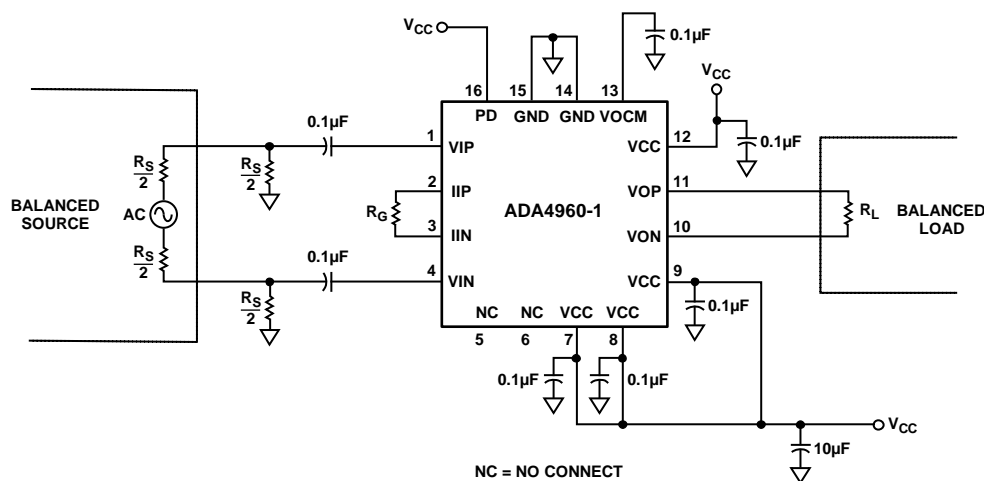


Figure 33. Basic Connections of the ADA4960-1

GAIN ADJUST

The gain of the ADA4960-1 is set with a single resistor, R_G , connected across the IIP and IIN pins. Because the output impedance is 150 Ω , the load affects the gain. The voltage gain can be calculated for both differential and single-ended inputs as follows:

$$A_V = 4.7 \frac{\left(\frac{150 R_L}{150 + R_L} \right)}{(35.5 + R_G)}$$

where R_L and R_G are the load and gain-setting resistors.

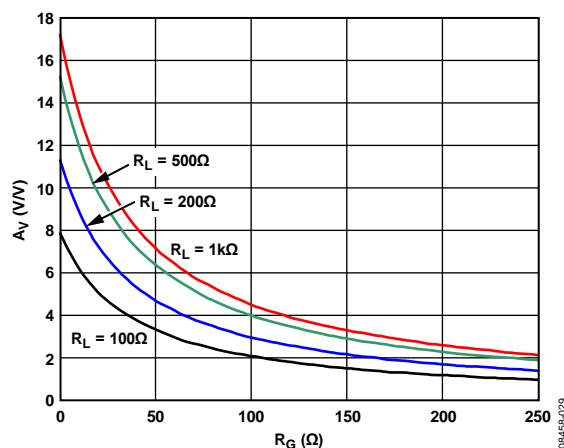


Figure 34. A_V vs. R_G for $R_L = 100 \Omega$, $R_L = 200 \Omega$, $R_L = 500 \Omega$, and $R_L = 1 \text{ k}\Omega$

Table 5. A_V vs. R_G for $R_L = 100 \Omega$, $R_L = 200 \Omega$, $R_L = 500 \Omega$, and $R_L = 1 \text{ k}\Omega$

A_V (dB)	R_G			
	$R_L = 100 \Omega$	$R_L = 200 \Omega$	$R_L = 500 \Omega$	$R_L = 1 \text{ k}\Omega$
0	246	370	505	576
6	106	167	237	271
12	35.2	65.7	101	118
18	0	15.2	32.8	41.7

BANDWIDTH EXTENSION

The bandwidth of the ADA4960-1 can be extended for both differential and single-ended input configurations by connecting a capacitor, C_S , in parallel with the gain-setting resistor, R_G , as shown in Figure 35.

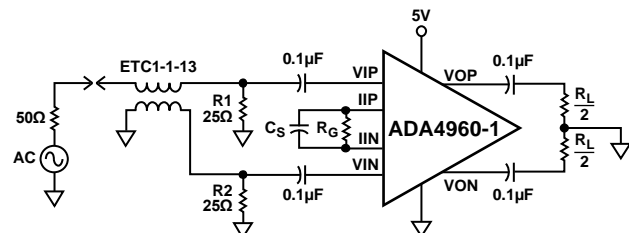


Figure 35. ADA4960-1 with Bandwidth Extension

Figure 36 shows the bandwidth extension for 6 dB and 12 dB gains. Figure 37 shows the recommended C_S values for most gains (dB).

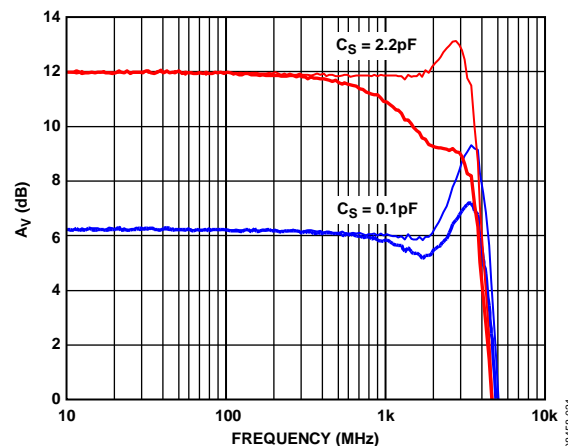


Figure 36. Bandwidth Extension for 6 dB and 12 dB Gains

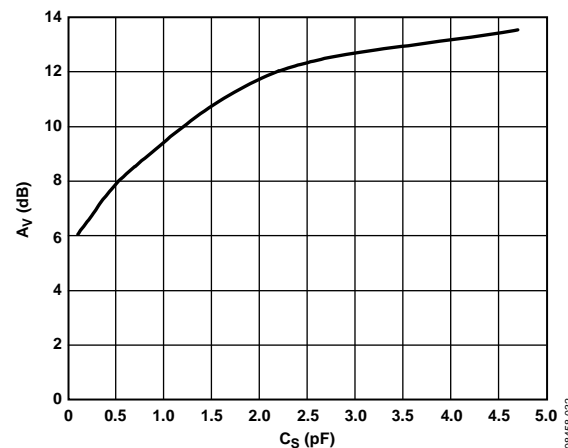


Figure 37. Recommended C_S Values for Most Gains

ADC INTERFACING

The ADA4960-1 is a high speed amplifier with linearity performance to drive high speed ADCs up to 1 GHz. Several options are available to the designer to interface with an ADC.

The ADA4960-1 in Figure 38 is a differential input configuration, using an input balun to provide the differential input signal. The 25 Ω resistors provide the input source match. The ADA4960-1 outputs can be directly connected to the ADC inputs as long as the ADC input common mode is within the output common-mode range of the ADA4960-1. The ADC V_{CM} output pin is connected to the ADA4960-1 VOCM input pin to align the ADA4960-1 output voltages with the ADC inputs.

A 100 Ω resistor across the outputs of the ADA4960-1 enhances system bandwidth and distortion performance when the ADA4960-1 is driving an ADC with high input impedance. Lighter load resistance improves distortion performance and lowers the overall bandwidth.

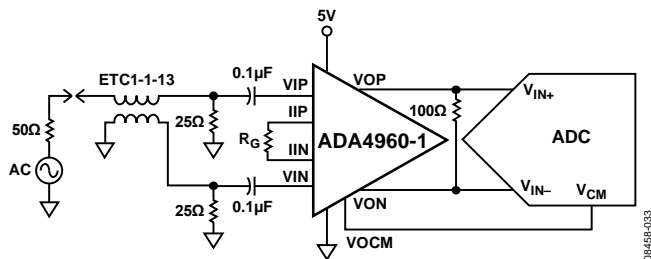


Figure 38. Differential Input Configuration Directly Driving the ADC

The ADA4960-1 in Figure 39 is a single-ended input configuration. The input is matched to the source with 50 Ω resistors. The ADA4960-1 outputs can be directly connected to the ADC inputs as long as the ADC input common mode is within the output common-mode range of the ADA4960-1.

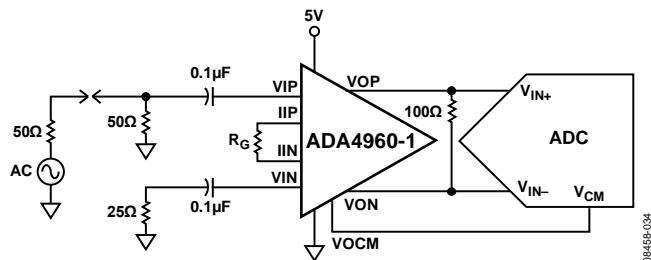


Figure 39. Single-Ended Input Configuration Directly Driving the ADC

The signal source can be directly connected to the ADA4960-1 inputs as long as the source dc level is within the common-mode input range of the ADA4960-1, as shown in Figure 40.

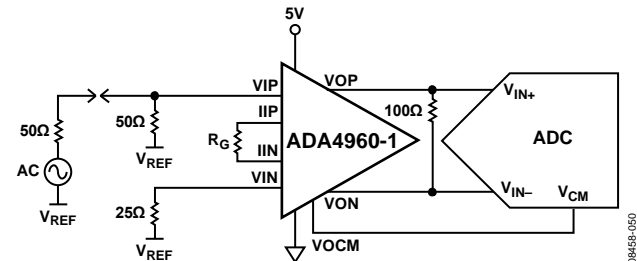


Figure 40. Single-Ended Input Configuration, DC-Coupled Inputs and Outputs

When the ADC input common mode is outside the output common-mode range of the ADA4960-1, the outputs can be ac-coupled to provide coupling, as shown in Figure 41.

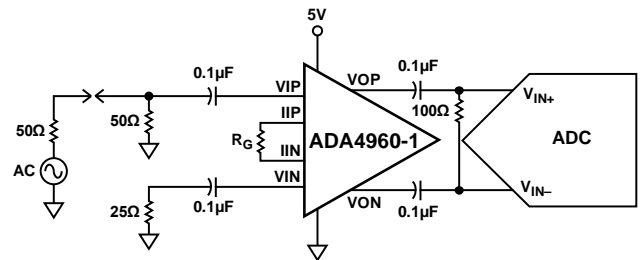


Figure 41. Single-Ended Input Configuration, AC-Coupled to the ADC

LINE DRIVER APPLICATIONS

The user accessible gain adjust and bandwidth extension features allow configuration of the ADA4960-1 for line driver and channel equalization applications from dc to 6.5 Gbps.

Because of its extremely low distortion performance and high linearity, the ADA4960-1 can be deployed in cable and backplane channels to extend channel length and improve signaling margin for serial links using receive equalization and transmit pre-emphasis. The ADA4960-1 unidirectional signal path is protocol and encoding agnostic, supporting myriad signaling types such as NRZ and PAM2/4/8/N, coded (8b/10b), uncoded, and out-of-band (SATA-OOB) data.

OVERDRIVE AND RECOVERY

When overdriven, the ADA4960-1 limits its outputs to 3.4 V typical with no overshoot, as shown in Figure 42. This feature protects the ADC from transients, eliminating the need for additional external clamping at the inputs of the ADC.

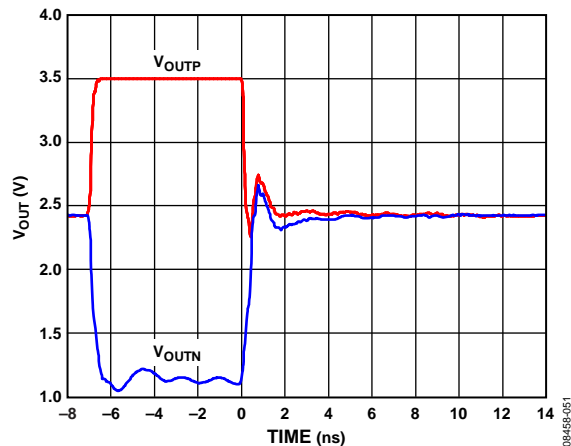


Figure 42. Output Overdrive, $V_{IN} = 1\text{ V p-p}$, $A_V = 12\text{ dB}$

Recovery from overdrive is 6.7 ns to 1%, 9.3 ns to 0.5%, and 12.6 ns to 0.25% of the final output voltage, see Figure 43.

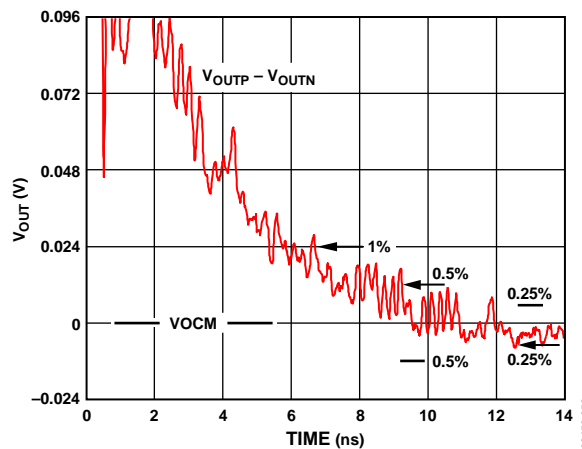
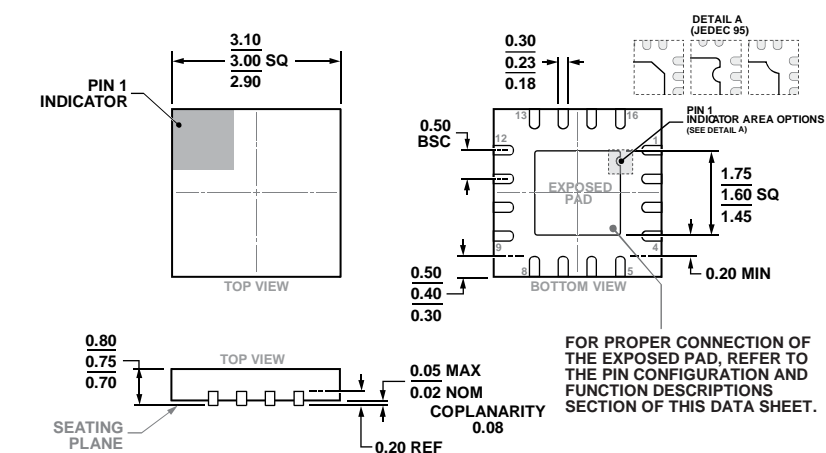


Figure 43. Output Overdrive Recovery

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 46. 16-Lead Lead Frame Chip Scale Package [LFCSP]

3 mm x 3 mm Body and 0.75 mm Package Height

(CP-16-22)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4960-1ACPZ-R2	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22	250	H23
ADA4960-1ACPZ-RL	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22	5,000	H23
ADA4960-1ACPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22	1,500	H23
ADA4960-1ACP-EBZ		Evaluation Board			

¹ Z = RoHS Compliant Part.