

# AD9283—SPECIFICATIONS ( $V_{DD} = 3.0\text{ V}$ , $V_D = 3.0\text{ V}$ ; single-ended input; external reference, unless otherwise noted)

| Parameter                                          | Temp | Test Level | AD9283BRS-100      |       |       | AD9283BRS-80       |       |       | AD9283BRS-50       |       |       | Unit   |
|----------------------------------------------------|------|------------|--------------------|-------|-------|--------------------|-------|-------|--------------------|-------|-------|--------|
|                                                    |      |            | Min                | Typ   | Max   | Min                | Typ   | Max   | Min                | Typ   | Max   |        |
| RESOLUTION                                         |      |            | 8                  |       |       | 8                  |       |       | 8                  |       |       | Bits   |
| DC ACCURACY                                        |      |            |                    |       |       |                    |       |       |                    |       |       |        |
| Differential Nonlinearity                          | 25°C | I          |                    | ±0.5  | +1.25 |                    | ±0.5  | +1.25 |                    | ±0.5  | +1.25 | LSB    |
|                                                    | Full | VI         |                    |       | +1.50 |                    |       | +1.50 |                    |       | +1.50 | LSB    |
| Integral Nonlinearity                              | 25°C | I          | −1.25              | ±0.75 | +1.25 | −1.25              | ±0.75 | +1.25 | −1.25              | ±0.75 | +1.25 | LSB    |
|                                                    | Full | VI         |                    |       | +2.25 |                    |       | +1.50 |                    |       | +1.50 | LSB    |
| No Missing Codes                                   | Full | VI         | Guaranteed         |       |       | Guaranteed         |       |       | Guaranteed         |       |       |        |
| Gain Error <sup>1</sup>                            | 25°C | I          | −6                 | ±2.5  | +6    | −6                 | ±2.5  | +6    | −6                 | ±2.5  | +6    | % FS   |
|                                                    | Full | VI         | −8                 |       | +8    | −8                 |       | +8    | −8                 |       | +8    | % FS   |
| Gain Tempco <sup>1</sup>                           | Full | VI         | 80                 |       |       | 80                 |       |       | 80                 |       |       | ppm/°C |
| ANALOG INPUT                                       |      |            |                    |       |       |                    |       |       |                    |       |       |        |
| Input Voltage Range                                | Full | V          |                    | ±512  |       |                    | ±512  |       |                    | ±512  |       | mV p-p |
| (With Respect to $A_{IN}$ )                        | Full | V          |                    | ±200  |       |                    | ±200  |       |                    | ±200  |       | mV     |
| Common-Mode Voltage                                | 25°C | I          | −35                | ±10   | +35   | −35                | ±10   | +35   | −35                | ±10   | +35   | mV     |
| Input Offset Voltage                               | Full | VI         |                    | ±40   |       |                    | ±40   |       |                    | ±40   |       | mV     |
| Reference Voltage                                  | Full | VI         | 1.2                | 1.25  | 1.3   | 1.2                | 1.25  | 1.3   | 1.2                | 1.25  | 1.3   | V      |
| Reference Tempco                                   | Full | VI         |                    | ±130  |       |                    | ±130  |       |                    | ±130  |       | ppm/°C |
| Input Resistance                                   | 25°C | I          | 7                  | 10    | 13    | 7                  | 10    | 13    | 7                  | 10    | 13    | kΩ     |
|                                                    | Full | VI         | 5                  |       | 16    | 5                  |       | 16    | 5                  |       | 16    | kΩ     |
| Input Capacitance                                  | 25°C | V          |                    | 2     |       |                    | 2     |       |                    | 2     |       | pF     |
|                                                    | Full | VI         |                    |       |       |                    |       |       |                    |       |       | μA     |
| Analog Bandwidth, Full Power                       | 25°C | V          |                    | 475   |       |                    | 475   |       |                    | 475   |       | MHz    |
| SWITCHING PERFORMANCE                              |      |            |                    |       |       |                    |       |       |                    |       |       |        |
| Maximum Conversion Rate                            | Full | VI         | 100                |       |       | 80                 |       |       | 50                 |       |       | MSPS   |
| Minimum Conversion Rate                            | 25°C | IV         |                    |       | 1     |                    |       | 1     |                    |       | 1     | MSPS   |
| Encode Pulsewidth High ( $t_{EH}$ )                | 25°C | IV         | 4.3                |       | 1000  | 5.0                |       | 1000  | 8.0                |       | 1000  | ns     |
| Encode Pulsewidth Low ( $t_{EL}$ )                 | 25°C | IV         | 4.3                |       | 1000  | 5.0                |       | 1000  | 8.0                |       | 1000  | ns     |
| Aperture Delay ( $t_A$ )                           | 25°C | V          |                    | 0     |       |                    | 0     |       |                    | 0     |       | ns     |
| Aperture Uncertainty (Jitter)                      | 25°C | V          |                    | 5     |       |                    | 5     |       |                    | 5     |       | ps rms |
| Output Valid Time ( $t_V$ ) <sup>2</sup>           | Full | VI         | 2.0                | 3.0   |       | 2.0                | 3.0   |       | 2.0                | 3.0   |       | ns     |
| Output Propagation Delay ( $t_{PD}$ ) <sup>2</sup> | Full | VI         |                    | 4.5   | 7.0   |                    | 4.5   | 7.0   |                    | 4.5   | 7.0   | ns     |
| DIGITAL INPUTS                                     |      |            |                    |       |       |                    |       |       |                    |       |       |        |
| Logic “1” Voltage                                  | Full | VI         | 2.0                |       |       | 2.0                |       |       | 2.0                |       |       | V      |
| Logic “0” Voltage                                  | Full | VI         |                    |       | 0.8   |                    |       | 0.8   |                    | 0.8   |       | V      |
| Logic “1” Current                                  | Full | VI         |                    |       | ±1    |                    |       | ±1    |                    |       | ±1    | μA     |
| Logic “0” Current                                  | Full | VI         |                    |       | ±1    |                    |       | ±1    |                    |       | ±1    | μA     |
| Input Capacitance                                  | 25°C | V          |                    | 2.0   |       |                    | 2.0   |       |                    | 2.0   |       | pF     |
| DIGITAL OUTPUTS                                    |      |            |                    |       |       |                    |       |       |                    |       |       |        |
| Logic “1” Voltage                                  | Full | VI         | 2.95               |       |       | 2.95               |       |       | 2.95               |       |       | V      |
| Logic “0” Voltage                                  | Full | VI         |                    |       | 0.05  |                    |       | 0.05  |                    |       | 0.05  | V      |
| Output Coding                                      |      |            | Offset Binary Code |       |       | Offset Binary Code |       |       | Offset Binary Code |       |       |        |
| POWER SUPPLY                                       |      |            |                    |       |       |                    |       |       |                    |       |       |        |
| Power Dissipation <sup>3, 4</sup>                  | Full | VI         |                    | 90    | 120   |                    | 90    | 115   |                    | 80    | 100   | mW     |
| Power-Down Dissipation                             | Full | VI         |                    | 4.2   | 7     |                    | 4.2   | 7     |                    | 4.2   | 7     | mW     |
| Power Supply Rejection Ratio (PSRR)                | 25°C | I          |                    |       | 18    |                    |       | 18    |                    |       | 18    | mV/V   |

| Parameter                                          | Temp | Test Level | AD9283BRS-100 |      |     | AD9283BRS-80 |      |     | AD9283BRS-50 |      |     | Unit |
|----------------------------------------------------|------|------------|---------------|------|-----|--------------|------|-----|--------------|------|-----|------|
|                                                    |      |            | Min           | Typ  | Max | Min          | Typ  | Max | Min          | Typ  | Max |      |
| DYNAMIC PERFORMANCE <sup>5</sup>                   |      |            |               |      |     |              |      |     |              |      |     |      |
| Transient Response                                 | 25°C | V          | 2             |      |     | 2            |      |     | 2            |      |     | ns   |
| Overvoltage Recovery Time                          | 25°C | V          | 2             |      |     | 2            |      |     | 2            |      |     | ns   |
| Signal-to-Noise Ratio (SNR)<br>(Without Harmonics) |      |            |               |      |     |              |      |     |              |      |     |      |
| f <sub>IN</sub> = 10.3 MHz                         | 25°C | I          |               | 46.5 |     |              | 47   |     | 44           | 47   |     | dB   |
| f <sub>IN</sub> = 27 MHz                           | 25°C | I          |               | 46.5 |     | 44           | 47   |     |              | 47   |     | dB   |
| f <sub>IN</sub> = 41 MHz                           | 25°C | I          | 43.5          | 46.5 |     |              | 47   |     |              |      |     | dB   |
| f <sub>IN</sub> = 76 MHz                           | 25°C | V          |               | 46.0 |     |              |      |     |              |      |     | dB   |
| Signal-to-Noise Ratio (SINAD)<br>(With Harmonics)  |      |            |               |      |     |              |      |     |              |      |     |      |
| f <sub>IN</sub> = 10.3 MHz                         | 25°C | I          |               | 45   |     |              | 47   |     | 43.5         | 46.5 |     | dB   |
| f <sub>IN</sub> = 27 MHz                           | 25°C | I          |               | 45.5 |     | 43.5         | 46.5 |     |              | 46   |     | dB   |
| f <sub>IN</sub> = 41 MHz                           | 25°C | I          | 42.5          | 45   |     |              | 42   |     |              |      |     | dB   |
| f <sub>IN</sub> = 76 MHz                           | 25°C | V          |               | 42.5 |     |              |      |     |              |      |     | dB   |
| Effective Number of Bits                           |      |            |               |      |     |              |      |     |              |      |     |      |
| f <sub>IN</sub> = 10.3 MHz                         | 25°C | I          |               | 7.3  |     |              | 7.5  |     |              | 7.6  |     | Bits |
| f <sub>IN</sub> = 27 MHz                           | 25°C | I          |               | 7.4  |     |              | 7.5  |     |              | 7.5  |     | Bits |
| f <sub>IN</sub> = 41 MHz                           | 25°C | I          |               | 7.3  |     |              | 7.5  |     |              |      |     | Bits |
| f <sub>IN</sub> = 76 MHz                           | 25°C | V          |               | 6.9  |     |              |      |     |              |      |     | Bits |
| 2nd Harmonic Distortion                            |      |            |               |      |     |              |      |     |              |      |     |      |
| f <sub>IN</sub> = 10.3 MHz                         | 25°C | I          |               | 57   |     |              | 60   |     | 55           | 60   |     | dBc  |
| f <sub>IN</sub> = 27 MHz                           | 25°C | I          |               | 60   |     | 55           | 60   |     |              | 56   |     | dBc  |
| f <sub>IN</sub> = 41 MHz                           | 25°C | I          | 50            | 58   |     |              | 55   |     |              |      |     | dBc  |
| f <sub>IN</sub> = 76 MHz                           | 25°C | V          |               | 46   |     |              |      |     |              |      |     | dBc  |
| 3rd Harmonic Distortion                            |      |            |               |      |     |              |      |     |              |      |     |      |
| f <sub>IN</sub> = 10.3 MHz                         | 25°C | I          |               | 54.5 |     |              | 70   |     | 55           | 70   |     | dBc  |
| f <sub>IN</sub> = 27 MHz                           | 25°C | I          |               | 55   |     | 55           | 62.5 |     |              | 60   |     | dBc  |
| f <sub>IN</sub> = 41 MHz                           | 25°C | I          | 47            | 52.5 |     |              | 60   |     |              |      |     | dBc  |
| f <sub>IN</sub> = 76 MHz                           | 25°C | V          |               | 53   |     |              |      |     |              |      |     | dBc  |
| Two-Tone Intermod Distortion<br>(IMD)              |      |            |               |      |     |              |      |     |              |      |     |      |
| f <sub>IN</sub> = 10.3 MHz                         | 25°C | V          |               | 52   |     |              | 52   |     |              | 52   |     | dBc  |

## NOTES

<sup>1</sup>Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.25 V external reference).

<sup>2</sup> $t_V$  and  $t_{PD}$  are measured from the 1.5 V level of the ENCODE input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of  $\pm 40 \mu\text{A}$ .

<sup>3</sup>Power dissipation measured with encode at rated speed and a dc analog input.

<sup>4</sup>Typical thermal impedance for the RS style (SSOP) 20-lead package:  $\theta_{JC} = 46^\circ\text{C/W}$ ,  $\theta_{CA} = 80^\circ\text{C/W}$ ,  $\theta_{JA} = 126^\circ\text{C/W}$ .

<sup>5</sup>SNR/harmonics based on an analog input voltage of  $-0.7 \text{ dBFS}$  referenced to a 1.024 V full-scale input range.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS\*

|                                    |                                              |
|------------------------------------|----------------------------------------------|
| $V_D, V_{DD}$ .....                | 4 V                                          |
| Analog Inputs .....                | $-0.5 \text{ V}$ to $V_D + 0.5 \text{ V}$    |
| Digital Inputs .....               | $-0.5 \text{ V}$ to $V_{DD} + 0.5 \text{ V}$ |
| $V_{REF IN}$ .....                 | $-0.5 \text{ V}$ to $V_D + 0.5 \text{ V}$    |
| Digital Output Current .....       | 20 mA                                        |
| Operating Temperature .....        | $-55^\circ\text{C}$ to $+125^\circ\text{C}$  |
| Storage Temperature .....          | $-65^\circ\text{C}$ to $+150^\circ\text{C}$  |
| Maximum Junction Temperature ..... | $150^\circ\text{C}$                          |
| Maximum Case Temperature .....     | $150^\circ\text{C}$                          |

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## ORDERING GUIDE

| Model          | Temperature Ranges                         | Package Descriptions | Package Options |
|----------------|--------------------------------------------|----------------------|-----------------|
| AD9283BRS      |                                            |                      |                 |
| -50, -80, -100 | $-40^\circ\text{C}$ to $+85^\circ\text{C}$ | 20-Lead SSOP         | RS-20           |
| AD9283/PCB     | $25^\circ\text{C}$                         | Evaluation Board     |                 |

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9283 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD9283

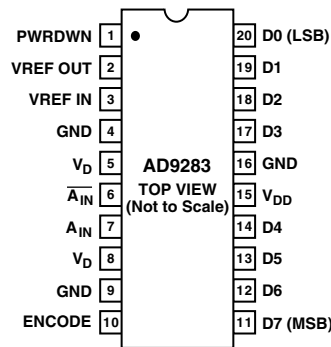
EXPLANATION OF TEST LEVELS

- Test Level**
- I 100% production tested.
  - II 100% production tested at 25°C and sample tested at specified temperatures.
  - III Sample tested only.
  - IV Parameter is guaranteed by design and characterization testing.
  - V Parameter is a typical value only.
  - VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

Table I. Output Coding (VREF = 1.25 V)

| Step | $A_{IN}-\overline{A_{IN}}$ | Digital Output |
|------|----------------------------|----------------|
| 255  | 0.512                      | 1111 1111      |
| •    | •                          | •              |
| •    | •                          | •              |
| 128  | 0.002                      | 1000 0000      |
| 127  | -0.002                     | 0111 1111      |
| •    | •                          | •              |
| •    | •                          | •              |
| 0    | -0.512                     | 0000 0000      |

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

| Pin Number   | Mnemonic            | Function                                                                                                                                                                                    |
|--------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1            | PWRDWN              | Power-Down Function Select; Logic HIGH for Power-Down Mode (Digital Outputs Go to High Impedance State)                                                                                     |
| 2            | VREF OUT            | Internal Reference Output (1.25 V typ); Bypass with 0.1 μF to Ground                                                                                                                        |
| 3            | VREF IN             | Reference Input for ADC (1.25 V typ)                                                                                                                                                        |
| 4, 9, 16     | GND                 | Ground                                                                                                                                                                                      |
| 5, 8         | V <sub>D</sub>      | Analog 3 V Power Supply                                                                                                                                                                     |
| 6            | $\overline{A_{IN}}$ | Analog Input for ADC (Can Be Left Open if Operating in Single-Ended Mode, but Recommend Connection to a 0.1 μF Capacitor and a 25 Ω Resistor in Series to Ground for Better Input Matching) |
| 7            | A <sub>IN</sub>     | Analog Input for ADC                                                                                                                                                                        |
| 10           | ENCODE              | Encode Clock for ADC (ADC Samples on Rising Edge of ENCODE)                                                                                                                                 |
| 11–14, 17–20 | D7–D4, D3–D0        | Digital Outputs of ADC                                                                                                                                                                      |
| 15           | V <sub>DD</sub>     | Digital output power supply. Nominally 2.5 V to 3.6 V                                                                                                                                       |

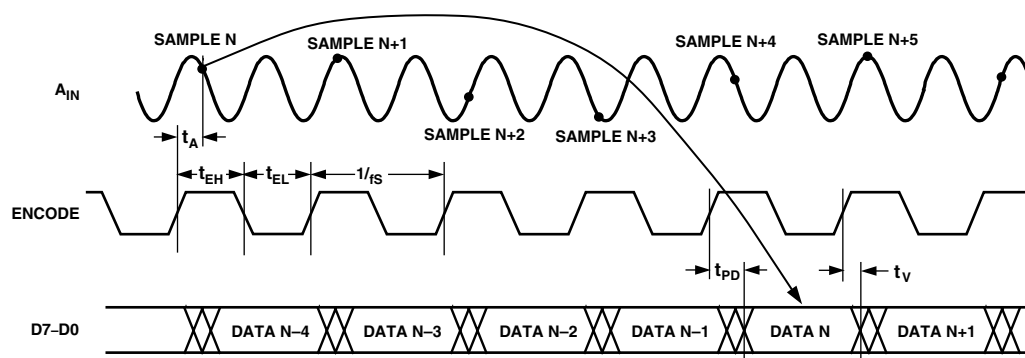


Figure 1. Timing Diagram

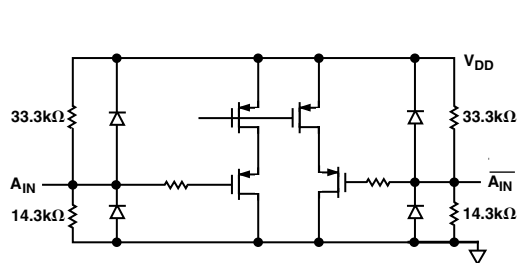


Figure 2. Equivalent Analog Input Circuit

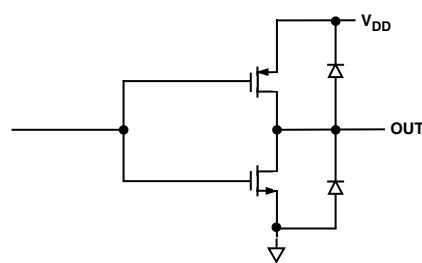


Figure 5. Equivalent Digital Output Circuit

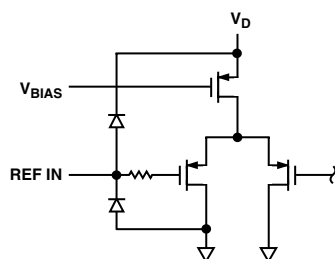


Figure 3. Equivalent Reference Input Circuit

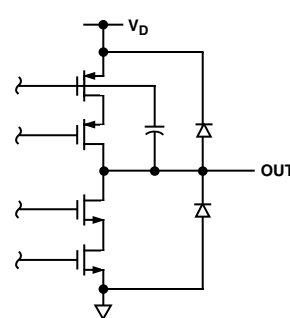


Figure 6. Equivalent Reference Output Circuit

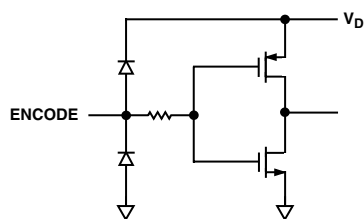
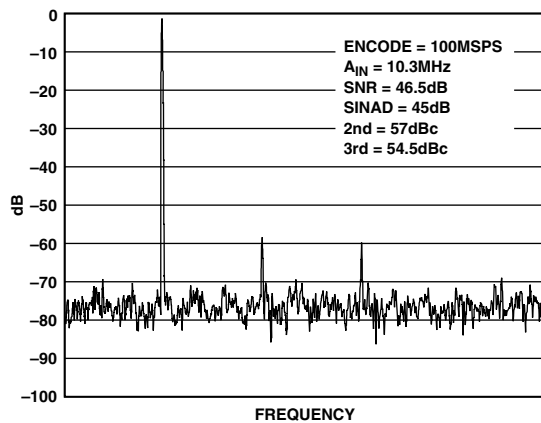
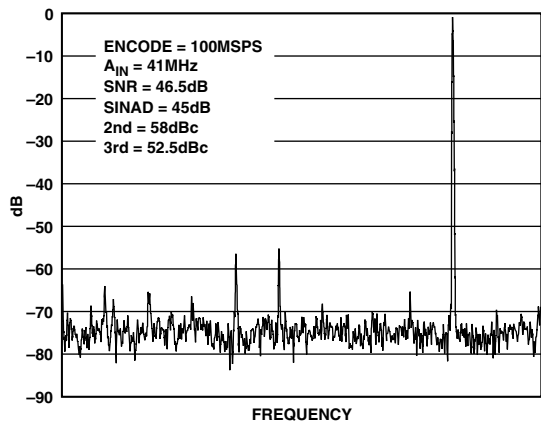


Figure 4. Equivalent Encode Input Circuit

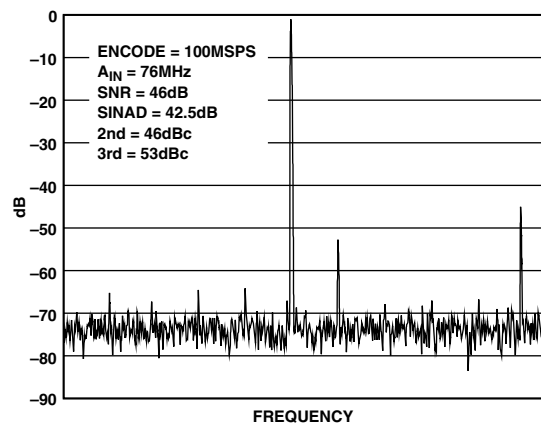
# AD9283— Typical Performance Characteristics



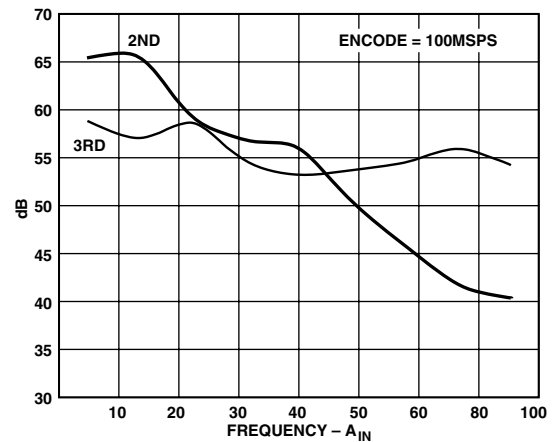
TPC 1. Spectrum:  $f_S = 100\text{ MSPS}$ ,  $f_{IN} = 10.3\text{ MHz}$



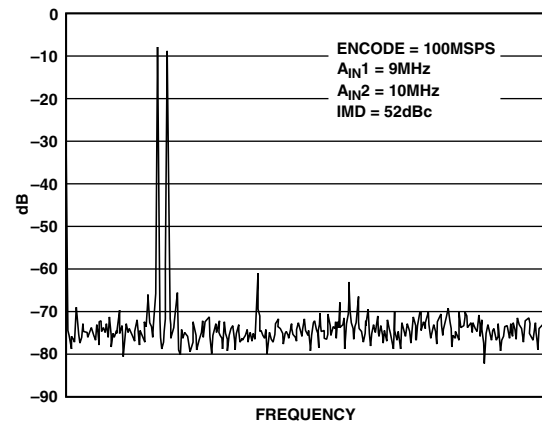
TPC 2. Spectrum:  $f_S = 100\text{ MSPS}$ ,  $f_{IN} = 40\text{ MHz}$



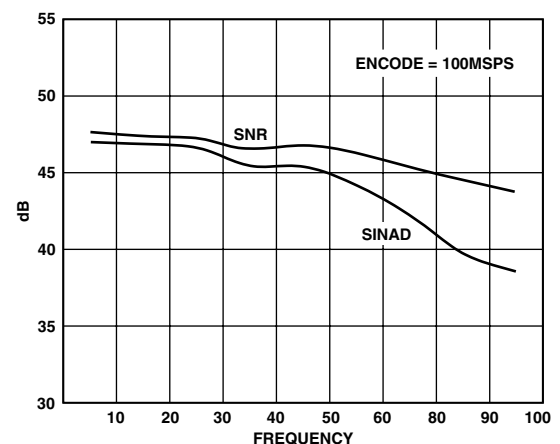
TPC 3. Spectrum:  $f_S = 100\text{ MSPS}$ ,  $f_{IN} = 76\text{ MHz}$



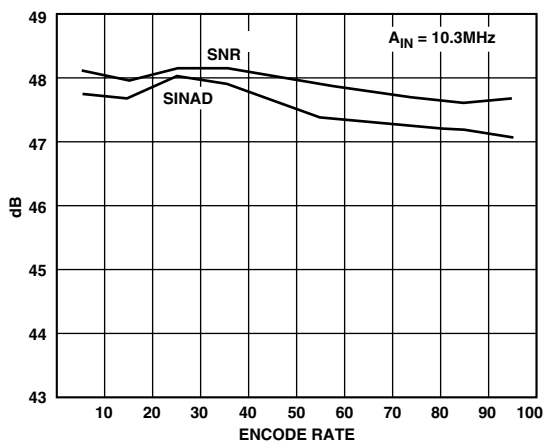
TPC 4. Harmonic Distortion vs.  $A_{IN}$  Frequency



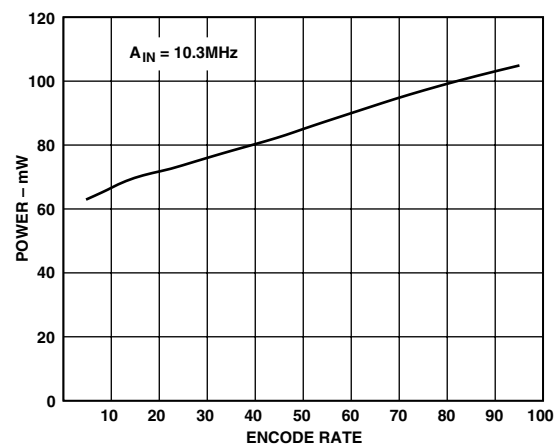
TPC 5. Two-Tone Intermodulation Distortion



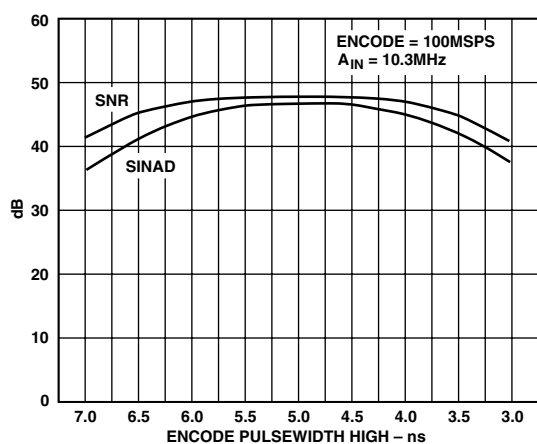
TPC 6. SINAD/SNR vs.  $A_{IN}$  Frequency



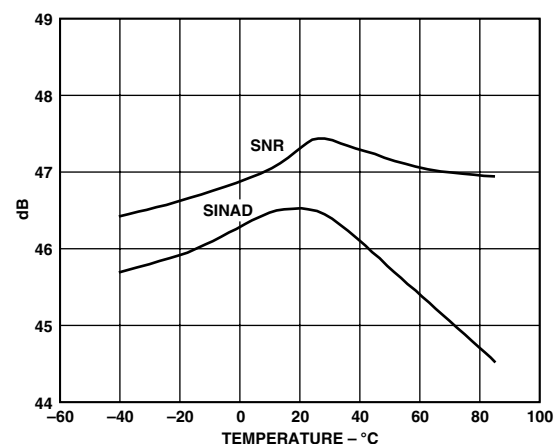
TPC 7. SINAD/SNR vs. Encode Rate



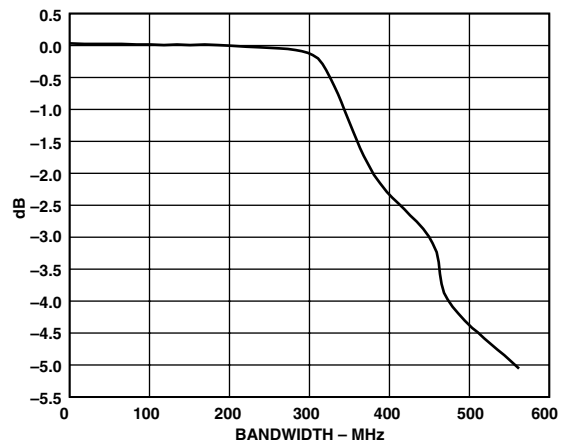
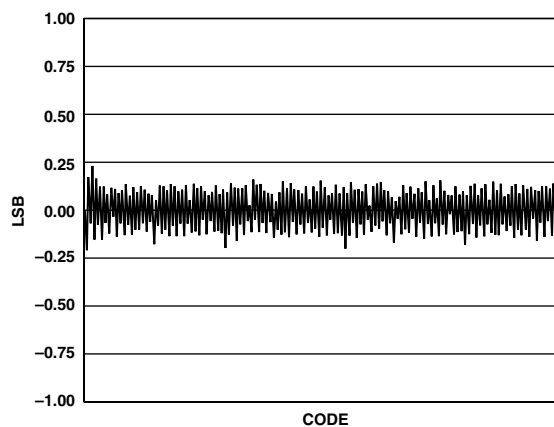
TPC 10. Analog Power Dissipation vs. Encode Rate



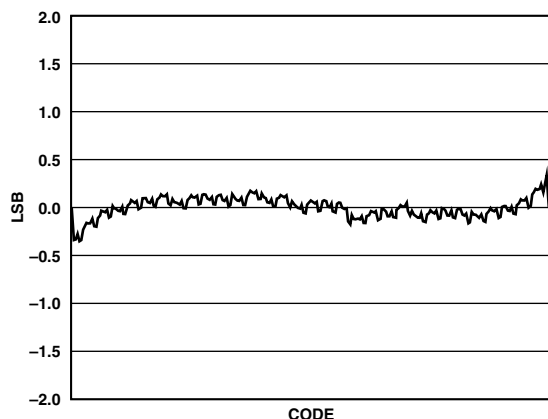
TPC 8. SINAD/SNR vs. Encode Pulsewidth High



TPC 11. SINAD/SNR vs. Temperature


TPC 9. ADC Frequency Response:  $f_s = 100$  MSPS


TPC 12. Differential Nonlinearity



TPC 13. Integral Nonlinearity

## APPLICATIONS

### Theory of Operation

The analog signal is applied differentially or single-endedly to the inputs of the AD9283. The signal is buffered and fed forward to an on-chip sample-and-hold circuit. The ADC core architecture is a bit-per-stage pipeline type converter utilizing switch capacitor techniques. The bit-per-stage blocks determine the 5 MSBs and drive a FLASH converter to encode the 3 LSBs. Each of the 5 MSB stages provides sufficient overlap and error correction to allow optimization of performance with respect to comparator accuracy. The output staging block aligns the data, carries out the error correction and feeds the data to the eight output buffers. The AD9283 includes an on-chip reference (nominally 1.25 V) and generates all clocking signals from one externally applied encode command. This makes the ADC easy to interface with and requires very few external components for operation.

### ENCODE Input

The ENCODE input is fully TTL/CMOS compatible with a nominal threshold of 1.5 V. Care was taken on the chip to match clock line delays and maintain sharp clock logic transitions. Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. This ADC uses an on-chip sample-and-hold circuit which is essentially a mixer. Any timing jitter on the ENCODE will be combined with the desired signal and degrade the high frequency performance of the ADC. The user is advised to give commensurate thought to the clock source.

### Analog Input

The analog input to the ADC is fully differential and both inputs are internally biased. This allows the most flexible use of ac or dc and differential or single-ended input modes. For peak performance the inputs are biased at  $0.3 \times V_D$ . See the specification table for allowable common-mode range when dc coupling the input. The inputs are also buffered to reduce the load the user needs to drive. For best dynamic performance, the impedances at  $A_{IN}$  and  $\bar{A}_{IN}$  should be matched. The importance of this increases with sampling rate and analog input frequency. The nominal input range is 1.024 V p-p.

### Digital Outputs

The digital outputs are TTL/CMOS compatible. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing to ease interfacing with 2.5 V or 3.3 V logic. The AD9283 goes into a low power state within two clock cycles following the assertion of the PWRDWN input. PWRDWN is asserted with a logic high. During power-down the outputs transition to a high impedance state. The time it takes to achieve optimal performance after disabling the power-down mode is approximately 15 clock cycles. Care should be taken when loading the digital outputs of any high speed ADC. Large output loads create current transients on the chip that can degrade the converter's performance.

### Voltage Reference

A stable and accurate 1.25 V voltage reference is built into the AD9283 (VREF OUT). In normal operation, the internal reference is used by strapping Pins 2 and 3 of the AD9283 together. The input range can be adjusted by varying the reference voltage applied to the AD9283. No degradation in performance occurs when the reference is adjusted  $\pm 5\%$ . The full-scale range of the ADC tracks reference voltage changes linearly. Whether used or not, the internal reference (Pin 2) should be bypassed with a 0.1  $\mu$ F capacitor to ground.

### Timing

The AD9283 provides latched data outputs with four pipeline delays. Data outputs are available one propagation delay ( $t_{PD}$ ) after the rising edge of the encode command (Figure 1. Timing Diagram). The minimum guaranteed conversion rate to the ADC is 1 MSPS. The dynamic performance of the converter will degrade at encode rates below this sample rate.

### Evaluation Board

The AD9283 evaluation board offers an easy way to test the AD9283. It only requires a 3 V supply, an analog input and encode clock to test the AD9283. The board is shipped with the 100 MSPS grade ADC.

The analog input to the board accepts a 1 V p-p signal centered at ground. J1 should be used (Jump E3–E4, E18–E19) to drive the ADC through Transformer T1. J2 should be used for single-ended input drive (Jump E19–E21).

Both J1 and J2 are terminated to 50  $\Omega$  on the PCB. Each analog path is ac-coupled to an on-chip resistor divider which provides the required dc bias.

A (TTL/CMOS Level) sample clock is applied to connector J3 which is terminated through 50  $\Omega$  on the PCB. This clock is buffered by U5 which also provides the clocks for the 574 latches, DAC, and the off-card latch clock CLKCON. (Timing can be modified at E17.)

There is a reconstruction DAC (AD9760) on the PCB. The DAC is on the board to assist in debug only—the outputs should not be used to measure performance of the ADC.

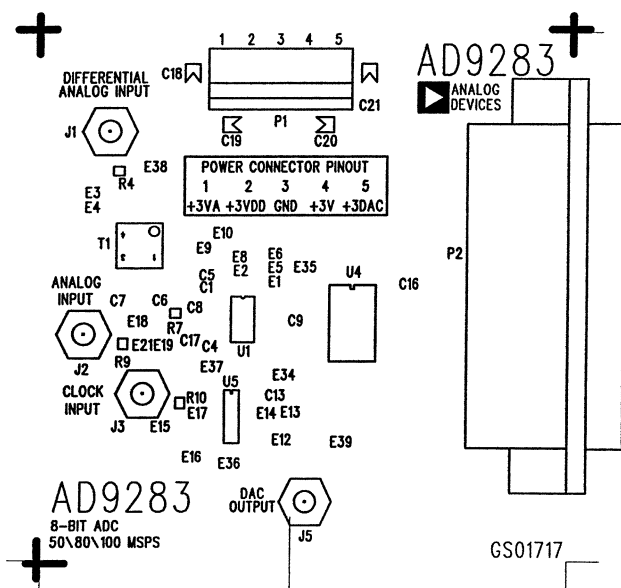


Figure 7. Printed Circuit Board Top Side Silkscreen

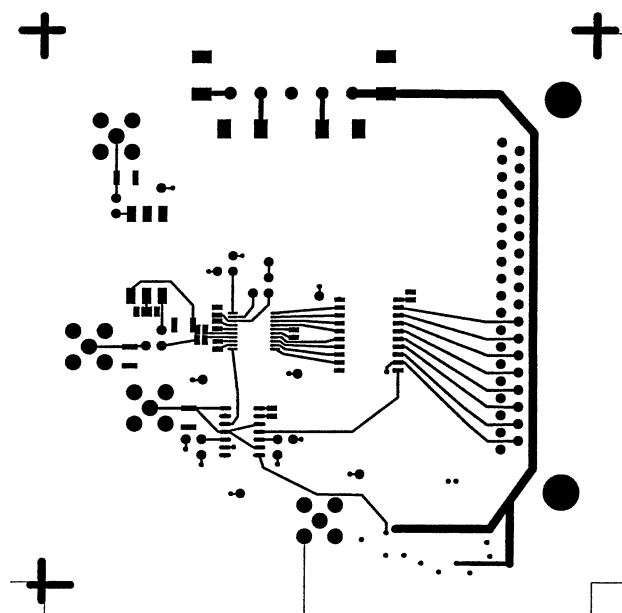


Figure 9. Printed Circuit Board Top Side Copper

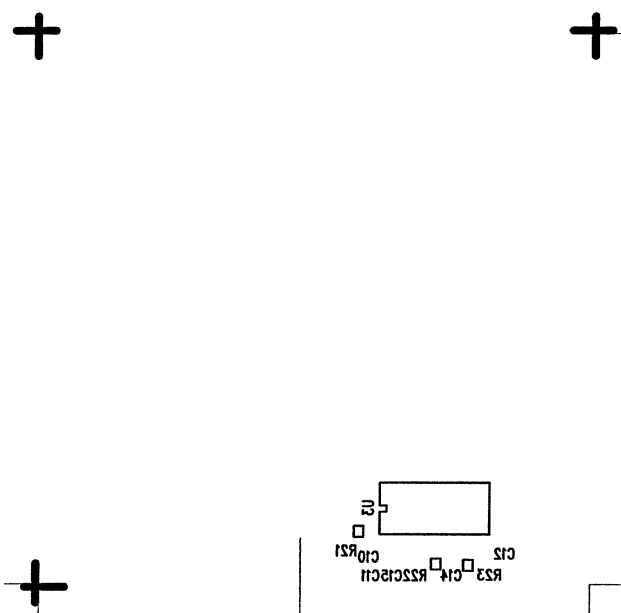


Figure 8. Printed Circuit Board Bottom Side Silkscreen

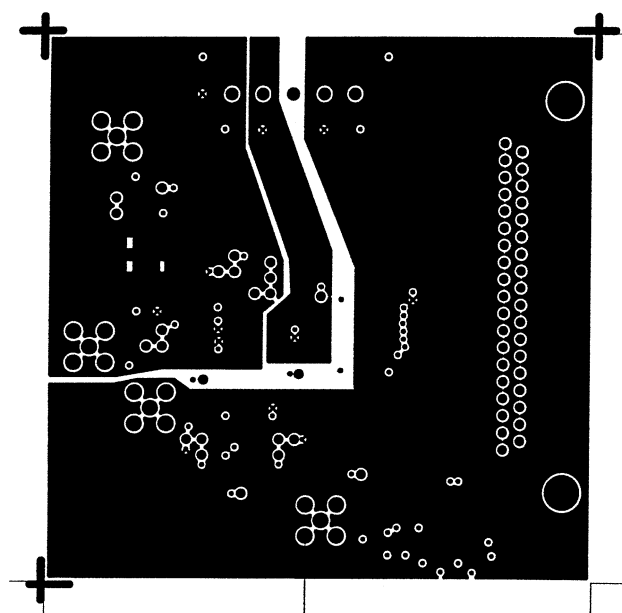


Figure 10. Printed Circuit Board "Split" Power Layer

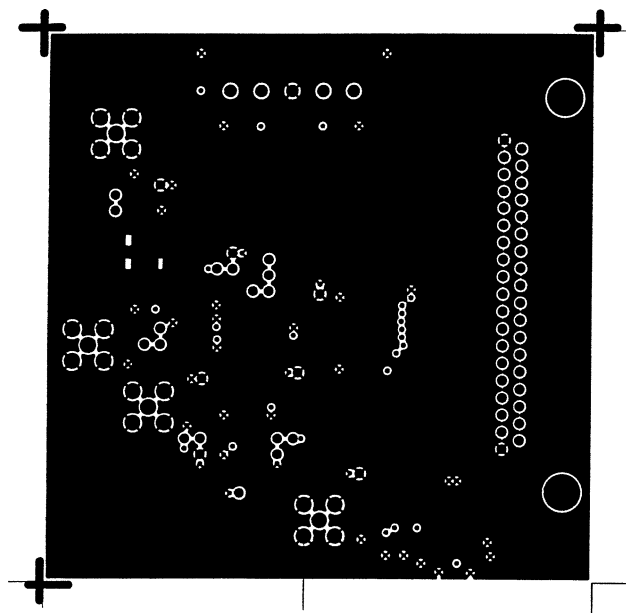


Figure 11. Printed Circuit Board Ground Layer

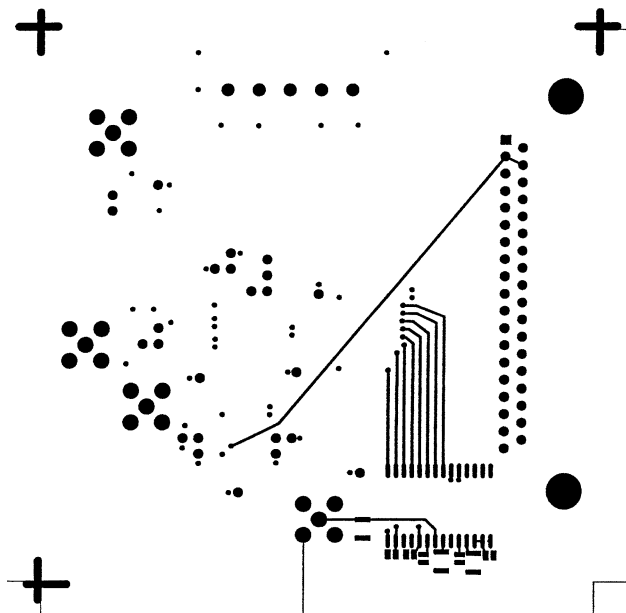


Figure 12. Printed Circuit Board Bottom Side Copper

EVALUATION BOARD BILL OF MATERIALS — GS01717

| #  | Qty | REFDES                               | Device           | Package  | Value                                                                      |
|----|-----|--------------------------------------|------------------|----------|----------------------------------------------------------------------------|
| 1  | 15  | C1, C4–C17                           | Ceramic Cap      | 0603     | 0.1 $\mu$ F                                                                |
| 2  | 4   | C18–C21                              | Tantalum Cap     | BCAPTAJD | 10 $\mu$ F                                                                 |
| 3  | 24  | E1–E6, E8–E10, E12–E19, E21, E34–E39 | W-HOLE           |          |                                                                            |
| 4  | 4   | J1, J2, J3, J5                       | Connector        | SMB      |                                                                            |
| 5  | 1   | P1                                   | 5-Pin Connector  |          | Wieland Connector<br>(P/N #25.602.2553.0 Top<br>P/N #Z5.530.0525.0 Bottom) |
| 6  | 1   | P2                                   | 37-Pin Connector |          | AMP-747462-2                                                               |
| 7  | 5   | R4, R9, R10, R21, R22                | Resistor         | 1206     | 50 $\Omega$                                                                |
| 8  | 1   | R7                                   | Resistor         | 1206     | 25 $\Omega$                                                                |
| 9  | 1   | R23                                  | Resistor         | 1206     | 2 k $\Omega$                                                               |
| 10 | 1   | T1                                   | Transformer      |          | Mini-Circuits T1-1T-KK81                                                   |
| 11 | 1   | U1                                   | AD9283           | SSOP-20  |                                                                            |
| 12 | 1   | U3                                   | AD9760           | SOIC-28  |                                                                            |
| 13 | 1   | U4                                   | 74ACQ574         | SOIC-20  |                                                                            |
| 14 | 1   | U5                                   | SN74LVC86        | SO14     |                                                                            |

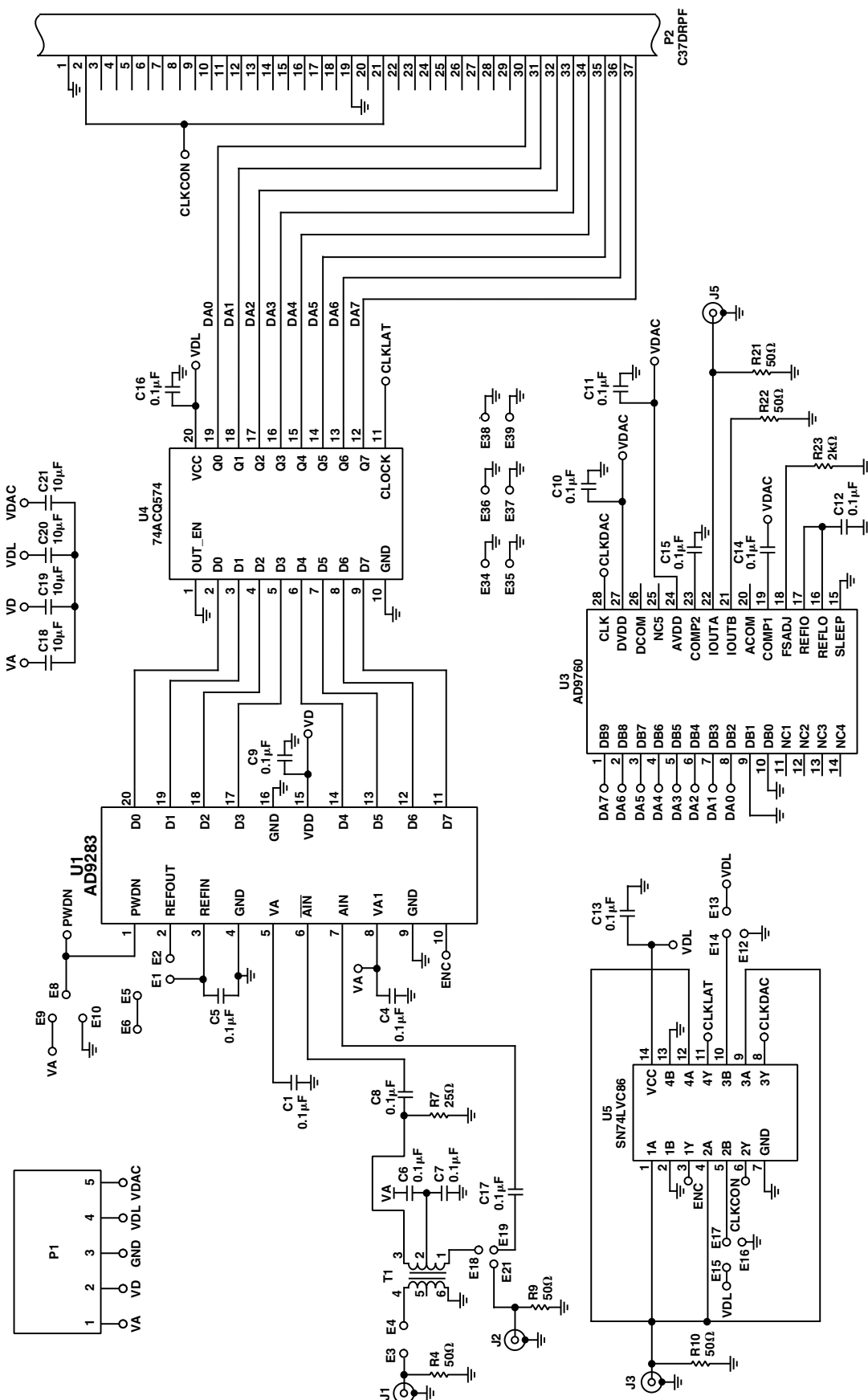


Figure 13. Printed Circuit Board Schematic

Dimensions shown in inches and (mm).

Figure 1: Mechanical drawing of the BSC package. The drawing shows three views: a top view, a side view, and a cross-sectional view. The top view shows a rectangular package with pins on all four sides. Dimensions include overall width (0.295 (7.50) / 0.271 (6.90)), overall height (0.311 (7.9) / 0.301 (7.64)), pin pitch (0.078 (1.98) / 0.068 (1.73)), and pin width (0.07 (1.78) / 0.066 (1.67)). The side view shows the package height (0.212 (5.38) / 0.205 (5.21)) and pin height (0.078 (1.98) / 0.068 (1.73)). The cross-sectional view shows the package thickness (0.008 (0.203) / 0.002 (0.050)), pin thickness (0.0256), seating plane (0.009 (0.229) / 0.005 (0.127)), and package width (0.037 (0.94) / 0.022 (0.559)). The cross-sectional view also shows a 8° angle and a 0° angle.

### Location

## Page

Edits to ABSOLUTE MAXIMUM RATINGS ..... 3