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REVISION HISTORY

8/2016—Rev. D to Rev. E

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8/2014—Rev. C to Rev. D

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7/2011—Rev. B to Rev. C

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6/2011—Rev. A to Rev. B

Changes to Table 1, Dynamic Performance, Self-Test Valid Time, t_{stv} Parameter ... 4
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7/2010—Rev. 0 to Rev. A

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4/2010—Revision 0: Initial Version

SPECIFICATIONS

VTOP = 7.5 V to 30 V, T_A = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TRIP POINT ERRORS					
Undervoltage Trip Point Error		−25		+25	mV
Overvoltage Trip Point Error		−15		+15	mV
Overtemperature Trip Point Error		−25		+25	mV
Hysteresis for Overvoltage, Undervoltage, and Overtemperature Trip Points		40	50	60	mV
CELL INPUTS (VIN0 TO VIN6)					
Input Bias Current		0		20	nA
Input Offset Current		0		20	nA
Input Voltage Range	One cell	0		5	V
Input Common-Mode Range		0		Top of stack	V
TEMPERATURE INPUTS (VT1, VT2)					
Input Bias Current		−10		+10	nA
Input Voltage Range		0		5	V
OVERVOLTAGE THRESHOLD INPUT (OV)					
Input Bias Current		0		20	nA
Input Voltage Range		3.6		4.6	V
UNDERVOLTAGE THRESHOLD INPUT (UV)					
Input Bias Current		0		20	nA
Input Voltage Range		1.4		3.3	V
OVERTEMPERATURE THRESHOLD INPUT (OT)					
Input Bias Current		0		20	nA
Input Voltage Range		1.5		4	V
INPUT/OUTPUT CHARACTERISTICS					
Logic 1 Current	AIINxx, AIOUTxx	100	150	200	µA
Logic 0 Current	AIINxx, AIOUTxx	10	30	50	µA
Logic 1 Voltage Input, V_{IH}	With respect to VBOTx				
All Pins Except TOP and BOT		2.0		LDO	V
TOP and BOT Pins		VTOP			V
Logic 0 Voltage Input, V_{IL}	With respect to VBOTx				
All Pins Except TOP and BOT				0.8	V
TOP and BOT Pins				VBOT	V
Logic 1 Voltage Output, V_{OH}	With respect to VBOTx	4.2			V
Logic 0 Voltage Output, V_{OL}	With respect to VBOTx			0.2	V
Input Bias Current	SEL0, SEL1, DGT0, DGT1, DGT2, NPTC, ALRMSEL			1	µA
REFERENCE AND LDO					
Reference Voltage		4.95	5.0	5.05	V
Reference Source Current				250	µA
LDO Voltage	0 mA ≤ LDO source current ≤ 10.0 mA	4.85	5.1	5.35	V
LDO Source Current				5.0	mA
DYNAMIC PERFORMANCE					
Fault Detection (Deglitch) Time Range	Seven settings: 0.0 sec, 80 ms, 625 ms, 1.25 sec, 2.5 sec, 5.0 sec, and 10.0 sec	0.0		10.0	sec
Fault Detection (Deglitch) Accuracy		−20		+20	%
Propagation Delay Time	No capacitor on daisy chain		4.0		µs
Start-Up Time	From application enabled to LDO = 90% of value			3.0	ms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Self-Test Completion Time, t_{ST}	Deglitch time = 0.0 sec	15		25	ms
	Deglitch time > 0.0 sec	650		1000	ms
Self-Test Valid Time, t_{STV}		0.0		2.0	µs
Delay Time for Self-Test Start, t_{RE}		6.0			µs
Delay Time for Data Valid, t_{FE}		6.0			µs
Rise Time for Self-Test Pulse, t_R	TESTI			1.0	ms
POWER SUPPLY					
Supply Voltage Range	VTOP with respect to VBOTx				
	LDO source current = 10.0 mA	7.5		30	V
	LDO source current = 0.0 mA	6.0		30	V
Quiescent Current					
Power Supply Enabled	Excluding LDO source current			2.0	mA
Power Supply Disabled				1.0	µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VTOP to VBOTx	−0.3 V to +33 V
VIN0 to VBOTx	−0.3 V to LDO + 0.3 V
VIN1 Through VIN5 Voltage to VBOTx	−0.3 V to VTOP + 0.3 V
VIN6 to VBOTx	−0.3 V to VTOP + 1.0 V
VIN6 to VTOP	−0.3 V to + 1.0 V
VTx to VBOTx	−0.3 V to LDO + 0.3 V
TESTI, ENBI to GNDx	−0.3 V to LDO + 0.3 V
DGTx, SELx, NPTC to GNDx	−0.3 V to LDO + 0.3 V
AVOUTxx to GNDx	−0.3 V to LDO + 0.3 V
TOP, BOT to VBOTx	−0.3 V to VTOP + 0.3 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-Lead LQFP (ST-48)	54	15	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

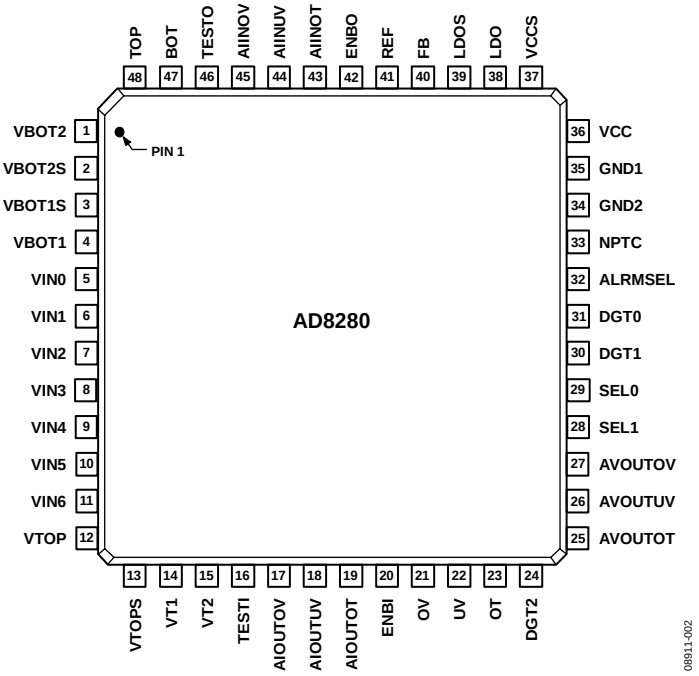


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VBOT2	Lowest Potential of Six-Cell Stack.
2	VBOT2S	Lowest Potential of Six-Cell Stack. Tie to VBOT2.
3	VBOT1S	Lowest Potential of Six-Cell Stack. Tie to VBOT1.
4	VBOT1	Lowest Potential of Six-Cell Stack.
5	VIN0	Input Voltage for Bottom of Cell 1.
6	VIN1	Input Voltage for Bottom of Cell 2/Top of Cell 1.
7	VIN2	Input Voltage for Bottom of Cell 3/Top of Cell 2.
8	VIN3	Input Voltage for Bottom of Cell 4/Top of Cell 3.
9	VIN4	Input Voltage for Bottom of Cell 5/Top of Cell 4.
10	VIN5	Input Voltage for Bottom of Cell 6/Top of Cell 5.
11	VIN6	Input Voltage for Top of Cell 6.
12	VTOP	Highest Potential of Six-Cell Stack.
13	VTOPS	Highest Potential of Six-Cell Stack. Tie to VTOP.
14	VT1	Temperature Input 1.
15	VT2	Temperature Input 2.
16	TESTI	Test Input.
17	AIOUTOV	Alarm Current Output, Overvoltage. Used in daisy-chain configuration.
18	AIOUTUV	Alarm Current Output, Undervoltage. Used in daisy-chain configuration.
19	AIOUTOT	Alarm Current Output, Overtemperature. Used in daisy-chain configuration.
20	ENBI	Enable Input. When ENBI is logic high, the device is enabled; when ENBI is logic low, the device is disabled.
21	OV	Overvoltage Trip Point.
22	UV	Undervoltage Trip Point.
23	OT	Overtemperature Trip Point.
24	DGT2	Digital Select Pin 2. Used with DGT0 and DGT1 to select deglitch time (see Table 7).
25	AVOUTOT	Alarm Voltage Output, Overtemperature.
26	AVOUTUV	Alarm Voltage Output, Undervoltage.
27	AVOUTOV	Alarm Voltage Output, Overvoltage.

Pin No.	Mnemonic	Description
28	SEL1	Digital Select Pin 1. Used with SEL0 to select channels to be used (see Table 5).
29	SEL0	Digital Select Pin 0. Used with SEL1 to select channels to be used (see Table 5).
30	DGT1	Digital Select Pin 1. Used with DGT0 and DGT2 to select deglitch time (see Table 7).
31	DGT0	Digital Select Pin 0. Used with DGT1 and DGT2 to select deglitch time (see Table 7).
32	ALRMSEL	Selects three separate alarms or one shared alarm. When ALRMSEL is logic high, three separate alarms are selected; when ALRMSEL is logic low, one shared alarm is selected.
33	NPTC	Selects NTC or PTC thermistor for VTx inputs. When NPTC is tied to logic high (LDO pin), a PTC thermistor is selected; when NPTC is tied to logic low (VBOTx pin), an NTC thermistor is selected.
34	GND2	Ground. Tie to same potential as VBOT1 and VBOT2.
35	GND1	Ground. Tie to same potential as VBOT1 and VBOT2.
36	VCC	Supply Voltage. Tie to LDO.
37	VCCS	Supply Voltage Sense. Tie to LDO.
38	LDO	LDO Output. Tie to VCC, VCCS, and LDOS.
39	LDOS	LDO Output Sense. Tie to LDO.
40	FB	Feedback Pin. Tie to REF.
41	REF	Reference Output. Tie to FB.
42	ENBO	Enable Output.
43	AIINOT	Alarm Current Input, Overtemperature. Used in daisy-chain configuration.
44	AIINUV	Alarm Current Input, Undervoltage. Used in daisy-chain configuration.
45	AIINOV	Alarm Current Input, Overvoltage. Used in daisy-chain configuration.
46	TESTO	Test Output.
47	BOT	Identifies the device at lowest potential in daisy chain (see Table 6).
48	TOP	Identifies the device at highest potential in daisy chain (see Table 6).

TYPICAL PERFORMANCE CHARACTERISTICS

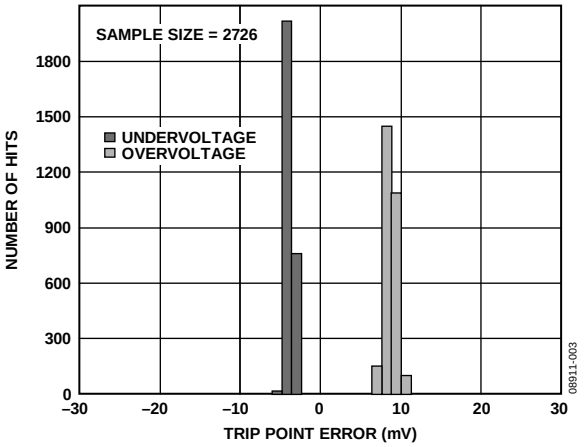


Figure 3. Overvoltage and Undervoltage Trip Point Error, Voltage Between VIN0 and VIN1

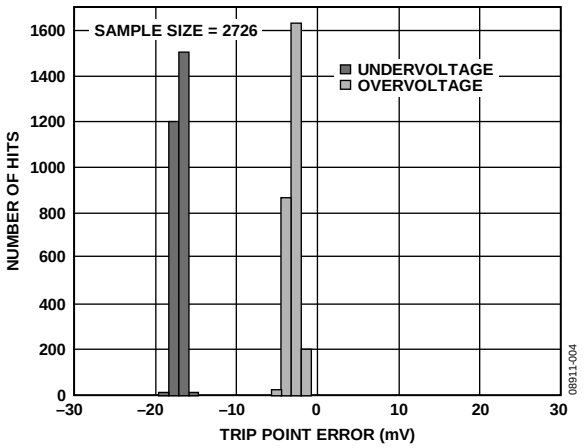


Figure 4. Overvoltage and Undervoltage Trip Point Error, Voltage Between VIN1 and VIN2

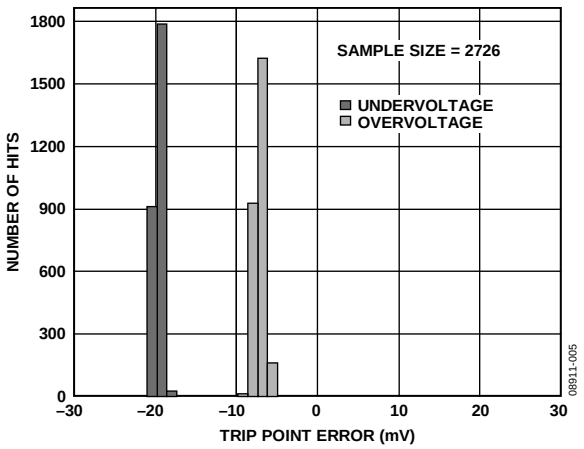


Figure 5. Overvoltage and Undervoltage Trip Point Error, Voltage Between VIN2 and VIN3

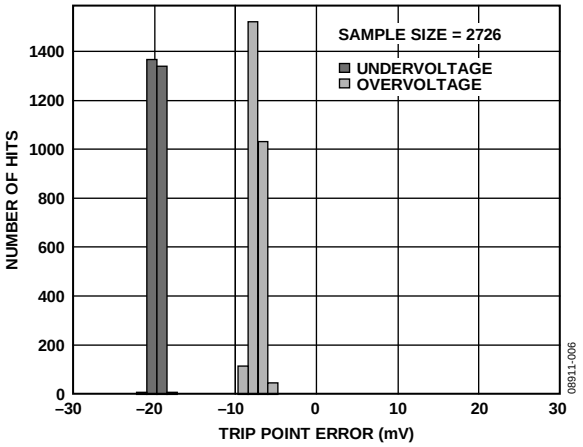


Figure 6. Overvoltage and Undervoltage Trip Point Error, Voltage Between VIN3 and VIN4

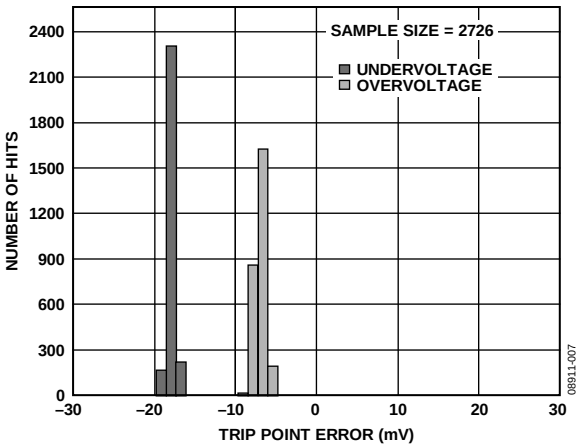


Figure 7. Overvoltage and Undervoltage Trip Point Error, Voltage Between VIN4 and VIN5

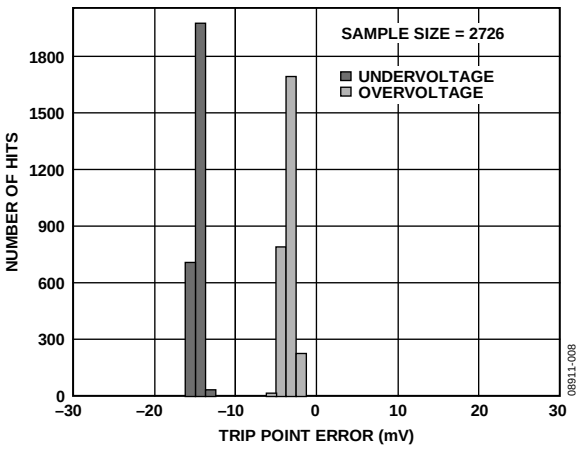


Figure 8. Overvoltage and Undervoltage Trip Point Error, Voltage Between VIN5 and VIN6

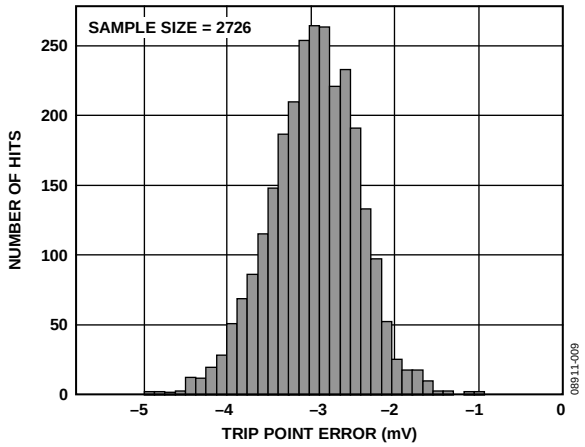


Figure 9. Overtemperature Trip Point Error

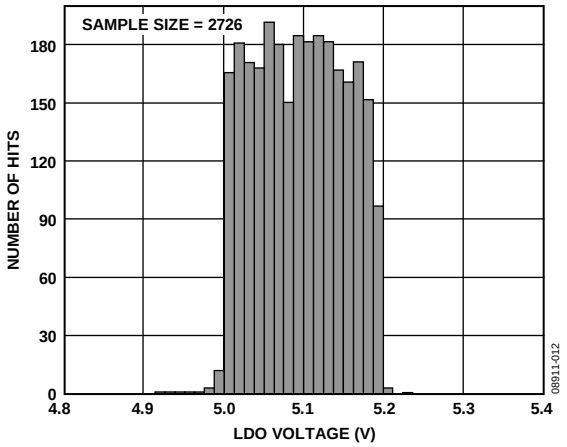


Figure 12. LDO Voltage

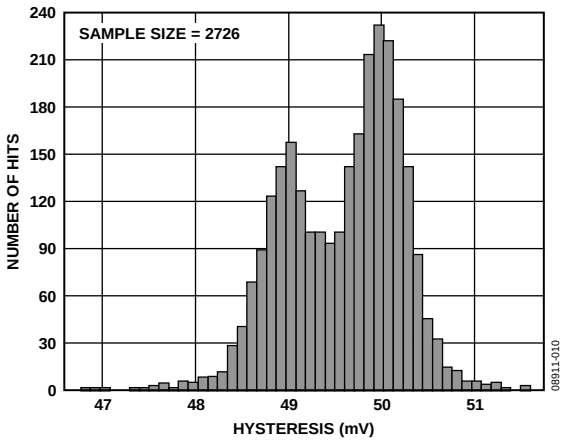


Figure 10. Overvoltage, Undervoltage, and Overtemperature Hysteresis

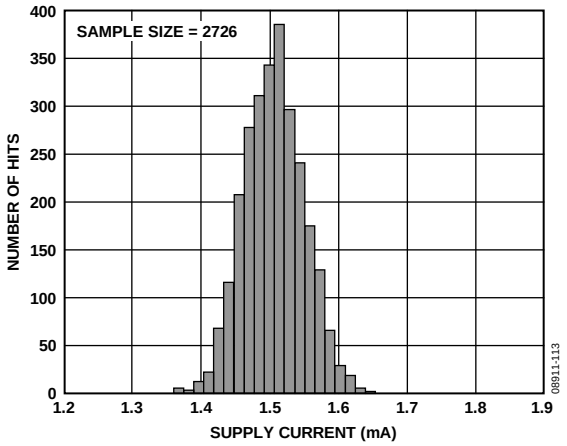


Figure 13. Supply Current

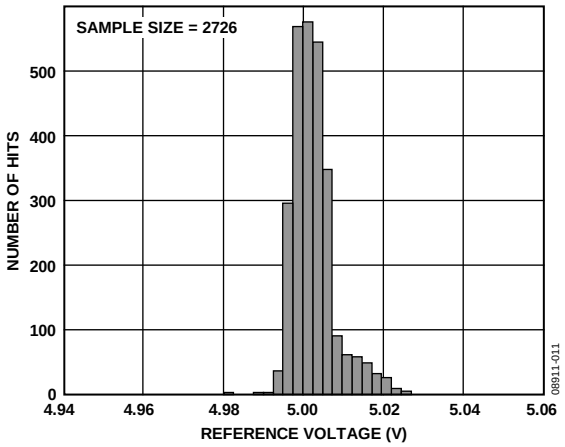


Figure 11. Reference Voltage

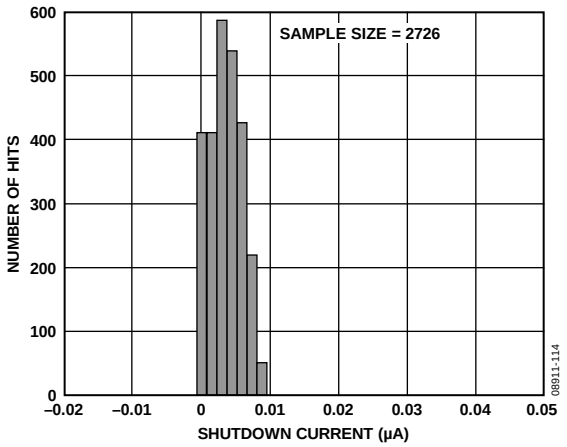


Figure 14. Supply Current, Power-Down Mode

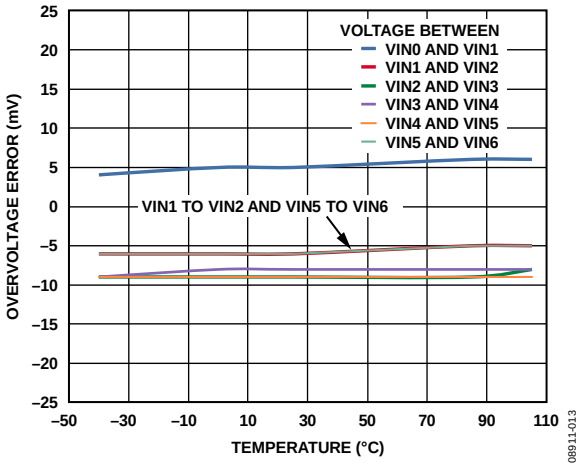


Figure 15. Overvoltage Error vs. Temperature

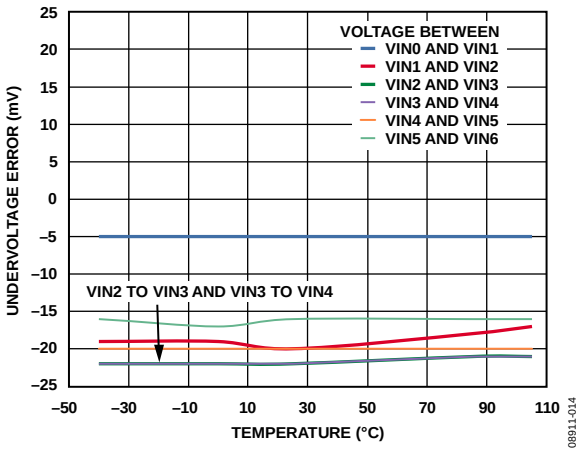


Figure 16. Undervoltage Error vs. Temperature

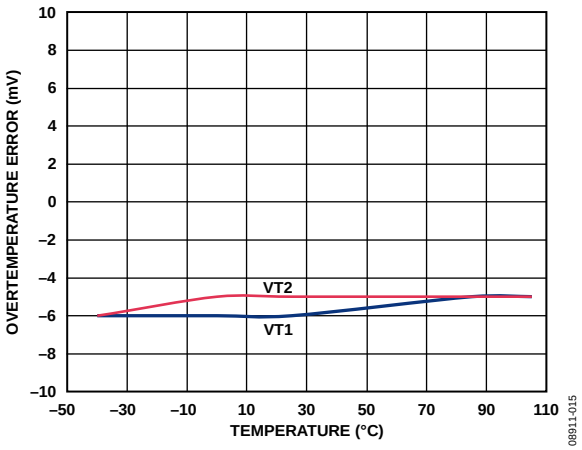


Figure 17. Overtemperature Error vs. Temperature

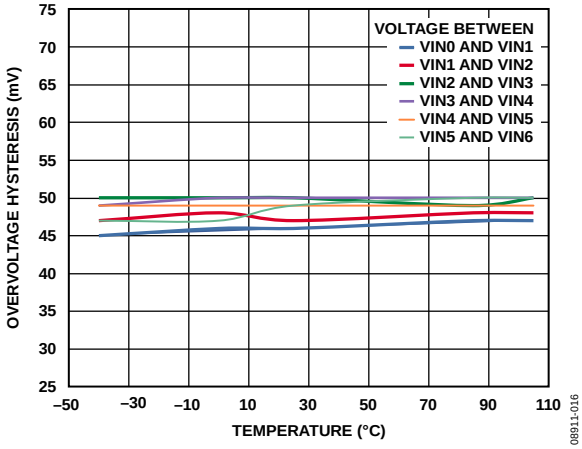


Figure 18. Overvoltage Hysteresis vs. Temperature

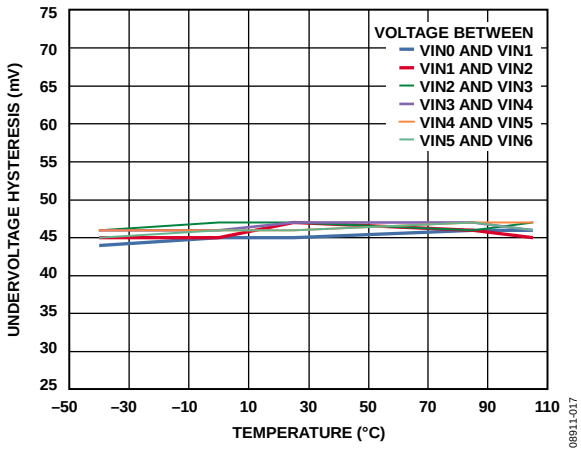


Figure 19. Undervoltage Hysteresis vs. Temperature

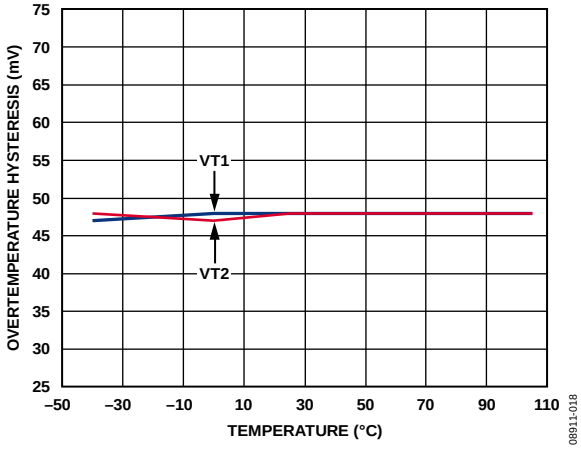


Figure 20. Overtemperature Hysteresis vs. Temperature

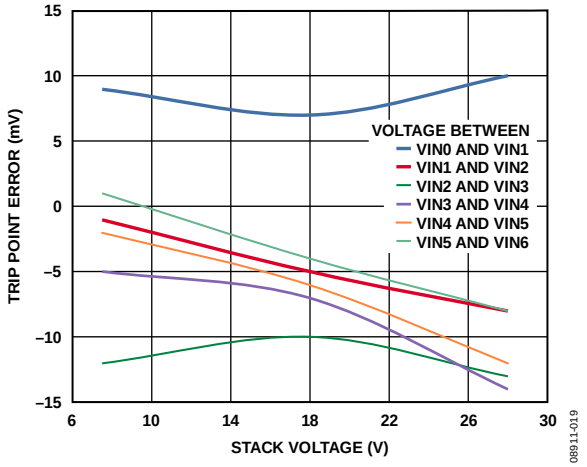


Figure 21. Overvoltage Trip Point Error vs. Stack Voltage (VIN6 – VIN0)

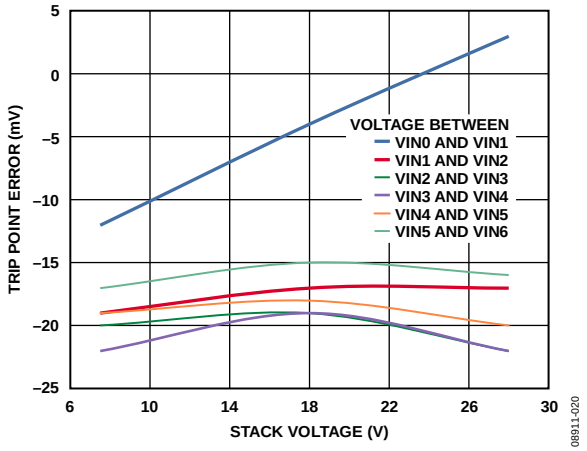


Figure 22. Undervoltage Trip Point Error vs. Stack Voltage (VIN6 – VIN0)

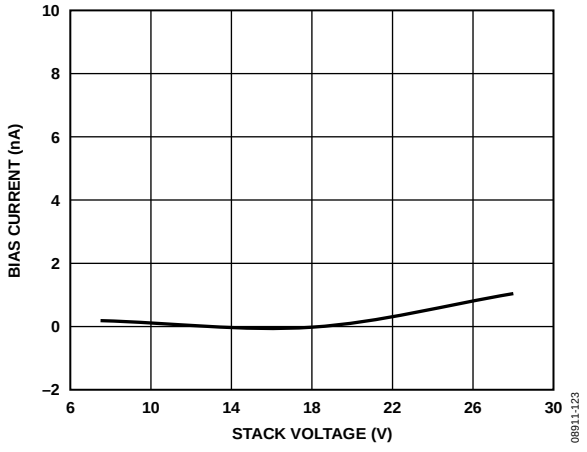


Figure 23. Input Bias Current vs. Stack Voltage (VIN6 – VIN0)

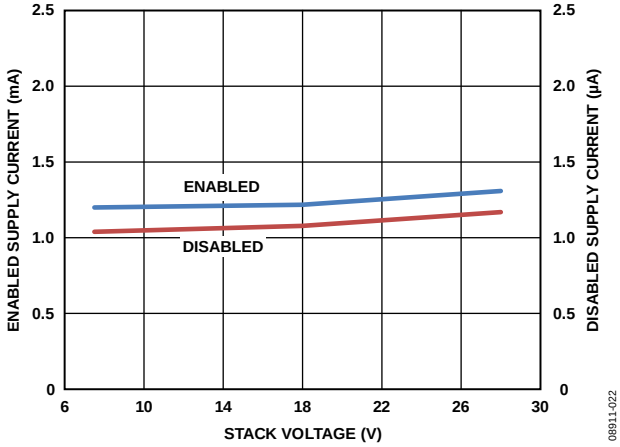


Figure 24. Supply Current vs. Stack Voltage (VIN6 – VIN0)

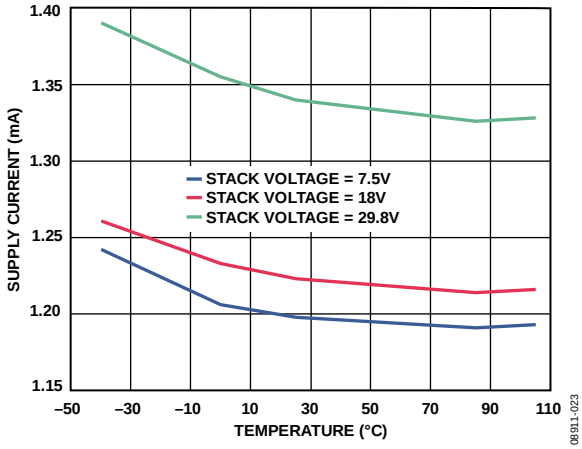


Figure 25. Enabled Supply Current vs. Temperature for Various Stack Voltages (VIN6 – VIN0)

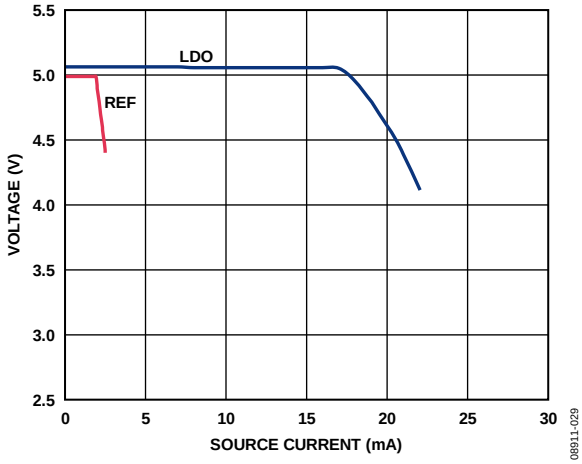


Figure 26. LDO and Reference Voltage vs. LDO Source Current, Stack Voltage = 7.5 V

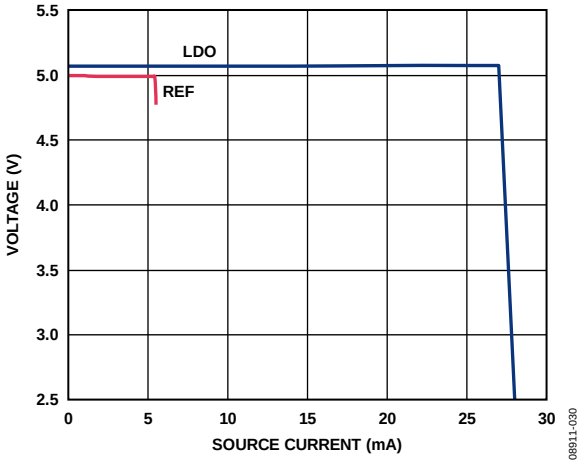


Figure 27. LDO and Reference Voltage vs. LDO Source Current, Stack Voltage = 18.0 V

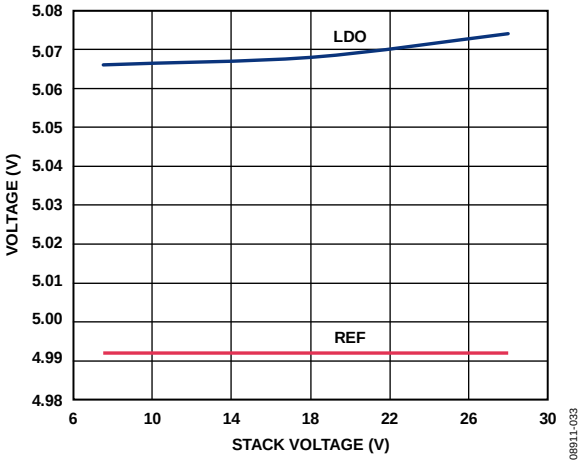


Figure 30. LDO and Reference Voltage vs. Stack Voltage (VIN6 – VIN0)

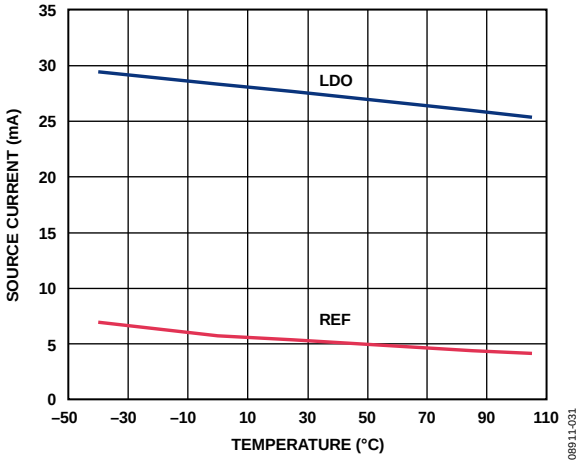


Figure 28. LDO and Reference Source Current vs. Temperature

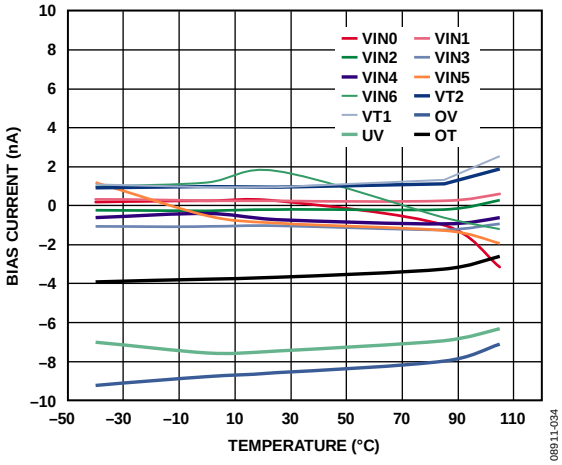


Figure 31. Input Bias Current vs. Temperature

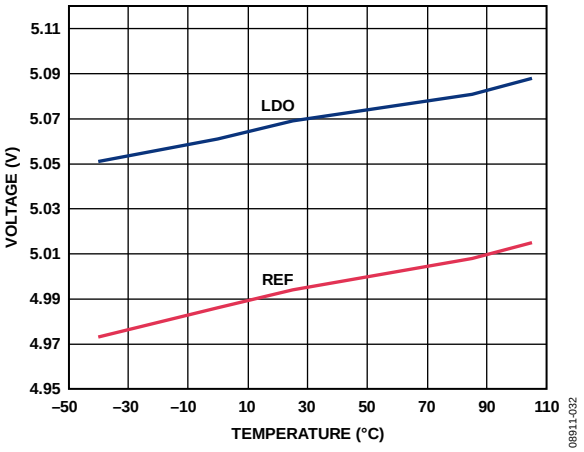


Figure 29. LDO and Reference Voltage vs. Temperature

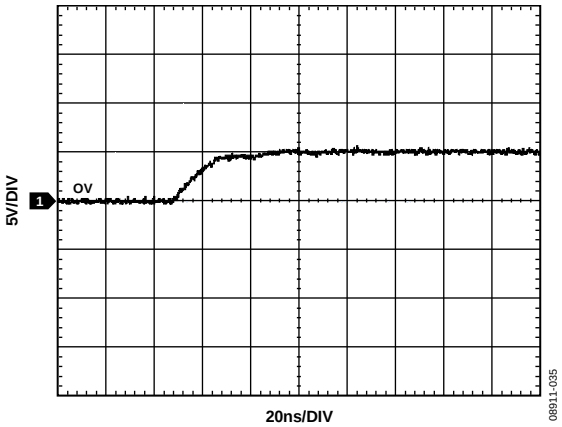


Figure 32. Alarm Rise Time

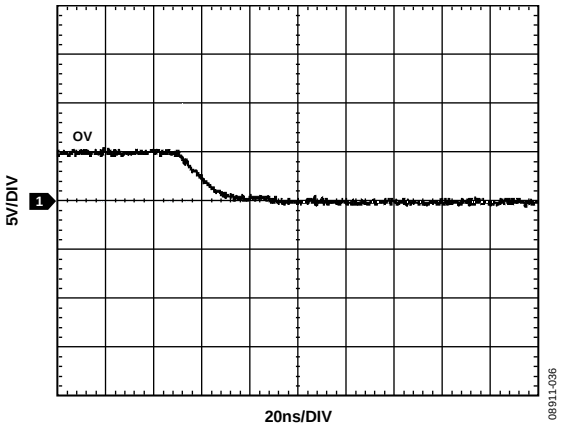


Figure 33. Alarm Fall Time

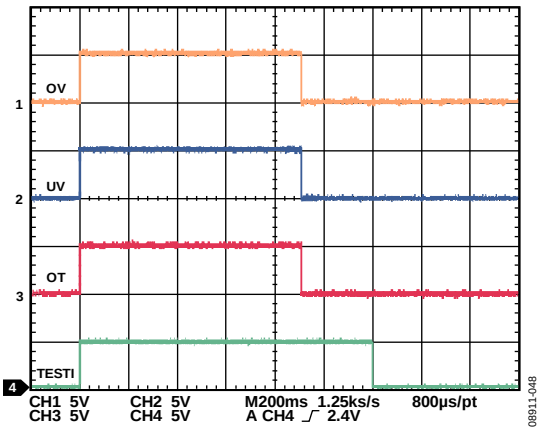


Figure 36. TESTI and AVOUTxx, Deglitch Time = 0.1 sec, Self-Test Passes

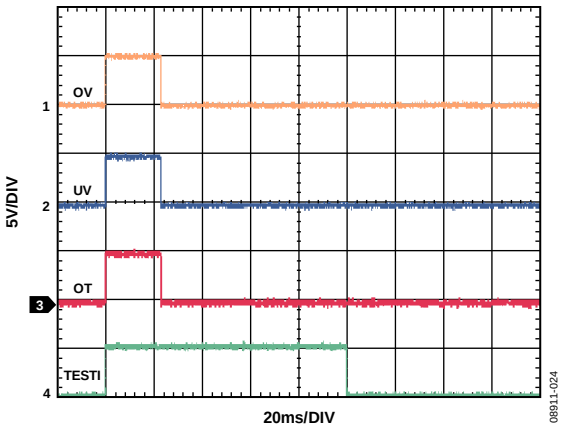


Figure 34. TESTI and AVOUTxx, Deglitch Time = 0.0 sec, Self-Test Passes

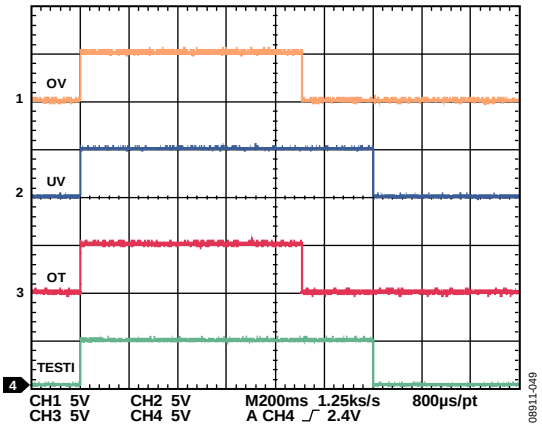


Figure 37. TESTI and AVOUTxx, Deglitch Time = 0.1 sec, Self-Test Fails (UV)

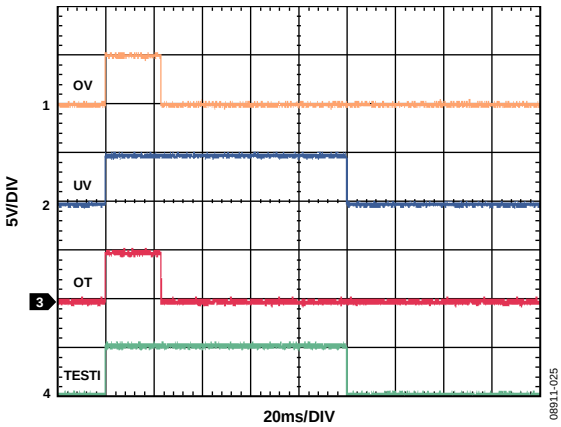


Figure 35. TESTI and AVOUTxx, Deglitch Time = 0.0 sec, Self-Test Fails (UV)

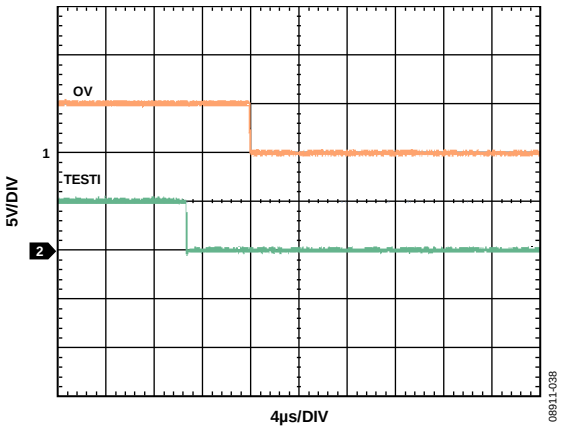


Figure 38. TESTI Edge and AVOUTxx, Self-Test Fails (Enlarged)

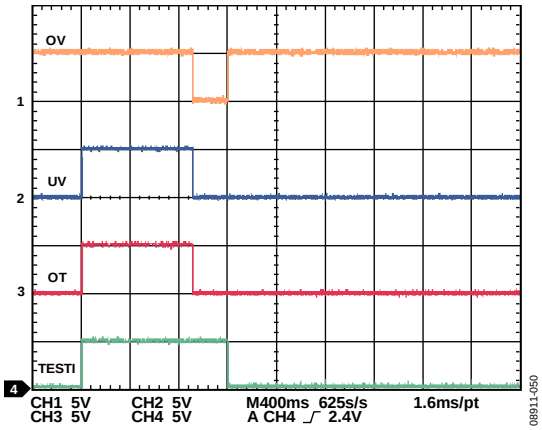


Figure 39. Alarm Condition Entering Self-Test, the Device Passes the Self-Test

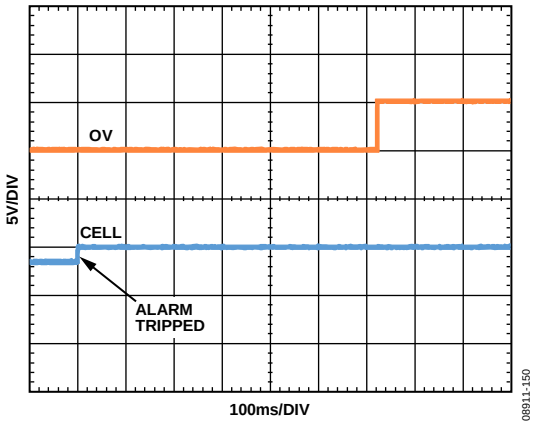


Figure 42. Cell Voltage Change to Trip Alarm, Deglitch Time = 625 ms

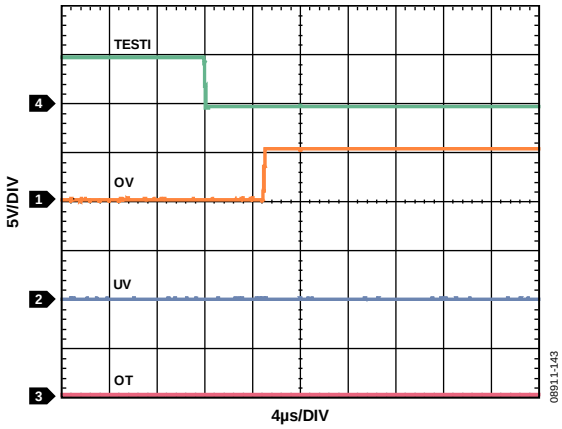


Figure 40. Alarm Condition Entering Self-Test, the Device Passes the Self-Test (Enlarged)

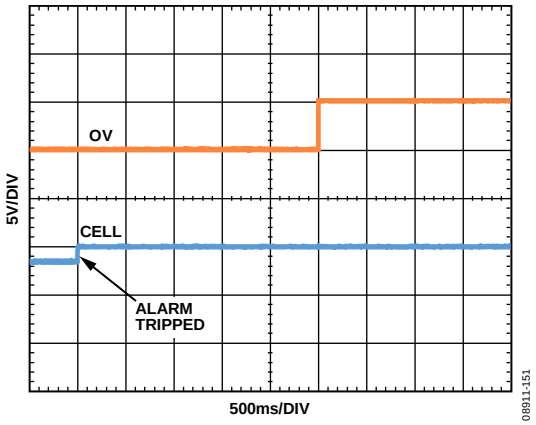


Figure 43. Cell Voltage Change to Trip Alarm, Deglitch Time = 2.5 sec

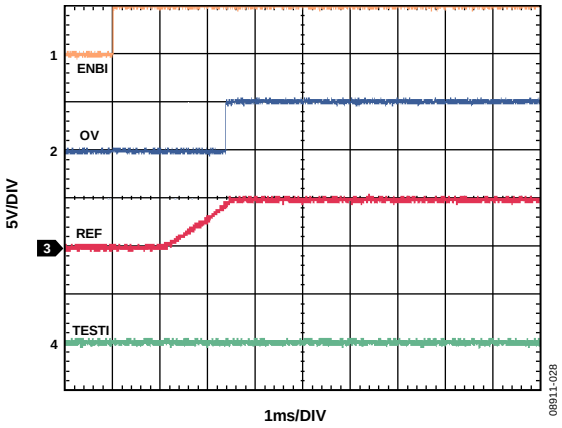


Figure 41. Start-Up Time

THEORY OF OPERATION

Figure 44 shows a block diagram of the AD8280. The AD8280 is a threshold monitor that can monitor up to six cell voltages and two temperature voltages. The device can also be used in a daisy-chain configuration to monitor as many cells as required. The benefit of the daisy-chain configuration is that isolation is required to bring the alarm signal away from the high voltage environment on only the bottom device of the chain, reducing system cost and minimizing the board space required.

The cell and temperature voltage inputs are connected to the device using the VIN0 through VIN6 inputs and the VT1 and VT2 inputs, respectively. Because the six-cell stack voltage can be up to 30 V, the input voltages are level-shifted and referenced to the lowest potential (device ground or VBOTx) of the AD8280. These voltages are then input into window comparators and compared to trip points set by external resistor dividers.

If the cell or temperature voltage inputs exceed or fall below the selected trip points, an alarm, in the form of a digital voltage level, changes state at the voltage output (AVOUTxx) of the device. The alarm state also exists in the form of a current output (AIOUTxx) that communicates to the other devices when multiple devices are used in a daisy-chain configuration.

The device contains programmable deglitching circuitry to ensure that transient voltages appearing at the cell inputs are ignored.

The device also contains an LDO and reference. The LDO can drive external components such as thermistors or isolators, whereas the reference can be used with the voltage dividers to establish the trip points.

The AD8280 has the following unique features and capabilities:

- Three, four, five, or six cells can be monitored.
- Negative or positive temperature coefficient thermistors can be used.
- Multiple devices can be configured in a daisy chain to monitor hundreds of cells. Information about the status of the alarms on the entire daisy chain, as well as input signals that enable the device and initiate self-test, are all communicated via the bottom, or master, device in the chain.
- Alarm outputs for overvoltage, undervoltage, and overtemperature status can be shared, with each output indicating the same status for any of the occurring alarm conditions, or the alarm outputs can function as separate entities with each indicating the status of the specific condition.
- An extensive self-test feature ensures that the internal components are functioning correctly. The self-test is initiated upon request to the TESTI pin.

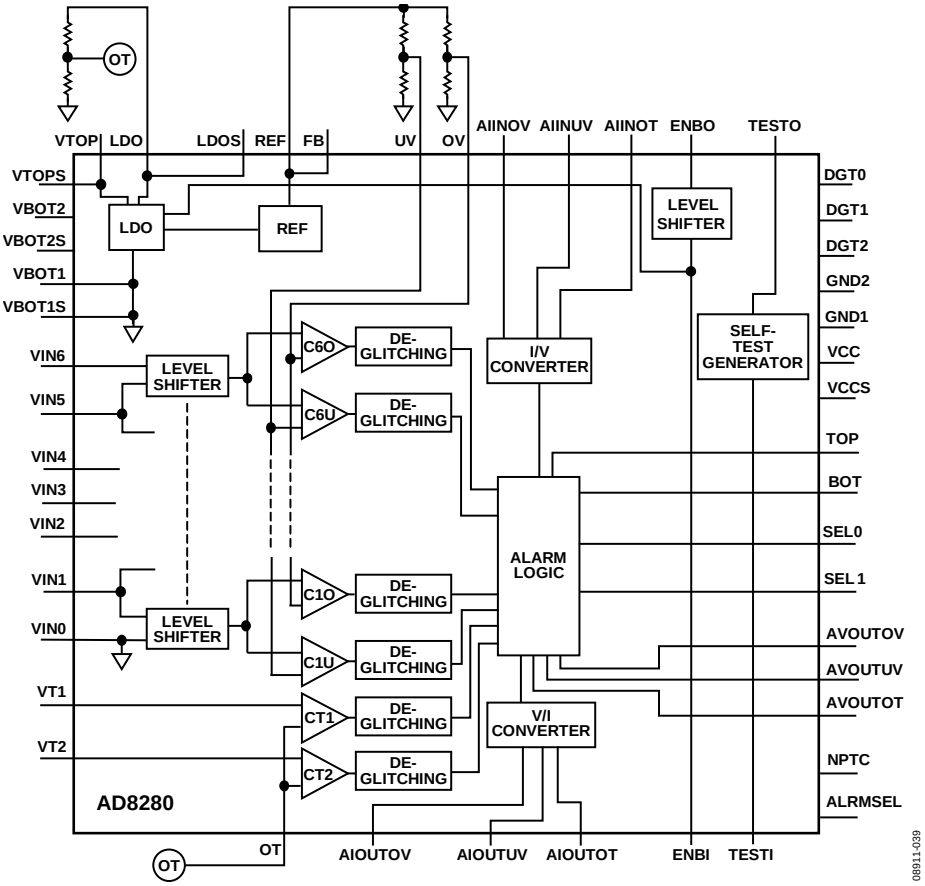


Figure 44. Functional Block Diagram

APPLICATIONS INFORMATION

TYPICAL CONNECTIONS

Figure 45 is a block diagram of the AD8280 typical connections.

CELL INPUTS

The battery stack of six cells must connect to VIN0 through VIN6, with the highest potential connected to VIN6 and the lowest to VIN0. Make the connections through a low-pass filter consisting of a 10 kΩ resistor and a 10 nF capacitor, as shown in Figure 45. The lowest potential of the six-cell stack must also connect to VBOT1, VBOT1S, VBOT2, and VBOT2S as well, whereas the highest potential must connect through a diode to VTOP and VTOPS. It is recommended that decoupling capacitors of 0.1 µF and 10 µF be used at the VTOP pin.

TEMPERATURE INPUTS AND THERMISTOR SELECTION

VT1 and VT2 are voltage inputs and are designed to work with thermistors that are configured as resistor dividers, as shown in Figure 45. The voltage at the top of the thermistor divider must be the +5 V output of the LDO. The LDO pin can source more current than the REF pin and is better suited to drive the thermistor dividers.

If a voltage source other than that of the AD8280 LDO drives the thermistor bridge (V_{TH}), it is important that the VT1 and VT2 voltages be brought to 0 V when the AD8280 is disabled or powered down because the VT1 and VT2 inputs must be at 0 V when the LDO is also at 0 V.

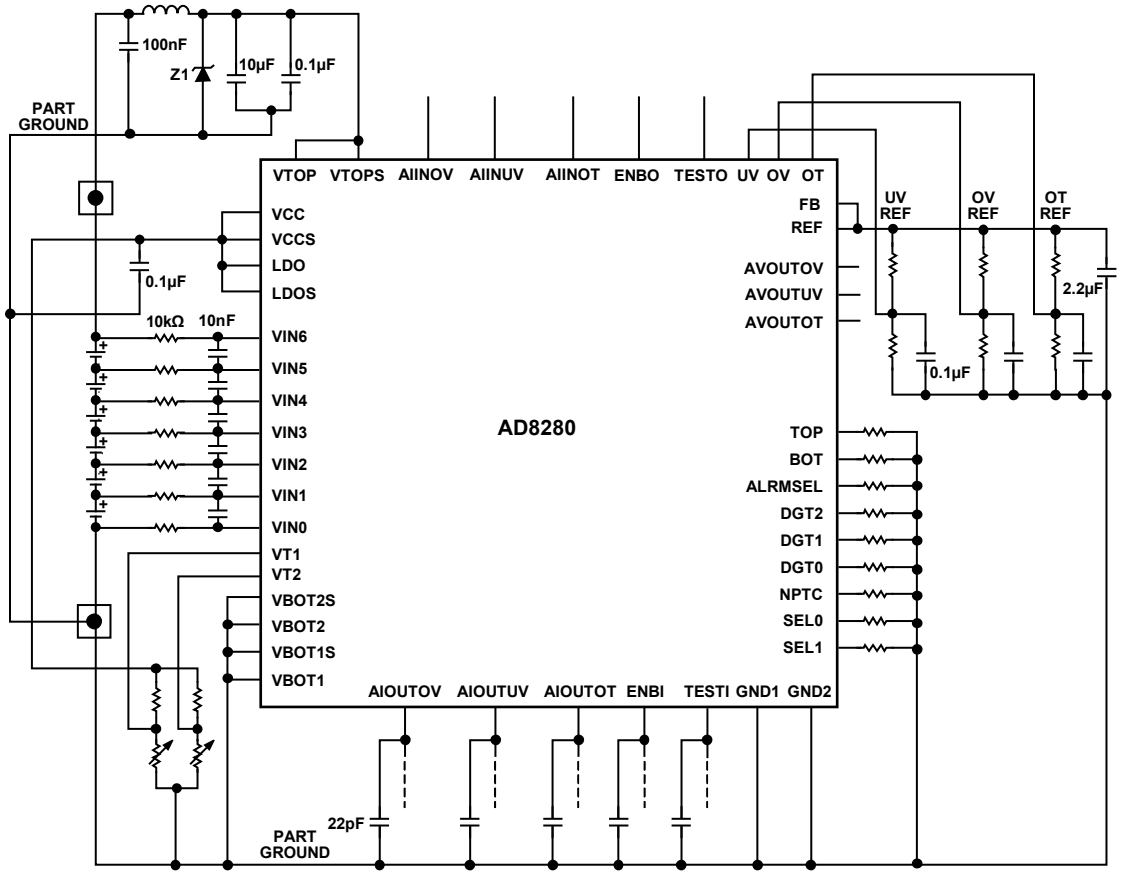


Figure 45. Typical Connections of the AD8280

In addition, if the resistor (R_{TOP}) used in the top of the thermistor bridge circuit is less than 10 kΩ, another resistor (R_{IN}) must be added in series to the input to the VTx pin (see Figure 46). The two resistors together must be greater than 10 kΩ (R_{TOP} + R_{IN} > 10 kΩ). This configuration is required only if V_{TH} is not the AD8280 LDO.

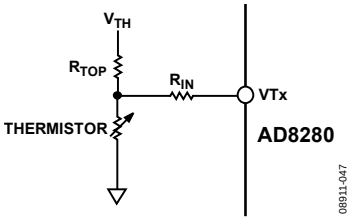


Figure 46. Input Configuration for VTx When Not Using the LDO for V_{TH}

The device can work with both negative temperature coefficient (NTC) and positive temperature coefficient (PTC) thermistors. For NTC, the NPTC pin must be tied to logic low (VBOTx pin); for PTC, the NPTC pin must be tied to logic high (LDO pin). If the device is set to NTC mode, the OT alarm is tripped when the voltages at VT1 and VT2 drop below the trip point. If the device is set to PTC mode, the OT alarm is tripped when the voltages at VT1 and VT2 rise above the trip point.

NUMBER OF CELLS SELECTION

The device can be configured to work with three, four, five, or six cells. Table 5 describes how to program the SEL0 and SEL1 pins to determine the number of cells being monitored. A logic low represents VBOTx, and a logic high represents the LDO output voltage. Figure 47 through Figure 49 show how to connect the cells to the device in a five-cell, four-cell, or three-cell application.

Table 5. SELx Pin Programming

Number of Cells Used	SEL0	SEL1
6 cells	0	0
5 cells (VIN5 shorted)	0	1
4 cells (VIN4 and VIN5 shorted)	1	0
3 cells (VIN3, VIN4, and VIN5 shorted)	1	1

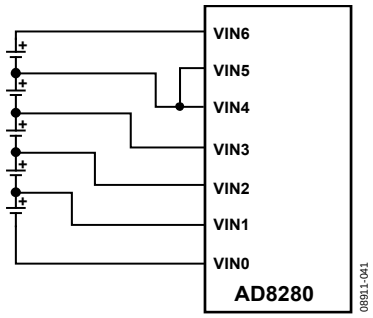


Figure 47. Five-Cell Connections for the AD8280

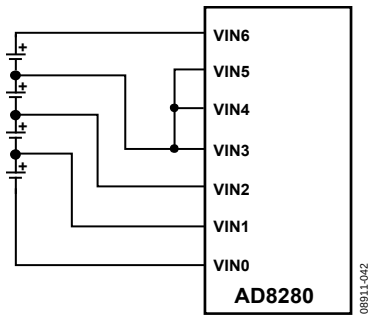


Figure 48. Four-Cell Connections for the AD8280

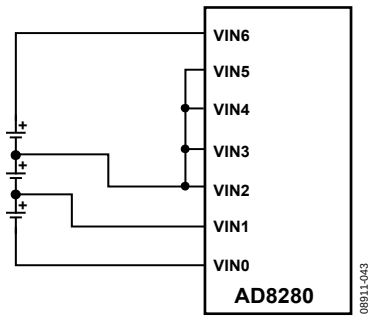


Figure 49. Three-Cell Connections for the AD8280

THRESHOLD INPUTS

The thresholds (or trip points) are set externally with a voltage divider providing maximum flexibility. The desired trip point voltage is connected to the following pins: OV (overvoltage trip point), UV (undervoltage trip point), and OT (overtemperature trip point). The +5 V output of either the reference (REF) or the LDO can be used as the top voltage of the divider. However, because the reference output is more accurate than the LDO output, the reference output is better suited to power the trip point setting dividers. If the thermistor dividers used for temperature sensing are driven from the LDO output, it is recommended the LDO drives the OT trip point divider as well for better temperature drift performance.

Decoupling capacitors (0.1 µF) must be used with the bottom leg of each divider in addition to a 2.2 µF capacitor at the REF output, as shown in Figure 45.

The REF pin must be loaded with no more than 25 kΩ of resistance. Therefore, when using REF to drive three voltage dividers (OV, UV, and OT), it is recommended that the resistance of each divider total at least 75 kΩ. If driving only two dividers (OV and UV) with the reference, each divider must total no less than 50 kΩ.

TOP AND BOTTOM DEVICE DESIGNATION

When configured in a daisy chain, the AD8280 operates differently, depending on where it is in the chain: top device (highest potential), middle device, or bottom device (lowest potential). The TOP and BOT pins designate the location of each device in the daisy chain. Table 6 is the logic table for identifying the location of the device in the daisy chain or, when not used in a daisy chain, identifying it as a single (standalone) device.

The logic high and logic low for the TOP and BOT pins are different from the other logic pins of the AD8280. The TOP and BOT pins are referenced to VTOP (logic high) and VBOTx (logic low), respectively.

Table 6. Designation of the AD8280 in Daisy-Chain and Standalone Configurations

Desired Condition	TOP[1]	BOT[1]
Middle device (middle potential device)	0	0
Bottom device (lowest potential device)	0	1
Top device (highest potential device)	1	0
Single device (highest and lowest potential device)	1	1

[1] For the TOP and BOT pins only, Logic 1 is VTOP and Logic 0 is VBOTx.

Bottom Device in Daisy-Chain Configuration

The bottom device in a daisy-chain configuration is the master device and accepts voltage inputs into the ENBI and TESTI pins. The AIINOV, AIINUV, and AIINOT pins of the bottom device are connected to the AIOUTOV, AIOUTUV, and AIOUTOT pins, respectively, of the next higher potential device in the daisy chain. The AIOUTOV, AIOUTUV, and AIOUTOT pins of the bottom device can be left floating, or they can be tied to device ground (VBOTx).

Middle Device in Daisy-Chain Configuration

When the AD8280 is designated as a middle device, the AIINOV, AIINUV, AIINOT, ENBO, and TESTO pins are connected to the AIOUTOV, AIOUTUV, AIOUTOT, ENBI, and TESTI pins, respectively, of the AD8280 above it.

Top Device in Daisy-Chain Configuration

When the AD8280 is designated as a top device, the AIINOV, AIINUV, AIINOT, ENBO, and TESTO pins can be left floating or tied to VTOP.

Standalone Device

When the AD8280 is designated as a single device (used as a standalone device), the AIOUTOV, AIOUTUV, and AIOUTOT pins can be left floating or tied to device ground (VBOTx). The AIINOV, AIINUV, AIINOT, ENBO, and TESTO pins can be left floating or tied to VTOP. The AD8280 accepts voltage inputs into the ENBI and TESTI pins.

Alarm Signals in Daisy-Chain Configuration

Regardless of the device designation, the alarm signals are available as voltage outputs on any device in the chain on the AVOUTOV, AVOUTUV, and AVOUTOT pins.

These signals indicate the status of the device where the voltage alarms are monitored, as well as the status of the devices above it in the daisy chain. Use isolators to bring the signals outside the high voltage battery environment.

TYPICAL DAISY-CHAIN CONNECTIONS

Figure 50 shows the typical connections for configuring the device in a daisy chain.

SHARED OR SEPARATE ALARMS

The AD8280 can be configured for three separate alarms or for one shared alarm. Tying the ALRMSEL pin to a 5 V logic high forces the device into separate alarm mode. In this mode, each alarm trips only for the designated monitoring function. That is, the OV alarm trips only if an overvoltage condition exists at any of the cell inputs, the UV alarm trips only if an undervoltage condition exists at any of the cell inputs, and the OT alarm trips only if an overtemperature condition exists at either of the temperature inputs.

In shared alarm mode, any of the three conditions—overvoltage, undervoltage, or overtemperature—trips the alarm on all three signal chains. In shared mode, it is necessary to monitor only one alarm because all three contain the same signal.

DEGLITCHING OPTIONS

The deglitching circuitry is available so the device is immune to transients occurring at the cell inputs. If a transient voltage of a high or low enough level to trip an alarm occurs at the input to the device, the alarm state does not occur if the transient voltage is present for less than the selected deglitch time.

The DGT0, DGT1, and DGT2 pins establish the deglitch time. Table 7 shows the options available and the corresponding logic levels to use when setting the deglitch time with the DGT0, DGT1, and DGT2 pins.

Table 7. Fault Detection Time Pin Programming

Deglitch Time	DGT0	DGT1	DGT2
0.0 sec	0	0	0
80 ms	0	0	1
625 ms	0	1	0
1.25 sec	0	1	1
2.5 sec	1	0	0
5.0 sec	1	0	1
10.0 sec	1	1	0

Do not tie all three deglitching pins (DGT0, DGT1, and DGT2) to logic high (111); this setting is used only during the testing of the device at the factory.

Setting the deglitch time to 0.0 sec (000) allows the use of an external deglitching circuit, if desired. Additionally, when the deglitch time is set to 0.0 sec, the time required to ensure the device completes the self-test is significantly reduced (see the Self-Test section). The DGTx pins must be tied to a fixed logic level and not toggled or changed during operation of the AD8280.

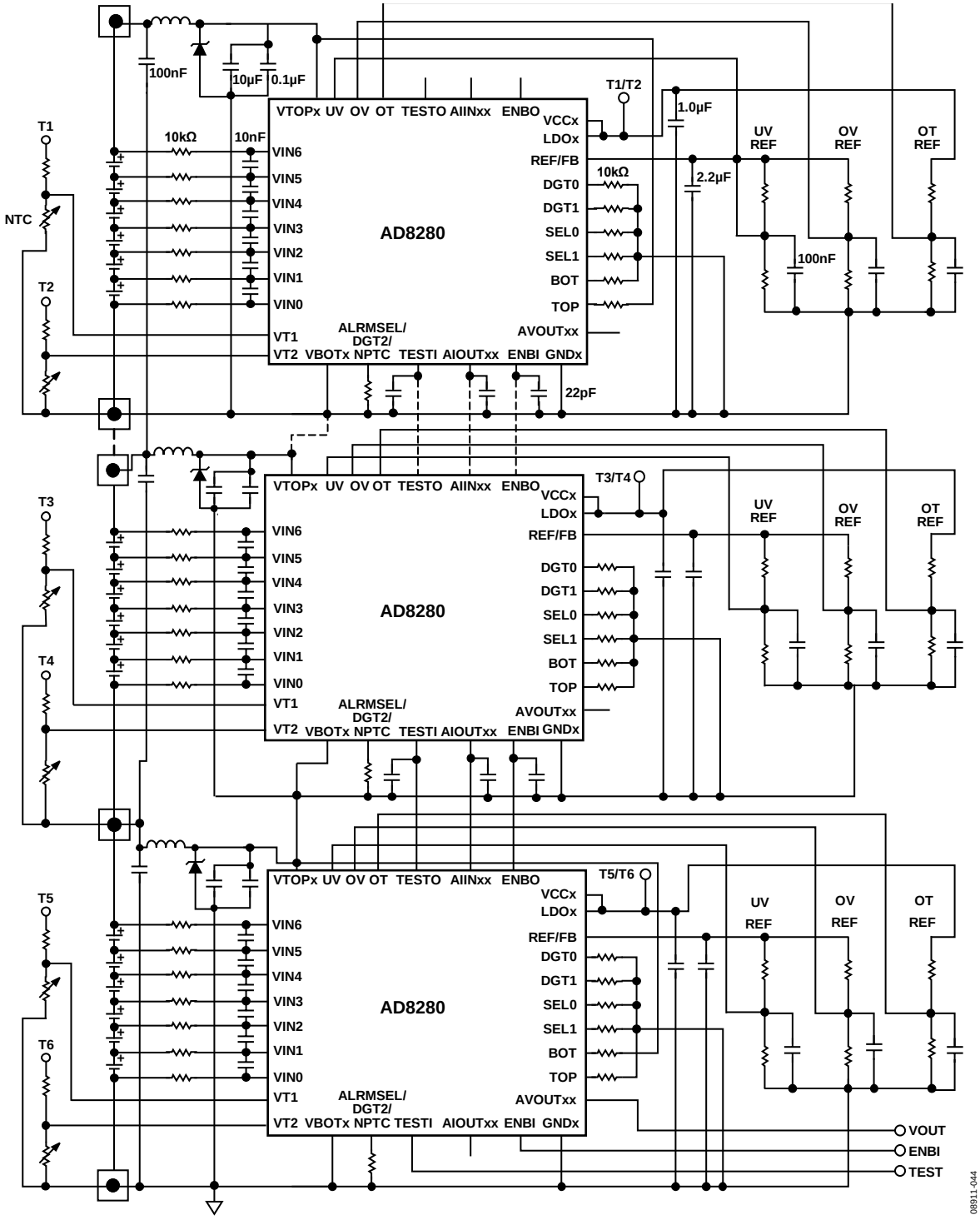


Figure 50. Typical Daisy-Chain Connections

ENABLING AND DISABLING THE AD8280

The AD8280 can be disabled or put into a standby mode by bringing the ENBI pin to logic low, lowering the quiescent current of the AD8280 from a maximum of 2.0 mA to 1.0 µA and dropping the LDO and reference output to 0 V. Bringing the ENBI pin to a logic high takes the device out of standby mode and enables it.

When using the AD8280 a daisy-chain configuration, the enable/disable signal is a voltage logic level sent to the device designated as the bottom device (the bottom device monitors the lowest voltage cells). The bottom device transfers the enable/disable signal up the daisy chain via a current out of the ENBO pin and into the ENBI pin of the next higher device in the daisy chain. All the devices in the daisy chain are enabled by sending a logic high to the ENBI pin of the bottom, or master, device. All the devices in the daisy chain are disabled by sending a logic low to the ENBI pin of the bottom device.

ALARM OUTPUT

The alarm status of the AD8280 appears as a voltage logic level at the AVOUTOV, AVOUTUV, and AVOUTOT pins. When the AD8280 is in a daisy-chain configuration, the alarm status is passed from the AIOUTxx pins of one device to the AIINxx pins of the next lower potential device in the daisy chain. Figure 51 shows the output state when the device is in an unalarmed (logic low) or alarmed (logic high) state.

If the AD8280 is configured for the shared alarm mode, the status of all three voltage output pins (AVOUTxx) is the same. In shared alarm mode, the unused pins can be left floating, tied to ground through a high resistance to limit the current draw, or tied together.

SELF-TEST

The AD8280 has the unique capability of extensively testing the internal components to ensure they are functioning correctly. This feature is very important to the designer concerned with meeting the difficult safety integrity level guidelines of IEC 61508 or ISO 26262.

The device produces internal fault conditions and compares the results to what is expected. The status of the alarm signals is interrupted during the self-test and the pass/fail status of the self-test is communicated via the alarm status signal pins (AVOUTxx and AIOUTxx).

Because the AD8280 uses an internal reference to perform the self-test, the self-test detects open circuits and short circuits at the threshold pins.

See Figure 51 for a timing diagram and notes. See Figure 52 for timing definitions related to the self-test feature.

To initiate a self-test, the TESTI pin is prompted with a rising edge from a 5 V logic level pulse (test pulse). The pulse applied at TESTI must stay high for a minimum time (t_{ST} minimum). Following the rising edge of the pulse to initiate the self-test, the alarm status for any AVOUTxx or AIOUTxx pin goes into a logic high status while the device performs the internal self-test. After sufficient time to perform the test elapses and assuming the device passes the self-test, the alarm status reverts to the unalarmed state, a logic low. If the device fails the self-test, the alarm remains in a logic high state when the falling edge of the test pulse applied at TESTI occurs.

The minimum t_{ST} is dependent on the status of the DGTx pins. If all three DGTx pins are tied to a logic low, the self-test ignores the deglitch function of the device and completes the self-test in a shorter time (25 ms maximum). When at least one DGTx pin is set to logic high, the AD8280 defaults to the minimum deglitch time of 80 ms during the self-test. Because the self-test includes multiple layers and passes, the minimum time to wait until the self-test is complete is 1000 ms. Therefore, if a faster self-test is required, set the internal deglitch time to 0.0 sec and use an external deglitch circuit if deglitch is required.

Self-Test in Daisy-Chain Configuration

The self-test can also be used when multiple AD8280 devices are configured in a daisy chain. The test pulse is applied to the TESTI pin of the bottom device as a voltage and then travels up the chain as a current. The self-test for each device is started as soon as the device sees the rising edge of the test pulse, virtually simultaneously. When the highest device in the chain passes the self-test, it sends that information to the next lower device in the daisy chain. Even if the device completes the self-test, it cannot pass the result on to the next device in the daisy chain until it receives the pass signal from the device above it.

This process continues with each device lower down the chain. Therefore, when a pass signal appears at the bottom device in the daisy chain, it indicates that every device in the daisy chain passed the self-test. If any device in the chain fails the self-test, the device below the failing device never receives a pass signal, and, subsequently, the bottom device never receives a pass signal either. Therefore, regardless of whether the bottom device passes the self-test, the AVOUTxx signals at the bottom device never change state from the logic high that occurred when the self-test initiates, and the user knows there is a failed device in the chain.

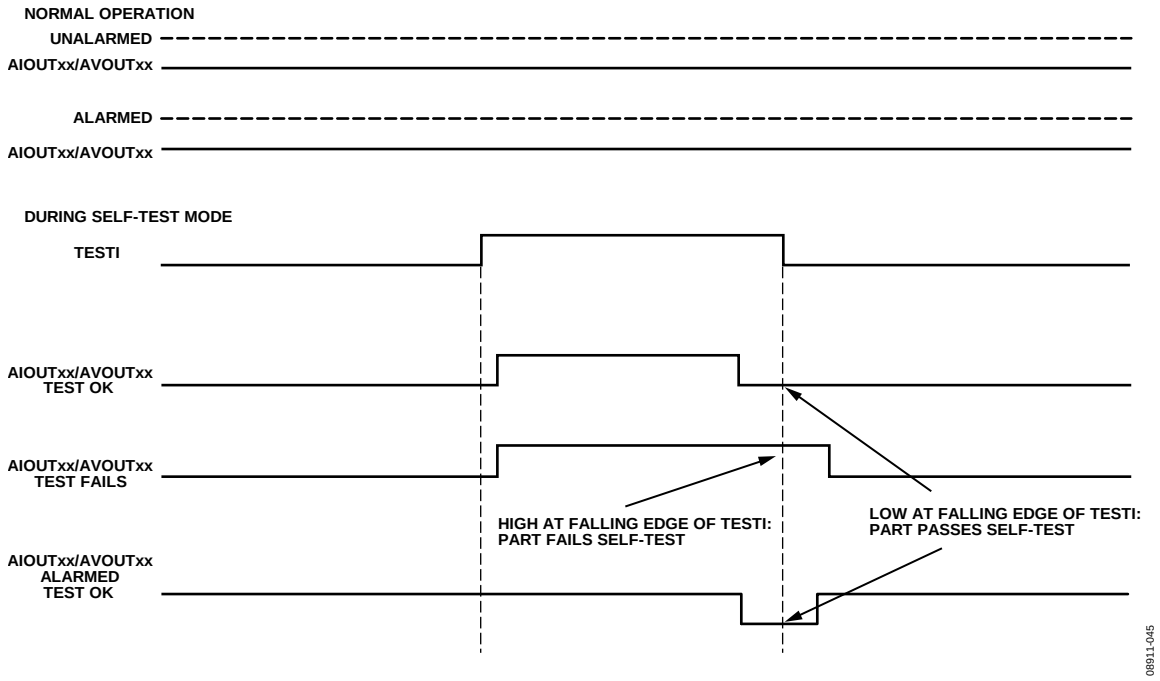


Figure 51. Timing Diagram for Alarms at AIOUTxx and AVOUTxx

Self-Test and Alarm Conditions

If an alarm occurs just prior to or just after the self-test pulse is initiated, the alarm causes the self-test to fail. The time span for this condition depends on the deglitch time.

- Deglitch time = 0.0 sec. The device fails self-test if an alarm occurs in the time period from 20 ms before the leading edge of the self-test pulse to 20 ms after the leading edge of the self-test pulse.
- Deglitch time > 0.0 sec. The device fails self-test if an alarm occurs in the time period from 100 ms before the leading edge of the self-test pulse to 100 ms after the leading edge of the self-test pulse.

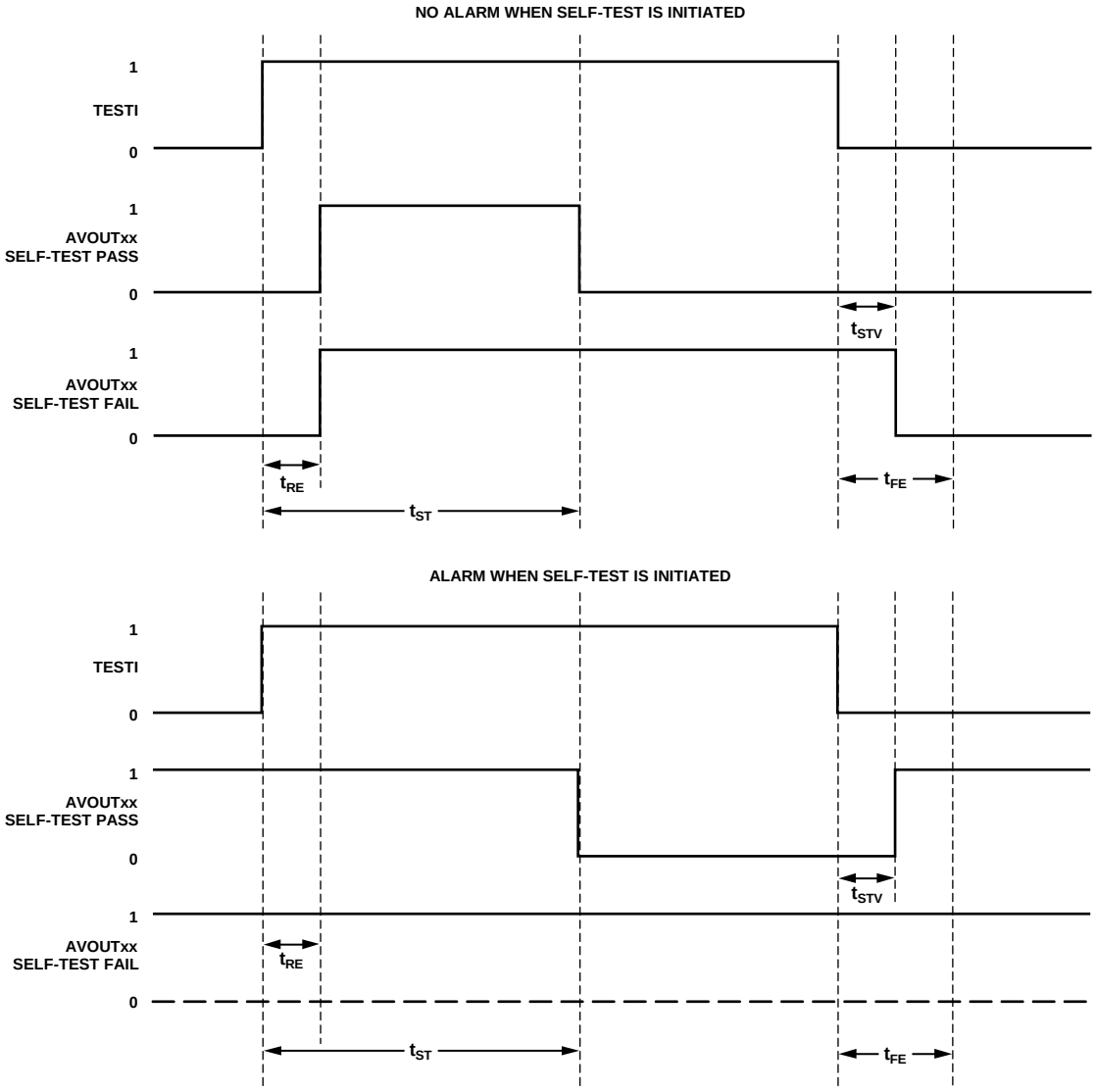
Therefore, in the unusual circumstance that the device fails self-test and there is an alarm condition state after the self-test, it is recommended to retest the device to ensure that an alarm did not occur just prior to or just after initiating the self-test.

The self-test works when the device is in the shared alarm mode or in the separate alarm mode. When the device is in the separate alarm mode, the self-test status on an output pertains only to the portion of the internal circuit relevant to the condition being monitored: overvoltage, undervoltage, or overtemperature.

Self-Test Timing and Monitoring Strategy

When monitoring the signals for self-test on the AD8280, note the following items:

- After initiating a self-test of the AD8280 with a rising edge on the TESTI pin, the alarm appearing at the AVOUTxx pin remains valid up to 2 µs after the rising edge on the TESTI pin.
- When the rising edge of the TESTI pulse occurs, monitor the AVOUTxx pin to ensure it is in the high state after the t_{RE} minimum time elapses.
- After the t_{ST} maximum time elapses, verify the AVOUTxx pin changed to the low state, indicating that the device or devices passed the self-test. Also ensure that the minimum length of the TESTI pulse is greater than t_{ST} maximum. The status of the self-test on the AVOUTxx pin is valid until t_{STV} maximum after the trailing edge of the TESTI pulse.
- The alarm state is valid again t_{FE} minimum after the trailing edge of the TESTI pulse.



NOTES
1. t_{RE} IS THE TIME FROM THE RISING EDGE OF THE TEST PULSE (TESTI) TO THE START OF THE SELF-TEST. WAIT A MINIMUM OF t_{RE} FROM THE EDGE OF TESTI BEFORE COUNTING ON A VALID SELF-TEST READING.
2. t_{ST} IS THE TIME FROM THE RISING EDGE OF THE TEST PULSE UNTIL THE DEVICE COMPLETES THE SELF-TEST (TEST PULSE MUST BE LONGER THAN t_{ST} MAX).
3. t_{STV} IS THE TIME FROM THE FALLING EDGE OF THE TEST PULSE THAT THE SELF-TEST INDICATION REMAINS VALID (LOW = PASS, HIGH = FAIL). TO MEASURE THE SELF-TEST SIGNAL AFTER TESTI GOES LOW (NOT RECOMMENDED), MEASURE BEFORE t_{STV} EXPIRED.
4. t_{FE} IS THE TIME FROM THE FALLING EDGE OF THE TEST PULSE UNTIL THE SELF-TEST DATA IS CLEARED AND THE ALARM DATA IS VALID AGAIN. WAIT A MINIMUM OF t_{FE} AFTER THE FALLING EDGE OF TESTI BEFORE RELYING ON THE ALARM SIGNALS.

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Figure 52. Timing Definitions

PROTECTION COMPONENTS AND PULL-UP/PULL-DOWN RESISTORS

As shown in Figure 45, several devices are added to provide protection in a high voltage environment. Zener Diode Z1 ensures that the six-cell stack voltage does not significantly exceed the maximum 30 V across the device. It is recommended that a 33 V rated Zener diode be used for Z1.

It is also possible to use diodes in the daisy-chain lines (anode to cathode from higher potential to lower potential) to protect the devices in the event that an open circuit appears on the battery connections, causing a high reverse voltage across the AD8280 (these diodes are not shown in Figure 45). The diodes must have a reverse voltage rating comparable to the highest voltage of the battery system.

If diodes are used in the daisy chain, it is also recommended that a diode be used between the top cell in the stack (anode) and VTOP (cathode) of the top device, as well as between VBOTx (anode) of each device and VTOP (cathode) of the next lowest potential device in the daisy chain.

Because there are no pull-up or pull-down resistors internal to the device, the user may want to pull down the TESTI pin of the bottom device through a 10 kΩ resistor to VBOTx (device ground). The addition of this resistor ensures that the device is not locked in self-test mode if the line opens. Also, the user may want to pull up the ENBI pin on the bottom device of a daisy chain so that if the line opens, the chain stays in the enabled (powered up) mode.

EMI CONSIDERATIONS

To increase immunity to electromagnetic interference (EMI), use the following components and layout schemes (see Figure 50).

- Use a 22 pF capacitor on each of the daisy-chain lines.
- Route the daisy-chain lines on an inner PCB layer.
- Use ground planes (connected to VBOTx from the higher potential device) both over and under the daisy-chain lines to shield them.
- Route the connections from VBOTx to VTOP to best ensure a low impedance connection between them.
- Use ferrite beads on the VTOP lines as shown in Figure 50.
- Use 100 nF capacitors across each of the six-cell battery stacks.
- Place the AD8280 devices as close together as possible on the board to minimize the length of the daisy-chain lines.

SYSTEM ACCURACY CALCULATION

When calculating system accuracy, there are four error sources to consider:

- Trip point error (see Table 1)
- Reference voltage error (see Table 1)
- Resistor tolerance
- Resistor temperature coefficient

Sample Calculation

Following is a sample calculation for overvoltage accuracy. In this calculation, the following conditions are assumed:

- Resistors used in the external resistor divider to set the trip points are ±1%, 100 ppm/°C resistors.
- Temperature range is −40°C to +85°C.
- Desired overvoltage trip point is 4.0 V (resistor values selected must be 15 kΩ and 60 kΩ).

The resulting sources of error are described in this section.

Maximum Trip Point Error

The maximum trip point error is ±15 mV.

Maximum Reference Error

The maximum reference error is as follows:

(60/(60 + 15)) × ±50 mV = ±40 mV

Maximum Resistor Tolerance Error

The maximum resistor tolerance error depends on the values of the resistors. If one resistor is high and the other is low, the worst-case error is as follows:

(60.6/(60.6 + 14.85)) × 5.00 V = 4.016 V (error of +16 mV)

(59.4/(59.4 + 15.15)) × 5.00 V = 3.984 V (error of −16 mV)

In this sample calculation, the maximum resistor tolerance error is ±16 mV.

Maximum Temperature Coefficient Error

If one resistor drifts high and the other resistor drifts low, the worst-case error is as follows:

60 kΩ + (100 ppm/°C × (25°C − (−40°C)) × 60 kΩ) = 60.39 kΩ

15 kΩ − (100 ppm/°C × (25°C − (−40°C)) × 15 kΩ) = 14.9 kΩ

(60.39/(60.39 + 14.90)) × 5.00 V = 4.010 V (error of +10 mV)

or

60 kΩ − (100 ppm/°C × (25°C − (−40°C)) × 60 kΩ) = 59.61 kΩ

15 kΩ + (100 ppm/°C × (25°C − (−40°C)) × 15 kΩ) = 15.1 kΩ

(59.61/(59.61 + 15.10)) × 5.00 V = 3.990 V (error of −10 mV)

In this sample calculation, the maximum temperature coefficient error is ±10 mV.

Total System Accuracy

The system accuracy, or the sum of all the errors, is ±81 mV. If the resistor pair coefficients are matched so that drift is in the same direction, that portion of the error can be ignored, and the total system accuracy is ±71 mV.

OUTLINE DIMENSIONS

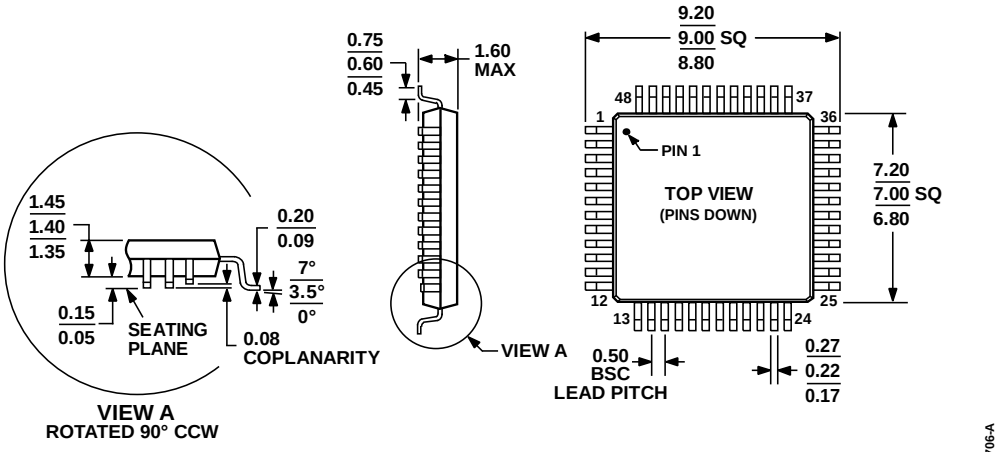

Figure 53. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD8280WASTZ	−40°C to +105°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD8280WASTZ-RL	−40°C to +105°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD8280-EVALZ		Evaluation Board with Two AD8280WASTZ Devices	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The AD8280W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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