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1/05—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = 2.7 V to 5.25 V; DV_{DD} = 2.7 V to 5.25 V; GND = 0 V; REFIN(+) = AV_{DD}; REFIN(−) = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	AD7798B/AD7799B[1]	Unit	Test Conditions/Comments
ADC CHANNEL			
Output Update Rate	4.17 – 470	Hz nom	
No Missing Codes[2]	24	Bits min	AD7799: f_{ADC} < 242 Hz
	16	Bits min	AD7798
Resolution			See Table 5 to Table 8
Output Noise and Update Rates			See Table 5 to Table 8
Integral Nonlinearity	±15	ppm of FSR max	
Offset Error[3]	±1	µV typ	
Offset Error Drift vs. Temperature[4]	±10	nV/°C typ	
Full-Scale Error[3, 5]	±10	µV typ	
Gain Drift vs. Temperature[4]	±1	ppm/°C typ	
Power Supply Rejection	100	dB min	AIN = 1 V/gain, gain ≥ 4
ANALOG INPUTS			
Differential Input Voltage Ranges	$\pm V_{REF}$/gain	V nom	V_{REF} = REFIN(+) – REFIN(–), gain = 1 to 128
Absolute AIN Voltage Limits[2]			
Unbuffered Mode	GND – 30 mV	V min	Gain = 1 or 2
	AV_{DD} + 30 mV	V max	
Buffered Mode	GND + 100 mV	V min	Gain = 1 or 2
	AV_{DD} – 100 mV	V max	
In-Amp Active	GND + 300 mV	V min	Gain = 4 to 128
	AV_{DD} – 1.1	V max	
Common-Mode Voltage, V_{CM}	0.5	V min	V_{CM} = (AIN(+) + AIN(–))/2, gain = 4 to 128
Analog Input Current			
Buffered Mode or In-Amp Active			
Average Input Current[2]	±1	nA max	Gain = 1 or 2, update rate < 100 Hz
	±250	pA max	Gain = 4 to 128, update rate < 100 Hz
	±1	nA max	AIN3(+)/AIN3(–), update rate < 100 Hz
Average Input Current Drift	±2	pA/°C typ	
Unbuffered Mode			Gain = 1 or 2
Average Input Current	±400	nA/V typ	Input current varies with input voltage
Average Input Current Drift	±50	pA/V/°C typ	
Normal Mode Rejection[2]			
@ 50 Hz, 60 Hz	65	dB min	80 dB typ, 50 ± 1 Hz, 60 ± 1 Hz (FS[3:0] = 1010)[6]
@ 50 Hz	80	dB min	90 dB typ, 50 ± 1 Hz (FS[3:0] = 1001)[6]
@ 60 Hz	90	dB min	100 dB typ, 60 ± 1 Hz (FS[3:0] = 1000)[6]
Common-Mode Rejection			
@ DC	100	dB min	AIN = 1 V/gain, gain ≥ 4
@ 50 Hz, 60 Hz[2]	100	dB min	50 ± 1 Hz, 60 ± 1 Hz (FS[3:0] = 1010)[6]
@ 50 Hz, 60 Hz[2]	100	dB min	50 ± 1 Hz (FS[3:0] = 1001[6]), 60 ± 1 Hz (FS[3:0] = 1000[6])

Parameter	AD7798B/AD7799B[1]	Unit	Test Conditions/Comments
REFERENCE			
External REFIN Voltage	2.5	V nom	REFIN = REFIN(+) − REFIN(−)
Reference Voltage Range[2]	0.1	V min	
	AV_{DD}	V max	When $V_{REF} = AV_{DD}$, the differential input must be limited to (0.9 x V_{REF}/gain) if the in-amp is active.
Absolute REFIN Voltage Limits[2]	GND − 30 mV	V min	
	AV_{DD} + 30 mV	V max	
Average Reference Input Current	400	nA/V typ	
Average Reference Input Current Drift	±0.03	nA/V/°C typ	
Normal Mode Rejection	Same as for analog inputs		
Common-Mode Rejection	100	dB typ	
Reference Detect Levels	0.3	V min	
	0.65	V max	NOXREF bit active if $V_{REF} < 0.3$ V
LOW-SIDE POWER SWITCH			
R_{ON}	7	Ω max	$AV_{DD} = 5$ V
	9	Ω max	$AV_{DD} = 3$ V
Allowable Current[2]	30	mA max	Continuous current
DIGITAL OUTPUTS (P1 and P2)			
Output High Voltage, V_{OH}[2]	AV_{DD} − 0.6	V min	$AV_{DD} = 3$ V, $I_{SOURCE} = 100$ µA
Output Low Voltage, V_{OL}[2]	0.4	V max	$AV_{DD} = 3$ V, $I_{SINK} = 100$ µA
Output High Voltage, V_{OH}[2]	4	V min	$AV_{DD} = 5$ V, $I_{SOURCE} = 200$ µA
Output Low Voltage, V_{OL}[2]	0.4	V max	$AV_{DD} = 5$ V, $I_{SINK} = 800$ µA
INTERNAL CLOCK			
Frequency[2]	64 ± 3%	kHz min/max	
LOGIC INPUTS			
$\overline{CS}$[2]			
Input Low Voltage, V_{INL}	0.8	V max	$DV_{DD} = 5$ V
	0.4	V max	$DV_{DD} = 3$ V
Input High Voltage, V_{INH}	2.0	V min	$DV_{DD} = 3$ V or 5 V
SCLK and DIN (Schmitt-Triggered Input)[2]			
$V_T(+)$	1.4/2	V min/max	$DV_{DD} = 5$ V
$V_T(-)$	0.8/1.7	V min/max	$DV_{DD} = 5$ V
$V_T(+) - V_T(-)$	0.1/0.17	V min/max	$DV_{DD} = 5$ V
$V_T(+)$	0.9/2	V min/max	$DV_{DD} = 3$ V
$V_T(-)$	0.4/1.35	V min/max	$DV_{DD} = 3$ V
$V_T(+) - V_T(-)$	0.06/0.13	V min/max	$DV_{DD} = 3$ V
Input Currents	±10	µA max	$V_{IN} = DV_{DD}$ or GND
Input Capacitance	10	pF typ	All digital inputs
LOGIC OUTPUTS			
Output High Voltage, V_{OH}[2]	DV_{DD} − 0.6	V min	$DV_{DD} = 3$ V, $I_{SOURCE} = 100$ µA
Output Low Voltage, V_{OL}[2]	0.4	V max	$DV_{DD} = 3$ V, $I_{SINK} = 100$ µA
Output High Voltage, V_{OH}[2]	4	V min	$DV_{DD} = 5$ V, $I_{SOURCE} = 200$ µA
Output Low Voltage, V_{OL}[2]	0.4	V max	$DV_{DD} = 5$ V, $I_{SINK} = 1.6$ mA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance	10	pF typ	
Data Output Coding	Offset binary		

Parameter	AD7798B/AD7799B[1]	Unit	Test Conditions/Comments
SYSTEM CALIBRATION[2]			
Full-Scale Calibration Limit	1.05 × FS	V max	FS = Full-scale analog input. When $V_{REF} = AV_{DD}$, the differential input must be limited to ($0.9 \times V_{REF}$/gain) if the in-amp is active.
Zero-Scale Calibration Limit	−1.05 × FS	V min	
Input Span	0.8 × FS	V min	
	2.1 × FS	V max	
POWER REQUIREMENTS[7]			
Power Supply Voltage			
AV_{DD} – GND	2.7/5.25	V min/max	
DV_{DD} – GND	2.7/5.25	V min/max	
Power Supply Currents			
I_{DD} Current	140	μA max	Unbuffered mode, 110 μA typ @ AV_{DD} = 3 V, 125 μA typ @ AV_{DD} = 5 V
	180	μA max	Buffered mode, gain = 1 or 2, 130 μA typ @ AV_{DD} = 3 V, 165 μA typ @ AV_{DD} = 5 V
	400	μA max	AD7798: gain = 4 to 128, 300 μA typ @ AV_{DD} = 3 V, 350 μA typ @ AV_{DD} = 5 V
	500	μA max	AD7799: gain = 4 to 128, 380 μA typ @ AV_{DD} = 3 V, 440 μA typ @ AV_{DD} = 5 V
I_{DD} (Power-Down Mode)	1	μA max	

[1] Temperature range is −40°C to +105°C. At the 19.6 Hz and 39.2 Hz update rates, the INL, power supply rejection (PSR), common-mode rejection (CMR), and normal mode rejection (NMR) do not meet the data sheet specification if the voltage on the AIN(+) or AIN(−) pins exceeds AV_{DD} − 1.6 V typically. When this voltage is exceeded, the INL, for example, is reduced to 18 ppm of FS typically and the PSR is reduced to 69 dB typically. Therefore, for guaranteed performance at these update rates, the absolute voltage on the analog input pins needs to be below AV_{DD} − 1.6 V.
[2] Specification is not production tested, but is supported by characterization data at initial product release.
[3] Following a calibration, this error is in the order of the noise for the programmed gain and update rate selected.
[4] Recalibration at any temperature removes these errors.
[5] Full-scale error applies to both positive and negative full-scale and applies at the factory calibration conditions (AV_{DD} = 4 V, gain = 1, T_A = 25°C).
[6] FS[3:0] are the four bits used in the mode register to select the output word rate.
[7] Digital inputs equal to DV_{DD} or GND.

TIMING CHARACTERISTICS

AV_{DD} = 2.7 V to 5.25 V, DV_{DD} = 2.7 V to 5.25 V, GND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = DV_{DD}, unless otherwise noted.

Table 2.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments
t_3	100	ns min	SCLK high pulse width
t_4	100	ns min	SCLK low pulse width
Read Operation			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_5[5, 6]	10	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	80	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high
Write Operation			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	30	ns min	Data valid to SCLK edge setup time
t_{10}	25	ns min	Data valid to SCLK edge hold time
t_{11}	0	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 3 and Figure 4.
[3] These times are measured with the load circuit of Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[4] SCLK active edge is the falling edge of SCLK.
[5] These times are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 2. The measured time is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.
[6] $\overline{RDY}$ returns high after a read of the ADC. In single-conversion mode and continuous-conversion mode, data can be reread, if required, while $\overline{RDY}$ is high, but care should be taken to ensure that subsequent reads do not occur close to the next output update. In continuous read mode, the digital word can be read only once.

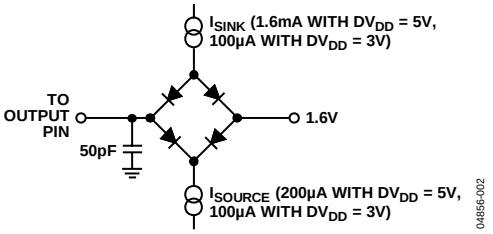

Figure 2. Load Circuit for Timing Characterization

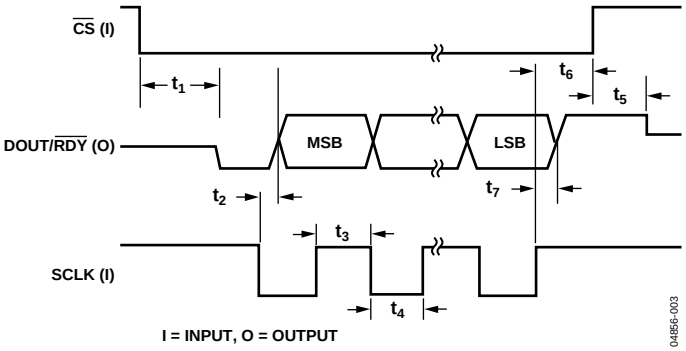

Figure 3. Read Cycle Timing Diagram

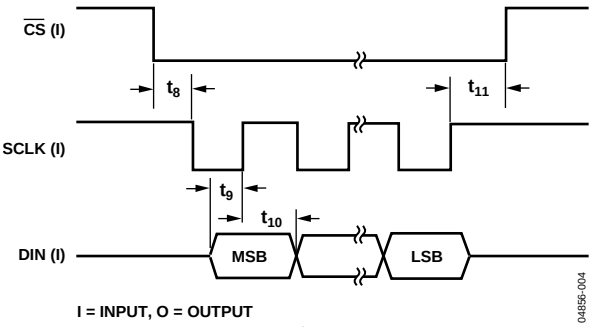

Figure 4. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +7 V
DV_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
AIN/Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP	
θ_{JA} Thermal Impedance	128°C/W
θ_{JC} Thermal Impedance	14°C/W
Lead Temperature, Soldering	
Reflow	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

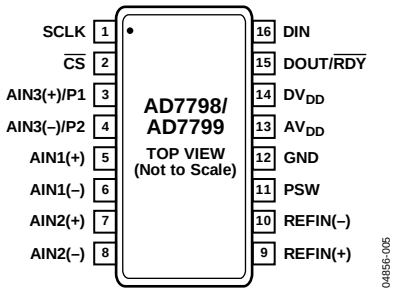

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous, with all data transmitted in a continuous train of pulses. Alternatively, it can be noncontinuous, with the information transmitted to or from the ADC in smaller batches of data.
2	$\overline{CS}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus, or it can be used as a frame synchronization signal when communicating with the device. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode, with SCLK, DIN, and DOUT/$\overline{RDY}$ used to interface with the device.
3	AIN3(+)/P1	Analog Input/Digital Output Pin. AIN3(+) is the positive terminal of the differential analog input pair AIN3(+)/AIN3(–). Alternatively, this pin can function as a general-purpose output bit referenced between AV_{DD} and GND
4	AIN3(–)/P2	Analog Input/Digital Output Pin. AIN3(–) is the negative terminal of the differential analog input pair AIN3(+)/AIN3(–). Alternatively, this pin can function as a general-purpose output bit referenced between AV_{DD} and GND
5	AIN1(+)	Analog Input. AIN1(+) is the positive terminal of the differential analog input pair AIN1(+)/AIN1(–).
6	AIN1(–)	Analog Input. AIN1(–) is the negative terminal of the differential analog input pair AIN1(+)/AIN1(–).
7	AIN2(+)	Analog Input. AIN2(+) is the positive terminal of the differential analog input pair AIN2(+)/AIN2(–).
8	AIN2(–)	Analog Input. AIN2(–) is the negative terminal of the differential analog input pair AIN2(+)/AIN2(–).
9	REFIN(+)	Positive Reference Input. An external reference can be applied between REFIN(+) and REFIN(–). REFIN(+) can lie anywhere between AV_{DD} and GND + 0.1 V. The nominal reference voltage (REFIN(+) – REFIN(–)) is 2.5 V, but the part can function with a reference from 0.1 V to AV_{DD}.
10	REFIN(–)	Negative Reference Input. REFIN(–) is the negative reference input for REFIN. This reference input can lie anywhere between GND and AV_{DD} – 0.1 V.
11	PSW	Low-Side Power Switch to GND.
12	GND	Ground Reference Point.
13	AV_{DD}	Supply Voltage. 2.7 V to 5.25 V.
14	DV_{DD}	Digital Interface Supply Voltage. The logic levels for the serial interface pins are related to this supply, which is between 2.7 V and 5.25 V. The DV_{DD} voltage is independent of the voltage on AV_{DD}; therefore, AV_{DD} can equal 5 V with DV_{DD} at 3 V, or vice versa.
15	DOUT/$\overline{RDY}$	Serial Data Output/Data Ready Output. DOUT/$\overline{RDY}$ serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{RDY}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{RDY}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{RDY}$ pin. With $\overline{CS}$ low, the data/control word information is placed on the DOUT/$\overline{RDY}$ pin on the SCLK falling edge and is valid upon the SCLK rising edge.
16	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers within the ADC, with the register selection bits of the communication register identifying the appropriate register.

OUTPUT NOISE AND RESOLUTION SPECIFICATIONS

AD7798

Table 5 shows the AD7798 output rms noise for some update rates and gain settings. The numbers given are for the bipolar input range with a 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 6 shows the effective resolution, and the output peak-to-peak resolution is shown in parentheses. It is important to note that the effective resolution is calculated using the rms noise, whereas the peak-to-peak resolution is based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 5. Output RMS Noise (μV) vs. Gain and Output Update Rate for the AD7798 Using a 2.5 V Reference

Update Rate	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17 Hz	0.64	0.6	0.29	0.22	0.1	0.065	0.039	0.041
8.33 Hz	1.04	0.96	0.38	0.26	0.13	0.078	0.057	0.055
16.7 Hz	1.55	1.45	0.54	0.36	0.18	0.11	0.087	0.086
33.2 Hz	2.3	2.13	0.74	0.5	0.23	0.17	0.124	0.118
62 Hz	2.95	2.85	0.92	0.58	0.29	0.2	0.153	0.144
123 Hz	4.89	4.74	1.49	1	0.48	0.32	0.265	0.283
242 Hz	11.76	9.5	4.02	1.96	0.88	0.45	0.379	0.397
470 Hz	11.33	9.44	3.07	1.79	0.99	0.63	0.568	0.593

Table 6. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7798 Using a 2.5 V Reference

Update Rate	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
8.33 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
16.7 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
33.2 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
62 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)
123 Hz	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.5)	16 (14.5)
242 Hz	16 (16)	16 (15.5)	16 (15.5)	16 (15.5)	16 (16)	16 (16)	16 (15)	16 (14)
470 Hz	16 (16)	16 (15.5)	16 (16)	16 (16)	16 (15.5)	16 (15.5)	16 (14.5)	15.5 (13.5)

AD7799

Table 7 shows the AD7799 output rms noise for some update rates and gain settings. The numbers given are for the bipolar input range with a 2.5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 8 shows the effective resolution, and the output peak-to-peak resolution is given in parentheses. Note that the effective resolution is calculated using the rms noise, whereas the peak-to-peak resolution is based on peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker. These numbers are typical and are rounded to the nearest LSB.

Table 7. Output RMS Noise (μV) vs. Gain and Output Update Rate for the AD7799 Using a 2.5 V Reference

Update Rate	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17 Hz	0.64	0.6	0.185	0.097	0.075	0.035	0.027	0.027
8.33 Hz	1.04	0.96	0.269	0.165	0.108	0.048	0.037	0.040
16.7 Hz	1.55	1.45	0.433	0.258	0.176	0.085	0.065	0.065
33.2 Hz	2.3	2.13	0.647	0.364	0.24	0.118	0.097	0.094
62 Hz	2.95	2.85	0.952	0.586	0.361	0.178	0.133	0.134
123 Hz	4.89	4.74	1.356	0.785	0.521	0.265	0.192	0.192
242 Hz	11.76	9.5	3.797	2.054	1.027	0.476	0.326	0.308
470 Hz	11.33	9.44	3.132	1.773	1.107	0.5	0.413	0.374

Table 8. Typical Resolution (Bits) vs. Gain and Output Update Rate for the AD7799 Using a 2.5 V Reference

Update Rate	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.17 Hz	23 (20.5)	22 (19.5)	22.5 (20)	22.5 (20)	22 (19.5)	22 (19.5)	21.5 (19)	20.5 (18)
8.33 Hz	22 (19.5)	21.5 (19)	22 (19.5)	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	20 (17.5)
16.7 Hz	21.5 (19)	20.5 (18)	21.5 (19)	21 (18.5)	21 (18.5)	21 (18.5)	20 (17.5)	19 (16.5)
33.3 Hz	21 (18.5)	20 (17.5)	21 (18.5)	20.5 (18)	20.5 (18)	20.5 (18)	19.5 (17)	18.5 (16)
62 Hz	20.5 (18)	19.5 (17)	20.5 (18)	20 (17.5)	19.5 (17)	19.5 (17)	19 (16.5)	18 (15.5)
123 Hz	20 (17.5)	19 (16.5)	20 (17.5)	19.5 (17)	19 (16.5)	19 (16.5)	18.5 (16)	17.5 (15)
242 Hz	18.5 (16)	18 (15.5)	18.5 (16)	18 (15.5)	18 (15.5)	18.5 (16)	18 (15.5)	17 (14.5)
470 Hz	18.5 (16)	18 (15.5)	18.5 (16)	18.5 (16)	18 (15.5)	18.5 (16)	17.5 (15)	16.5 (14)

TYPICAL PERFORMANCE CHARACTERISTICS

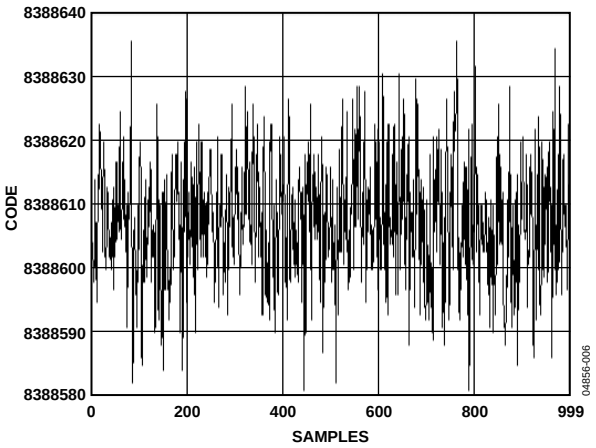

Figure 6. AD7799 Noise (V_{REF} = AV_{DD}/2, Gain = 64, Update Rate = 4.17 Hz)

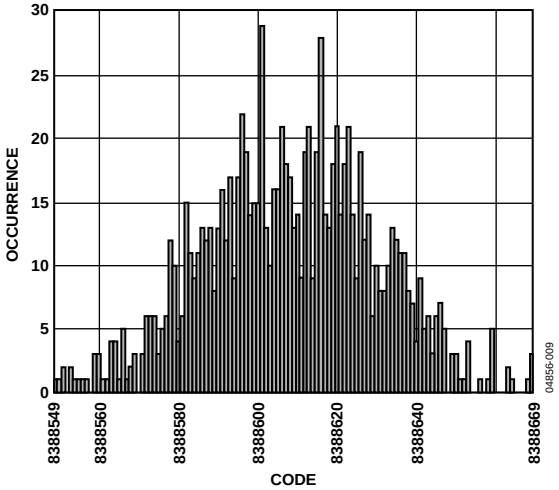

Figure 9. AD7799 Noise Distribution Histogram (V_{REF} = AV_{DD}/2, Gain = 64, Update Rate = 16.7 Hz)

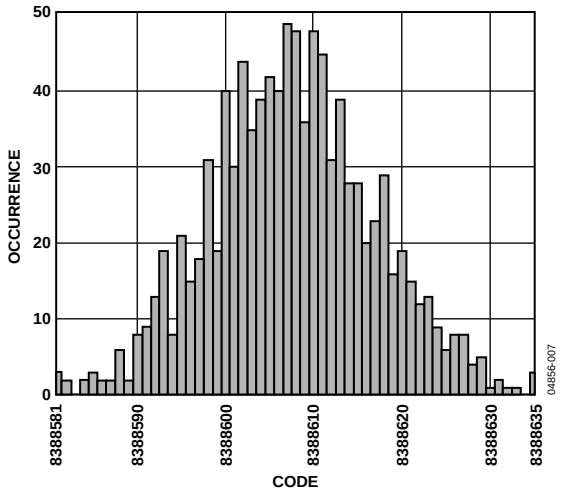

Figure 7. AD7799 Noise Distribution Histogram (V_{REF} = AV_{DD}/2, Gain = 64, Update Rate = 4.17 Hz)

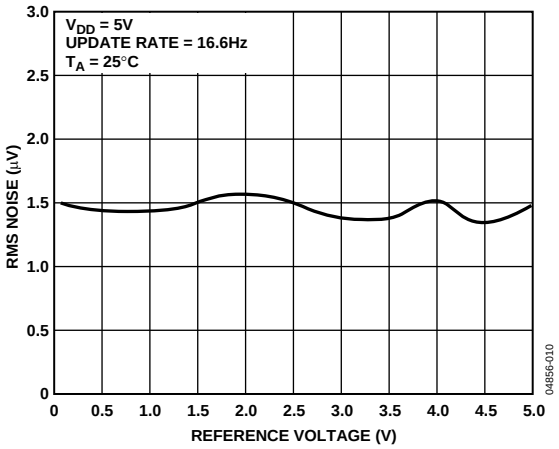

Figure 10. RMS Noise vs. Reference Voltage (Gain = 1)

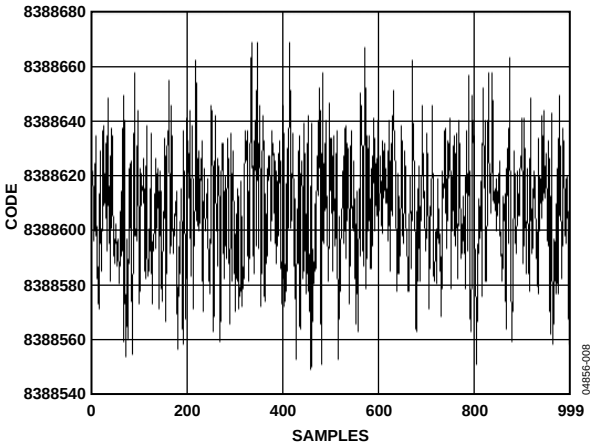

Figure 8. AD7799 Noise (V_{REF} = AV_{DD}/2, Gain = 64, Update Rate = 16.7 Hz)

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers, which are described on the following pages. In the following descriptions, *set* implies a Logic 1 state and *cleared* implies a Logic 0 state, unless otherwise stated.

COMMUNICATION REGISTER

RS2, RS1, RS0 = 0, 0, 0

The communication register is an 8-bit, write-only register. All communication to the part must start with a write operation to the communication register. The data written to the communication register determines whether the next operation is a read or write operation, and to which register this operation takes place. After the read or write operation is complete, the interface returns to its default state, where it expects a write operation to the communication register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 9 outlines the bit designations for the communication register. CR0 through CR7 indicate the bit location, with CR denoting that the bits are in the communication register. CR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{WEN}$(0)	R/$\overline{W}$(0)	RS2(0)	RS1(0)	RS0(0)	CREAD(0)	0(0)	0(0)

Table 9. Communication Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{WEN}$	Write Enable Bit. A 0 must be written to this bit so that the write to the communication register occurs. If a 1 is the first bit written, the part does not clock subsequent bits into the register. It stays at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{WEN}$ bit, the next seven bits are loaded to the communication register.
CR6	R/$\overline{W}$	Read/$\overline{Write}$ Bit. A 0 in this bit location indicates that the next operation is a write to a specified register. A 1 in this position indicates that the next operation is a read from the designated register.
CR5 to CR3	RS2 to RS0	Register Address Bits. These bits are used to select the register during the serial interface communication. See Table 10.
CR2	CREAD	Continuous Read of the Data Register Bit. When this bit is set to 1 and the data register is selected, the serial interface is configured so that the data register can be continuously read, that is, the contents of the data register are placed on the DOUT pin automatically when the SCLK pulses are applied after the $\overline{RDY}$ pin goes low to indicate that a conversion is complete. The communication register does not have to be written to for data reads. To enable continuous read mode, the instruction 01011100 must be written to the communication register. To exit the continuous read mode, the instruction 01011000 must be written to the communication register while the $\overline{RDY}$ pin is low. While in continuous read mode, the ADC monitors activity on the DIN line for the instruction to exit continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.
CR1 to CR0	0	These bits must be programmed to Logic 0 for correct operation.

Table 10. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communication register during a write operation	8 bits
0	0	0	Status register during a read operation	8 bits
0	0	1	Mode register	16 bits
0	1	0	Configuration register	16 bits
0	1	1	Data register	16 bits (AD7798)/24 bits (AD7799)
1	0	0	ID register	8 bits
1	0	1	IO register	8 bits
1	1	0	Offset register	16 bits (AD7798)/24 bits (AD7799)
1	1	1	Full-scale register	16 bits (AD7798)/24 bits (AD7799)

STATUS REGISTER

RS2, RS1, RS0 = 0, 0, 0; Power-On/Reset = 0x80 (AD7798)/0x88 (AD7799)

The status register is an 8-bit, read-only register. To access the status register, the user must write to the communication register, select the next operation to be a read, and load Bit RS2, Bit RS1, and Bit RS0 with 0. Table 11 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, with SR denoting that the bits are in the status register. SR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of the bit.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{\text{RDY}}$(1)	ERR(0)	NOREF(0)	0(0)	0/1	CH2(0)	CH1(0)	CH0(0)

Table 11. Status Register Bit Designations

Bit Location	Bit Name	Description
SR7	$\overline{\text{RDY}}$	Ready Bit. Cleared when data is written to the data register. Set after the data register is read or after a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is also set when the part is placed in power-down mode. The end of a conversion is indicated by the DOUT/$\overline{\text{RDY}}$ pin. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
SR6	ERR	Error Bit. This bit is written to at the same time as the $\overline{\text{RDY}}$ bit. Set to indicate that the result written to the data register is clamped to all 0s or all 1s. Error sources include overrange and underrange. Cleared by a write operation to start a conversion.
SR5	NOREF	No Reference Bit. Set to indicate that the reference (REFIN) is at a voltage below a specified threshold. When NOREF is set, conversion results are clamped to all 1s. Cleared to indicate that a valid reference is applied to the reference pins. The NOREF bit is enabled by setting the REF_DET bit in the configuration register to 1.
SR4	0	This bit is automatically cleared.
SR3	0/1	This bit is automatically cleared on the AD7798 and automatically set on the AD7799.
SR2 to SR0	CH2 to CH0	These bits indicate which channel is being converted by the ADC.

MODE REGISTER

RS2, RS1, RS0 = 0, 0, 1; Power-On/Reset = 0x000A

The mode register is a 16-bit register from which data can be read or to which data can be written. This register is used to select the operating mode, update rate, and low-side power switch. Table 12 outlines the bit designations for the mode register. MR0 through MR15 indicate the bit locations, with MR denoting that the bits are in the mode register. MR15 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit. A write to the mode register resets the modulator and filter and sets the $\overline{\text{RDY}}$ bit.

MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8
MD2(0)	MD1(0)	MD0(0)	PSW(0)	0(0)	0(0)	0(0)	0(0)
MR7	**MR6**	**MR5**	**MR4**	**MR3**	**MR2**	**MR1**	**MR0**
0(0)	0(0)	0(0)	0(0)	FS3(1)	FS2(0)	FS1(1)	FS0(0)

Table 12. Mode Register Bit Designations

Bit Location	Bit Name	Description
MR15 to MR13	MD2 to MD0	Mode Select Bits. These bits select the operational mode of the AD7798/AD7799 (see Table 13).
MR12	PSW	Power Switch Control Bit. Set by user to close the power switch PSW to GND. The power switch can sink up to 30 mA. Cleared by user to open the power switch. When the ADC is placed in power-down mode, the power switch is opened.
MR11 to MR4	0	These bits must be programmed with a Logic 0 for correct operation.
MR3 to MR0	FS3 to FS0	Filter Update Rate Select Bits (see Table 14).

Table 13. Operating Modes

MD2	MD1	MD0	Mode
0	0	0	Continuous-Conversion Mode (Default). In continuous-conversion mode, the ADC continuously performs conversions and places the result in the data register. RDY goes low when a conversion is complete. After power-on, a channel change, or a write to the mode, configuration, or IO registers, the first conversion is available after a period of $2/f_{ADC}$, and subsequent conversions are available at a frequency of f_{ADC}.
0	0	1	Single-Conversion Mode. When single-conversion mode is selected, the ADC powers up and performs a single conversion. The oscillator requires 1 ms to power up and settle. The ADC then performs the conversion, which takes a time of $2/f_{ADC}$. The conversion result is placed in the data register, RDY goes low, and the ADC returns to power-down mode. The conversion remains in the data register and RDY remains active (low) until the data is read or another conversion is performed.
0	1	0	Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state, although the modulator clocks are still provided.
0	1	1	Power-Down Mode. In this mode, all AD7798/AD7799 circuitry is powered down, including the burnout currents.
1	0	0	Internal Zero-Scale Calibration. An internal short is automatically connected to the enabled channel. A calibration takes two conversion cycles to complete. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel.
1	0	1	Internal Full-Scale Calibration. A full-scale input voltage is automatically connected to the selected analog input for this calibration. When the gain equals 1, a calibration takes two conversion cycles to complete. For higher gains, four conversion cycles are required to perform the full-scale calibration. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. Internal full-scale calibrations cannot be performed when the gain equals 128. The ADC is factory-calibrated at a gain of 128 and this factory-generated value is placed in the full-scale register on power up and when the gain is set to 128. With this gain setting, a system full-scale calibration can be performed. To minimize the full-scale error, a full-scale calibration is required each time the gain of a channel is changed.
1	1	0	System Zero-Scale Calibration. Users should connect the system zero-scale input to the channel input pins as selected by the CH2 to CH0 bits. A system offset calibration takes two conversion cycles to complete. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel. A zero-scale calibration is required each time the gain of a channel is changed.
1	1	1	System Full-Scale Calibration. Users should connect the system full-scale input to the channel input pins, as selected by the CH2 to CH0 bits. A calibration takes two conversion cycles to complete. RDY goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed.

Table 14. Update Rates Available

FS3	FS2	FS1	FS0	f_{ADC} (Hz)	t_{SETTLE} (ms)	Rejection @ 50 Hz/60 Hz
0	0	0	0	Reserved		
0	0	0	1	470	4	
0	0	1	0	242	8	
0	0	1	1	123	16	
0	1	0	0	62	32	
0	1	0	1	50	40	
0	1	1	0	39	48	
0	1	1	1	33.2	60	
1	0	0	0	19.6	101	90 dB (60 Hz only)
1	0	0	1	16.7	120	80 dB (50 Hz only)
1	0	1	0	16.7	120	65 dB
1	0	1	1	12.5	160	66 dB
1	1	0	0	10	200	69 dB
1	1	0	1	8.33	240	70 dB
1	1	1	0	6.25	320	72 dB
1	1	1	1	4.17	480	74 dB

CONFIGURATION REGISTER

RS2, RS1, RS0 = 0, 1, 0; Power-On/Reset = 0x0710

The configuration register is a 16-bit register from which data can be read or to which data can be written. This register is used to configure the ADC for unipolar or bipolar mode, to enable or disable the buffer, to enable or disable the burnout currents, to select the gain, and to select the analog input channel. Table 15 outlines the bit designations for the filter register. CON0 through CON15 indicate the bit locations, with CON denoting that the bits are in the configuration register. CON15 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of the bit.

CON15	CON14	CON13	CON12	CON11	CON10	CON9	CON8
0(0)	0(0)	BO(0)	U/$\overline{B}$ (0)	0(0)	G2(1)	G1(1)	G0(1)
CON7	**CON6**	**CON5**	**CON4**	**CON3**	**CON2**	**CON1**	**CON0**
0(0)	0(0)	REF_DET(0)	BUF(1)	0(0)	CH2(0)	CH1(0)	CH0(0)

Table 15. Configuration Register Bit Designations

Bit Location	Bit Name	Description
CON15 to CON14	0	These bits must be programmed with a Logic 0 for correct operation.
CON13	BO	Burnout Current Enable Bit. When this bit is set to 1 by the user, the 100 nA current sources in the signal path are enabled. When BO = 0, the burnout currents are disabled. The burnout currents can be enabled only when the buffer or in-amp is active.
CON12	U/$\overline{B}$	Unipolar/Bipolar Bit. Set by the user to enable unipolar coding, that is, zero differential input results in 0x000000 output, and a full-scale differential input results in 0xFFFFFF output. Cleared by the user to enable bipolar coding. Negative full-scale differential input results in an output code of 0x000000, zero differential input results in an output code of 0x800000, and a positive full-scale differential input results in an output code of 0xFFFFFF.
CON11	0	This bit must be programmed with a Logic 0 for correct operation.
CON10 to CON8	G2 to G0	Gain Select Bits. Written to by the user to select the ADC input range as follows:

G2	G1	G0	Gain	ADC Input Range (2.5 V Reference)
0	0	0	1 (in-amp not used)	2.5 V
0	0	1	2 (in-amp not used)	1.25 V
0	1	0	4	625 mV
0	1	1	8	312.5 mV
1	0	0	16	156.2 mV
1	0	1	32	78.125 mV
1	1	0	64	39.06 mV
1	1	1	128	19.53 mV

CON7 to CON6	0	These bits must be programmed with a Logic 0 for correct operation.
CON5	REF_DET	Enables the reference detect function. When REF_DET is set, the NOREF bit in the status register indicates when the external reference being used by the ADC is open circuit or less than 0.5 V. When cleared, the reference detect function is disabled.
CON4	BUF	Configures the ADC for buffered or unbuffered modes. If BUF is cleared, the ADC operates in unbuffered mode, lowering the power consumption of the device. If BUF is set, the ADC operates in buffered mode, allowing the user to place source impedances on the front end without contributing gain errors to the system. The buffer can be disabled when the gain equals 1 or 2. For higher gains, the buffer is automatically enabled. With the buffer disabled, the voltage on the analog input pins can range from 30 mV below GND to 30 mV above AV_{DD}. When the buffer is enabled, it requires some headroom; therefore, the voltage on any input pin must be limited to 100 mV within the power supply rails.
CON3	0	This bit must be programmed with a Logic 0 for correct operation.
CON2 to CON0	CH2 to CH0	Channel Select Bits. Written to by the user to select the active analog input channel to the ADC as follows:

CH2	CH1	CH0	Channel	Calibration Pair
0	0	0	AIN1(+) – AIN1(–)	0
0	0	1	AIN2(+) – AIN2(–)	1
0	1	0	AIN3(+) – AIN3(–)	2
0	1	1	AIN1(–) – AIN1(–)	0
1	0	0	Reserved	
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	AV_{DD} monitor	Automatically selects gain = 1/6 and internal reference = 1.17 V

DATA REGISTER

RS2, RS1, RS0 = 0, 1, 1; Power-On/Reset = 0x0000(00)

The conversion result from the ADC is stored in the data register. This is a read-only register. Upon completion of a read operation from this register, the $\overline{RDY}$ bit and DOUT/$\overline{RDY}$ pin are set.

ID REGISTER

RS2, RS1, RS0 = 1, 0, 0; Power-On/Reset = 0xX8 (AD7798)/0xX9 (AD7799)

The identification number for the AD7798/AD7799 is stored in the ID register. This is a read-only register.

IO REGISTER

RS2, RS1, RS0 = 1, 0, 1; Power-On/Reset = 0x00

The IO register is an 8-bit register from which data can be read or to which data can be written. This register is used to select the function of the AIN3(+)/AIN3(−) pins. Table 16 outlines the bit designations for the IO register. IO0 through IO7 indicate the bit locations, with IO denoting that the bits are in the IO register. IO7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
0(0)	IOEN(0)	IO2DAT(0)	IO1DAT(0)	0(0)	0(0)	0(0)	0(0)

Table 16. IO Register Bit Designations

Bit Location	Bit Name	Description
IO7	0	This bit must be programmed with a Logic 0 for correct operation.
IO6	IOEN	Configures the pins AIN3(+)/P1 and AIN3(−)/P2 as analog input pins or digital output pins. When this bit is set, the pins are configured as Digital Output Pins P1 and P2. When this bit is cleared, these pins are configured as analog input pins AIN3(+) and AIN3(−).
IO5, IO4	IO2DAT, IO1DAT	P1/P2 Data. When IOEN is set, the data for the Digital Output Pins P1 and P2 is written to Bit IO1DAT and Bit IO2DAT.
IO3 to IO0	0	These bits must be programmed with a Logic 0 for correct operation.

OFFSET REGISTER

RS2, RS1, RS0 = 1, 1, 0; Power-On/Reset = 0x8000(AD7798)/0x800000 (AD7799)

Each analog input channel has a dedicated offset register that holds the offset calibration coefficient for the channel. This register is 16 bits wide on the AD7798 and 24 bits wide on the AD7799, and its power-on/reset value is 8000(00) hex. The offset register is used in conjunction with its associated full-scale register to form a register pair. The power-on/reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user. The offset register is a read/write register. However, the AD7798/AD7799 must be in idle mode or power-down mode when writing to the offset register.

FULL-SCALE REGISTER

RS2, RS1, RS0 = 1, 1, 1; Power-On/Reset = 0x5XXX (AD7798)/0x5XXX00 (AD7799)

The full-scale register is a 16-bit register on the AD7798 and a 24-bit register on the AD7799. The full-scale register holds the full-scale calibration coefficient for the ADC. The AD7798/AD7799 has three full-scale registers, with each channel having a dedicated full-scale register. The full-scale registers are read/write registers. However, when writing to the full-scale registers, users must place the ADC in power-down mode or idle mode. Upon power-on, these registers are configured with factory-calibrated, full-scale calibration coefficients, with the calibration performed at gain = 128, the default gain setting. The default value is automatically overwritten if an internal or system full-scale calibration is initiated by the user, or the full-scale register is written to.

ADC CIRCUIT INFORMATION

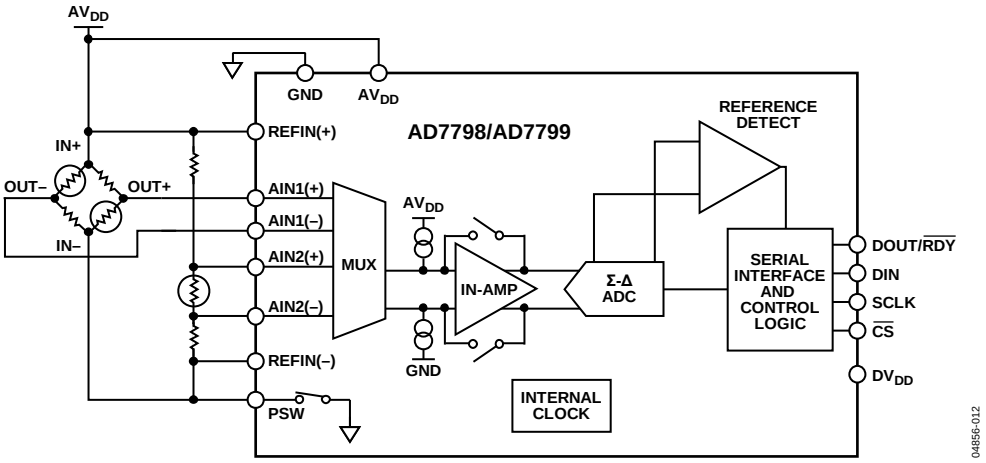

Figure 11. Basic Connection Diagram

OVERVIEW

The AD7798/AD7799 are low power ADCs that each incorporate a Σ-Δ modulator, a buffer, an in-amp, and on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals, such as those in pressure transducers and weigh scales.

Each part has three differential inputs that can be buffered or unbuffered. The reference is provided by an external reference source. Figure 11 shows the basic connections required to operate the parts.

The output rate of the AD7798/AD7799 (f_{ADC}) is user-programmable. The allowable update rates, along with the corresponding settling times, are listed in Table 14. Normal mode rejection is the major function of the digital filter. Simultaneous 50 Hz and 60 Hz rejection is optimized when the update rate equals 16.7 Hz or less, because notches are placed at both 50 Hz and 60 Hz with these update rates (see Figure 13).

The AD7798/AD7799 use slightly different filter types, depending on the output update rate, so that the rejection of quantization noise and device noise is optimized. When the update rate ranges from 4.17 Hz to 12.5 Hz, a sinc3 filter, along with an averaging filter, is used. When the update rate ranges from 16.7 Hz to 39 Hz, a modified sinc3 filter is used. This filter gives simultaneous 50 Hz and 60 Hz rejection when the update rate equals 16.7 Hz. A sinc4 filter is used when the update rate ranges from 50 Hz to 242 Hz. Finally, an integrate-only filter is used when the update rate equals 470 Hz. Figure 12 through Figure 15 show the frequency responses of the different filter types for a few of the update rates.

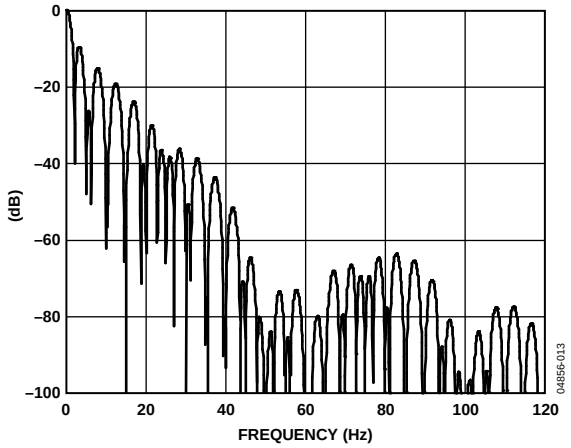

Figure 12. Filter Profile with Update Rate = 4.17 Hz

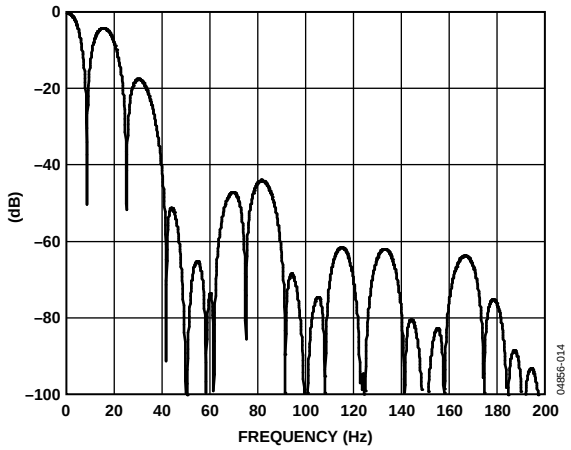

Figure 13. Filter Profile with Update Rate = 16.7 Hz

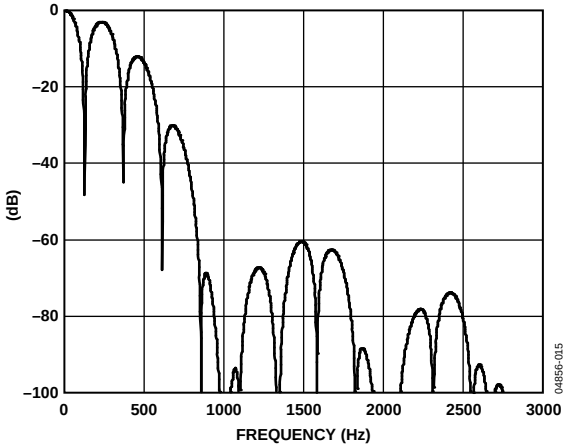

Figure 14. Filter Profile with Update Rate = 242 Hz

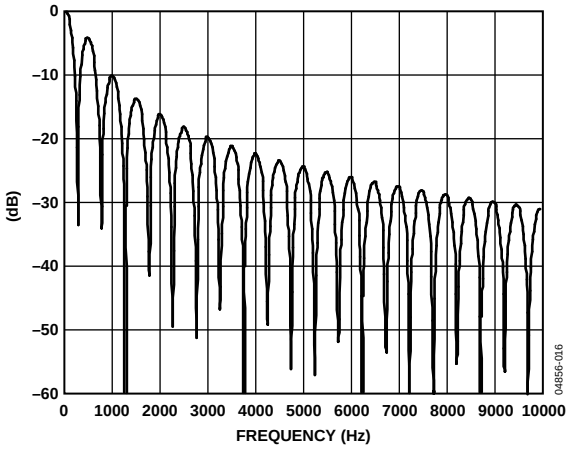

Figure 15. Filter Response with Update Rate = 470 Hz

DIGITAL INTERFACE

As previously outlined, the programmable functions of the AD7798/AD7799 are controlled using a set of on-chip registers. Data is written to these registers via the serial interface, which also provides read access to the on-chip registers. All communication with the part must start with a write to the communication register. After power-on or reset, the device expects a write to its communication register. The data written to this register determines whether the next operation is a read or write operation and to which register this operation occurs. Therefore, write access to any register begins with a write operation to the communication register, followed by a write to the selected register. A read operation from any other register (except when continuous-read mode is selected) starts with a write to the communication register, followed by a read operation from the selected register.

The serial interface of the AD7798/AD7799 consists of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line is used to transfer data into the on-chip registers, and DOUT/$\overline{RDY}$ is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT/$\overline{RDY}$) occur with respect to the SCLK signal. The DOUT/$\overline{RDY}$ pin operates as a data ready signal, with the line going low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the data register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select a device. It can be used to decode the AD7798/AD7799 in systems where several components are connected to the serial bus.

Figure 3 and Figure 4 show timing diagrams for interfacing to the AD7798/AD7799, with $\overline{CS}$ being used to decode the part. Figure 3 shows the timing for a read operation from the AD7798/AD7799 output shift register, and Figure 4 shows the timing for a write operation to the input shift register. It is possible to read the same word from the data register several times, even though the DOUT/$\overline{RDY}$ line returns high after the first read operation. However, care must be taken to ensure that the read operations are complete before the next output update occurs. In continuous-read mode, the data register can only be read once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD7798/AD7799. The end of the conversion can be monitored using the $\overline{RDY}$ bit in the status register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin. For microcontroller interfaces, it is recommended that SCLK idles high between data transfers.

The AD7798/AD7799 can be operated with $\overline{CS}$ being used as a frame-synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$, because $\overline{CS}$ normally occurs after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided that the timing numbers are obeyed.

The serial interface can be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7798/AD7799 line for at least 32 serial clock cycles, the serial interface is reset. This ensures that the interface can be reset to a known state if the interface is lost due to a software error or a glitch in the system. Reset returns the interface to the state in which it is expecting a write to the communication register. This operation resets the contents of all registers to their power-on values. Following a reset, the user should allow a period of 500 microseconds before addressing the serial interface.

The AD7798/AD7799 can be configured to continuously convert or to perform a single conversion (See Figure 16 through Figure 18).

Single-Conversion Mode

In single-conversion mode, the AD7798/AD7799 is placed in power-down mode after conversions. When a single conversion is initiated by setting MD2, MD1, and MD0 to 0, 0, and 1 in the mode register, the AD7798/AD7799 powers up, performs a single conversion, and then returns to power-down mode. The on-chip oscillator requires approximately 1 ms to power up. A conversion requires a time period of $2 \times t_{ADC}$. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. If $\overline{CS}$ is low, DOUT/$\overline{RDY}$ remains high until another conversion is initiated and completed. The data register can be read several times if required, even when DOUT/$\overline{RDY}$ is high.

Continuous-Conversion Mode

This is the default power-up mode. The AD7798/AD7799 continuously converts, with the $\overline{RDY}$ bit in the status register going low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, the user can write to the communication register, indicating that the next operation is a read of the data register. The digital conversion is placed on the DOUT/$\overline{RDY}$ pin as soon as SCLK pulses are applied to the ADC. DOUT/$\overline{RDY}$ returns high when the conversion is read. The user can reread this register if required. However, the user must ensure that the data register is not accessed at the completion of the next conversion, or the new conversion word is lost.

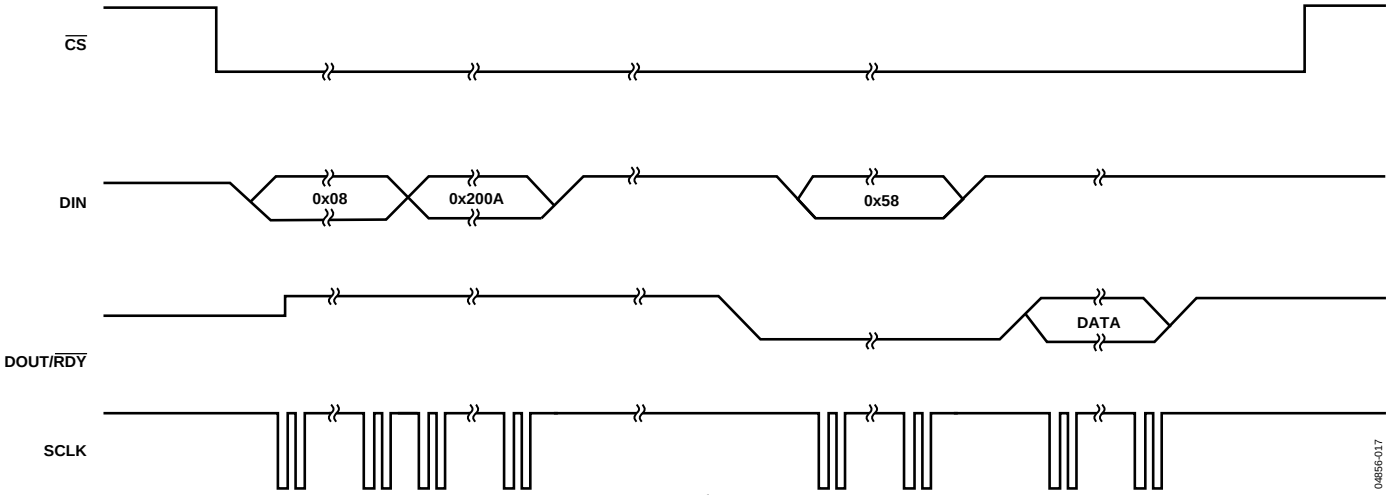

Figure 16. Single Conversion

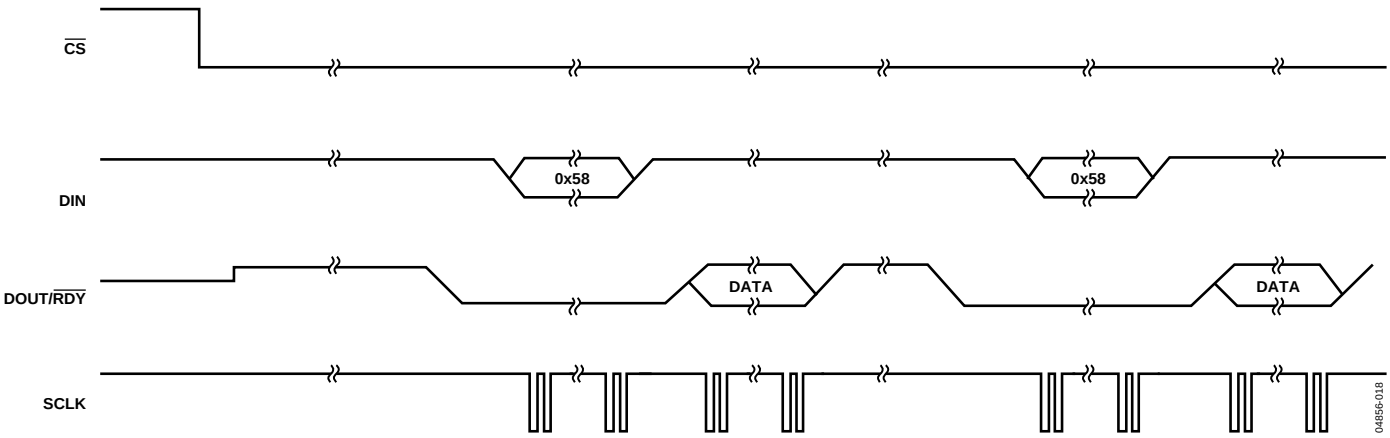

Figure 17. Continuous Conversion

Continuous Read

Rather than write to the communication register to access the data each time a conversion is complete, the AD7798/AD7799 can be configured so that the conversions are placed on the DOUT/$\overline{\text{RDY}}$ line automatically. By writing 01011100 to the communication register, the user need only apply the appropriate number of SCLK cycles to the ADC, and the 16-/24-bit word is automatically placed on the DOUT/$\overline{\text{RDY}}$ line when a conversion is complete. The ADC should be configured for continuous conversion mode.

When DOUT/$\overline{\text{RDY}}$ goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC, and the data conversion is placed on the DOUT/$\overline{\text{RDY}}$ line. When the conversion is read, DOUT/$\overline{\text{RDY}}$ returns high until the next conversion is available. In this mode, the data can only be read once. In addition, the user must ensure that the data-word is read before the next conversion is complete. If the user does not read the conversion before the completion of the next conversion, or if insufficient serial clocks are applied to the AD7798/AD7799 to read the word, the serial output register is reset when the next conversion is complete, and the new conversion is placed in the output serial register.

To exit the continuous-read mode, the instruction 01011000 must be written to the communication register while the DOUT/$\overline{\text{RDY}}$ pin is low. While in continuous-read mode, the ADC monitors activity on the DIN line in case the instruction to exit the continuous-read mode occurs. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous-read mode until an instruction is written to the device.

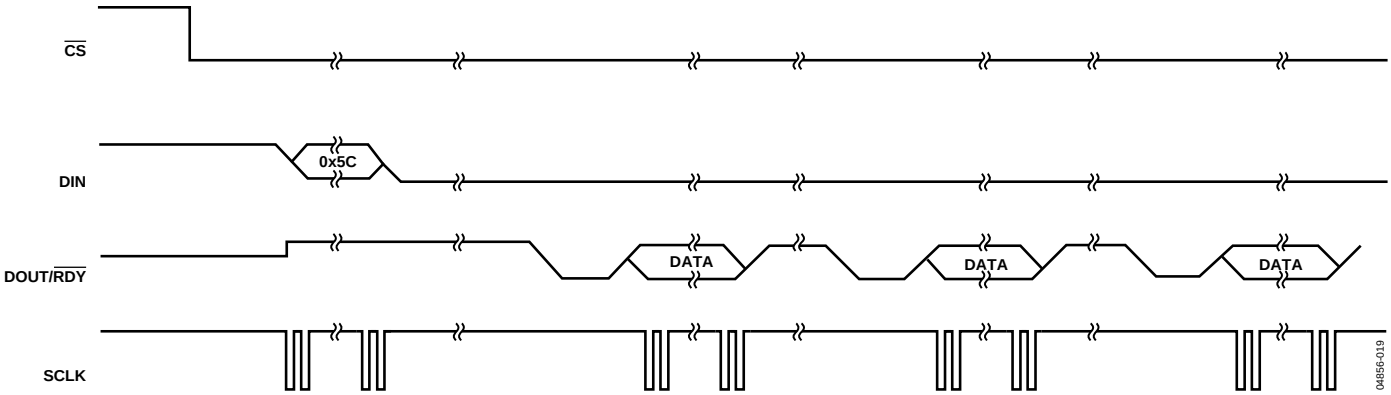

Figure 18. Continuous Read

CIRCUIT DESCRIPTION

ANALOG INPUT CHANNEL

The AD7798/AD7799 each have three differential analog input channels. These are connected to the on-chip buffer amplifier when the devices are operated in buffered mode, and directly to the modulator when the devices are operated in unbuffered mode. In buffered mode (the BUF bit in the mode register is set to 1), the input channel feeds into a high impedance input stage of the buffer amplifier. Therefore, the input can tolerate significant source impedances and is tailored for direct connection to external resistive-type sensors, such as strain gages or resistance temperature detectors (RTDs).

When BUF = 0, the parts are operated in unbuffered mode. This results in a higher analog input current. Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause gain errors, depending on the output impedance of the source that is driving the ADC input. Table 17 shows the allowable external resistance/capacitance values for unbuffered mode such that no gain error at the 20-bit level is introduced.

Table 17. External Resistance/Capacitance Combination for Unbuffered Mode (Without 20-Bit Gain Error)

Capacitance (pF)	Resistance (Ω)
50	9 k
100	6 k
500	1.5 k
1000	900
5000	200

The AD7798/AD7799 can be operated in unbuffered mode only when the gain equals 1 or 2. At higher gains, the buffer is automatically enabled. The absolute input voltage range in buffered mode is restricted to a range between GND + 100 mV and AV_{DD} − 100 mV. When the gain is set to 4 or higher, the in-amp is enabled. The absolute input voltage range when the in-amp is active is restricted to a range between GND + 300 mV and AV_{DD} − 1.1 V. Care must be taken in setting up the common-mode voltage so that these limits are not exceeded; otherwise, linearity and noise performance degrade.

The absolute input voltage in unbuffered mode includes the range between GND − 30 mV and AV_{DD} + 30 mV as a result of being unbuffered. The negative absolute input voltage limit allows the possibility of monitoring small true bipolar signals with respect to GND.

INSTRUMENTATION AMPLIFIER

When the gain equals 4 or higher, the output from the buffer is applied to the input of the on-chip instrumentation amplifier. This low noise in-amp means that signals of small amplitude can be gained within the AD7798/AD7799 while still maintaining excellent noise performance. For example, when the gain is set to 64 and the update rate equals 4.17 Hz, the rms noise is 27 nV typically for the AD7799, which is equivalent to 25.5 bits effective resolution, or 20 bits peak-to-peak resolution when V_{REF} = 5 V.

The AD7798/AD7799 can be programmed to have a gain of 1, 2, 4, 8, 16, 32, 64, or 128 using Bit G2 to Bit G0 in the configuration register. Therefore, with a 2.5 V reference, the unipolar ranges are from (0 mV to 19.53 mV) to (0 V to 2.5 V), and the bipolar ranges are from ±19.53 mV to ±2.5 V. When the in-amp is active (gain ≥ 4), the common-mode voltage (AIN(+) + AIN(−))/2 must be greater than or equal to 0.5 V.

If the AD7798/AD7799 operate with a reference that has a value equal to AV_{DD}, the analog input signal must be limited to 90% of V_{REF}/gain when the in-amp is active for correct operation.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog input to the AD7798/AD7799 can accept either unipolar or bipolar input voltage ranges. A bipolar input range does not imply that the parts can tolerate negative voltages with respect to system GND. Unipolar and bipolar signals on the AIN(+) input are referenced to the voltage on the AIN(−) input. For example, if AIN(−) is 2.5 V and the ADC is configured for unipolar mode and a gain of 1, the input voltage range on the AIN(+) pin is 2.5 V to 5 V.

If the ADC is configured for bipolar mode, the analog input range on the AIN(+) input is 0 V to 5 V. The bipolar/unipolar option is chosen by programming the U/$\overline{B}$ bit in the configuration register.

DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 00...00, a midscale voltage resulting in a code of 100...000, and a full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = (2^N \times AIN \times GAIN)/V_{REF}$$

When the ADC is configured for bipolar operation, the output code is offset binary, with a negative full-scale voltage resulting in a code of 000...000, a zero differential input voltage resulting in a code of 100...000, and a positive full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(AIN \times GAIN/V_{REF}) + 1]$$

where:
AIN is the analog input voltage.
N = 16 for the AD7798, and *N* = 24 for the AD7799.

BURNOUT CURRENTS

The AD7798/AD7799 each contain two 100 nA constant current generators—one sourcing current from AV_{DD} to AIN(+), and one sinking current from AIN(−) to GND. The currents are switched to the selected analog input pair. Both currents are either on or off, depending on the burnout current enable (BO) bit in the configuration register. These currents can be used to verify that an external transducer is still operational before attempting to take measurements on that channel. Once the burnout currents are turned on, they flow into the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If the resultant voltage measured is full scale, the user must determine why this is the case. A full-scale reading could mean that the front-end sensor is open circuit, that the front-end sensor is overloaded and is justified in outputting full scale, or that the reference is absent and, thus, clamping the data to all 1s.

When reading all 1s from the output, the user should check these three cases before making a judgment. If the voltage measured is 0 V, it might indicate that the transducer has short-circuited. For normal operation, these burnout currents are turned off by writing a 0 to the BO bit in the configuration register. The current sources work over the normal absolute input voltage range specifications with buffers on.

REFERENCE

The common-mode range for these differential inputs is from GND to AV_{DD}. The reference input is unbuffered; therefore, excessive resistance/capacitance source impedances introduce gain errors. The reference voltage REFIN (REFIN(+) − REFIN(−)) is 2.5 V nominal, but the AD7798/AD7799 are functional with reference voltages from 0.1 V to AV_{DD}. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source is removed because the application is ratiometric. If the AD7798/AD7799 are used in a nonratiometric application, a low noise reference should be used.

Recommended 2.5 V reference voltage sources for the AD7798/AD7799 include the ADR381 and ADR391, which are low noise, low power references. Also note that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors, depending on the output impedance of the source driving the reference inputs.

Reference voltage sources such as those recommended above (for example, ADR391) typically have low output impedances and are, therefore, tolerant to having decoupling capacitors on REFIN(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor means that the reference input sees a significant external source impedance. External decoupling on the REFIN pins is not recommended in this type of circuit configuration.

REFERENCE DETECT

The AD7798/AD7799 include on-chip circuitry to detect if there is a valid reference for conversions or calibrations. This feature is enabled when the REF_DET bit in the configuration register is set to 1. If the voltage between the REFIN(+) and REFIN(−) pins goes below 0.3 V, or either the REFIN(+) or REFIN(−) inputs are open circuit, the AD7798/AD7799 detect that there is no longer a valid reference. In this case, the NOREF bit of the status register is set to 1. If the AD7798/AD7799 are performing normal conversions and the NOREF bit becomes active, the conversion results revert to all 1s. Therefore, it is not necessary to continuously monitor the status of the NOREF bit when performing conversions. It is only necessary to verify its status if the conversion result read from the ADC data register is all 1s. If the AD7798/AD7799 are performing an offset of full-scale calibration and the NOREF bit becomes active, the updating of the respective calibration registers is inhibited to avoid loading incorrect coefficients to these registers, and the ERR bit in the status register is set. If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, the status of the ERR bit should be checked at the end of the calibration cycle.

RESET

The circuitry and serial interface of the AD7798/AD7799 can be reset by writing 32 consecutive 1s to the device. This resets the logic, the digital filter, and the analog modulator, and all on-chip registers are reset to their default values. A reset is automatically performed upon power-up. When a reset is initiated, the user must allow a period of 500 µs before accessing an on-chip register. A reset is useful if the serial interface becomes asynchronous due to noise on the SCLK line.

AV_{DD} MONITOR

Along with converting external voltages, the ADC can be used to monitor the voltage on the AV_{DD} pin. When Bits CH2 to CH0 equal 1, the voltage on the AV_{DD} pin is internally attenuated by 6, and the resulting voltage is applied to the Σ-Δ modulator using an internal 1.17 V reference for analog-to-digital conversion. This is useful because variations in the power supply voltage can be monitored.

CALIBRATION

The AD7798/AD7799 provide four calibration modes that can be programmed via the mode bits in the mode register. These are internal zero-scale calibration, internal full-scale calibration, system zero-scale calibration, and system full-scale calibration, which effectively reduce the offset error and full-scale error to the order of the noise. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register. The offset calibration coefficient is subtracted from the result prior to multiplication by the full-scale coefficient.

To start a calibration, write the relevant value to the MD2 to MD0 bits in the mode register. After the calibration is complete, the contents of the corresponding calibration registers are updated, the $\overline{RDY}$ bit in the status register is set, the DOUT/$\overline{RDY}$ pin goes low (if $\overline{CS}$ is low), and the AD7798/AD7799 revert to idle mode.

During an internal zero-scale or full-scale calibration, the respective zero-scale and full-scale input are automatically connected internally to the ADC input pins. A system calibration, however, expects the system zero-scale and system full-scale voltages to be applied to the ADC pins before the calibration mode is initiated. In this way, external ADC errors are removed.

From an operational point of view, a calibration should be treated like an ADC conversion. A zero-scale calibration (if required) should always be performed before a full-scale calibration. System software should monitor the $\overline{RDY}$ bit in the status register or the DOUT/$\overline{RDY}$ pin to determine the end of calibration via a polling sequence or an interrupt-driven routine.

Both an internal offset calibration and system offset calibration take two conversion cycles. An internal offset calibration is not needed because the ADC itself removes the offset continuously.

To perform an internal full-scale calibration, a full-scale input voltage is automatically connected to the selected analog input for this calibration. When the gain equals 1, a calibration takes two conversion cycles to complete. For higher gains, four conversion cycles are required to perform the full-scale calibration. DOUT/$\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. Internal full-scale calibrations cannot be performed when the gain equals 128. A factory calibration is performed at this gain setting, and the factory value is automatically loaded into the full-scale register when the gain is set to 128. With this gain setting, a system full-scale calibration can be performed. A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error.

An internal full-scale calibration can only be performed at specified update rates. For gains of 1, 2, and 4, an internal full-scale calibration can be performed at any update rate. However, for higher gains, internal full-scale calibrations must be performed when the update rate is less than or equal to 16.7 Hz, 33.2 Hz, or 50 Hz. Because the full-scale error does not vary with the update rate, a calibration at one update rate is valid for all update rates (assuming the gain or reference source is not changed).

A system full-scale calibration takes two conversion cycles to complete, irrespective of the gain setting. A system full-scale calibration can be performed at all gains and update rates. If system offset calibrations are performed along with system full-scale calibrations, the offset calibration should be performed before the system full-scale calibration is initiated.

GROUNDING AND LAYOUT

Because the analog inputs and reference inputs of the ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the parts removes common-mode noise on these inputs. The digital filter provides rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7798/AD7799 are more immune to noise interference than conventional high resolution converters. However, because the resolution of the AD7798/AD7799 is so high and the noise levels from the AD7798/AD7799 are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7798/AD7799 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it provides the best shielding.

It is recommended that the GND pin be tied to the AGND plane of the system. In any layout, it is important that the user keep in mind the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The ground planes should be allowed to run under the AD7798/AD7799 to prevent noise coupling. The power supply lines to the AD7798/AD7799 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clock signals, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique works best, but it is not always possible to use this method with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. AV_{DD} should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to GND. DV_{DD} should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to the system's DGND plane, with the system's AGND-to-DGND connection being close to the AD7798/AD7799. To achieve the best from these decoupling components, they should be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF ceramic capacitors to DGND.

APPLICATIONS INFORMATION

The AD7798/AD7799 provide a low cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a Σ-Δ architecture, the parts are more immune to noisy environments, making them ideal for use in sensor measurement and industrial and process-control applications.

WEIGH SCALES

Figure 19 shows the AD7798/AD7799 being used in a weigh scale application. The load cell is arranged in a bridge network and gives a differential output voltage between its OUT+ and OUT– terminals. Assuming a 5 V excitation voltage, the full-scale output range from the transducer is 10 mV when the sensitivity is 2 mV/V. The excitation voltage for the bridge can be used to directly provide the reference for the ADC because the reference input range includes the supply voltage.

A second advantage of using the AD7798/AD7799 in transducer-based applications is that the low-side power switch can be fully utilized in low power applications. The low-side power switch is connected in series with the cold side of the bridge. In normal operation, the switch is closed and measurements can be taken. In applications where power is of concern, the AD7798/AD7799 can be placed in standby mode, thus significantly reducing the power consumed in the application. In addition, the low-side power switch can be opened while in standby mode, thus avoiding unnecessary power consumption by the front-end transducer. When the part is taken out of standby mode and the low-side power switch is closed, the user should ensure that the front end circuitry is fully settled before attempting a read from the AD7798/AD7799.

In Figure 19, temperature compensation is performed using a thermistor. In addition, the reference voltage for the temperature measurement is derived from a precision resistor in series with the thermistor. This allows a ratiometric measurement—that is, the ratio of the precision reference resistance to the thermistor resistance is measured; therefore, variations of the reference voltage do not affect the measurement.

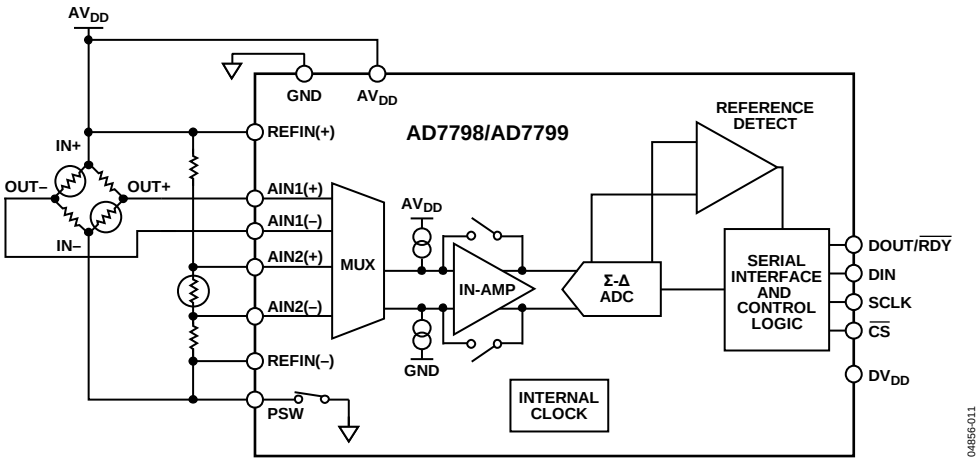

Figure 19. Weigh Scales Using the AD7798/AD7799

OUTLINE DIMENSIONS

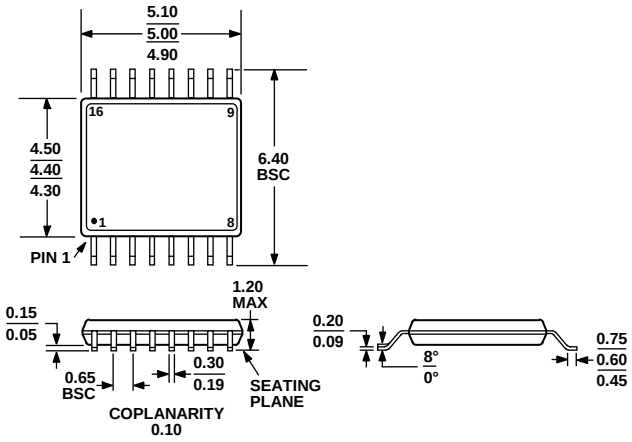

Figure 20. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7798BRUZ	–40°C to +105°C	16-Lead TSSOP	RU-16
AD7798BRUZ-REEL	–40°C to +105°C	16-Lead TSSOP	RU-16
EVAL-AD7798EBZ		Evaluation Board	
AD7799BRU	–40°C to +105°C	16-Lead TSSOP	RU-16
AD7799BRU-REEL	–40°C to +105°C	16-Lead TSSOP	RU-16
AD7799BRUZ	–40°C to +105°C	16-Lead TSSOP	RU-16
AD7799BRUZ-REEL	–40°C to +105°C	16-Lead TSSOP	RU-16
EVAL-AD7799EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES