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REVISION HISTORY

1/09—Rev. A to Rev. B

Updated Format ... Universal
Changes to Table 1 ... 3
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 15

5/87—Rev. 0 to Rev. A

SPECIFICATIONS

V_{DD} = 11.4 V to 15.75 V[1], V_{REF} = 10 V; V_{PIN3} = V_{PIN4} = 0 V, V_{SS} = −300 mV; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[2]	A, J Versions	B, K Versions	S Version	T Version	Unit	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Over temperature
Full-Scale Error						Measured using internal R_{FB} DAC
+25°C	±4	±4	±4	±4	LSB max	Registers loaded with all 1s
T_{MIN} to T_{MAX}	±8	±5	±10	±6	LSB max	
Gain Temperature Coefficient[3]; ΔGain/ΔTemperature	±2	±2	±2	±2	ppm/°C typ	
Output Leakage Current I_{OUT} (Pin 3)						
25°C	±5	±5	±5	±5	nA max	All digital inputs 0 V
T_{MIN} to T_{MAX}	±10	±10	±20	±20	nA max	V_{SS} = −300 mV
T_{MIN} to T_{MAX}	±25	±25	±150	±150	nA max	V_{SS} = 0 V
REFERENCE INPUT						
Input Resistance (Pin 1)	3.5	3.5	3.5	3.5	kΩ min	Typical input resistance = 6 kΩ
	10	10	10	10	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
25°C	±1	±1	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
T_{MIN} to T_{MAX}	±10	±10	±10	±10	µA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V min/V max	Specification guaranteed over this range
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/ mV max	Specification guaranteed over this range
I_{DD}	4	4	4	4	mA max	All digital inputs are V_{IL} or V_{IH}
	500	500	500	500	µA max	All digital inputs are 0 V or V_{DD}

[1] Specifications are guaranteed for a V_{DD} of 11.4 V to 15.75 V. At V_{DD} = 5 V, the device is fully functional with degraded specifications.
[2] Temperature range as follows: J, K Versions: 0°C to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C
[3] Sample tested to ensure compliance.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test. V_{DD} = 11.4 V to 15.75 V, V_{REF} = 10 V, V_{PIN3} = V_{PIN4} = 0 V, V_{SS} = 0 V or −300 mV, output amplifier is AD711 except where noted.

Table 2.

Parameter	T_A = 25°C T_A = T_{MIN}, T_{MAX}		Unit	Test Conditions/Comments
Output Current Settling Time	1.5		µs max	To 0.003% of full-scale range I_{OUT} load= 100 Ω, C_{EXT} = 13 pF DAC register alternately loaded with all 1s and all 0s; typical value of settling time is 0.8 µs
Digital-to-Analog Glitch Impulse	20		nV-sec typ	Measured with V_{REF} = 0 V. I_{OUT} load = 100 Ω, C_{EXT} = 13 pF; DAC register alternately loaded with all 1s and all 0s
Multiplying Feedthrough Error	3	5	mV p-p typ	V_{REF} = ±10 V, 10 kHz sine wave DAC Register loaded with all 0s
Power Supply Rejection				
ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 3)	260	260	pF max	DAC register loaded with all 1s
C_{OUT} (Pin 3)	130	130	pF max	DAC register loaded with all 0s
Output Noise Voltage Density				
(10 Hz to 100 kHz)	15		nV√Hz typ	Measured between R_{FB} and I_{OUT}

TIMING CHARACTERISTICS

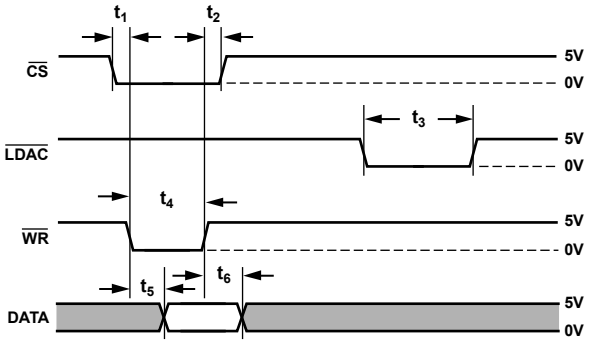
V_{DD} = 11.4 V to 15.75 V, V_{REF} = 10 V, V_{PIN3} = V_{PIN4} = 0 V, V_{SS} = 0 V or −300 mV. All specifications T_{MIN} to T_{MAX} unless otherwise noted. See Figure 2 for a timing diagram.

Table 3.

Parameter[1]	Limit at T_A = +25°C	Limit at T_A = 0°C to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Unit	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ setup time
t_2	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ hold time
t_3	170	200	240	ns min	$\overline{LDAC}$ pulse width
t_4	170	200	240	ns min	Write pulse width
t_5	140	160	180	ns min	Data setup time
t_6	20	20	30	ns min	Data hold time

[1] Temperature range as follows: J, K Versions: 0°C to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

TIMING DIAGRAM



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURES FROM 10% TO 90% OF 5V, $t_R = t_F = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.
3. IF $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

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Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C unless, otherwise stated.

Table 4.

Parameter	Rating
V_{DD} (Pin 23) to DGND	−0.3 V, +17 V
V_{SS} (Pin 24) to AGND	−15 V, +0.3 V
V_{REF} (Pin 1) to AGND	±25 V
V_{RFB} (Pin 2) to AGND	±25 V
Digital Input Voltage (Pins 6 to 22) to DGND	−0.3 V, V_{DD} +0.3 V
V_{PIN3} to DGND	−0.3 V, V_{DD} +0.3 V
AGND to DGND	−0.3 V, V_{DD} +0.3 V
Power Dissipation (Any Package)	
To 75°C	1000 mW
Derates Above 75°C	10 mW/°C
Operating Temperature Range	
Commercial (J, K Versions)	0°C to +70°C
Industrial (A, B Versions)	−25°C to +85°C
Extended (S, T Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

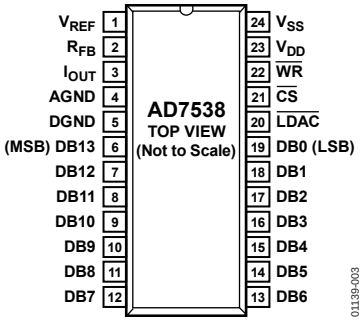


Figure 3. Pin Configuration

Table 5. Pin Function Description

Pin No.	Mnemonic	Description			
1	V_{REF}	Voltage Reference.			
2	R_{FB}	Feedback Resistor. Used to close the loop around an external op amp.			
3	I_{OUT}	Current Output Terminal.			
4	AGND	Analog Ground			
5	DGND	Digital Ground.			
6 to 19	DB13 to DB0	Data Inputs. Bit DB13 (MSB) to Bit DB0 (LSB).			
20	$\overline{LDAC}$	Chip Select Input. Active low.			
21	$\overline{CS}$	Asynchronous Load DAC Input. Active low.			
22	$\overline{WR}$	Write Input. Active low.			
		$\overline{CS}$	**$\overline{LDAC}$**	**$\overline{WR}$**	**Operation**
		0	1	0	Load input register.
		1	0	X[1]	Load DAC register from input register.
		0	0	0	Input and DAC registers are transparent.
		1	1	X[1]	No operation.
		X[1]	1	1	No operation.
23	V_{DD}	+12 V to +15 V Supply Input.			
24	V_{SS}	Bias pin for high temperature low leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figure 6 and Figure 8 for recommended circuitry.			

[1] X = don't care.

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in least significant bits or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum over the operating temperature range ensures monotonicity.

Gain Error
Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after the offset error has been adjusted out and is expressed in least significant bits. Gain error is adjustable to zero with an external potentiometer.

Digital-To-Analog Glitch Impulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state is called digital-to-analog glitch impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. It is measured with V_{REF} = AGND.

Output Capacitance
This is the capacitance from I_{OUT} to AGND.

Output Leakage Current
Output leakage current is current which appears at I_{OUT} with the DAC register loaded to all 0s.

Multiplying Feedthrough Error
This is the ac error due to capacitive feedthrough from the V_{REF} terminal to I_{OUT} with the DAC register loaded to all zeros.

DAC SECTION

Figure 4 shows a simplified circuit diagram for the AD7538 DAC section. The three MSBs of the 14-bit data word are decoded to drive the seven switches (A to G). The 11 LSBs of the data word consist of an R-2R ladder operated in a current steering configuration.

The R-2R ladder current is ⅛ of the total reference input current. ⅞ current flows in the parallel ladder structure.

Switch A to Switch G steer equally weighted currents between I_{OUT} and AGND.

Because the input resistance at V_{REF} is constant, it may be driven by a voltage source or a current source of positive or negative polarity.

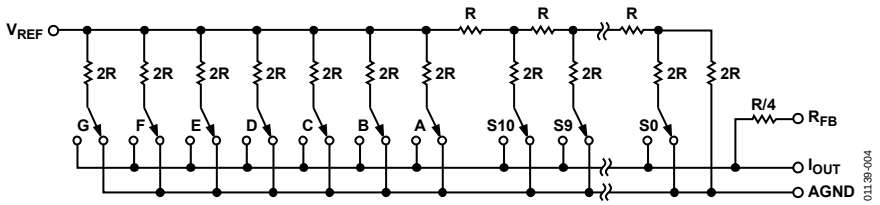


Figure 4. Simplified Circuit Diagram for the AD7538 DAC Section

CIRCUIT INFORMATION

EQUIVALENT CIRCUIT ANALYSIS

Figure 5 shows an equivalent circuit for the analog section of the AD7538 DAC. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The R_O resistor denotes the equivalent output resistance of the DAC, which varies with input code. C_{OUT} is the capacitance due to the current steering switches and varies from about 90 pF to 180 pF (typical values) depending upon the digital input. g(V_{REF}, N) is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the transfer function of the DAC ladder, N.

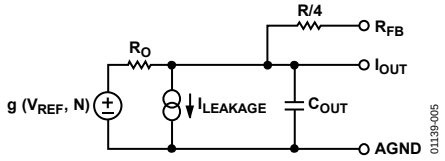


Figure 5. AD7538 Equivalent Analog Output Circuit

DIGITAL SECTION

The digital inputs are designed to be both TTL and 5 V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1 nA. To minimize power supply currents, it is recommended that the digital input voltages be driven as close as possible to 0 V and 5 V logic levels.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 6 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 6 is given in Table 6.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high-speed op amps are used.

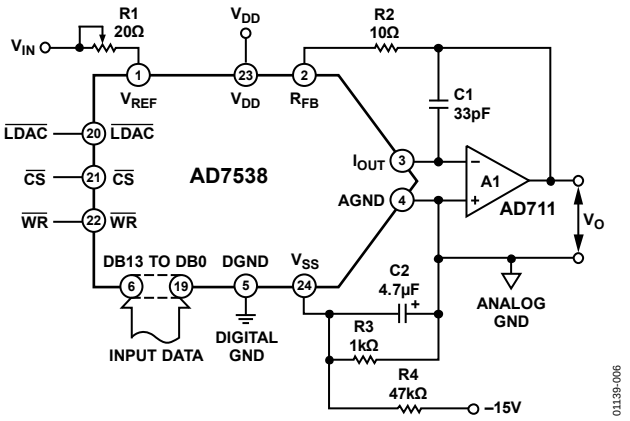


Figure 6. Unipolar Binary Operation

Table 6. Unipolar Binary Code Table

Binary Number In DAC Register MSB LSB	Analog Output, V_{OUT}
11 1111 1111 1111	$-V_{IN}$(16,383/16,384)
10 0000 0000 0000	$-V_{IN}$(8192/16,384) = $-½V_{IN}$
00 0000 0000 0001	$-V_{IN}$(1/16,384)
00 0000 0000 0000	0 V

For zero offset adjustment, the DAC register is loaded with all 0s and amplifier offset (V_{OS}) adjusted so that V_{OUT} is 0 V. Adjusting V_{OUT} to 0 V is not necessary in many applications, but it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) to maintain specified DAC accuracy (see the Application Hints section).

Full-scale trimming is accomplished by loading the DAC register with all 1s and adjusting R1 so that $V_{OUTA} = -V_{IN}$ (16,383/16,384). For high temperature operation, resistors and potentiometers should have a low temperature coefficient. In many applications, because of the excellent gain TC and gain error specifications of the AD7538, gain error trimming is not necessary. In fixed reference applications, full scale can also be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 8. Offset binary coding is used. The code table for Figure 8 is given in Table 7.

With the DAC loaded to 10 0000 0000 0000, adjust R1 for V_O = 0 V. Alternatively, one can omit R1 and R2 and adjust the ratio of R5 and R6 for V_O = 0 V. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R7.

The values given for R1, R2 are the minimum necessary to calibrate the system for Resistors R5, R6, R7 ratio matched to 0.1%. System linearity error is independent of resistor ratio matching and is affected by DAC linearity error only.

When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

LOW LEAKAGE CONFIGURATION

For CMOS multiplying DAC, as the device is operated at higher temperatures, the output leakage current increases. For a 14-bit resolution system, this can be a significant source of error. The AD7538 features a leakage reduction configuration to keep the leakage current low over an extended temperature range. One may operate the device with or without this configuration. If V_{SS} (Pin 24) is tied to AGND then the DAC exhibits normal output leakage currents at high temperatures. To use the low leakage facility, V_{SS} should be tied to a voltage of approximately −0.3 V as in Figure 6 and Figure 8. A simple resistor divider (R3, R4) produces approximately −300 mV from −15 V. The C2 capacitor in parallel with R3 is an integral part of the low leakage configuration and must be 4.7 µF or greater. Figure 7 is a plot of leakage current vs. temperature for both conditions. It clearly shows the improvement gained by using the low leakage configuration.

Table 7. Bipolar Code Table for the Offset Binary Circuit of Figure 8

Binary Number In DAC Register MSB LSB	Analog Output V_{OUT}
11 1111 1111 1111	$+V_{IN}$(8191/8192)
10 0000 0000 0001	$+V_{IN}$(1/8192)
10 0000 0000 0000	0 V
01 1111 1111 1111	$-V_{IN}$(1/8192)
00 0000 0000 0000	$-V_{IN}$(8191/8192)

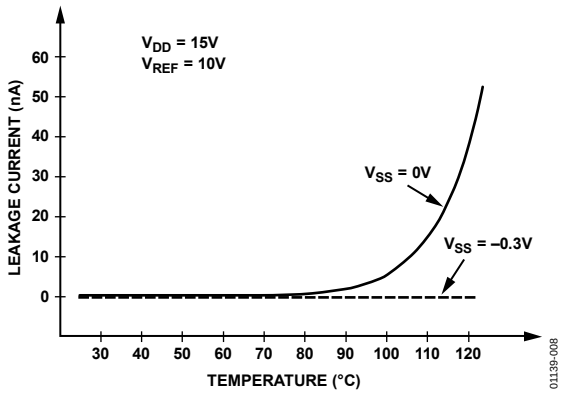


Figure 7. Graph of Typical Leakage Current vs. Temperature for AD7538

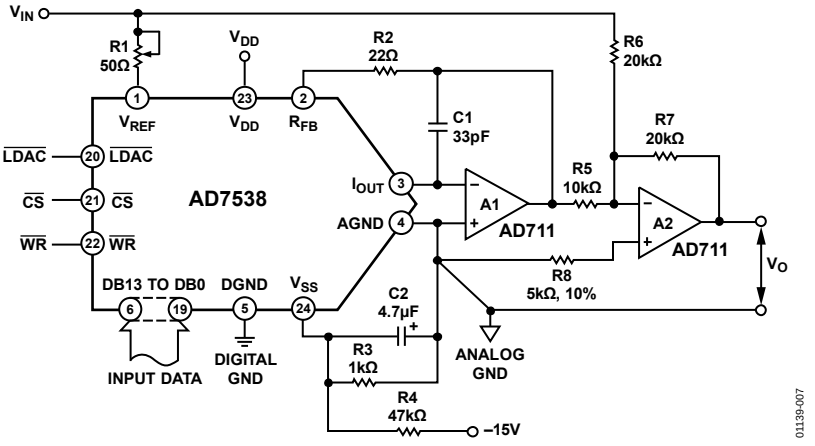


Figure 8. Bipolar Operation

PROGRAMMABLE GAIN AMPLIFIER

The circuit shown in Figure 9 provides a programmable gain amplifier (PGA). In it the DAC behaves as a programmable resistance and thus allows the circuit gain to be digitally controlled.

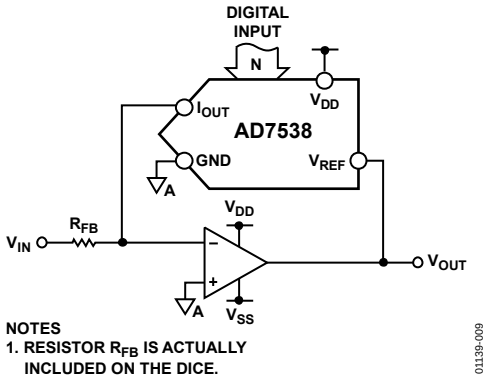


Figure 9. Programmable Gain Amplifier (PGA)

The transfer function of Figure 9 is:

$$Gain = \frac{V_{OUT}}{V_{IN}} = -\frac{R_{EQ}}{R_{FB}} \quad (1)$$

R_{EQ} is the equivalent transfer impedance of the DAC from the V_{REF} pin to the I_{OUT} pin and can be expressed as

$$R_{EQ} = \frac{2^n R_{IN}}{N} \quad (2)$$

where:
n is the resolution of the DAC.
N is the DAC input code in decimal.
R_{IN} is the constant input impedance of the DAC ($R_{IN} = R_{LAD}$).

Substituting this expression into Equation 1 and assuming zero gain error for the DAC ($R_{IN} = R_{FB}$), the transfer function simplifies to

$$\frac{V_{OUT}}{V_{IN}} = -\frac{2^n}{N} \quad (3)$$

The ratio $N/2^n$ is commonly represented by the term, D, and, as such, is the fractional representation of the digital input word.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{-2^n}{N} = \frac{-1}{D} \quad (4)$$

Equation 4 indicates that the gain of the circuit can be varied from 16,384 down to unity (actually 16,384/16,383) in 16,383 steps. The all 0s code is never applied. This avoids an open-loop condition thereby saturating the amplifier. With the all 0s code excluded there remains $(2^n - 1)$ possible input codes allowing a choice of $(2^n - 1)$ output levels. In decibels the dynamic range is

$$20 \log_{10} \frac{V_{OUT}}{V_{IN}} = 20 \log_{10} (2^n - 1) = 84 \text{ dB}$$

APPLICATION HINTS

OUTPUT OFFSET

CMOS DACs in circuits such as Figure 6 and Figure 8 exhibit a code dependent output resistance, which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the DAC nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. To maintain specified accuracy with V_{REF} at 10 V, it is recommended that V_{OS} be no greater than 0.25 mV, or (25×10^{-6}) (V_{REF}), over the temperature range of operation. The AD711 is a suitable op amp. The op amp has a wide bandwidth and high slew rate and is recommended for ac and other applications requiring fast settling.

GENERAL GROUND MANAGEMENT

Because the AD7538 is specified for high accuracy, it is important to use a proper grounding technique. AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7538. In more complex systems where the AGND and DGND intertie on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7538 AGND and DGND pins (1N914 or equivalent).

MICROPROCESSOR INTERFACING

The AD7538 is designed for easy interfacing to 16-bit microprocessors and can be treated as a memory mapped peripheral. This reduces the amount of external logic needed for interfacing to a minimal.

AD7538-TO-8086 INTERFACE

Figure 10 shows the 8086 processor interface to a single device. In this setup, the double buffering feature (using $\overline{\text{LDAC}}$) of the DAC is not used. The 14-bit word is written to the DAC in one MOVE instruction and the analog output responds immediately.

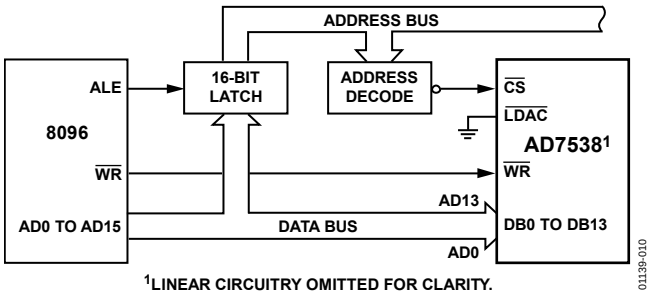


Figure 10. AD7538-to-8086 Interface Circuit

In a multiple DAC system, the double buffering of the AD7538 allows the user to simultaneously update all DACs. In Figure 11, a 14-bit word is loaded to the input registers of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (that is, $\overline{\text{LDAC}}$) is brought low, updating all the DACs simultaneously.

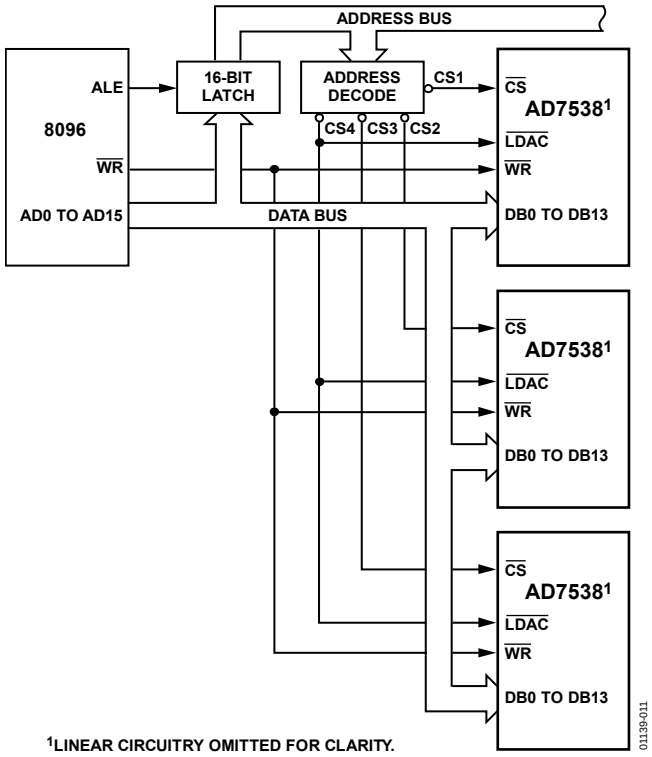


Figure 11. AD7538-to-8086 Interface: Multiple DAC System

AD7538-TO-MC68000 INTERFACE

Figure 12 shows the MC68000 processor interface to a single device. In this setup, the double buffering feature of the DAC is not used and the appropriate data is written into the DAC in one MOVE instruction.

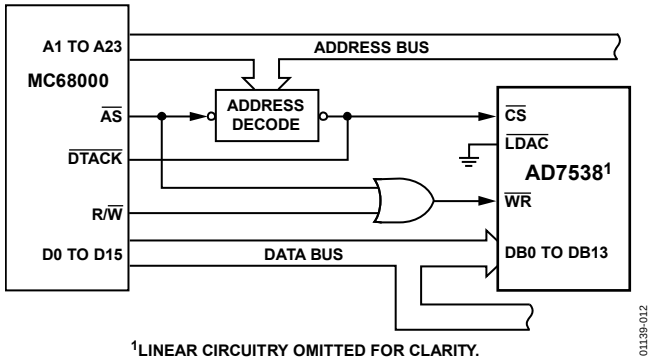


Figure 12. AD7538-to-MC68000 Interface

DIGITAL FEEDTHROUGH

The digital inputs to the AD7538 are directly connected to the microprocessor bus in the preceding interface configurations. These inputs are constantly changing even when the device is not selected. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this digital feedthrough isolate the DAC from the noise source. Figure 13 shows an interface circuit, which uses this technique. All data inputs are latched from the bus by the $\overline{CS}$ signal. One may also use other means, such as peripheral interface devices, to reduce the digital feedthrough.

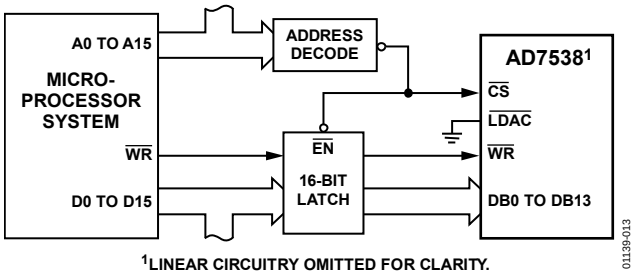
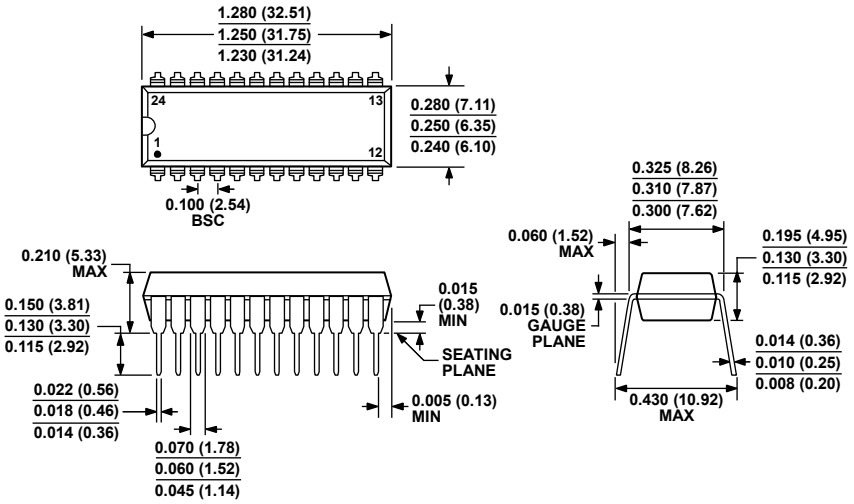


Figure 13. AD7538 Interface Circuit Using Latches to Minimize Digital Feedthrough

OUTLINE DIMENSIONS

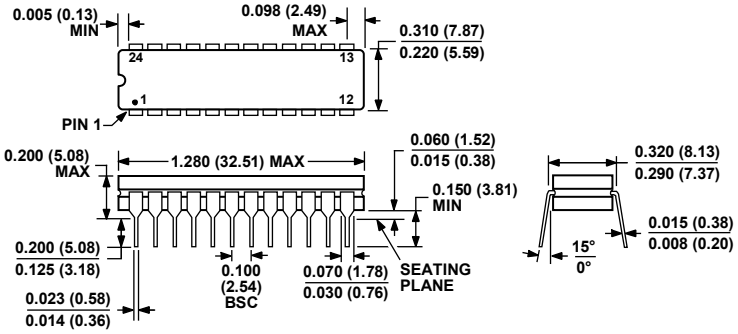


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

071006-A

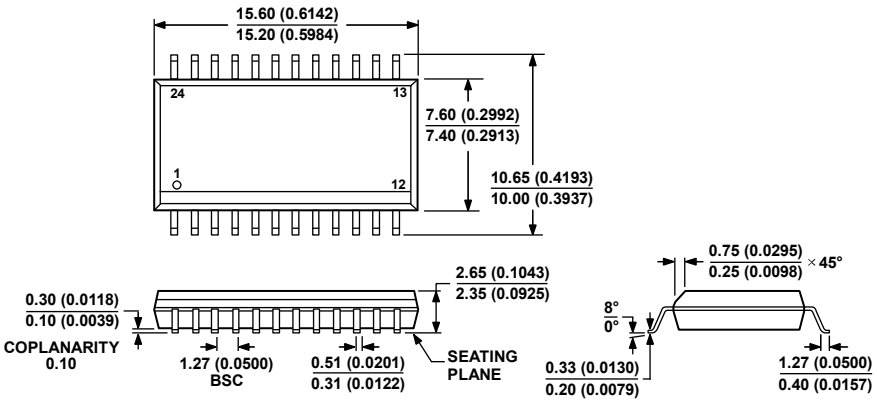
Figure 14. 24-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-24-1)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

100808-A

Figure 15. 24-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-24-1)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AD
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060706-A

Figure 16. 24-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-24)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Full-Scale Error	Package Description	Package Option
AD7538JN	0°C to +70°C	±2 LSB	±8 LSB	24-Lead PDIP	N-24-1
AD7538JNZ[1]	0°C to +70°C	±2 LSB	±8 LSB	24-Lead PDIP	N-24-1
AD7538KN	0°C to +70°C	±1 LSB	±5 LSB	24-Lead PDIP	N-24-1
AD7538KNZ[1]	0°C to +70°C	±1 LSB	±5 LSB	24-Lead PDIP	N-24-1
AD7538JR	0°C to +70°C	±2 LSB	±8 LSB	24-Lead SOIC_W	RW-24
AD7538JR-REEL	0°C to +70°C	±2 LSB	±8 LSB	24-Lead SOIC_W	RW-24
AD7538JRZ[1]	0°C to +70°C	±2 LSB	±8 LSB	24-Lead SOIC_W	RW-24
AD7538JRZ-REEL[1]	0°C to +70°C	±2 LSB	±8 LSB	24-Lead SOIC_W	RW-24
AD7538KR	0°C to +70°C	±1 LSB	±5 LSB	24-Lead SOIC_W	RW-24
AD7538KR-REEL	0°C to +70°C	±1 LSB	±5 LSB	24-Lead SOIC_W	RW-24
AD7538KRZ[1]	0°C to +70°C	±1 LSB	±5 LSB	24-Lead SOIC_W	RW-24
AD7538KRZ-REEL[1]	0°C to +70°C	±1 LSB	±5 LSB	24-Lead SOIC_W	RW-24
AD7538AQ	−25°C to +85°C	±2 LSB	±8 LSB	24-Lead CERDIP	Q-24-1
AD7538BQ	−25°C to +85°C	±1 LSB	±5 LSB	24-Lead CERDIP	Q-24-1
AD7538SQ	−55°C to +125°C	±2 LSB	±10 LSB	24-Lead CERDIP	Q-24-1
AD7538TQ	−55°C to +125°C	±1 LSB	±6 LSB	24-Lead CERDIP	Q-24-1

[1] Z = RoHS Compliant Part.

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