

# AD558—SPECIFICATIONS (@ T<sub>A</sub> = +25°C, V<sub>CC</sub> = +5 V to +15 V unless otherwise noted)

| Model  | AD558J   |     |     | AD558K  |     |     | AD558S <sup>1</sup>   |     |     | AD558T <sup>1</sup>   |     |     | Units                                    |
|--|--|-----|-----|---|-----|-----|---|-----|-----|---|-----|-----|--|
|  | Min  | Typ | Max | Min   | Typ | Max | Min   | Typ | Max | Min   | Typ | Max |  |
| RESOLUTION   | 8  |     |     | 8   |     |     | 8   |     |     | 8   |     |     | Bits                                     |
| RELATIVE ACCURACY <sup>2</sup><br>0°C to +70°C<br>–55°C to +125°C  | ±1/2   |     |     | ±1/4  |     |     | ±1/2<br>±3/4  |     |     | ±1/4<br>±3/8  |     |     | LSB<br>LSB                               |
| OUTPUT<br>Ranges <sup>3</sup><br><br>Current Source<br>Sink  | 0 to +2.56<br>0 to +10<br><br>+5<br>Internal Passive<br>Pull-Down to Ground <sup>4</sup> |     |     | 0 to +2.56<br>0 to +10<br><br>+5<br>Internal Passive<br>Pull-Down to Ground |     |     | 0 to +2.56<br>0 to +10<br><br>+5<br>Internal Passive<br>Pull-Down to Ground |     |     | 0 to +2.56<br>0 to +10<br><br>+5<br>Internal Passive<br>Pull-Down to Ground |     |     | V<br>V<br>mA                             |
| OUTPUT SETTLING TIME <sup>5</sup><br>0 to 2.56 Volt Range<br>0 to 10 Volt Range <sup>4</sup>   | 0.8 1.5<br>2.0 3.0   |     |     | 0.8 1.5<br>2.0 3.0  |     |     | 0.8 1.5<br>2.0 3.0  |     |     | 0.8 1.5<br>2.0 3.0  |     |     | μs<br>μs                                 |
| FULL-SCALE ACCURACY <sup>6</sup><br>@ 25°C<br>T <sub>MIN</sub> to T <sub>MAX</sub>   | ±1.5<br>±2.5   |     |     | ±0.5<br>±1  |     |     | ±1.5<br>±2.5  |     |     | ±0.5<br>±1  |     |     | LSB<br>LSB                               |
| ZERO ERROR<br>@ 25°C<br>T <sub>MIN</sub> to T <sub>MAX</sub>   | ±1<br>±2   |     |     | ±1/2<br>±1  |     |     | ±1<br>±2  |     |     | ±1/2<br>±1  |     |     | LSB<br>LSB                               |
| MONOTONICITY <sup>7</sup><br>T <sub>MIN</sub> to T <sub>MAX</sub>  | Guaranteed   |     |     | Guaranteed  |     |     | Guaranteed  |     |     | Guaranteed  |     |     |  |
| DIGITAL INPUTS<br>T <sub>MIN</sub> to T <sub>MAX</sub><br>Input Current<br>Data Inputs, Voltage<br>Bit On-Logic “1”<br>Bit On-Logic “0”<br>Control Inputs, Voltage<br>On-Logic “1”<br>On-Logic “0”<br>Input Capacitance                                | ±100<br><br>2.0<br>0<br><br>2.0<br>0<br><br>4  |     |     | ±100<br><br>2.0<br>0<br><br>2.0<br>0<br><br>4                               |     |     | ±100<br><br>2.0<br>0<br><br>2.0<br>0<br><br>4                               |     |     | 100<br><br>2.0<br>0<br><br>2.0<br>0<br><br>4                                |     |     | μA<br><br>V<br>V<br><br>V<br>V<br><br>pF |
| TIMING <sup>8</sup><br>t <sub>W</sub> Strobe Pulse Width<br>T <sub>MIN</sub> to T <sub>MAX</sub><br>t <sub>DH</sub> Data Hold Time<br>T <sub>MIN</sub> to T <sub>MAX</sub><br>t <sub>DS</sub> Data Set-Up Time<br>T <sub>MIN</sub> to T <sub>MAX</sub> | 200<br>270<br>10<br>10<br>200<br>270   |     |     | 200<br>270<br>10<br>10<br>200<br>270  |     |     | 200<br>270<br>10<br>10<br>200<br>270  |     |     | 200<br>270<br>10<br>10<br>200<br>270  |     |     | ns<br>ns<br>ns<br>ns<br>ns<br>ns         |
| POWER SUPPLY<br>Operating Voltage Range (V <sub>CC</sub> )<br>2.56 Volt Range<br>10 Volt Range<br>Current (I <sub>CC</sub> )<br>Rejection Ratio  | +4.5<br>+11.4<br>15<br>25<br>0.03  |     |     | +4.5<br>+11.4<br>15<br>25<br>0.03   |     |     | +4.5<br>+11.4<br>15<br>25<br>0.03   |     |     | +4.5<br>+11.4<br>15<br>25<br>0.03   |     |     | V<br>V<br>mA<br>%/%                      |
| POWER DISSIPATION, V <sub>CC</sub> = 5 V<br>V <sub>CC</sub> = 15 V   | 75 125<br>225 375  |     |     | 75 125<br>225 375   |     |     | 75 125<br>225 375   |     |     | 75 125<br>225 375   |     |     | mW<br>mW                                 |
| OPERATING TEMPERATURE RANGE  | 0 +70  |     |     | 0 +70   |     |     | –55 +125  |     |     | –55 +125  |     |     | °C                                       |

## NOTES

<sup>1</sup>The AD558 S & T grades are available processed and screened to MIL-STD-883 Class B. Consult Analog Devices' Military Databook for details.

<sup>2</sup>Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the offset to the full scale of the device. See “Measuring Offset Error”.

<sup>3</sup>Operation of the 0 volt to 10 volt output range requires a minimum supply voltage of +11.4 volts.

<sup>4</sup>Passive pull-down resistance is 2 kΩ for 2.56 volt range, 10 kΩ for 10 volt range.

<sup>5</sup>Settling time is specified for a positive-going full-scale step to ±1/2 LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

<sup>6</sup>The full range output voltage for the 2.56 range is 2.55 V and is guaranteed with a +5 V supply, for the 10 V range, it is 9.960 V guaranteed with a +15 V supply.

<sup>7</sup>A monotonic converter has a maximum differential linearity error of ±1 LSB.

<sup>8</sup>See Figure 7.

Specifications shown in **boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

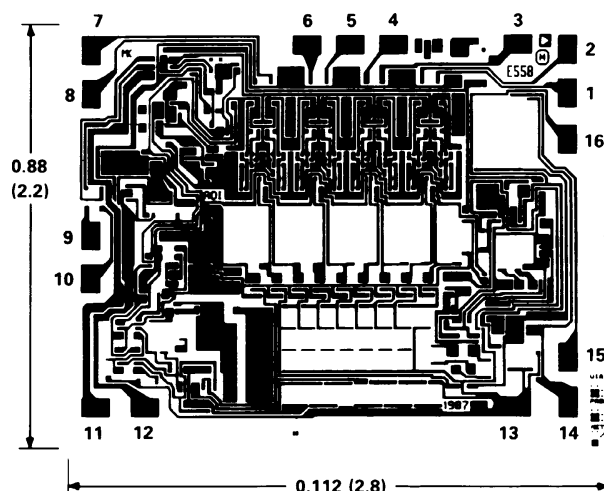
## ABSOLUTE MAXIMUM RATINGS\*

|                                      |   |
|--------------------------------------|---|
| $V_{CC}$ to Ground                   | 0 V to +18 V  |
| Digital Inputs (Pins 1–10)           | 0 V to +7.0 V   |
| $V_{OUT}$                            | Indefinite Short to Ground<br>Momentary Short to $V_{CC}$ |
| Power Dissipation                    | 450 mW  |
| Storage Temperature Range            |   |
| N/P (Plastic) Packages               | –25°C to +100°C   |
| D (Ceramic) Package                  | –55°C to +150°C   |
| Lead Temperature (soldering, 10 sec) | +300°C  |
| Thermal Resistance                   |   |
| Junction to Ambient/Junction to Case |   |
| D (Ceramic) Package                  | 100°C/W/30°C/W  |
| N/P (Plastic) Packages               | 140°C/W/55°C/W  |

\*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## AD558 METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



## Bond Pad Coordinates

| Pad No. | Pad Name        | X Coordinate | Y Coordinate |
|---------|-----------------|--------------|--------------|
| 1       | DB0             | –702         | 1265         |
| 2       | DB1             | –927         | 1265         |
| 3       | DB2             | –957         | 1004         |
| 4       | DB3             | –957         | 347          |
| 5       | DB4             | –957         | 115          |
| 6       | DB5             | –957         | –111         |
| 7       | DB6             | –927         | –1248        |
| 8       | DB7             | –702         | –1248        |
| 9       | $\overline{CE}$ | 47           | –1248        |
| 10      | $\overline{CS}$ | 272          | –1248        |
| 11      | $V_{CC}$        | 957          | –1225        |
| 12      | GND             | 957          | –965         |
| 13      | GND             | 946          | 970          |
| 14      | $V_{OUT}SELECT$ | 923          | 1265         |
| 15      | $V_{OUT}SENSE$  | 689          | 1265         |
| 16      | $V_{OUT}$       | –461         | 1265         |

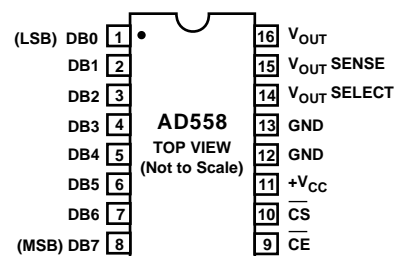


Figure 1a. AD558 Pin Configuration (DIP)

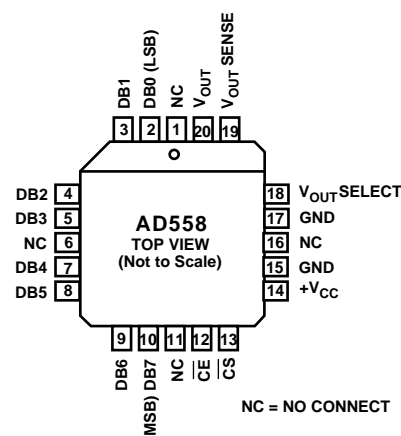


Figure 1b. AD558 Pin Configuration (PLCC and LCC)

AD558

CIRCUIT DESCRIPTION

The AD558 consists of four major functional blocks, fabricated on a single monolithic chip (see Figure 2). The main D-to-A converter section uses eight equally-weighted laser-trimmed current sources switched into a silicon-chromium thin-film R/2R resistor ladder network to give a direct but unbuffered 0 mV to 400 mV output range. The transistors that form the DAC switches are PNPs; this allows direct positive-voltage logic interface and a zero-based output range.

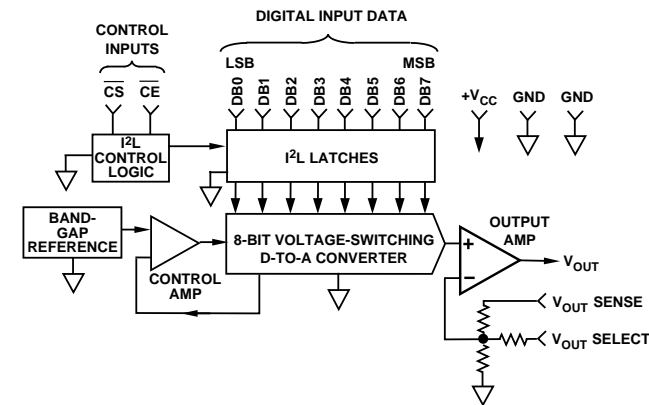


Figure 2. AD558 Functional Block Diagram

The high speed output buffer amplifier is operated in the non-inverting mode with gain determined by the user-connections at the output range select pin. The gain-setting application resistors are thin-film laser-trimmed to match and track the DAC resistors and to assure precise initial calibration of the two output ranges, 0 V to 2.56 V and 0 V to 10 V. The amplifier output stage is an NPN transistor with passive pull-down for zero-based output capability with a single power supply. The internal precision voltage reference is of the patented bandgap type. This design produces a reference voltage of 1.2 volts and thus, unlike 6.3 volt temperature compensated Zeners, may be operated from a single, low voltage logic power supply. The microprocessor interface logic consists of an 8-bit data latch and control circuitry. Low power, small geometry and high speed are advantages of the I²L design as applied to this section. I²L is bipolar process compatible so that the performance of the analog sections need not be compromised to provide on-chip logic capabilities. The control logic allows the latches to be operated from a decoded microprocessor address and write signal. If the application does not involve a  $\mu$ P or data bus, wiring CS and CE to ground renders the latches “transparent” for direct DAC access.

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD558, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further ensure reliability, military temperature range AD558 grades S and T are available screened to MIL-STD-883. For more complete data sheet information consult the Analog Devices’ Military Databook.

CHIP AVAILABILITY

The AD558 is available in laser-trimmed, passivated chip form. AD558J and AD558T chips are available. Consult the factory for details.

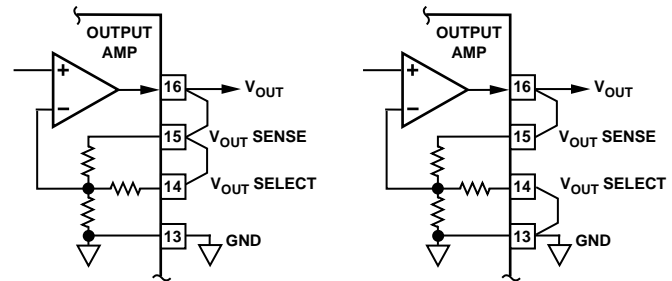
Input Logic Coding

| Digital Input Code |             |         | Output Voltage |                |
|--------------------|-------------|---------|----------------|----------------|
| Binary             | Hexadecimal | Decimal | 2.56 V Range   | 10.000 V Range |
| 0000 0000          | 00          | 0       | 0              | 0              |
| 0000 0001          | 01          | 1       | 0.010 V        | 0.039 V        |
| 0000 0010          | 02          | 2       | 0.020 V        | 0.078 V        |
| 0000 1111          | 0F          | 15      | 0.150 V        | 0.586 V        |
| 0001 0000          | 10          | 16      | 0.160 V        | 0.625 V        |
| 0111 1111          | 7F          | 127     | 1.270 V        | 4.961 V        |
| 1000 0000          | 80          | 128     | 1.280 V        | 5.000 V        |
| 1100 0000          | C0          | 192     | 1.920 V        | 7.500 V        |
| 1111 1111          | FF          | 255     | 2.55 V         | 9.961 V        |

CONNECTING THE AD558

The AD558 has been configured for ease of application. All reference, output amplifier and logic connections are made internally. In addition, all calibration trims are performed at the factory assuring specified accuracy without user trims. The only connection decision that must be made by the user is a single jumper to select output voltage range. Clean circuit board layout is facilitated by isolating all digital bit inputs on one side of the package; analog outputs are on the opposite side.

Figure 3 shows the two alternative output range connections. The 0 V to 2.56 V range may be selected for use with any power supply between +4.5 V and +16.5 V. The 0 V to 10 V range requires a power supply of +11.4 V to +16.5 V.



a. 0 V to 2.56 V Output Range b. 0 V to 10 V Output Range  
Figure 3. Connection Diagrams

Because of its precise factory calibration, the AD558 is intended to be operated without user trims for gain and offset; therefore no provisions have been made for such user trims. If a small increase in scale is required, however, it may be accomplished by slightly altering the effective gain of the output buffer. A resistor in series with  $V_{OUT}$  SENSE will increase the output range.

For example if a 0 V to 10.24 V output range is desired (40 mV = 1 LSB), a nominal resistance of 850  $\Omega$  is required. It must be remembered that, although the internal resistors all ratio-match and track, the absolute tolerance of these resistors is typically  $\pm 20\%$  and the absolute TC is typically  $-50$  ppm/ $^{\circ}$ C (0 to  $-100$  ppm/ $^{\circ}$ C). That must be considered when rescaling is performed. Figure 4 shows the recommended circuitry for a full-scale output range of 10.24 volts. Internal resistance values shown are nominal.

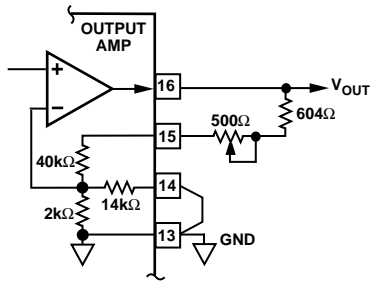


Figure 4. 10.24 V Full-Scale Connection

NOTE: Decreasing the scale by putting a resistor in series with GND will not work properly due to the code-dependent currents in GND. Adjusting offset by injecting dc at GND is not recommended for the same reason.

## GROUNDING AND BYPASSING\*

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the AD558 is intended for application in microcomputer systems where digital noise is prevalent, special care must be taken to assure that its inherent precision is realized.

The AD558 has two ground (common) pins; this minimizes ground drops and noise in the analog signal path. Figure 5 shows how the ground connections should be made.

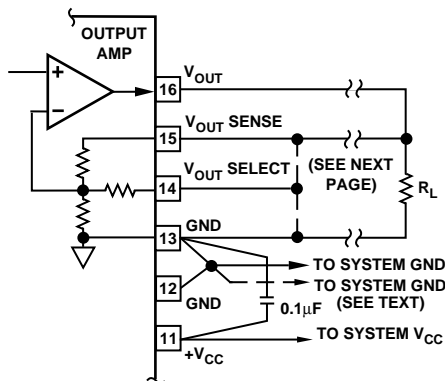


Figure 5. Recommended Grounding and Bypassing

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common in one place only. If the common tie-point is remote and accidental disconnection of that one common tie-point occurs due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the AD558, it is recommended that common ground tie-points should be provided at each such device. If only one system ground can be connected directly to the AD558, it is recommended that analog common be selected.

## POWER SUPPLY CONSIDERATIONS

The AD558 is designed to operate from a single positive power supply voltage. Specified performance is achieved for any supply voltage between +4.5 V and +16.5 V. This makes the AD558 ideal for battery-operated, portable, automotive or digital main-frame applications.

\*For additional insight, "An IC Amplifier Users' Guide to Decoupling, Grounding and Making Things Go Right For A change," is available at no charge from any Analog Devices Sales Office.

The only consideration in selecting a supply voltage is that, in order to be able to use the 0 V to 10 V output range, the power supply voltage must be between +11.4 V and +16.5 V. If, however, the 0 V to 2.56 V range is to be used, power consumption will be minimized by utilizing the lowest available supply voltage (above +4.5 V).

## TIMING AND CONTROL

The AD558 has data input latches that simplify interface to 8- and 16-bit data buses. These latches are controlled by Chip Enable ( $\overline{CE}$ ) and Chip Select ( $\overline{CS}$ ) inputs.  $\overline{CE}$  and  $\overline{CS}$  are internally "NORed" so that the latches transmit input data to the DAC section when both  $\overline{CE}$  and  $\overline{CS}$  are at Logic "0". If the application does not involve a data bus, a "00" condition allows for direct operation of the DAC. When either  $\overline{CE}$  or  $\overline{CS}$  go to Logic "1", the input data is latched into the registers and held until both  $\overline{CE}$  and  $\overline{CS}$  return to "0". (Unused  $\overline{CE}$  or  $\overline{CS}$  inputs should be tied to ground.) The truth table is given in Table I. The logic function is also shown in Figure 6.

Table I. AD558 Control Logic Truth Table

| Input Data | $\overline{CE}$ | $\overline{CS}$ | DAC Data      | Latch Condition |
|------------|-----------------|-----------------|---------------|-----------------|
| 0          | 0               | 0               | 0             | "Transparent"   |
| 1          | 0               | 0               | 1             | "Transparent"   |
| 0          | g               | 0               | 0             | Latching        |
| 1          | g               | 0               | 1             | Latching        |
| 0          | 0               | g               | 0             | Latching        |
| 1          | 0               | g               | 1             | Latching        |
| X          | 1               | X               | Previous Data | Latched         |
| X          | X               | 1               | Previous Data | Latched         |

### NOTES

X = Does not matter.

g = Logic Threshold at Positive-Going Transition.

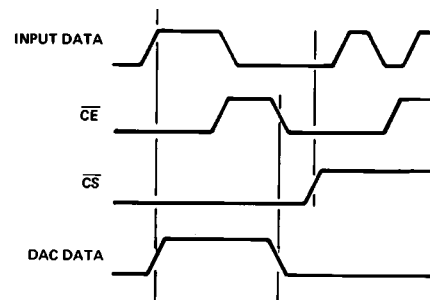


Figure 6. AD558 Control Logic Function

In a level-triggered latch such as that in the AD558 there is an interaction between data setup and hold times and the width of the enable pulse. In an effort to reduce the time required to test all possible combinations in production, the AD558 is tested with  $t_{DS} = t_W = 200$  ns at 25°C and 270 ns at  $T_{MIN}$  and  $T_{MAX}$ , with  $t_{DH} = 10$  ns at all temperatures. Failure to comply with these specifications may result in data not being latched properly.

Figure 7 shows the timing for the data and control signals;  $\overline{CE}$  and  $\overline{CS}$  are identical in timing as well as in function.

# AD558

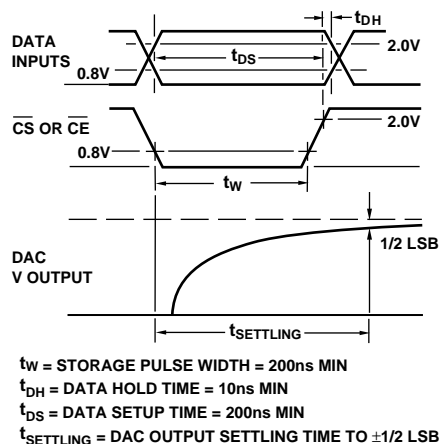
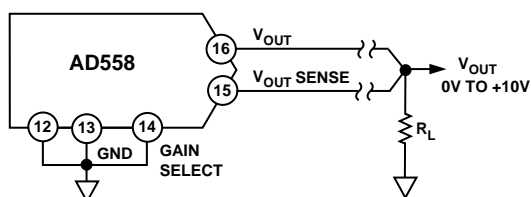


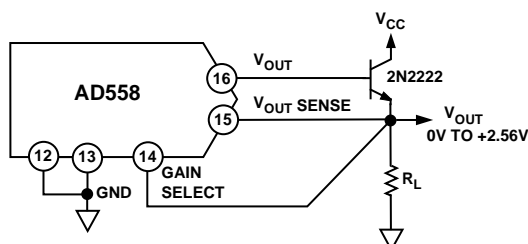
Figure 7. AD558 Timing

## USE OF $V_{OUT\ SENSE}$

Separate access to the feedback resistor of the output amplifier allows additional application versatility. Figure 8a shows how  $I \times R$  drops in long lines to remote loads may be cancelled by putting the drops “inside the loop.” Figure 8b shows how the separate sense may be used to provide a higher output current by feeding back around a simple current booster.



a. Compensation for  $I \times R$  Drops in Output Lines



b. Output Current Booster  
Figure 8. Use of  $V_{OUT\ Sense}$

## OPTIMIZING SETTling TIME

In order to provide single-supply operation and zero-based output voltage ranges, the AD558 output stage has a passive “pull-down” to ground. As a result, settling time for negative-going output steps may be longer than for positive-going output steps. The relative difference depends on load resistance and capacitance. If a negative power supply is available, the negative-going settling time may be improved by adding a pull-down resistor from the output to the negative supply as shown in Figure 9. The value of the resistor should be such that, at zero voltage out, current through that resistor is 0.5 mA max.

## BIPOLAR OUTPUT RANGES

The AD558 was designed for operation from a single power supply and is thus capable of providing only unipolar (0 V to +2.56 V and 0 V to 10 V) output ranges. If a negative supply is

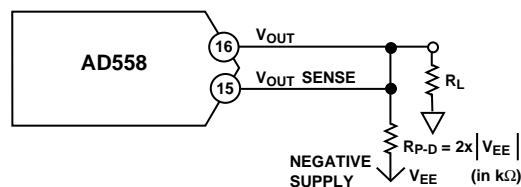


Figure 9. Improved Settling Time

available, bipolar output ranges may be achieved by suitable output offsetting and scaling. Figure 10 shows how a  $\pm 1.28$  volt output range may be achieved when a  $-5$  volt power supply is available. The offset is provided by the AD589 precision 1.2 volt reference which will operate from a  $+5$  volt supply. The AD544 output amplifier can provide the necessary  $\pm 1.28$  volt output swing from  $\pm 5$  volt supplies. Coding is complementary offset binary.

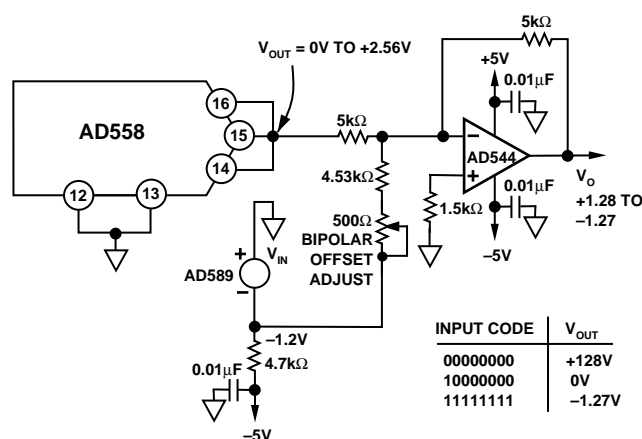


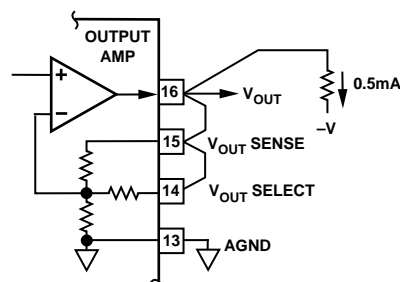
Figure 10. Bipolar Operation of AD558 from  $\pm 5$  V Supplies

## MEASURING OFFSET ERROR

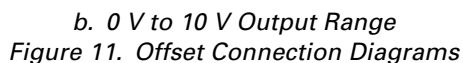
One of the most commonly specified endpoint errors associated with real-world nonideal DACs is offset error.

In most DAC testing, the offset error is measured by applying the zero-scale code and measuring the output deviation from 0 volts. There are some DACs, like the AD558 where offset errors may be present but not observable at the zero scale, because of other circuit limitations (such as zero coinciding with single-supply ground) so that a nonzero output at zero code cannot be read as the offset error. Factors like this make testing the AD558 a little more complicated.

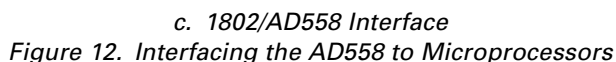
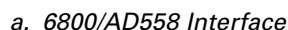
By adding a pulldown resistor from the output to a negative supply as shown in Figure 11, we can now read offset errors at zero code that may not have been observable due to circuit limitations. The value of the resistor should be such that, at zero voltage out, current through the resistor is 0.5 mA max.



a. 0 V to 2.56 V Output Range

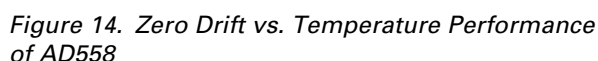
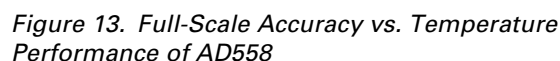


The AD558 is configured to act like a “write only” location in memory that may be made to coincide with a read only memory location or with a RAM location. The latter case allows data previously written into the DAC to be read back later via the RAM. Address decoding is partially complete for either ROM or RAM. Figure 12 shows interfaces for three popular microprocessor systems.



**Figure 12. Interfacing the AD558 to Microprocessors**

### Performance (typical @ +25°C, $V_{CC} \pm +5\text{ V}$ to +15 V unless otherwise noted)





# AD558

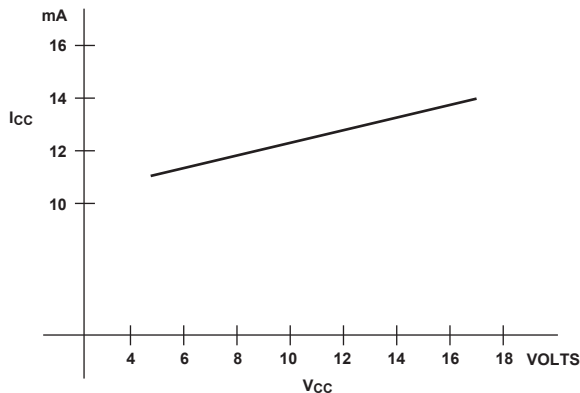
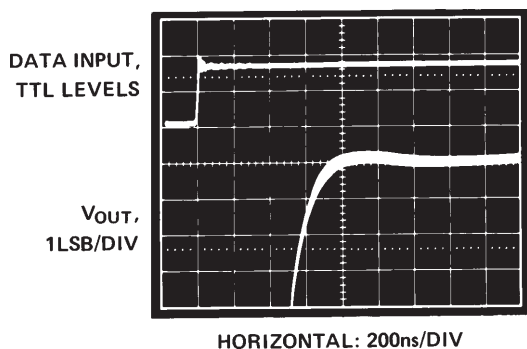
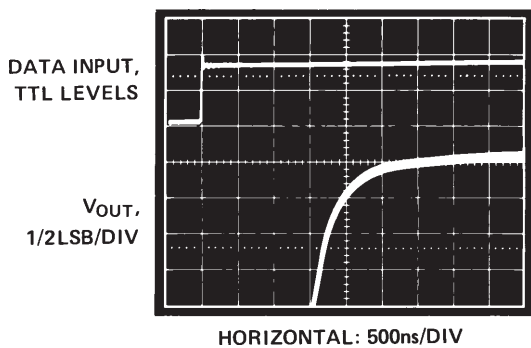


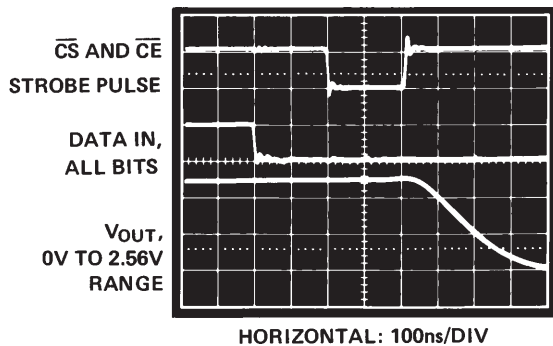
Figure 15. Quiescent Current vs. Power Supply Voltage for AD558



*Figure 16. AD558 Settling Characteristics Detail  
0 V to 2.56 V Output Range Full-Scale Step*

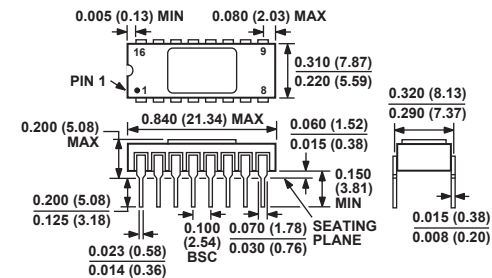
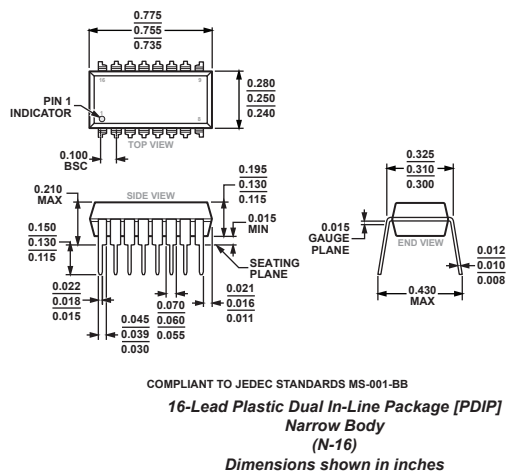


*Figure 17. AD558 Settling Characteristic Detail  
0 V to 10 V Output Range Full-Scale Step*



*Figure 18. AD558 Logic Timing*

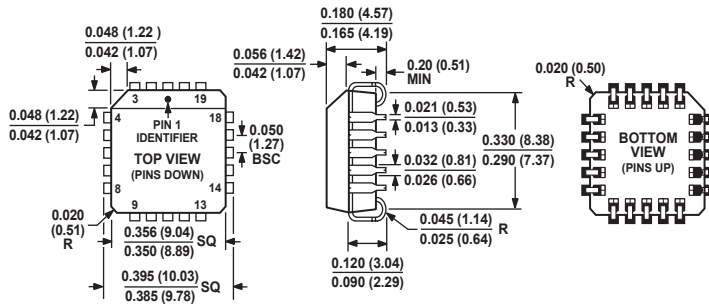
## OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

**16-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]  
(D-16)**

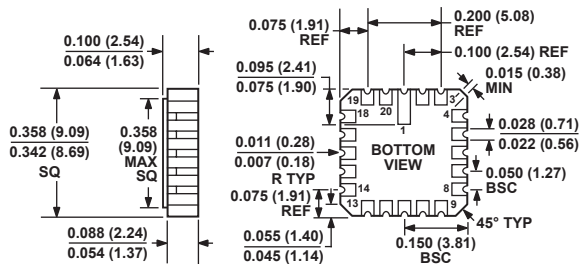
**Dimensions shown in inches and (millimeters)**



COMPLIANT TO JEDEC STANDARDS MO-047-AA  
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

**20-Lead Plastic Leaded Chip Carrier [PLCC]  
(P-20)**

**Dimensions shown in inches and (millimeters)**



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

### 20-Terminal Ceramic Leadless Chip Carrier [LCC] (E-20-1)

**Dimensions shown in inches and (millimeters)**

## ORDERING GUIDE

| Model          | Temperature Range | Relative Accuracy Error Max<br>$T_{MIN}$ to $T_{MAX}$ | Full Scale Error Max<br>$T_{MIN}$ to $T_{MAX}$ | Package Option |
|----------------|-------------------|---|--|----------------|
| AD558JN        | 0°C to +70°C      | ±1/2 LSB  | ±2.5 LSB                                       | PDIP (N-16)    |
| AD558JNZ       | 0°C to +70°C      | ±1/2 LSB  | ±2.5 LSB                                       | PDIP (N-16)    |
| AD558JP        | 0°C to +70°C      | ±1/2 LSB  | ±2.5 LSB                                       | PLCC (P-20)    |
| AD558JP-REEL7  | 0°C to +70°C      | ±1/2 LSB  | ±2.5 LSB                                       | PLCC (P-20)    |
| AD558JPZ       | 0°C to +70°C      | ±1/2 LSB  | ±2.5 LSB                                       | PLCC (P-20)    |
| AD558JPZ-REEL  | 0°C to +70°C      | ±1/2 LSB  | ±2.5 LSB                                       | PLCC (P-20)    |
| AD558JPZ-REEL7 | 0°C to +70°C      | ±1/2 LSB  | ±2.5 LSB                                       | PLCC (P-20)    |
| AD558JD        | 0°C to +70°C      | ±1/2 LSB  | ±2.5 LSB                                       | SBDIP (D-16)   |
| AD558KN        | 0°C to +70°C      | ±1/4 LSB  | ±1 LSB   | PDIP (N-16)    |
| AD558KNZ       | 0°C to +70°C      | ±1/4 LSB  | ±1 LSB   | PDIP (N-16)    |
| AD558KP        | 0°C to +70°C      | ±1/4 LSB  | ±1 LSB   | PLCC (P-20)    |
| AD558KPZ       | 0°C to +70°C      | ±1/4 LSB  | ±1 LSB   | PLCC (P-20)    |
| AD558KPZ-REEL7 | 0°C to +70°C      | ±1/4 LSB  | ±1 LSB   | PLCC (P-20)    |
| AD558KD        | 0°C to +70°C      | ±1/4 LSB  | ±1 LSB   | SBDIP (D-16)   |
| AD558SD        | −55°C to +125°C   | ±3/4 LSB  | ±2.5 LSB                                       | SBDIP (D-16)   |
| AD558TD        | −55°C to +125°C   | ±3/8 LSB  | ±1 LSB   | SBDIP (D-16)   |
| AD558TCHIPS    | −55°C to +125°C   | ±3/8 LSB  | ±1 LSB   | Die part       |
| AD558SD/883B   | −55°C to +125°C   | ±3/4 LSB  | ±2.5 LSB                                       | SBDIP (D-16)   |
| AD558SE/883B   | −55°C to +125°C   | ±3/4 LSB  | ±2.5 LSB                                       | LCC (E-20-1)   |
| AD558TD/883B   | −55°C to +125°C   | ±3/8 LSB  | ±1 LSB   | SBDIP (D-16)   |
| AD558TE/883B   | −55°C to +125°C   | ±3/8 LSB  | ±1 LSB   | LCC (E-20-1)   |

<sup>1</sup> For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the [Analog Devices Military Products Databook](#) or current [AD558/883B](#) data sheet.

<sup>2</sup>S = Ceramic SBDIP; N = Plastic PDIP; P = Plastic Leaded Chip Carrier.

## REVISION HISTORY

## 6/2017—Rev. A to Rev. B

|                                       |   |
|---------------------------------------|---|
| Added Bond Pad Coordinates Table..... | 3 |
| Updated Outline Dimensions.....       | 8 |
| Changes to Ordering Guide.....        | 9 |