Selection Guide

Part Number	Pb-free	Packing	Terminals	Package
~~A3935KLQTR~~[1]	–	1500 pieces/reel	36	QSOP (similar to SOICW) surface mount
~~A3935KLQTR-T~~[2]	Yes			

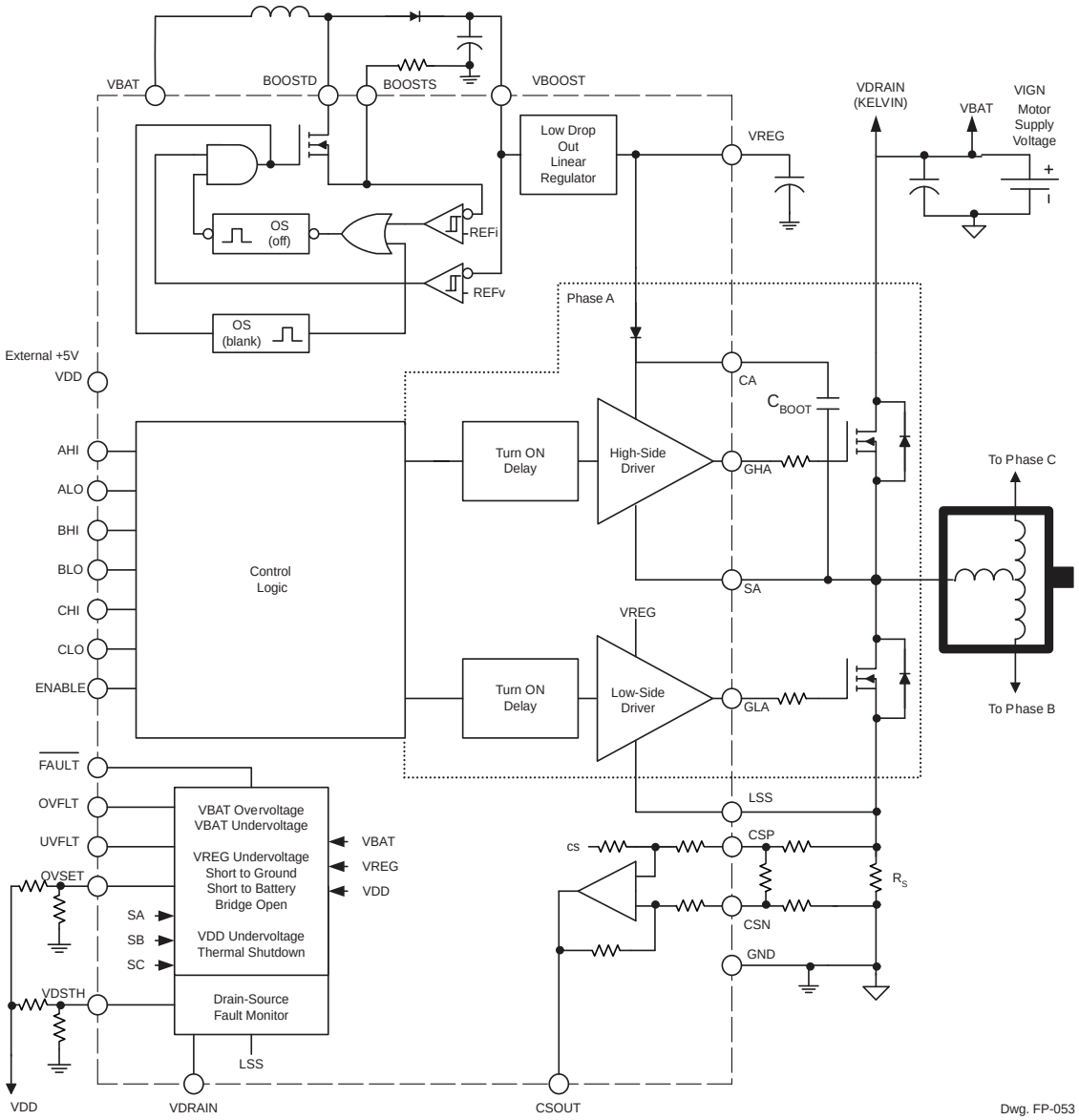
[1]Variant has been determined to be obsolete and is no longer in production. Status change: October 31, 2011.

[2]Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: October 31, 2011.

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Units
Load Supply Voltage	V_{BAT}	VBAT pin	–0.6 to 40	V
	V_{DRAIN}	VDRAIN pin		
	V_{BOOST}	VBOOST pin		
	V_{BOOSTD}	VBOOSTD pin		
Output Voltage Range	V_{GHx}	GHA, GHB, and GHC pins	–4 to 55	V
	V_{Sx}	SA, SB, and SC pins	–4 to 40	V
	V_{GLx}	GLA, GLB, and GLC pins	–4 to 16	V
	V_{Cx}	CA, CB, and CC pins	–0.6 to 55	V
Sense Circuit Voltage	V_{CSx}	CSN and CSP pins	–4 to 6.5	V
	V_{LSS}	LSS pin		
Logic Supply Voltage	V_{DD}	VDD pin	–0.3 to 6.5	V
Logic Input/Output	V_{OVSET}	OVSET pin		
	V_{BOOSTS}	BOOSTS pin		
	V_{CSOUT}	CSOUT pin		
	V_{DSTH}	VDSTH pin		
		remaining logic pins		
ESD Rating – Human Body Model		AEC-Q100-002; all pins	2.5	kV
ESD Rating – Charged Device Model		AEC-Q100-011; all pins	1050	V
Operating Temperature	T_A	Range K	–40 to 135	°C
Junction Temperature*	$T_{J(max)}$	Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.	150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

Functional Block Diagram



ELECTRICAL CHARACTERISTICS at T_J = –40°C to 150°C, V_{BAT} = 7 to 16 V, V_{DD} = 4.75 to 5.25 V, ENABLE = 22.5 kHz, 50% duty cycle, two phases active;unless otherwise noted

Characteristics	Symbol	Conditions	Min.	Typ[1].	Max.	Units
Power Supply						
V_{DD} Supply Current	I_{DD}	All logic inputs = 0 V	–	–	7.0	mA
V_{BAT} Supply Current	I_{BAT}	All logic inputs = 0 V	–	–	3.0	mA
Battery Voltage Operating Range	V_{BAT}		7.0	–	40	V
Bootstrap Diode Forward Voltage	V_{DBOOT}	$I_{DBOOT} = -I_{Cx}$ = 10 mA, $V_{DBOOT} = V_{REG} - V_{Cx}$	0.8	–	2.0	V
		$I_{DBOOT} = -I_{Cx}$ = 100 mA	1.5	–	2.3	V
Bootstrap Diode Resistance	r_{DBOOT}	r_{DBOOT}(100 mA) = (V_{DBOOT}(150 mA) – V_{DBOOT}(50 mA)) / 100 mA	2.5	–	7.5	Ω
Bootstrap Diode Current Limit[2]	I_{DM}	3 V < $V_{REG} - V_{Cx}$ < 12 V	–150	–	–1150	mA
Bootstrap Quiescent Current	I_{Cx}	V_{Cx} = 40 V, GHx = ON	10	–	30	µA
Bootstrap Refresh Time	$t_{refresh}$	V_{Sx} = low, to guarantee ΔV = +0.5 V refresh of 0.47 µF Bootstrap Capacitor, CBOOT, to $V_{Cx} - V_{Sx}$ = +10 V	–	–	2.0	µs
VREG Output Voltage[3]	V_{REG}	V_{BAT} = 7 to 40 V, V_{BOOST} from Boost Regulator	12.7	–	14	V
VREG Dropout Voltage[4]	V_{REGDO}	$V_{REGDO} = V_{BOOST} - V_{REG}$, I_{REG} = 40 mA	–	0.9	–	V
Gate Drive Average Supply Current	I_{REG}	No external dc load at VREG, C_{REG} = 10 µF	–	–	40	mA
VREG Input Bias Current	$I_{REGbias}$	Current into V_{BOOST}, ENABLE = 0	–	–	4.0	mA
Boost Supply						
VBOOST Output Voltage Limit	V_{BOOSTM}	V_{BAT} = 7 V	14.9	–	16.3	V
VBOOST Output Voltage Limit Hysteresis	ΔV_{BOOSTM}		35	–	180	mV
Boost Switch On Resistance	$r_{DS(on)}$	I_{BOOSTD} < 300 mA	–	1.4	3.3	Ω
Boost Switch Maximum Current	$I_{BOOSTSW}$		–	–	300	mA
Boost Current Limit Threshold Voltage	$V_{BI(th)}$	Increasing V_{BOOSTS}	0.45	–	0.55	V
Off Time	t_{off}		3.0	–	8.0	µs
Blanking Time	t_{blank}		100	–	220	ns
Control Logic						
Logic Input Voltage	$V_{I(1)}$	Minimum high level input for logic 1	2.0	–	–	V
	$V_{I(0)}$	Maximum low level input for logic 0	–	–	0.8	V
Logic Input Current	$I_{I(1)}$	$V_I = V_{DD}$	–	–	500	µA
	$I_{I(0)}$	V_I = 0.8 V	50	–	–	µA
Logic Input Hysteresis	V_{Ihys}		100	–	300	mV
Logic Output High Voltage	$V_{O(H)}$	$I_{O(H)}$ = –800 µA	V_{DD} – 0.8	–	–	V
Logic Output Low Voltage	$V_{O(L)}$	$I_{O(L)}$ = 1.6 mA	–	–	0.4	V
Gate Drives, GH*x* (internal source, or upper, switch stages)[5]						
Output High Voltage	$V_{DSL(H)}$	GHx: I_{xU} = –10 mA, V_{Sx} = 0	V_{REG} – 2.26	–	V_{REG}	V
		GLx: I_{xU} = –10 mA, V_{LSS} = 0	V_{REG} – 0.26	–	V_{REG}	V
Source Current (pulsed)	I_{xU}	V_{SDU} = 10 V, T_J = 25°C	–	800	–	mA
		V_{SDU} = 10 V, T_J = 135°C	400	–	–	mA
Source On Resistance	$r_{SDU(on)}$	I_{xU} = –150 mA, T_J = 25°C	4.0	–	10	Ω
		I_{xU} = –150 mA, T_J = 135°C	7.0	–	15	Ω

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ELECTRICAL CHARACTERISTICS (continued) at T_J = –40°C to 150°C, V_{BAT} = 7 to 16 V, V_{DD} = 4.75 to 5.25 V, ENABLE = 22.5 kHz, 50% duty cycle, two phases active;unless otherwise noted

Characteristics	Symbol	Conditions	Min.	Typ[1].	Max.	Units
Gate Drives, GL*x* (internal sink or lower switch stages)[6]						
Sink Current (pulsed)	I_{xL}	V_{DSL} = 10 V, T_J = 25°C	–	850	–	mA
		V_{DSL} = 10 V, T_J = 135°C	550	–	–	mA
Sink On Resistance	$r_{DSL(on)}$	I_{xL} = 150 mA, T_J = 25°C	1.8	–	6.0	Ω
		I_{xL} = 150 mA, T_J = 135°C	3.0	–	7.5	Ω
Gate Drives, GH*x*, GL*x* (General)[5,6]						
Propagation Delay, Logic only	t_{pd}	Logic input to unloaded GH*x*, GL*x*	–	–	150	ns
Output Skew Time	$t_{sk(o)}$	Grouped by edge, phase–to–phase	–	–	50	ns
Dead Time (shoot–through prevention)	t_{dead}	Between GH*x*, GL*x* transitions of same phase	75	–	180	ns
Sense Amplifier						
Input Bias Current[2]	I_{bias}	CSP = CSN = 0 V	–180	–	–360	µA
Input Offset Current[2]	I_{IO}	CSP = CSN = 0 V	–	–	±35	µA
Input Resistance	r_i	CSP with respect to GND	–	80	–	kΩ
		CSN with respect to GND	–	4.0	–	kΩ
Diff. Input Operating Voltage	V_{ID}	V_{ID} = CSP – CSN, –1.3V < CSP,N < 4V	–	–	±200	mV
Output Offset Voltage	V_{OO}	CSP = CSN = 0 V	77	250	450	mV
Output Offset Voltage Drift	ΔV_{OO}	CSP = CSN = 0 V	–	100	–	µV/°C
Input Common Mode Operating Range	V_{IC}	CSP = CSN	–1.5	–	4.0	V
Voltage Gain	A_V	V_{ID} = 40 to 200 mV	18.6	19.2	19.8	V/V
Low Output Voltage Error	E_V	V_{ID} = 0 to 40 mV, V_O = (19.2 × V_{ID}) + V_O + E_v	–	–	±25	mV
DC Common Mode Attenuation	A_{VC}	CSP = CSN = 200 mV	28	–	–	dB
Output Resistance	r_O	V_{CSOUT} = 2.0 V	–	8.0	–	Ω
Output Dynamic Range	V_{CSOUT}	I_{CSOUT} = –100 µA at top rail, 100 µA at bottom rail	0.075	–	V_{DD} – 0.25	V
Output Current, Sink	I_{sink}	V_{CSOUT} = 2.5 V	20	–	–	mA
Output Current, Source[2]	I_{source}	V_{CSOUT} = 2.5 V	–1.0	–	–	mA
VDD Supply Ripple Rejection	$PSRR_{VDD}$	CSP = CSN = GND, frequency = 0 to 1 MHz	20	–	–	dB
VREG Supply Ripple Rejection	$PSRR_{VREG}$	CSP = CSN = GND, frequency = 0 to 300 kHz	45	–	–	dB
Small Signal 3 dB Bandwidth	BW_{f3db}	10 mV input	–	1.6	–	MHz
AC Common Mode Attenuation	$A_{VC(ac)}$	V_{cm} = 250 mV(pp), frequency = 0 to 800 kHz	26	–	–	dB
Output Slew Rate (positive or negative)	SR	200 mV step input, measured at 10/90% points	10	–	–	V/µs
Fault Logic						
VDD Undervoltage	$V_{DD(uv)}$	Decreasing V_{DD}	3.8	–	4.3	V
VDD Undervoltage Hysteresis	$\Delta V_{DD(uv)}$	$V_{DD(recovery)}$ – $V_{DD(uv)}$	100	–	300	mV
OVSET Operating Voltage Range	$V_{SET(ov)}$		0	–	V_{DD}	V
OVSET Calibrated Voltage Range	$V_{SET(ov)cal}$		0	–	2.5	V
OVSET Input Current Range[2]	$I_{SET(ov)}$		–1.0	–	1.0	µA
VBAT Overvoltage Range	$V_{BAT(ov)}$	0 V < $V_{SET(ov)}$ < 2.5 V	19.4	–	40	V
		Increasing V_{BAT}, $V_{SET(ov)}$ = 0 V	19.4	22.4	25.4	V
VBAT Overvoltage Hysteresis	$\Delta V_{BAT(ov)}$	Percent of $V_{BAT(ov)}$ value set by $V_{SET(ov)}$	9.0	–	15	%

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ELECTRICAL CHARACTERISTICS (continued) at T_J = –40°C to 150°C, V_{BAT} = 7 to 16 V, V_{DD} = 4.75 to 5.25 V, ENABLE = 22.5 kHz, 50% duty cycle, two phases active;unless otherwise noted

Characteristics	Symbol	Conditions	Min.	Typ[1].	Max.	Units
VBAT Overvoltage Gain Constant	$K_{BAT(ov)}$	$V_{BAT(ov)} = (K_{BAT(ov)} \times V_{SET(ov)}) + V_{BAT(ov)}(0)$; $V_{BAT(ov)(0)}$ at $V_{SET(ov)} = 0$	–	12	–	V/V
VBAT Undervoltage	$V_{BAT(uv)}$	Decreasing V_{BAT}	5.0	5.25	5.5	V
VBAT Undervoltage Hysteresis	$V_{BAT(uv)}$	Percent of $V_{BAT(uv)}$	8.0	–	12	%
VREG Undervoltage	$V_{REG(uv)}$	Decreasing V_{REG}	9.9	–	11.1	V
VDSTH Input Range	V_{DSTH}		0.5	–	3.0	V
VDSTH Input Current	I_{DSTH}	V_{DSTH} > 0.8 V	40	–	100	µA
Short–to–Ground Threshold	$V_{STG(th)}$	With a high–side driver on, as V_{SX} decreases, $V_{DRAIN} - V_{Sx} > V_{STG}$ causes a fault	V_{DSTH} – 0.3	–	V_{DSTH} + 0.2	V
Short–to–Battery Threshold	$V_{STB(th)}$	With a low–side driver on, as V_{SX} increases, $V_{Sx} - V_{LSS} > V_{STB}$ causes a fault	V_{DSTH} – 0.3	–	V_{DSTH} + 0.2	V
VDRAIN-Open Bridge Operating Range	V_{DRAIN}	7 V < V_{BAT} < 40 V	–0.3	–	V_{BAT} + 2.0	V
VDRAIN Open Bridge Current	I_{VDRAIN}	7 V < V_{BAT} < 40 V	0	–	1.0	mA
VDRAIN /Open Bridge Threshold Voltage	$V_{BDGO(th)}$	If V_{DRAIN} < V_{BDGOTH} then a bridge fault occurs	1.0	–	3.0	V
Thermal Shut Down Temperature	T_J		160	170	180	°C
Thermal Shutdown Hysteresis	ΔT_J		7.0	10	13	°C

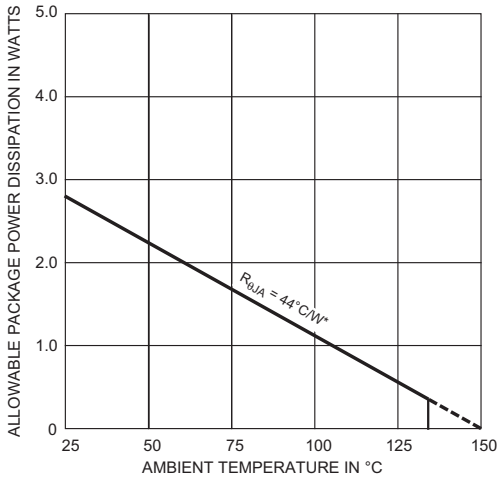
[1]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.
[2]Negative current is defined as coming out of (sourcing) the specified device terminal.
[3]For V_{BOOSTM} < V_{BOOST} < 40 V power dissipation in the V_{REG} LDO increases. Observe T_J < 150°C limit.
[4]With V_{BOOST} decreasing, dropout voltage measured at $V_{REG} = V_{REG(ref)} - 200$ mV where $V_{REG(ref)} = V_{REG}$ at V_{BOOST} = 16 V.
[5]For GHx: $V_{SDU} = V_{Cx} - V_{GHx}$, $V_{DSL} = V_{GHx} - V_{Sx}$, $V_{DSL(H)} = V_{Cx} - V_{SDU} - V_{Sx}$.
[6]For GL*x*: $V_{SDU} = V_{REG} - V_{GLx}$, $V_{DSL} = V_{GLx} - V_{LSS}$, $V_{DSL(H)} = V_{REG} - V_{SDU} - V_{LSS}$.

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB, based on JEDEC standard	44	ºC/W

*Additional thermal information available on Allegro Web site.

Power Dissipation versus Ambient Temperature



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Terminal Descriptions

AHI, BHI, and CHI. Direct control of high-side gate outputs GHA, GHB, and GHC. Logic 1 drives the gate on. Logic 0 pulls the gate down, turning off the external power MOSFET. Internally pulled down when the terminal is open.

ALO, BLO, and CLO. Direct control of low-side gate outputs GHA, GHB, and GHC. Logic 1 drives the gate on. Logic 0 pulls the gate down, turning off the external power MOSFET**.** Internally pulled down when the terminal is open.

BOOSTD. Boost converter switch drain connection**.**

BOOSTS. Boost converter switch source connection.

CA, CB, and CC. High-side connection for the bootstrap capacitors, CBOOT*x*, positive supply for high-side gate drive. The bootstrap capacitor is charged to V_{REG} when the output S*x* terminal is low. When the output swings high, the voltage on this terminal rises with the output to provide the boosted gate voltage needed for N-channel power MOSFETs.

CSN. Input for current-sense differential amplifier, on the inverting, negative side. Kelvin connection for the ground side of the current-sense resistor, RSENSE.

CSOUT. Amplifier output voltage proportional to the current sensed across an external low-value resistor placed in the ground side of the power MOSFET bridge.

CSP. Input for current-sense differential amplifier, on the non-inverting, positive side. Connected to the positive side of the sense resistor, RSENSE.

ENABLE. Logic 0 disables the gate control signals and switches off all the gate drivers (low) causing a coast condition. Can be used in conjunction with the gate inputs to PWM (pulse wave modulate) the load current. Internally pulled down when the terminal is open.

$\overline{\text{FAULT}}$. Diagnostic logic output signal. When low, indicates that one or more fault conditions have occurred.

GHA, GHB, and GHC. High-side gate drive outputs for N-channel MOSFET drivers. External series gate resistors can control the slew rate seen at the power driver gate, thereby controlling the *di*/*dt* and *dv*/*dt* of S*x* outputs.

GLA, GLB, and GLC. Low-side gate drive outputs for external, N-channel MOSFET drivers. External series gate resistors can control slew rate.

GND. Ground, or negative, side of VDD and VBAT supplies.

LSS. Low-side gate driver return. Connects to the common sources on the low sides of the power MOSFET bridge.

OVFLT. Logic 1 indicates that the V_{BAT} level exceeded the VBAT overvoltage trip point set by the OVSET level. It will recover after exceeding a hysteresis below that maximum value. Normally, it has a high-impedance state. If OVFLT and UVFLT are both in high-impedance state; then, at least, a thermal shutdown or VDD undervoltage has occurred.

OVSET. A positive dc level that controls the VBAT overvoltage trip point. Usually, set by a precision resistor divider network between VDD and GND, but can be held grounded for a preset value. When this terminal is open, it sets an unspecified but high overvoltage trip point.

SA, SB, and SC. Directly connected to the motor terminals, these terminals sense the voltages switched across the load and are connected to the negative side of the bootstrap capacitors, CBOOT*x*. Also, are the negative supply connection for the floating high-side drivers.

UVFLT. Logic 1 indicates that the V_{BAT} level is below its minimum value. It will recover after exceeding a hysteresis above that minimum value. Has a high-impedance state. If UVFLT and OVFLT are both in high-impedance state; then, at least, a thermal shutdown or VDD undervoltage has occurred.

VBAT. Battery voltage. Positive input. usually connected to the motor voltage supply.

VBOOST. Boost converter output, 16 V nominal, is also the input to the regulator for VREG. Has internal boost-current and boost-voltage control loops. In high-voltage systems is approximately one diode drop below V_{BAT}.

VDD. Logic supply, +5 V nominal.

VDRAIN. Kelvin connection for drain-to-source voltage monitor. Connected to the high-side drains of the MOSFET bridge. High impedance when this terminal is open, and registers as a short-to-ground fault on all motor phases.

VDSTH. A positive dc level that sets the drain-to-source monitor threshold voltage. Internally pulled down when this terminal is open.

VREG. High-side gate driver supply, 13.5 V nominal. Has low-voltage dropout (LDO) feature.

Functional Description

Motor Lead Protection. A fault detection circuit monitors the voltage across the drain-to-source of the external MOSFETs. A fault is asserted low on the output terminal, $\overline{\text{FAULT}}$, if the drain-to-source voltage of any MOSFET that is instructed to turn on is greater than the voltage applied to the V_{DSTH} input terminal. When a high-side switch is turned on, the voltage from V_{DRAIN} to the appropriate motor phase output, V_{SX}, is examined. If the motor lead is shorted to ground before the high-side is turned on, the measured voltage will exceed the threshold and the $\overline{\text{FAULT}}$ terminal will go low. Similarly, when a low-side MOSFET is turned on, the differential voltage between the motor phase (drain) and the LSS terminal (source) is monitored. V_{DSTH} is set by a resistor divider to V_{DD}.

The V_{DRAIN} is intended to be a Kelvin connection for the high-side, drain-to-source monitor circuit. Voltage drops across the power bus are eliminated by connecting an isolated PCB trace from the V_{DRAIN} terminal to the drain of the MOSFET bridge. This allows improved accuracy in setting the V_{DSTH} threshold voltage. The low-side, drain-to-source monitor uses the LSS terminal, rather than V_{DRAIN}, for comparison with V_{DSTH}. The A3935 just reports these motor faults.

Fault Outputs. Transient faults on any of the fault outputs are to be expected during switching, and will not disable the gate drive outputs. External circuitry or controller logic must determine if the faults represent a hazardous condition.

$\overline{\text{FAULT}}$. This terminal will go active low when any of the following conditions occur:

- V_{BAT} overvoltage
- V_{BAT} undervoltage
- V_{REG} undervoltage
- Motor lead short-to-ground
- Motor lead short-to-supply or short-to-battery
- Bridge (or V_{DRAIN}) open
- V_{DD} undervoltage
- Thermal shut down

OVFLT. Asserts high when a V_{BAT} overvoltage fault occurs and resets low after a recovery hysteresis. It has a high-impedance state when a thermal shutdown or V_{DD} undervoltage occurs. The voltage at the OVSET terminal, V_{OVSET}, controls the V_{BAT} overvoltage set point $V_{BAT(ov)}$, as follows:

$$V_{BAT(ov)} = (A_{BAT(ov)} \times V_{SET(ov)}) + V_{BAT(ov)(0)},$$

where $A_{BAT(ov)}$ is the gain (12) and $V_{BAT(ov)(0)}$ is the value of $V_{BAT(ov)}$ when $V_{SET(ov)} = 0$ ($V_{BAT(ov)} \approx 22.4$). For the above formula to be valid, all variables must be in range and below the maximum operating specification.

UVFLT. Asserts high when a V_{BAT} undervoltage fault occurs and resets low after exceeding a recovery hysteresis. It has a high-impedance state when a thermal shut down or V_{DD} undervoltage occurs. OVFLT and UVFLT are mutually exclusive by definition.

Current Sensing. A current-sense amplifier is provided to allow system monitoring of the load current. The differential amplifier inputs are intended to be Kelvin-connected across a low-value sense resistor or current shunt. The output voltage is represented by:

$$V_{CSOUT} = (I_{LOAD} \times A_V \times R_{SENSE}) + V_{OS}$$

where V_{OS} is the output voltage calibrated at zero load current and A_V is the differential amplifier gain of about 19.2. If either the CSP or CSN pin is open, the CSOUT pin will go to its maximum positive level.

Shut Down. If a fault occurs because of excessive junction temperature or undervoltage on V_{DD} or V_{BAT}, all gate driver outputs are driven low until the fault condition is removed. In addition, the boost supply switch and VREG are turned off until those undervoltages and junction temperatures recover.

Boost Supply. V_{BOOST} is controlled by an inner current-control loop, and by an outer voltage-feedback loop. The current-control loop turns off the boost switch for 5 µs whenever the voltage across the boost current-sense resistor exceeds 500 mV. A diode reverse-recovery current flows through the sense resistor whenever the boost switch turns on, which could result in turning off the switch again if not for the blanking-time circuit. Adjustment of this external sense resistor determines the maximum current in the inductor. Whenever V_{BOOST} exceeds the predefined threshold, 16 V nominal the boost switch is inhibited.

Input Logic Table

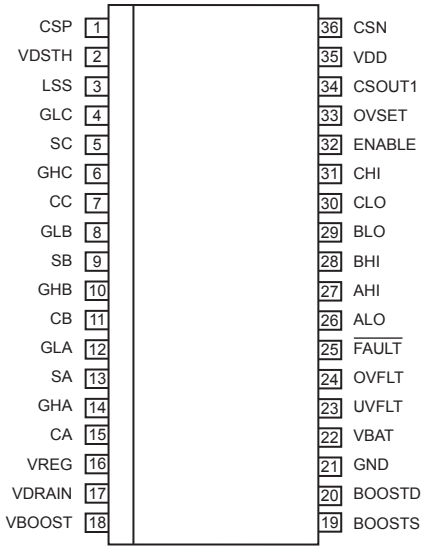
Input			Output		Mode of Operation
ENABLE	*x*LO	*x*HI	GL*x*	GH*x*	
0	Don't Care	Don't Care	0	0	All gate drive outputs low
1	0	0	0	0	Both gate drive outputs low
1	0	1	0	1	High-side on
1	1	0	1	0	Low-side on
1	1	1	0	0	XOR circuitry prevents shoot-through

Fault Response Table

Operating Conditions		Fault Output			Regulator State		Driver Output	
Fault Mode	ENABLE	$\overline{\text{FAULT}}$	OVFLT	UVFLT	Boost	V_{REG}	GH*x*	GL*x*
No Fault	Don't Care	1	0	0	ON	ON	[a]	[a]
Short-to-Battery	1[b]	0	0	0	ON	ON	[a]	[a]
Short-to-Ground	1[c]	0	0	0	ON	ON	[a]	[a]
Bridge (VDRAIN) Fault	1[d]	0	0	0	ON	ON	[a]	[a]
VREG Undervoltage	Don't Care	0	0	0	ON	ON	[a]	[a]
VBAT Overvoltage	Don't Care	0	1	0	OFF[e]	ON	[a]	[a]
VBAT Undervoltage[f]	Don't Care	0	0	1	OFF	OFF	0	0
VDD Undervoltage[f]	Don't Care	0	High Z	High Z	OFF	OFF	0	0
Thermal Shut Down[f]	Don't Care	0	High Z	High Z	OFF	OFF	0	0

[a]Determined by input states: *x*LO, *x*HI, and ENABLE. See Input Logic table.
[b]Short-to-battery can only be detected when the corresponding GLx = 1. This fault is not detected when ENABLE = 0.
[c]Short-to-ground can only be detected when the corresponding GHx = 1. This fault is not detected when ENABLE = 0.
[d]Bridge fault appears as a short-to-ground fault on all motor phases. This fault is not detected when ENABLE = 0.
[e]Off only because $V_{BOOST} \approx V_{BAT}$, which is above the voltage threshold of the Boost regulator voltage control loop.
[f]These faults are not only reported, but also action is taken by the internal logic to protect the A3935 and the system.

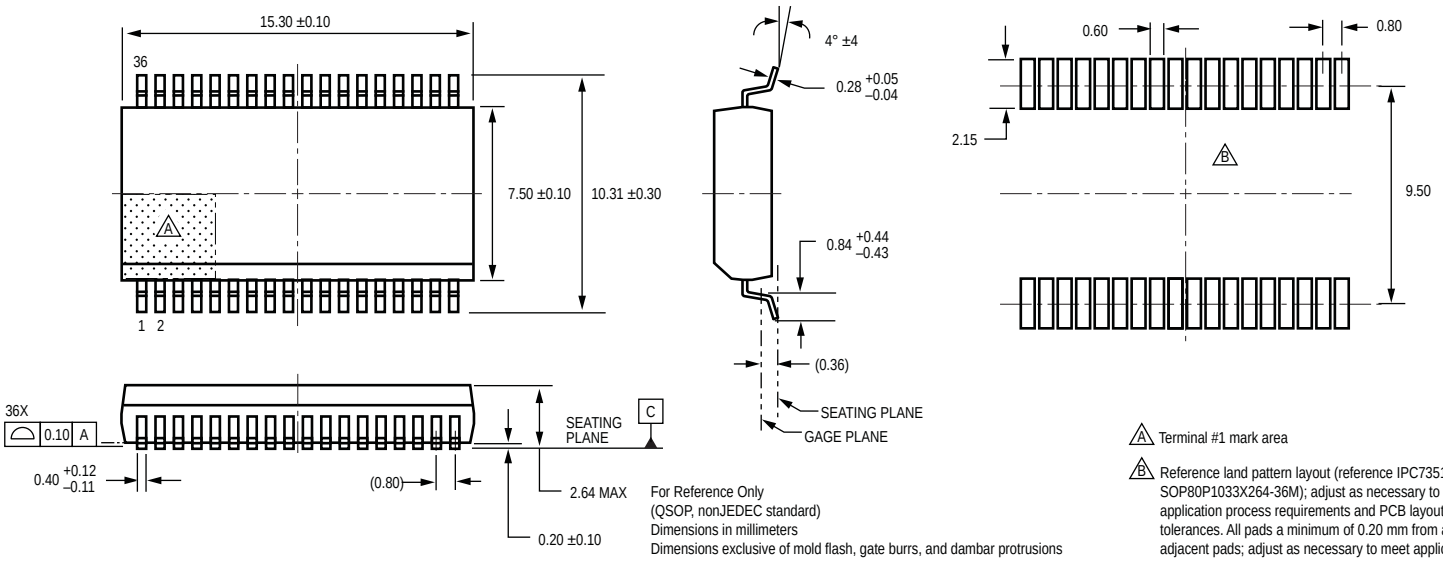
Pin-out Diagram



Terminal List

Number	Name	Function	Number	Name	Function
1	CSP	Current-sense input, positive-side	19	BOOSTS	Boost switch, source
2	VDSTH	DC input, drain-to-source monitor threshold voltage	20	BOOSTD	Boost switch, drain
3	LSS	Gate-drive source return, low-side	21	GND	Ground, dc supply returns, negative
4	GLC	Gate-drive C output, low-side	22	VBAT	Battery supply, positive
5	SC	Load phase C input	23	UVFLT	VBAT undervoltage fault output
6	GHC	Gate-drive C output, high-side	24	OVFLT	VBAT overvoltage fault output
7	CC	Bootstrap capacitor C	25	$\overline{\text{FAULT}}$	Active-low fault output, primary
8	GLB	Gate-drive B output, low-side	26	ALO	Gate control input A, low-side
9	SB	Load phase B input	27	AHI	Gate control input A, high-side
10	GHB	Gate-drive B output, high-side	28	BHI	Gate control input B, high-side
11	CB	Bootstrap capacitor B	29	BLO	Gate control input B, low-side
12	GLA	Gate-drive A output, low-side	30	CLO	Gate control input C, low-side
13	SA	Load phase A input	31	CHI	Gate control input C, high-side
14	GHA	Gate-drive A output, high-side	32	ENABLE	Gate output enable
15	CA	Bootstrap capacitor A	33	OVSET	DC input, overvoltage threshold setting for VBAT
16	VREG	Gate drive supply, positive	34	CSOUT	Current-sense amplifier output
17	VDRAIN	Kelvin connection to MOSFET high-side drains	35	VDD	Logic supply, nominally +5 V
18	VBOOST	Boost supply output	36	CSN	Current-sense input, negative-side

Package LQ, 36-pin QSOP



For Reference Only
(QSOP, nonJEDEC standard)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP80P1033X264-36M); adjust as necessary to meet application process requirements and PCB layout tolerances. All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Revision History

Revision	Revision Date	Description of Revision
Rev. J	October 31, 2011	Update product availability

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