

1 Characteristics

Table 1. Absolute ratings

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 air discharge IEC 61000-4-2 contact discharge MIL STD883G-Method 3015-7	± 15 ± 15 ± 25	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Maximum junction temperature		+125	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C

Table 2. Electrical characteristics ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
I_{RM}	Leakage current	$V_{RM} = 5\text{ V}$			0.5	μA
V_{BR}	Breakdown voltage between V_{BUS} and GND	$I_R = 1\text{ mA}$	6			V
V_{CL}	Clamping voltage	$I_{PP} = 1\text{ A}$, 8/20 μs Any I/O pin to GND			12	V
		$I_{PP} = 5\text{ A}$, 8/20 μs Any I/O pin to GND			17	V
$C_{i/o-GND}$	Capacitance between I/O and GND	$V_R = 0\text{ V}$, $F = 1\text{ MHz}$ Any I/O pin to ground		1.0	1.2	pF
		$V_R = 0\text{ V}$, $F = 240\text{ MHz}$ Any I/O pin to ground		0.7	0.85	
$\Delta C_{i/o-GND}$	Capacitance variation between I/O and GND	$V_R = 0\text{ V}$, $F = 1\text{ MHz}$ Any I/O pin to ground		0.02		
$C_{i/o-i/o}$	Capacitance between I/O	$V_R = 0\text{ V}$, $F = 1\text{ MHz}$ Ground not connected		0.47	0.55	
		$V_R = 0\text{ V}$, $F = 240\text{ MHz}$ Ground not connected		0.45	0.55	

Figure 2. Relative variation of leakage current versus junction temperature (typical values)

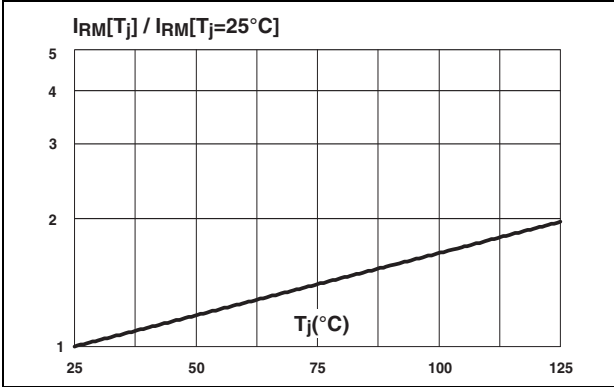


Figure 3. Typical frequency response

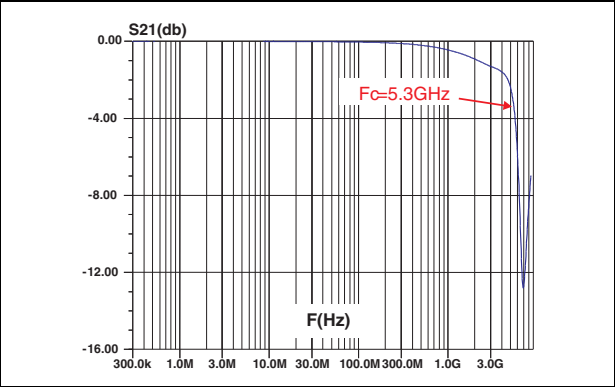


Figure 4. Crosstalk measurement

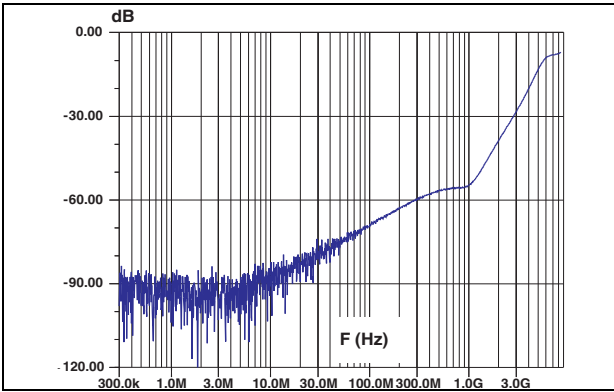


Figure 5. Line capacitance versus frequency (typical values)

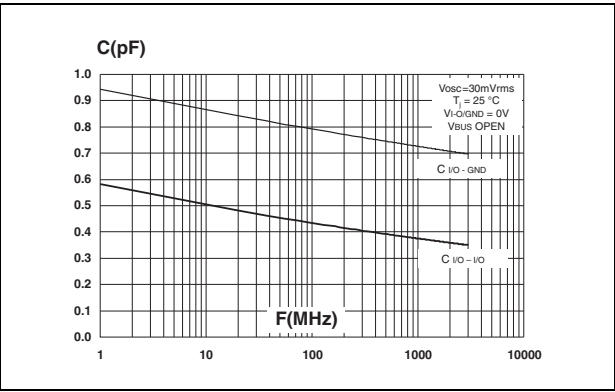


Figure 6. Remaining voltage on I/O1 after USBULC-2P6 during positive ESD surge (+15 kV air discharge)

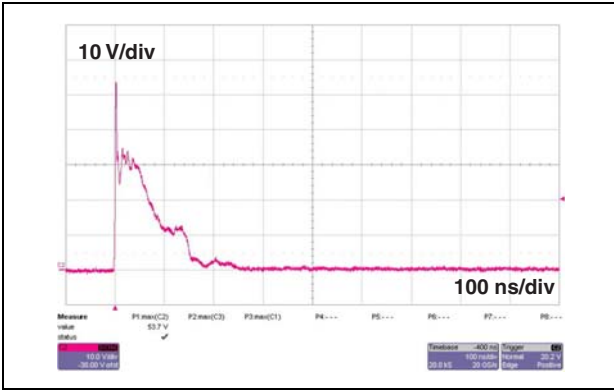


Figure 7. Remaining voltage on I/O2 after USBULC-2P6 during negative ESD surge (-15 kV air discharge)

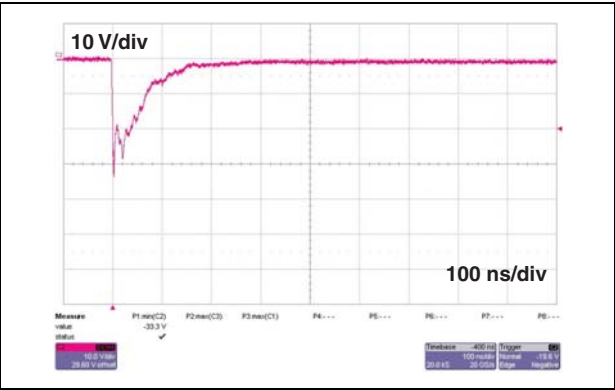


Figure 8. Remaining voltage on V_{BUS} after USBULC6-2P6 during positive ESD surge (+15 kV air discharge)

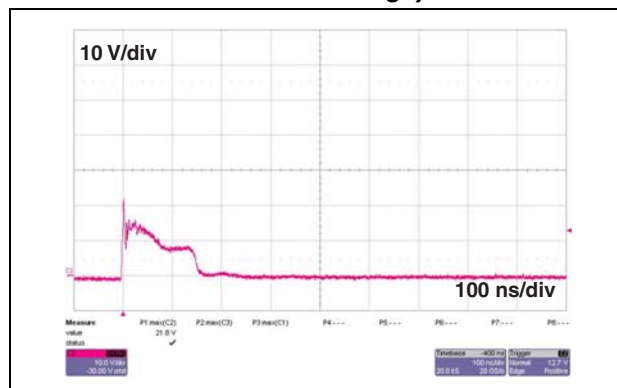


Figure 9. Remaining voltage on V_{BUS} after USBULC6-2P6 during negative ESD surge (-15 kV air discharge)

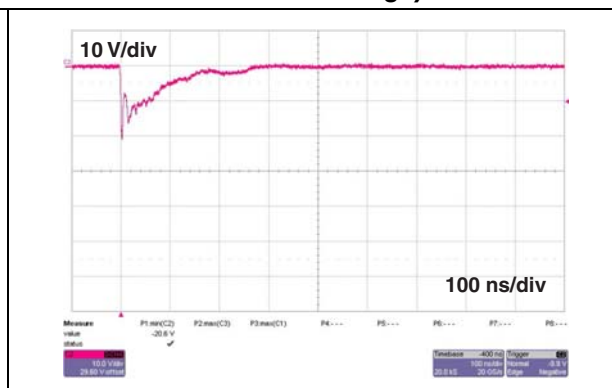


Figure 10. Eye diagram PCB only, 400 mV amplitude, $F = 480$ Mbps

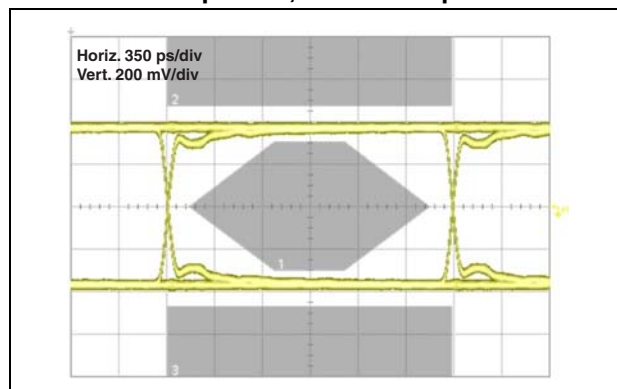


Figure 11. Eye diagram PCB + USBULC6-2P6, 400 mV amplitude, $F = 480$ Mbps

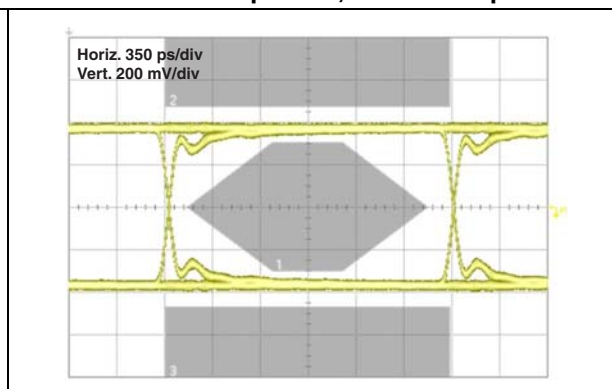
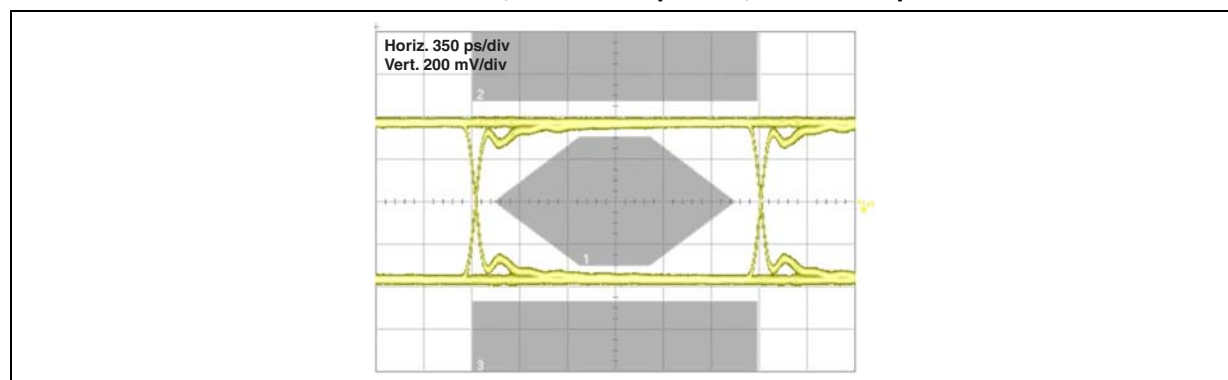
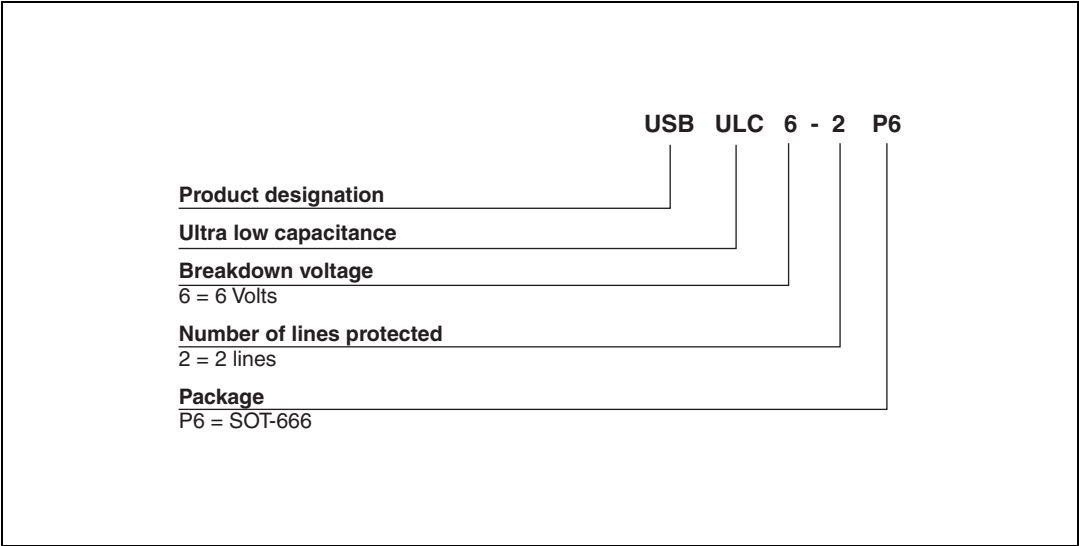


Figure 12. Eye diagram PCB + USBULC6-2P6, +5 V on V_{BUS} , decoupling capacitor 100 nF, 400 mV amplitude, $F = 480$ Mbps



2 Ordering information scheme

Figure 13. Ordering information scheme



3 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Table 3. SOT-666 dimensions

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45		0.60	0.018		0.024
A3	0.08		0.18	0.003		0.007
b	0.17		0.34	0.007		0.013
b1	0.19	0.27	0.34	0.007	0.011	0.013
D	1.50		1.70	0.059		0.067
E	1.50		1.70	0.059		0.067
E1	1.10		1.30	0.043		0.051
e		0.50			0.020	
L1		0.19			0.007	
L2	0.10		0.30	0.004		0.012
L3		0.10			0.004	

Figure 14. SOT-666 footprint

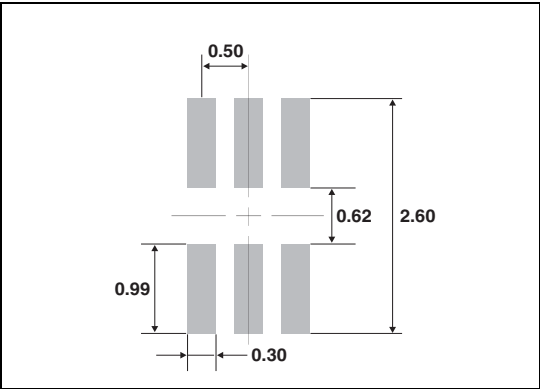
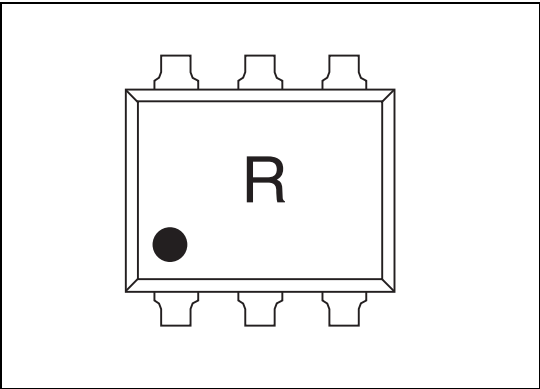


Figure 15. SOT-666 marking



4 Ordering information

Table 4. Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
USBULC6-2P6	R	SOT-666	2.9 mg	3000	Tape and reel

5 Revision history

Table 5. Document revision history

Date	Revision	Description of changes
31-Mar-2014	1	First issue.

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