Table of Contents

Features 1
Applications 1
Description 1
Pin Configuration 1
Table of Contents 2
Revision History 2
Order Information 3
Absolute Maximum Ratings Note 1 4
ESD Rating 4
Thermal Information 4
Electrical Characteristics 5
Typical Performance Characteristics 6
Application Information 10
Tape and Reel Information 13
Package Outline Dimensions 14
SC70-5 14
SOT23-5 14
SOIC-8 15
MSOP-8 16
SOIC-14 17
TSSOP-14 18

Revision History

Date	Revision	Notes
2014	1.0	Initial Version
2018/12/31	Rev A	Update with new format, Update Datasheet Limit. Correct the Mark of TP2111-CR: B1C -> B1T

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TP2111-TR	-40 to 125°C	5-Pin SOT23	B1TYW [Note 1]	3	Tape and Reel, 3000
TP2111-CR	-40 to 125°C	5-Pin SC70	B1TYW [Note 1]	3	Tape and Reel, 3000
TP2112-SR	-40 to 125°C	8-Pin SOIC	B12S AAYW [Note 1]	3	Tape and Reel, 4000
TP2112-VR	-40 to 125°C	8-Pin MSOP	B12V AAYW [Note 1]	3	Tape and Reel, 3000
TP2114-SR [Note 2]	-40 to 125°C	14-Pin SOIC	2114 AAYW [Note 1]	3	Tape and Reel, 2500
TP2114-TR [Note 2]	-40 to 125°C	14-Pin TSSOP	2114 AAYW [Note 1]	3	Tape and Reel, 3000

Note 1: "AA" identify the manufacture site. "YW" is the date code means manufacture year and week as following.

Note 2: The sample will be ready in 1 month.

The calendar year and the workweek coding scheme is as follows:

Year	Code	Year	Code
2010	A	2023	N
2011	B	2024	O
2012	C	2025	P
2013	D	2026	Q
2014	E	2027	R
2015	F	2028	S
2016	G	2029	T
2017	H	2030	U
2018	I	2031	V
2019	J	2032	W
2020	K	2033	X
2021	L	2034	Y
2022	M	2035	Z

Workweek	Code	Workweek	Code	Workweek	Code	Workweek	Code	Workweek	Code
1	1	14	E	27	R	40	e	53	r
2	2	15	F	28	S	41	f		
3	3	16	G	29	T	42	g		
4	4	17	H	30	U	43	h		
5	5	18	I	31	V	44	i		
6	6	19	J	32	W	45	j		
7	7	20	K	33	X	46	k		
8	8	21	L	34	Y	47	l		
9	9	22	M	35	Z	48	m		
10	A	23	N	36	a	49	n		
11	B	24	O	37	b	50	o		
12	C	25	P	38	c	51	p		
13	D	26	Q	39	d	52	q		

Absolute Maximum Ratings Note 1

Parameters	Rating
Supply Voltage, $(+V_S)-(-V_S)$	6 V
Input Voltage	$(-V_S)$ – 0.3 to $(+V_S)$ + 0.3
Differential Input Voltage	±6V
Input Current: +IN, –IN Note 2	±10mA
Output Short-Circuit Duration Note 3	Infinite
Maximum Junction Temperature	150°C
Operating Temperature Range	–40 to 125°C
Storage Temperature Range	–65 to 150°C
Lead Temperature (Soldering, 10 sec)	260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD Rating

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	6	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	2	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
5-Pin SC70	400		°C/W
5-Pin SOT23	250	81	°C/W
8-Pin SOIC	158	43	°C/W
8-Pin MSOP	210	45	°C/W
14-Pin SOIC	120	36	°C/W
14-Pin TSSOP	180	35	°C/W

Electrical Characteristics

All test condition is V_S = 5V, T_A = 25°C, R_L = 100kΩ to V_S/2, unless otherwise noted.

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Unit
Power Supply							
V_S	Supply Voltage Range			1.8		5.5	V
I_Q	Quiescent Current per Amplifier	V_S = 5V			500	600	nA
			-40°C to 125°C			900	nA
PSRR	Power Supply Rejection Ratio	V_S = 1.8V to 5.5V		70	90		dB
Input Characteristics							
V_{OS}	Input Offset Voltage	V_S = 5V, V_{CM} = 2.5V		-1.5	0.1	1.5	mV
			-40°C to 125°C	-2.5		2.5	mV
V_{OS} TC	Input Offset Voltage Drift		-40°C to 125°C		0.4		µV/°C
I_B	Input Bias Current				1		pA
			-40°C to 125°C		10		pA
I_{OS}	Input Offset Current				1		pA
C_{IN}	Input Capacitance	Differential Mode			3		pF
		Common Mode			5		pF
Av	Open-loop Voltage Gain			80	120		dB
V_{CMR}	Common-mode Input Voltage Range			(V-)		(V+)	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 3.5V		78	100		dB
		V_{CM} = 0V to 5V		60	80		dB
Output Characteristics							
V_{OH}	Output Swing from Positive Rail	R_{LOAD} = 100kΩ to V_S/2			10	30	mV
			-40°C to 125°C			50	mV
V_{OL}	Output Swing from Negative Rail	R_{LOAD} = 100kΩ to V_S/2			10	30	mV
			-40°C to 125°C			50	mV
I_{SC}	Output Short-Circuit Current				20		mA
AC Specifications							
GBW	Gain-Bandwidth Product				10		KHz
SR	Slew Rate	G = 1, 2V step			6		mV/µs
t_S	Settling Time, 0.1%	G = 1, 2V step			0.5		ms
	Settling Time, 0.01%				0.55		ms
PM	Phase Margin	R_L=100K, C_L=60pF			65		°
GM	Gain Margin	R_L=100K, C_L=60pF			10		dB
Noise Performance							
E_N	Input Voltage Noise	f = 0.1Hz to 10Hz			10		$µV_{PP}$
e_N	Input Voltage Noise Density	f = 1kHz			265		nV/√Hz

Typical Performance Characteristics

V_S = 5V, V_{CM} = 2.5V, RL = Open, unless otherwise specified.

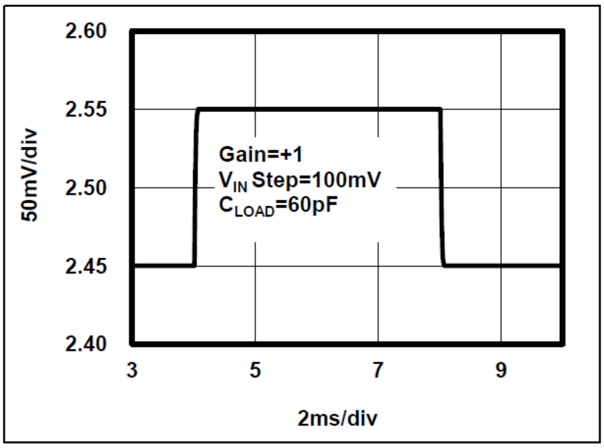


Figure 1. Small-Signal Step Response, 100mV Step

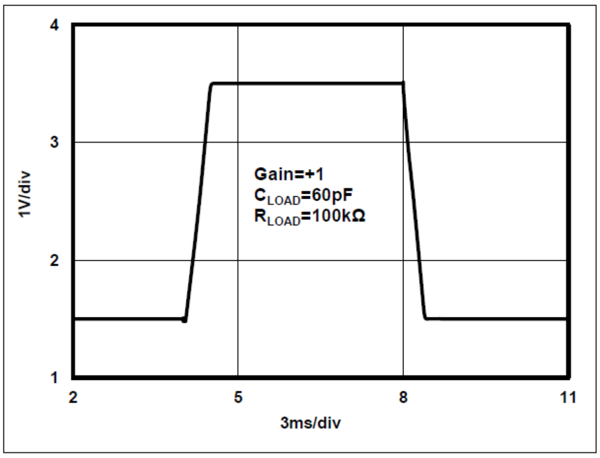


Figure 2. Large-Signal Step Response, 2V Step

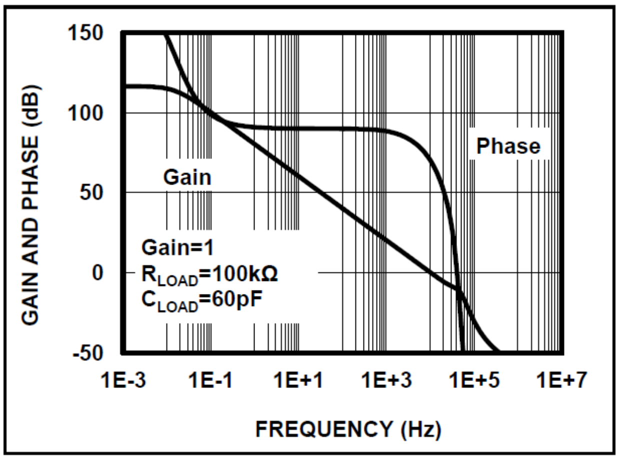


Figure 3. Open-Loop Gain and Phase

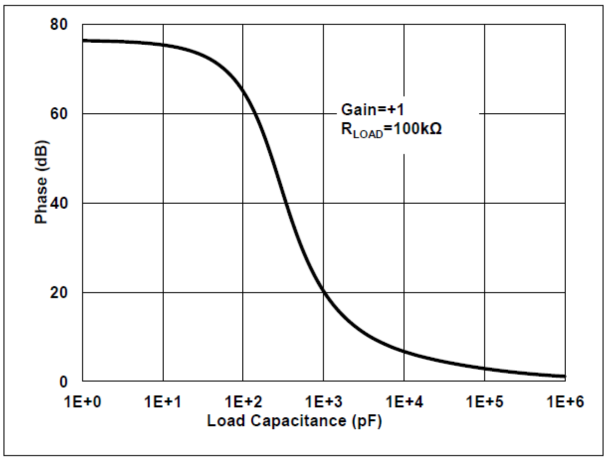


Figure 4. Phase Margin vs. C_{LOAD} (Stable for Any C_{LOAD})

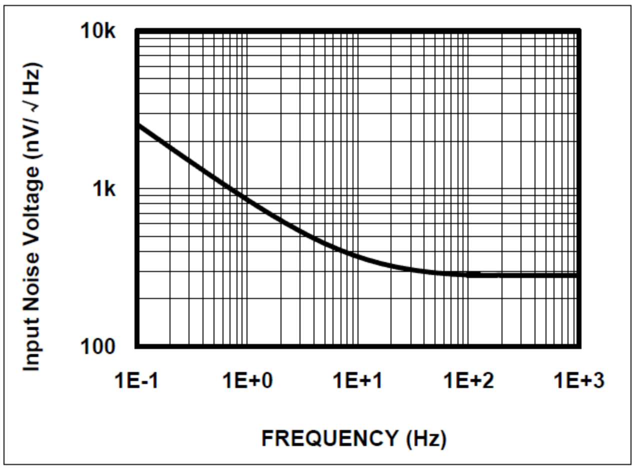


Figure 5. Input Voltage Noise Spectral Density

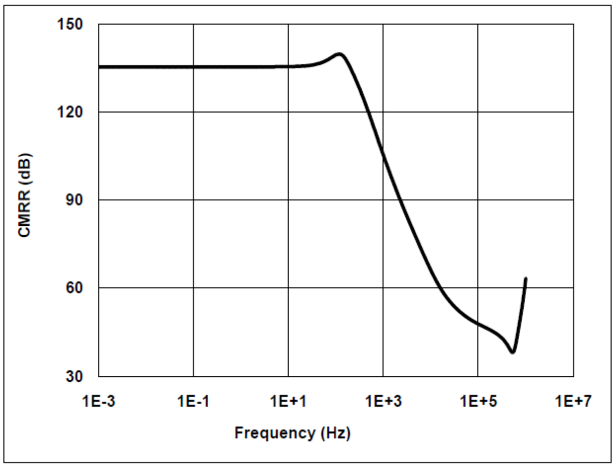


Figure 6. Common-Mode Rejection Ratio

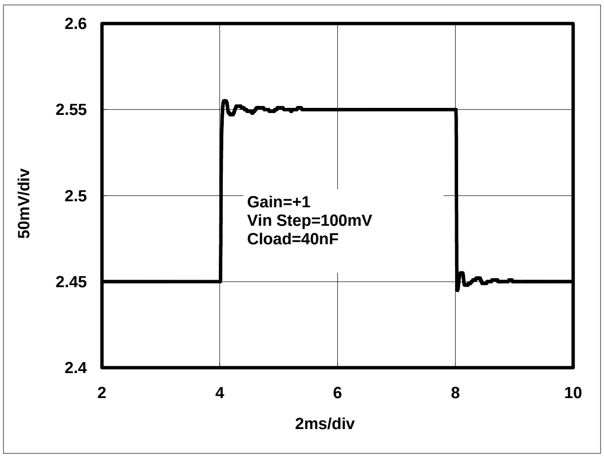


Figure 7. Over-Shoot Voltage, C_{LOAD} = 40nF, Gain = +1, RFB=100kΩ

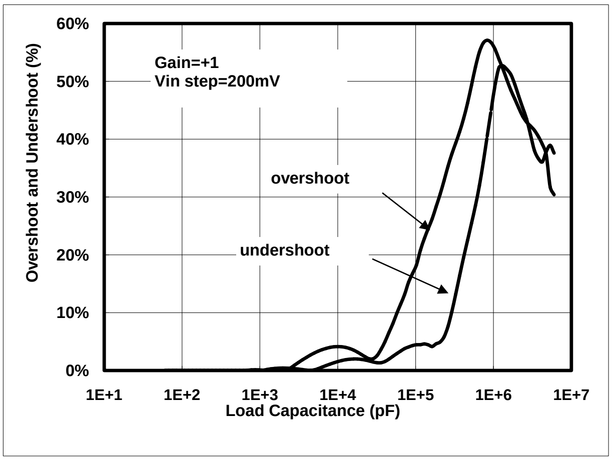


Figure 8. Over-Shoot % vs. C_{LOAD}, Gain = +1, RFB = 1MΩ

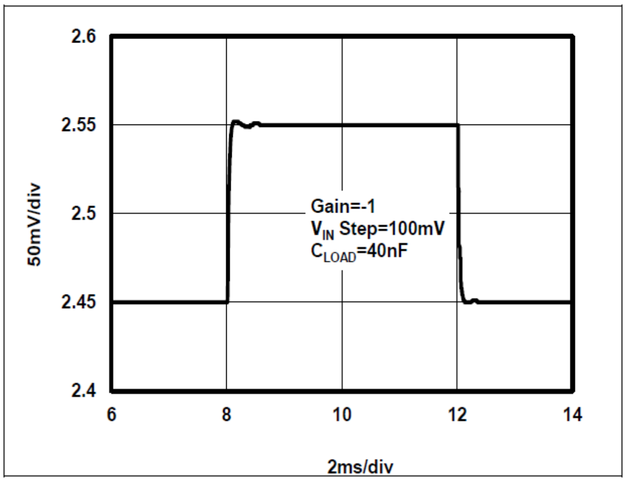


Figure 9. Over-Shoot Voltage, C_{LOAD}=40nF, Gain= -1, RFB=100kΩ

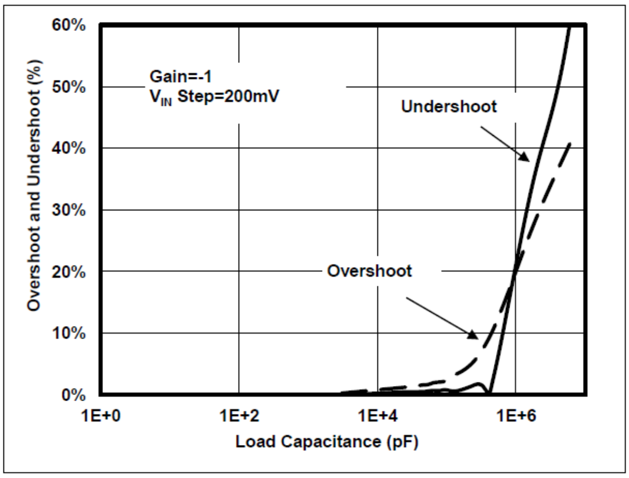


Figure 10. Over-Shoot % vs. C_{LOAD}, Gain = -1, RFB = 1MΩ

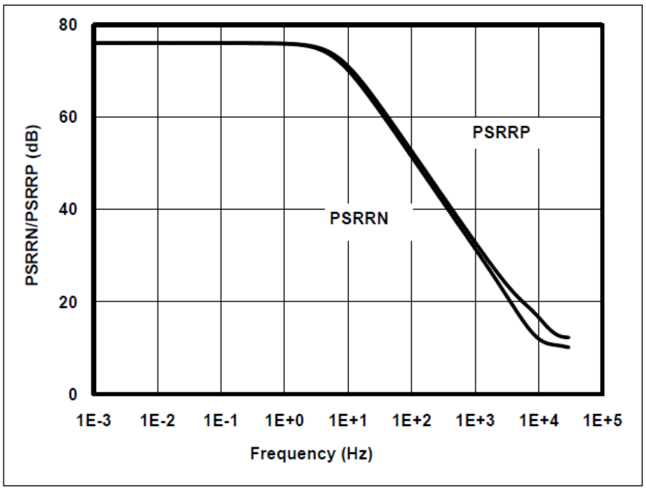


Figure 11. Power-Supply Rejection Ratio

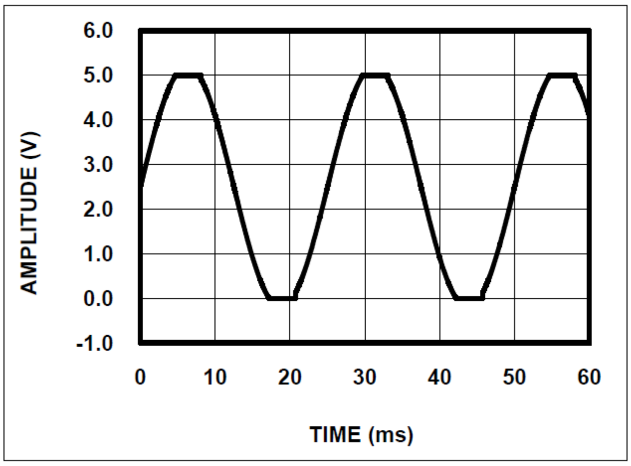


Figure 12. VIN = -0.2V to 5.2V, No Phase Reversal

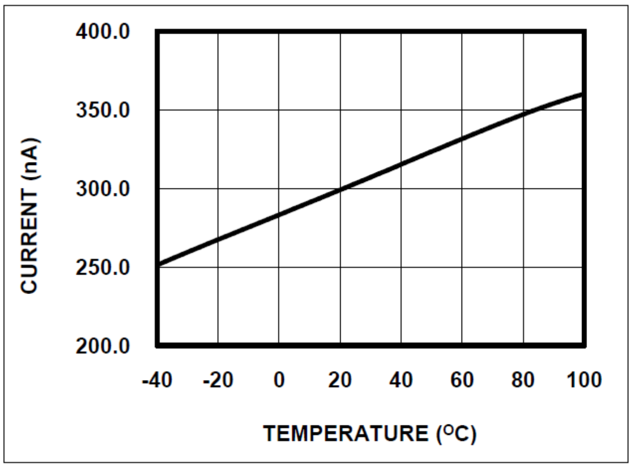


Figure 13. Quiescent Supply Current vs. Temperature

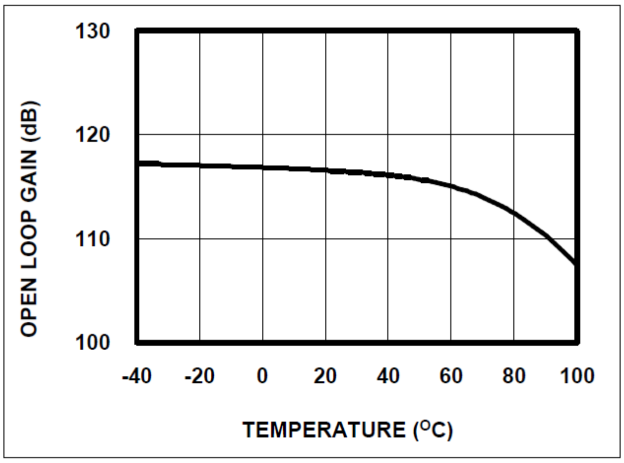


Figure 14. Open-Loop Gain vs. Temperature

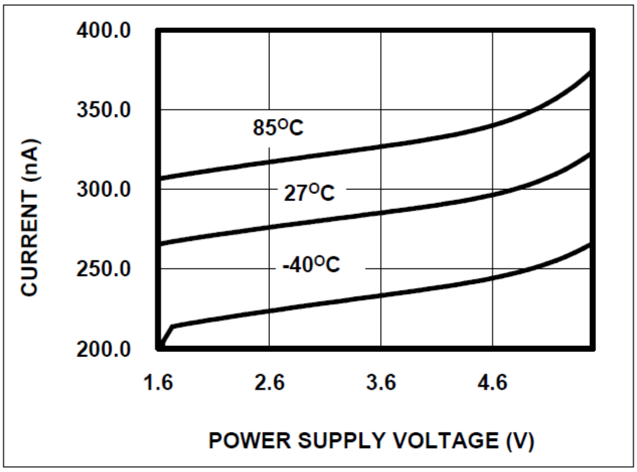


Figure 15. Quiescent Supply Current vs. Supply Voltage

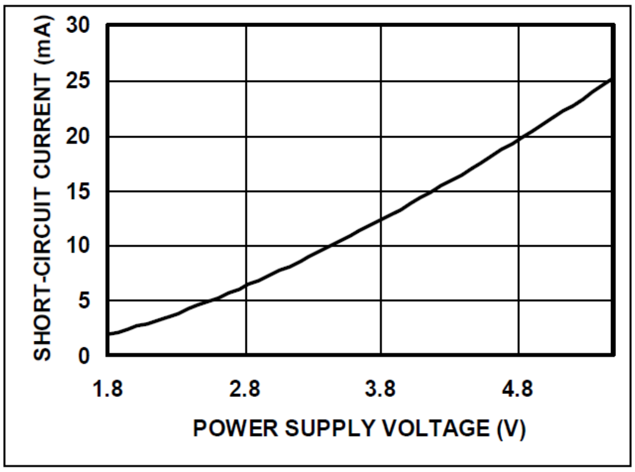


Figure 16. Short-Circuit Current vs. Supply Voltage

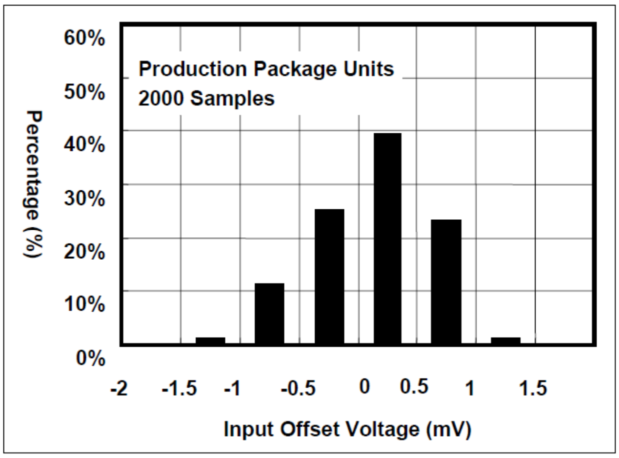


Figure 17. Input Offset Voltage Distribution

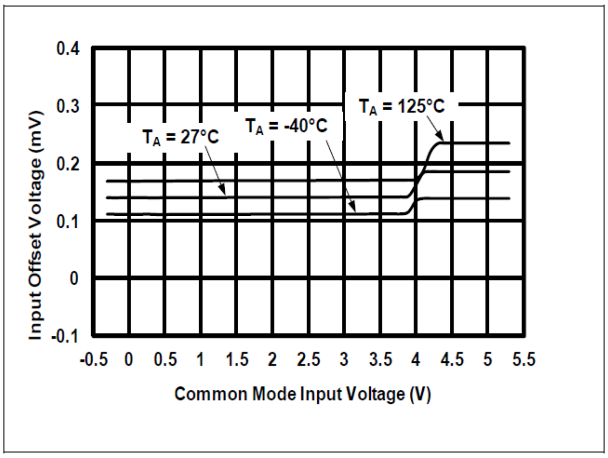


Figure 18. Input Offset Voltage vs. Common Mode Input Voltage

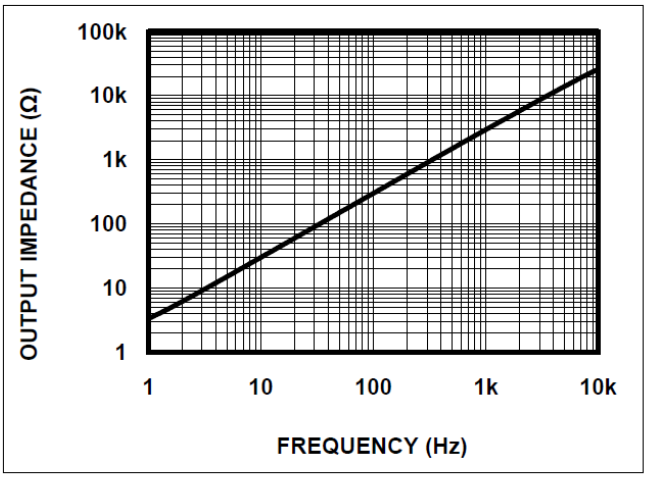


Figure 19. Closed-Loop Output Impedance vs. Frequency

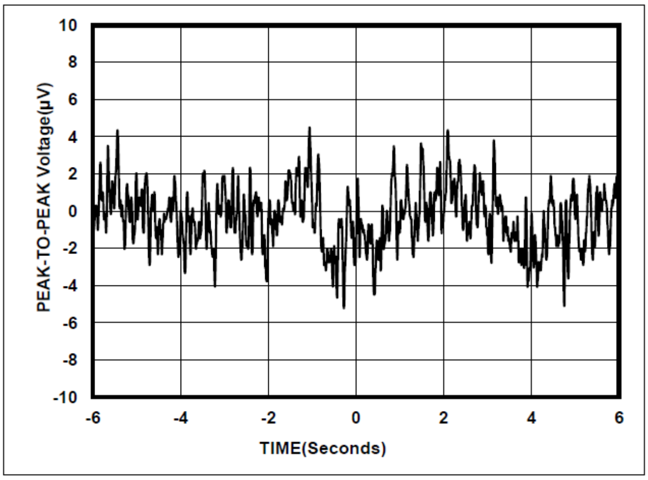


Figure 20. 0.1Hz to 10Hz Time Domain Output Voltage Noise

Application Information

Low Supply Voltage and Low Power Consumption

The TP211X family of operational amplifiers can operate with power supply voltages from 2.1V to 6.0V. Each amplifier draws only 300nA quiescent current. The low supply voltage capability and low supply current are ideal for portable applications demanding HIGH CAPACITIVE LOAD DRIVING CAPABILITY and CONSTANT WIDE BANDWIDTH. The TP211X family is optimized for wide bandwidth low power applications. They have an industry leading high GBWP to power ratio and are unity gain stable for ANY CAPACITIVE load. When the load capacitance increases, the increased capacitance at the output pushed the non-dominant pole to lower frequency in the open loop frequency response, lowering the phase and gain margin. Higher gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin.

Low Input Referred Noise

The TP211X family provides a low input referred noise density of 296nV/√Hz at 1kHz. The voltage noise will grow slowly with the frequency in wideband range, and the input voltage noise is typically 12μV_{P-P} at the frequency of 0.1Hz to 10Hz.

Low Input Offset Voltage

The TP211X family has a low offset voltage of 1.5mV maximum which is essential for precision applications. The offset voltage is trimmed with a proprietary trim algorithm to ensure low offset voltage for precision signal processing requirement.

Low Input Bias Current

The TP211X family is a CMOS OPA family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on "PCB Surface Leakage" for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the TP211X OPA's input bias current at +27°C (±1pA, typical). It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 1 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common Mode input voltage.
2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

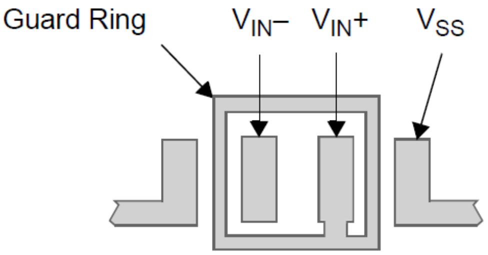


Figure 1

Ground Sensing and Rail to Rail Output

The TP211X family has excellent output drive capability, delivering over 10mA of output drive current. The output stage is a rail-to-rail topology that is capable of swinging to within 10mV of either rail. Since the inputs can go 300mV beyond either rail, the op-amp can easily perform ‘true ground’ sensing.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

ESD

The TP211X family has reverse-biased ESD protection diodes on all inputs and output. Input and out pins can not be biased more than 300mV beyond either supply rail.

Driving Large Capacitive Load

The TP211X family of OPA is designed to drive large capacitive loads. Refer to Typical Performance Characteristics for “Phase Margin vs. Load Capacitance”. As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop’s phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer (G = +1V/V) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the TP211X OPA family (e.g., > 200 pF when G = +1V/V), a small series resistor at the output (R_{ISO} in Figure 3) improves the feedback loop’s phase margin and stability by making the output load resistive at higher frequencies.

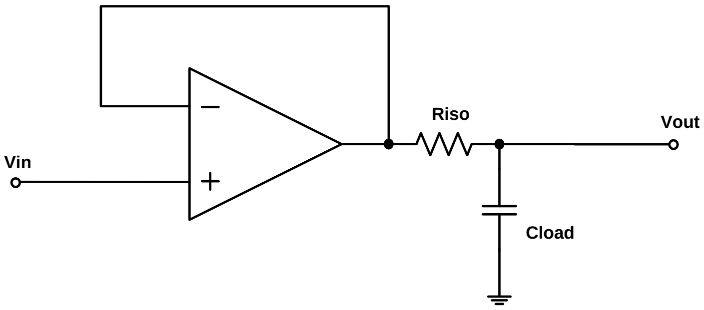


Figure 3

Power Supply Layout and Bypass

The TP211X OPA’s power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA’s inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps’ pins as possible.

Proper Board Layout

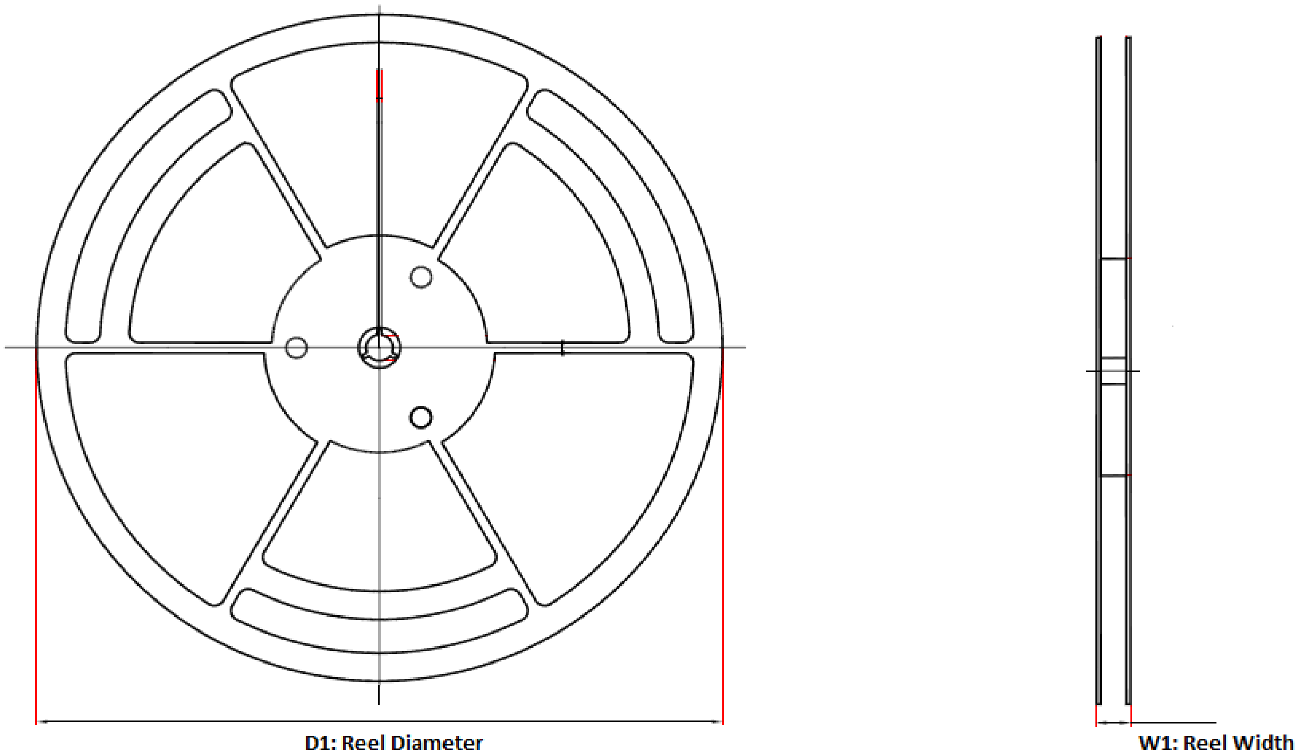
To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

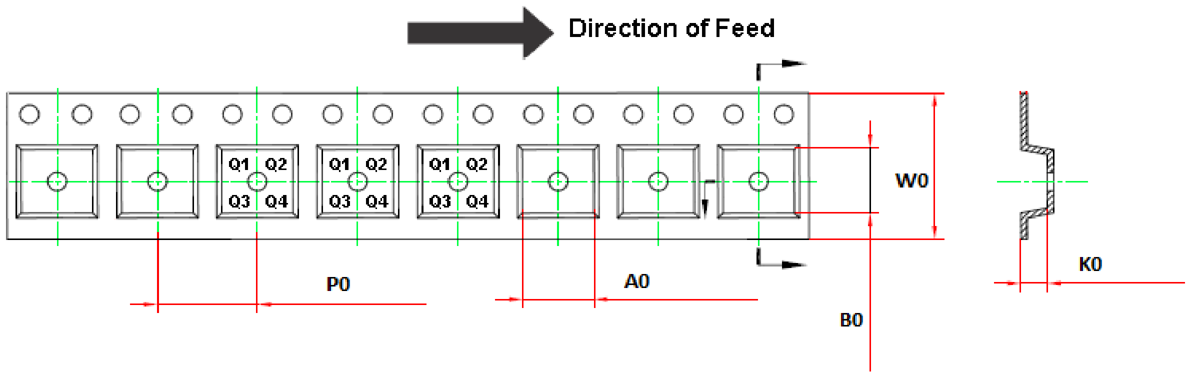
Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

Tape and Reel Information

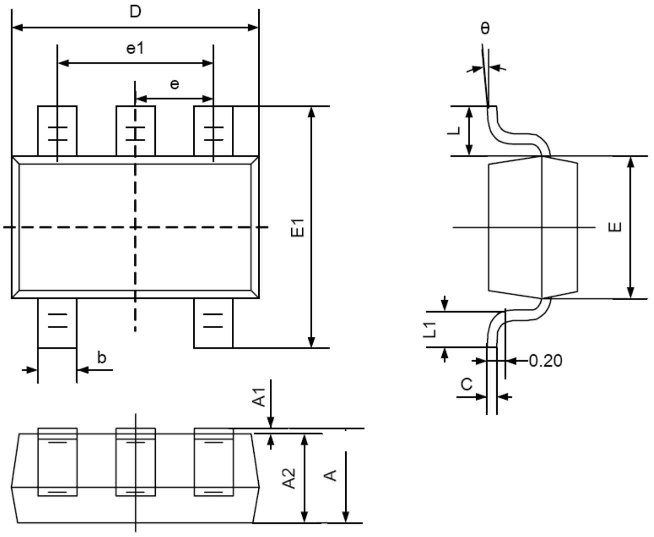




Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TP2111-CR	5-Pin SC70	178.0	12.3	2.4	2.5	1.2	4.0	8.0	Q3
TP2111-TR	5-Pin SOT23	180.0	13.1	3.2	3.2	1.4	4.0	8.0	Q3
TP2112-SR	8-Pin SOIC	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TP2112-VR	8-Pin MSOP	330.0	17.6	5.2	3.3	1.5	8.0	12.0	Q1
TP2114-SR	14-Pin SOIC	330.0	21.6	6.5	9.0	2.1	8.0	16.0	Q1
TP2114-TR	14-Pin TSSOP	330.0	17.6	6.8	5.4	1.2	8.0	12.0	Q1

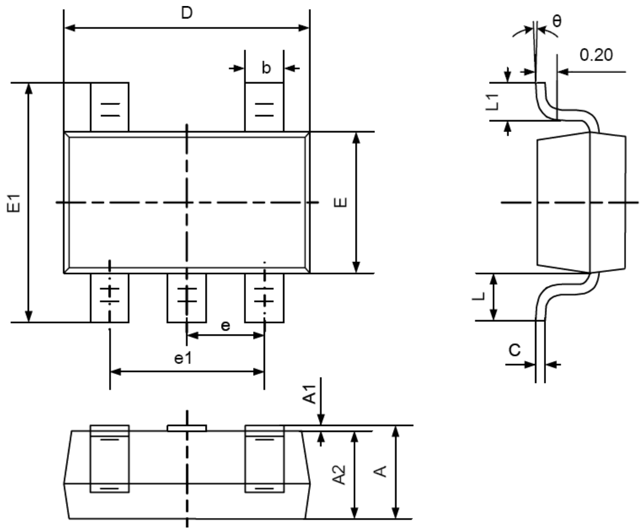
Package Outline Dimensions

SC70-5



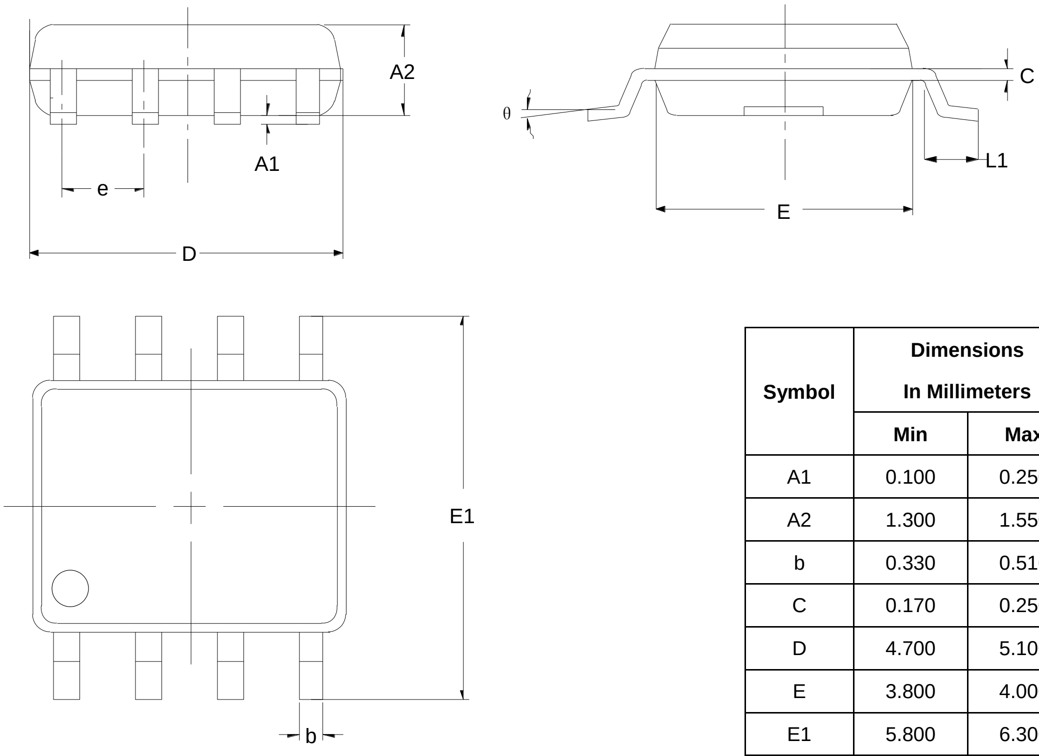
Symbol	Dimensions In Millimeters	
	Min	Max
A	0.900	1.100
A1	0.000	0.100
A2	0.900	1.000
b	0.150	0.350
C	0.110	0.175
D	2.000	2.200
E	1.150	1.350
E1	2.150	2.450
e	0.650TYP	
e1	1.200	1.400
L	0.525REF	
L1	0.260	0.460
θ	0°	8°

SOT23-5



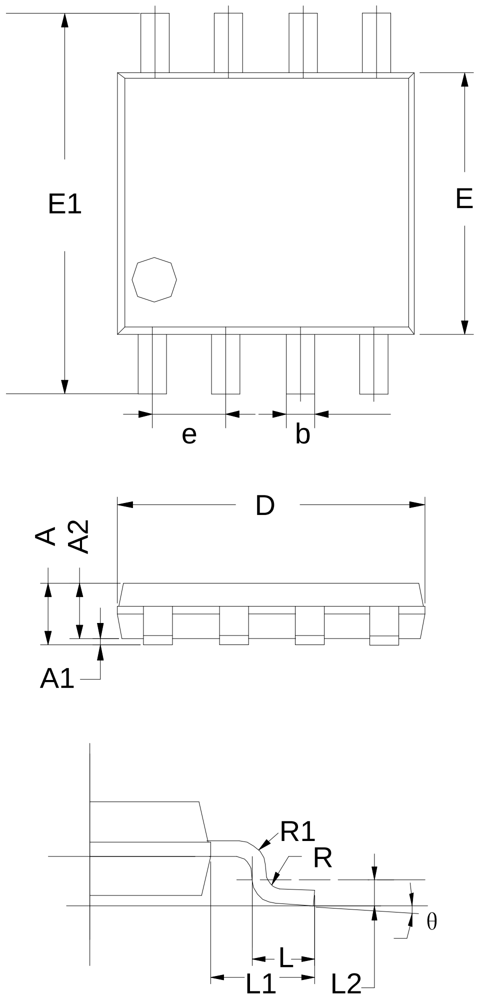
Symbol	Dimensions In Millimeters	
	Min	Max
A	1.050	1.250
A1	0.000	0.100
A2	1.000	1.150
b	0.300	0.500
C	0.100	0.200
D	2.820	3.020
E	1.500	1.700
E1	2.600	3.000
e	0.950TYP	
e1	1.800	2.000
L	0.600REF	
L1	0.300	0.600
θ	0°	8°

SOIC-8



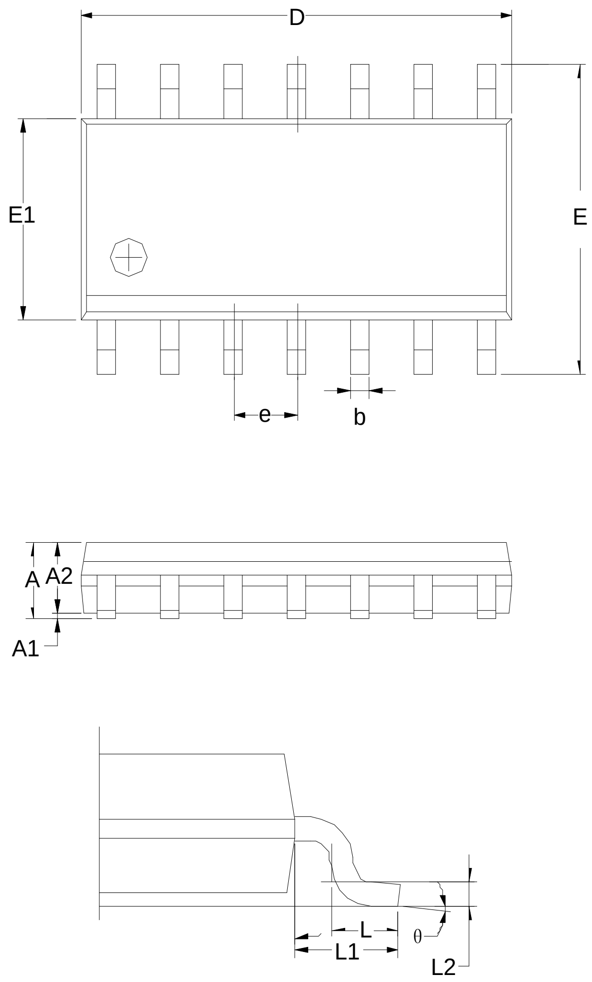
Symbol	Dimensions In Millimeters	
	Min	Max
A1	0.100	0.250
A2	1.300	1.550
b	0.330	0.510
C	0.170	0.250
D	4.700	5.100
E	3.800	4.000
E1	5.800	6.300
e	1.270TYP	
L1	0.400	0.900
θ	0°	8°

MSOP-8



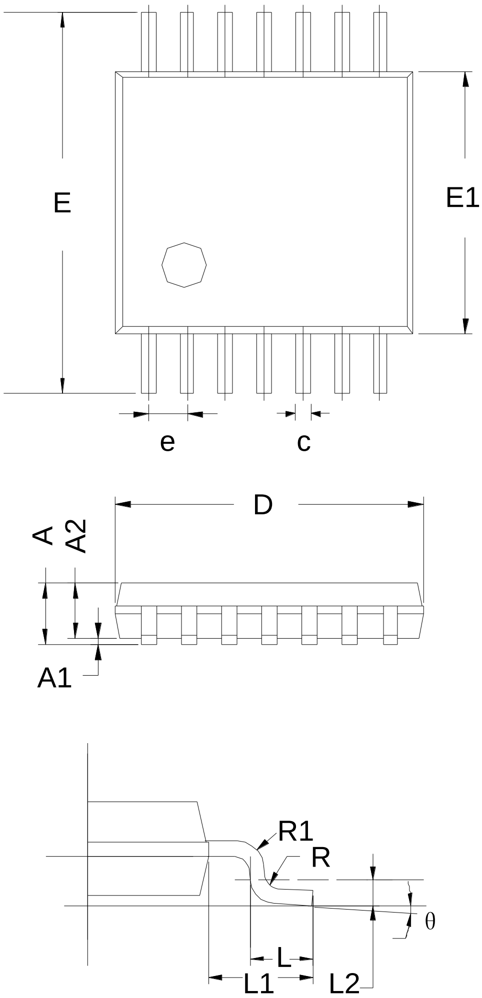
Symbol	Dimensions In Millimeters	
	Min	Max
A	0.800	1.200
A1	0.000	0.200
A2	0.750	0.950
b	0.30 TYP	
C	0.15 TYP	
D	2.900	3.100
e	0.65 TYP	
E	2.900	3.100
E1	4.700	5.100
L	0.400	0.800
L1	0.95 TYP	
L2	0.25 TYP	
θ	0°	6°

SOIC-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.31		0.51
D	8.45	8.63	8.85
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	0.60	0.80
L1	1.05 REF		
L2	0.25 BSC		
θ	0°		8°

TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
c	0.19	-	0.30
D	4.86	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°