Ordering Information

RT9078/N-□□□□□

- Pin 1 Orientation***
  (2) : Quadrant 2, Follow EIA-481-D
- Package Type
  J5 : TSOT-23-5
  QZ : ZQFN-4L 1x1 (Z-Type)
  (ZDFN-4L 1x1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Output Voltage
  08 : 0.8V
  :
  33 : 3.3V
  1B : 1.25V
  1H : 1.85V
  2H : 2.85V
  1K : 1.05V
  3D : 3.45V (ZQFN-4L 1x1 only)
  Special Request : Any voltage between 0.8V and 3.3V under specific business agreement
- Pin Function
  RT9078 : Without SNS Pin
  RT9078N : With SNS Pin**

Note :

***Empty means Pin1 orientation is Quadrant 1

**Available for output target adjustment (Ex : RT9078N-08GJ5 with 0.8V reference level for output target adjustment)

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

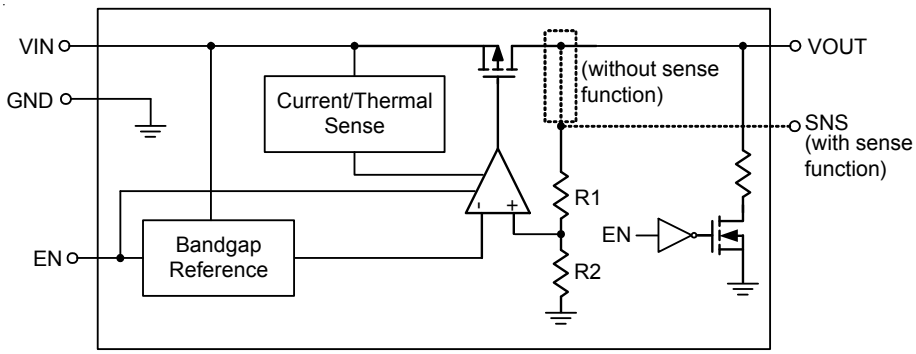
Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Functional Pin Description

Pin No.		Pin Name	Pin Function
TSOT-23-5	ZQFN-4L 1x1 (ZDFN-4L 1x1)		
1	4	VIN	Regulator input pin. Input capacitor should be placed directly at this pin.
2	2	GND	Ground.
3	3	EN	Chip enable pin. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value.
4	--	SNS	Output voltage sense. (RT9078N only)
		NC	No internal connection.
5	1	VOUT	Regulator output pin. Output capacitor should be placed directly at this pin.
--	5 (Exposed Pad)	SGND	Substrate of chip. Tie to GND plane for maximum thermal dissipation.

Functional Block Diagram



Operation

Basic Operation

The RT9078 is a low quiescent current linear regulator designed especially for low external components system. The input voltage range is from 1.2V to 5.5V.

The minimum required output capacitance for stable operation is 1μF capacitance after consideration of the temperature and voltage coefficient of the capacitor.

Pass Transistor

The RT9078 builds in a P-MOSFET pass transistor which provides a low switch-on resistance for low dropout voltage applications.

Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider, and controls the gate voltage of P-MOSFET.

Chip Enable and Shutdown

The RT9078 provides an EN pin, as an external chip enable control, to enable or disable the device. The V_{EN} below 0.4V turns the regulator off and enters the shutdown mode, while V_{EN} above 0.9V turns the regulator on. When the regulator is shutdown, the ground current is reduced to a maximum of 0.5μA.

Current-Limit Protection

The RT9078 contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 0.6A (typ.). The current limiting level is reduced to around 0.3A named fold-back current limit when the output voltage is further decreased. The output can be shorted to ground indefinitely without damaging the part.

Over-Temperature Protection

The over-temperature protection function will turn off the P-MOSFET when the junction temperature exceeds 150°C (typ.), and the output current exceeds 80mA. Once the junction temperature cools down by approximately 20°C, the regulator will automatically resume operation.

Output Active Discharge

When the RT9078 is operating at shutdown mode, the device has an internal active pull down circuit that connects the output to GND through a resistor for output discharging purpose.

Absolute Maximum Ratings (Note 1)

- VIN, VOUT, SNS, EN to GND ---------- –0.3V to 6.5V
- VOUT to VIN ---------- –6.5V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  - TSOT-23-5 ---------- 0.43W
  - ZQFN-4L 1x1 (ZDFN-4L 1x1) ---------- 0.44W
- Package Thermal Resistance (Note 2)
  - TSOT-23-5, θ_{JA} ---------- 230.6°C/W
  - TSOT-23-5, θ_{JC} ---------- 21.8°C/W
  - ZQFN-4L 1x1 (ZDFN-4L 1x1), θ_{JA} ---------- 226°C/W
  - ZQFN-4L 1x1 (ZDFN-4L 1x1), θ_{JC} ---------- 43°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage, VIN ---------- 1.2V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{OUT} + 1 < V_{IN} < 5.5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Fixed Output Voltage Range	V_{OUT}		0.8	--	3.45	V
DC Output Accuracy		I_{LOAD} = 1mA	–2	--	2	%
SNS Reference Voltage (for RT9078N-08GJ5 only)	V_{REF}	I_{LOAD} = 1mA	0.784	0.8	0.816	V
Dropout Voltage (I_{LOAD} = 300mA) (Note 5)	V_{DROP}	0.8V ≤ V_{OUT} < 1.05V	--	0.7	0.97	V
		1.05V ≤ V_{OUT} < 1.2V	--	0.5	0.92	
		1.2V ≤ V_{OUT} < 1.5V	--	0.4	0.57	
		1.5V ≤ V_{OUT} < 1.8V	--	0.3	0.47	
		1.8V ≤ V_{OUT} < 2.1V	--	0.24	0.33	
		2.1V ≤ V_{OUT} < 2.5V	--	0.21	0.3	
		2.5V ≤ V_{OUT} < 2.8V	--	0.18	0.25	
		2.8V ≤ V_{OUT} < 3V	--	0.16	0.23	
		3V ≤ V_{OUT}	--	0.15	0.2	
Dropout Voltage (I_{LOAD} = 200mA) (Note 6)	V_{DROP}	1.8V ≤ V_{OUT} < 2.1V	--	0.16	0.2	V
V_{CC} Consumption Current	I_Q	I_{LOAD} = 0mA, V_{OUT} ≤ 5.5V V_{IN} ≥ V_{OUT} + V_{DROP}	--	2	4	μA

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Shutdown GND Current (Note 7)			V_{EN} = 0V		--	0.1	0.5	μA
Shutdown Leakage Current (Note 7)			V_{EN} = 0V, V_{OUT} = 0V		--	0.1	0.5	μA
EN Input Current		I_{EN}	V_{EN} = 5.5V		--	--	0.1	μA
Line Regulation		ΔLINE	I_{LOAD} = 1mA	1.2V ≤ V_{IN} < 1.5V	--	0.3	0.6	%
				1.5V ≤ V_{IN} < 1.8V	--	0.15	0.3	
				1.8V ≤ V_{IN} ≤ 5.5V	--	0.13	0.35	
Load Regulation		ΔLOAD	1mA < I_{LOAD} < 300mA		--	0.5	1	%
Power Supply Rejection Ratio		PSRR	V_{IN} = 3V, I_{LOAD} = 50mA, C_{OUT} = 1μF, V_{OUT} = 2.5V, f = 1kHz		--	75	--	dB
Output Voltage Noise			C_{OUT} = 1μF, I_{LOAD} = 150mA, BW = 10Hz to 100kHz, V_{IN} = V_{OUT} + 1V	V_{OUT} = 0.8V	--	38	--	μV_{RMS}
				V_{OUT} = 1.2V	--	46	--	
				V_{OUT} = 1.8V	--	48	--	
				V_{OUT} = 3.3V	--	51	--	
Output Current Limit		I_{LIM}	V_{OUT} = 90% of $V_{OUT(NOM)}$		350	600	--	mA
Enable Threshold Voltage	H-Level	V_{ENH}	V_{IN} = 5V		0.5	0.7	0.9	V
	L-Level	V_{ENL}	V_{IN} = 5V		0.4	0.65	0.85	
Thermal Shutdown Temperature		T_{SD}	I_{LOAD} = 30mA, V_{IN} ≥ 1.5V		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}			--	20	--	°C
Discharge Resistance			EN = 0V, V_{OUT} = 0.1V		--	80	--	Ω

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Richtek Evaluation Board for ZQFN-4L 1x1 (ZDFN-4L1x1) Package.

θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7 for TSOT-23-5 Package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. The dropout voltage is defined as V_{IN} – V_{OUT}, when V_{OUT} is 98% of the normal value of V_{OUT}.

Note 6. For the application under following condition :

1.8V ≤ V_{OUT} < 2.1V, I_{LOAD} = 200mA, T_A = 85°C, the maximum dropout voltage is guaranteed by design that not over 0.28V.

Note 7. The specification is tested at wafer stage and guaranteed by design after assembly.

Typical Application Circuit

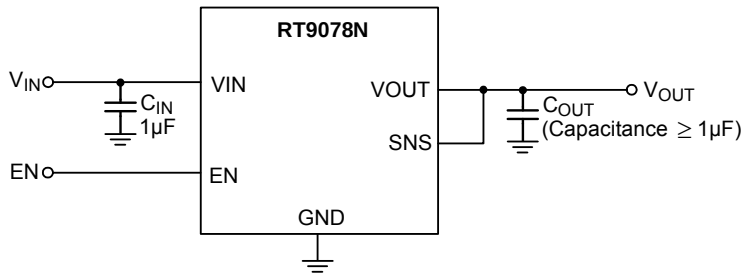


Figure 1. Application with Sense Function

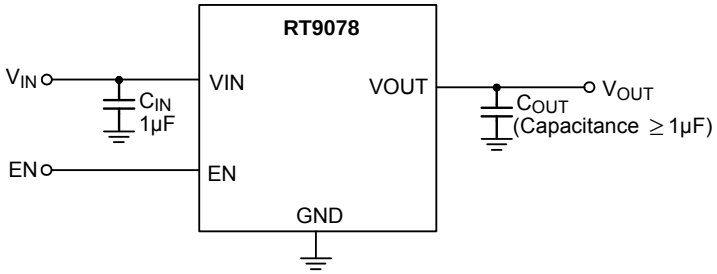


Figure 2. Application without Sense Function

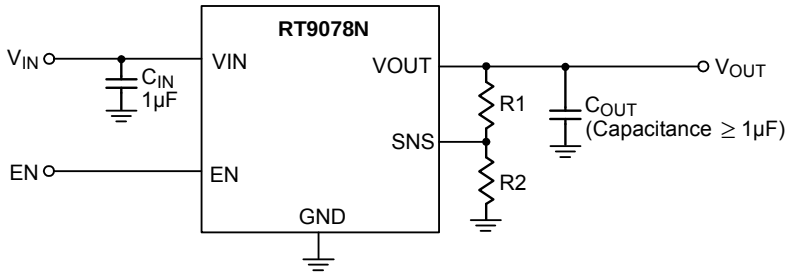


Figure 3. Adjustable Output Voltage Application Circuit

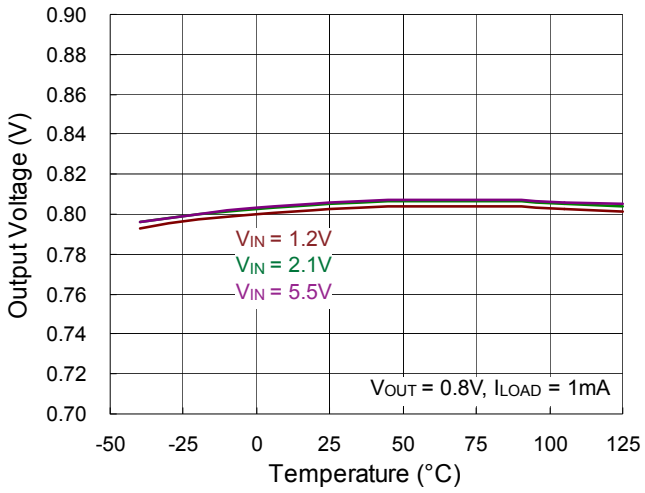
Table 1. Recommended External Components

Component	Description	Vendor P/N
C_{IN}	1μF, 10V, X5R, 0402	GRM155R61A105KE15 (Murata)
* C_{OUT}	1μF, 6.3V, X5R, 0402	GRM153R60J105ME95(Murata) CGB2A3X5R0J105M033BB(TDK)
	2.2μF, 6.3V, X5R, 0402	GRM153R60J225ME95 (Murata) C1005X5R0J225M050BC (TDK)
	4.7μF, 6.3V, X5R, 0402	GRM153R60J475ME15 (Murata) C1005X5R0J475K050BE(TDK)

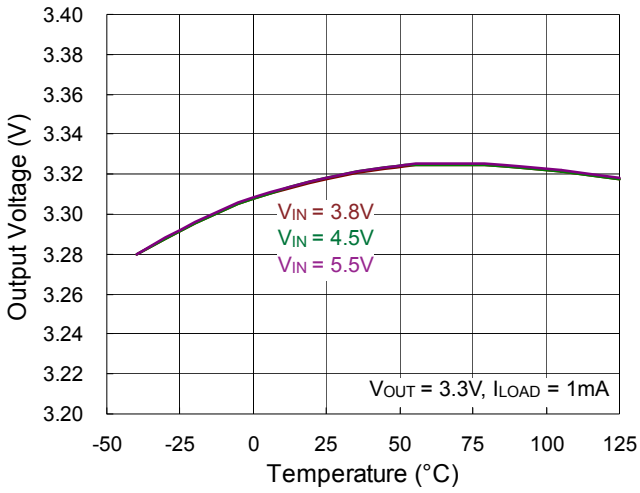
*: Considering the effective capacitance derated with biased voltage level, the C_{OUT} component needs satisfy the effective capacitance at least 0.7μF or above at targeted output level for stable and normal operation.

Typical Operating Characteristics

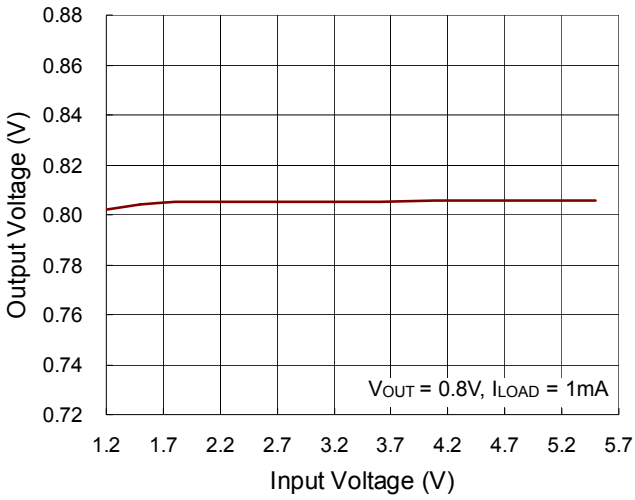
Output Voltage vs. Temperature



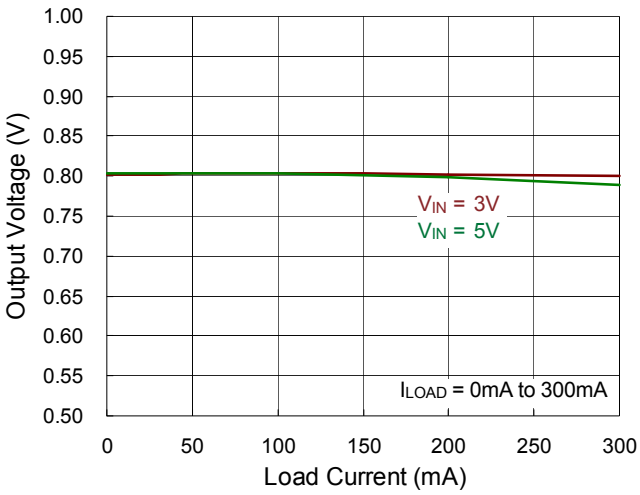
Output Voltage vs. Temperature



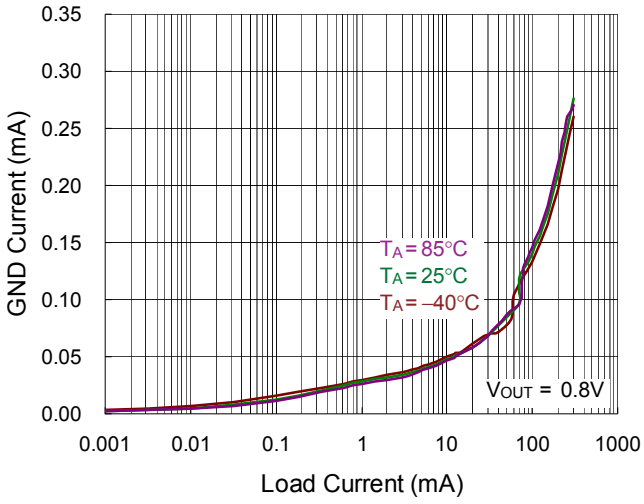
Output Voltage vs. Input Voltage



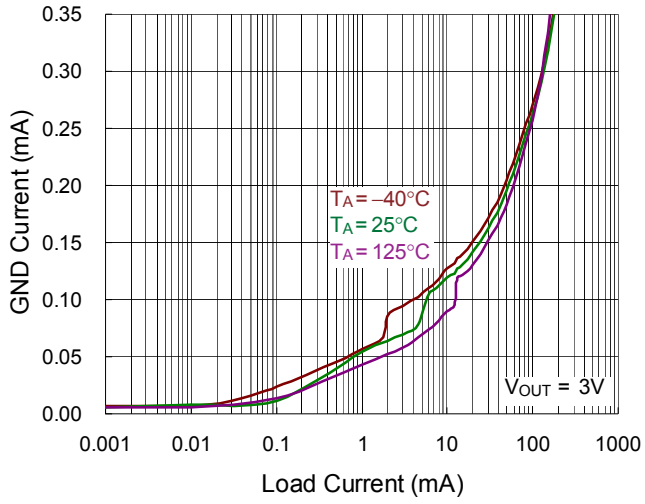
Output Voltage vs. Load Current



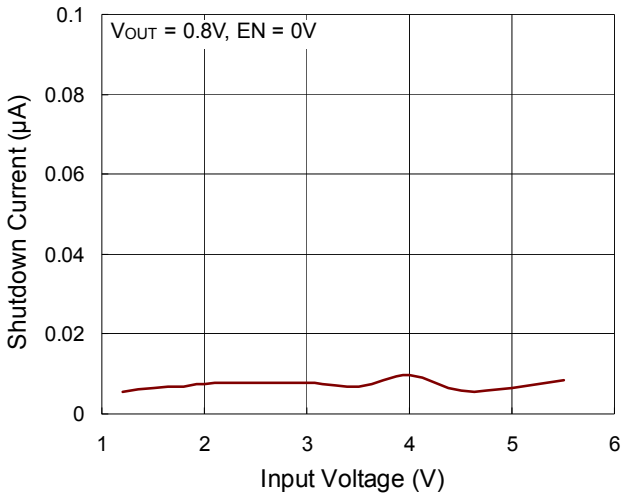
Ground Current vs. Load Current



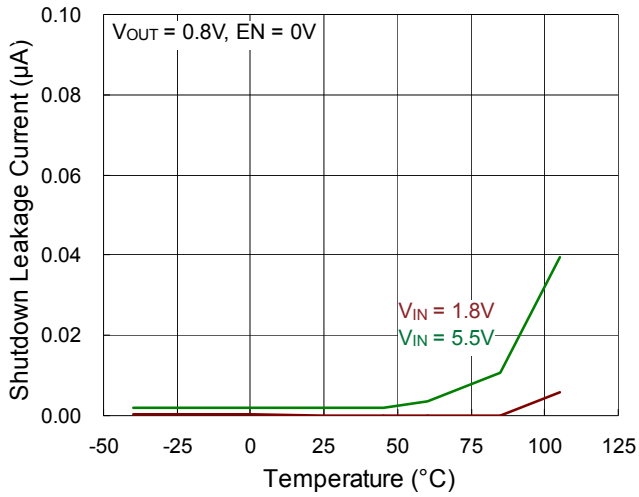
Ground Current vs. Load Current



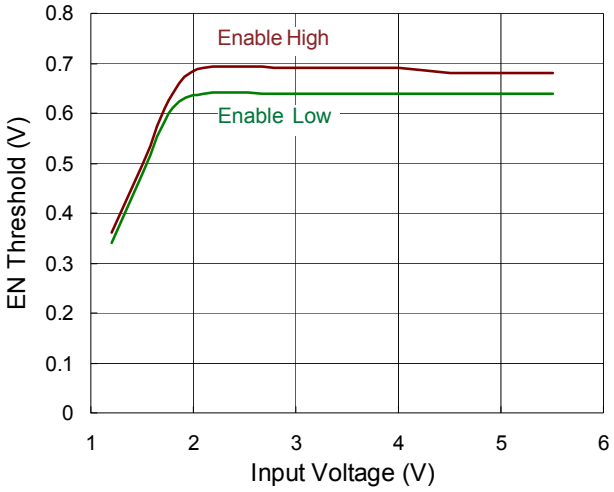
Shutdown Current vs. Input Voltage



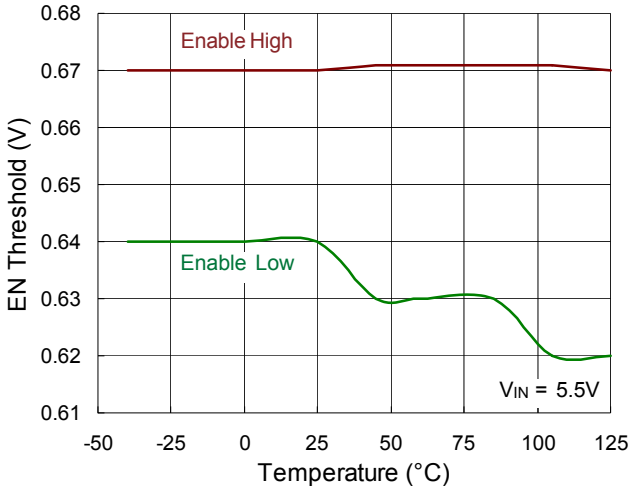
Shutdown Leakage Current vs. Temperature



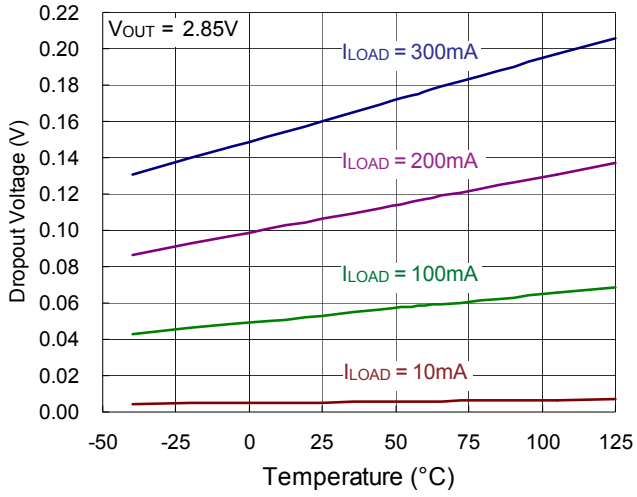
EN Threshold vs. Input Voltage



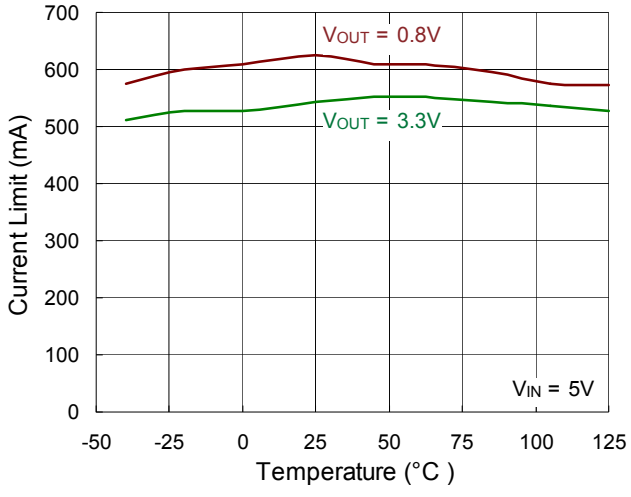
EN Threshold vs. Temperature



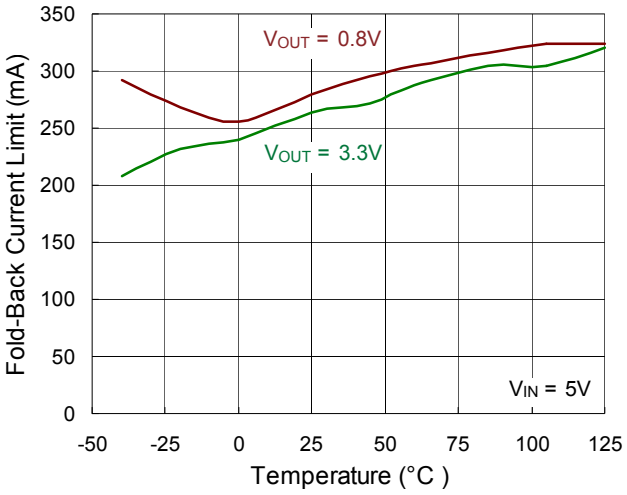
Dropout Voltage vs. Temperature



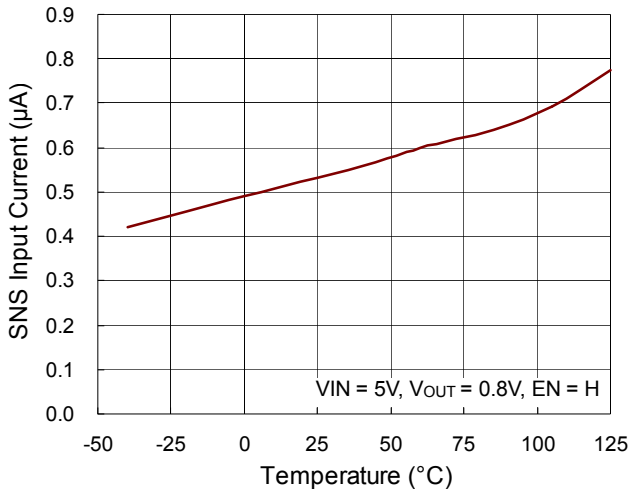
Current Limit vs. Temperature



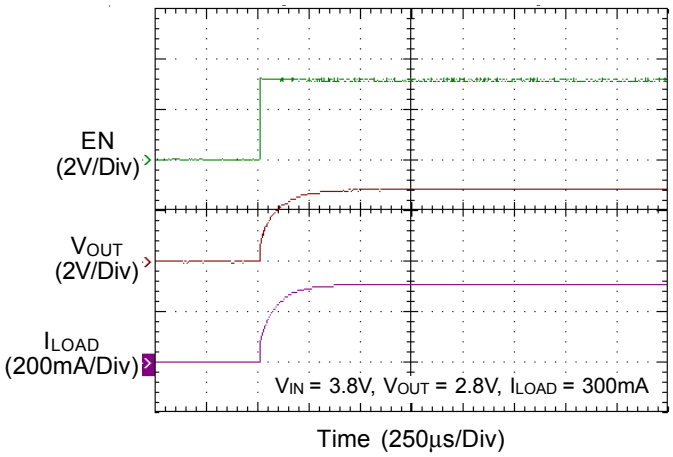
Fold-Back Current Limit vs. Temperature



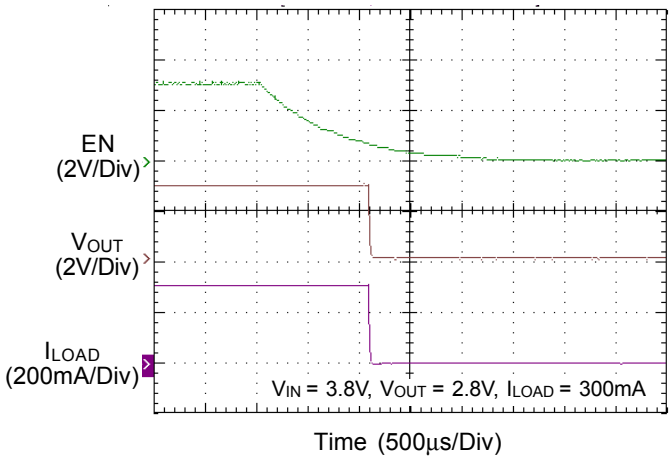
SNS Input Current vs. Temperature



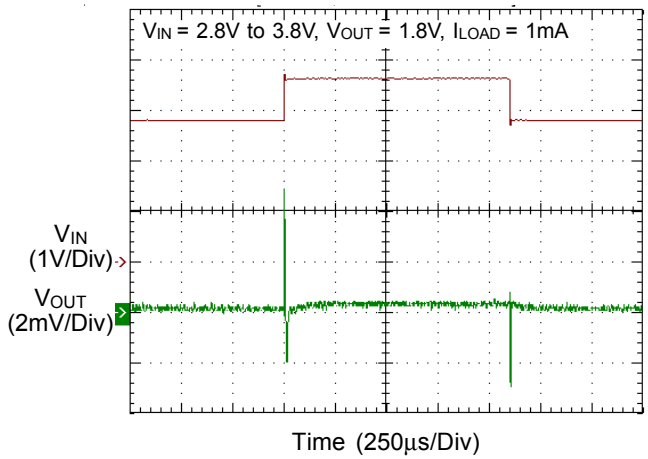
Power On from EN



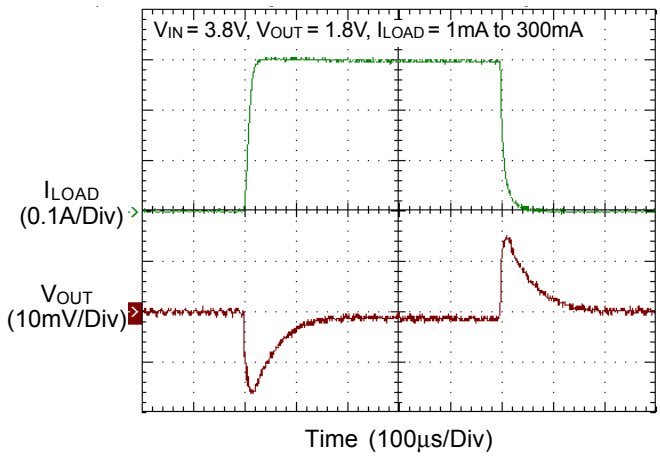
Power Off from EN



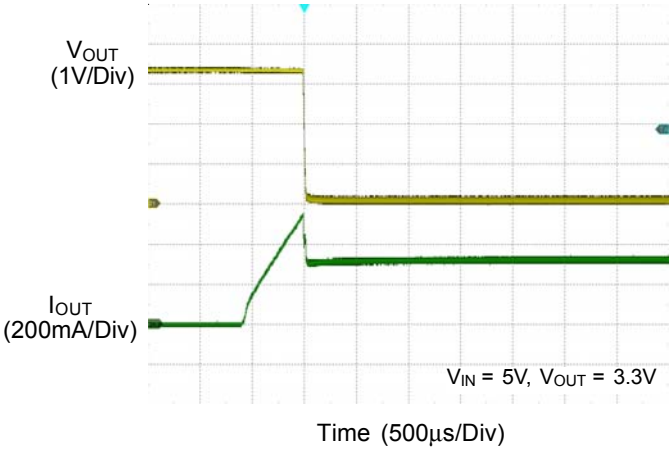
Line Transient



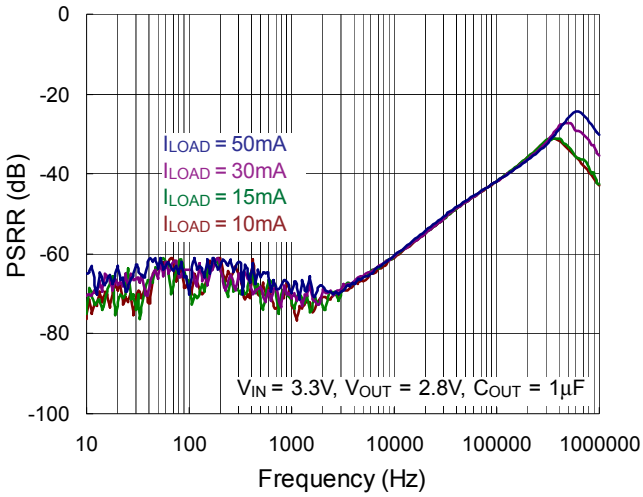
Load Transient



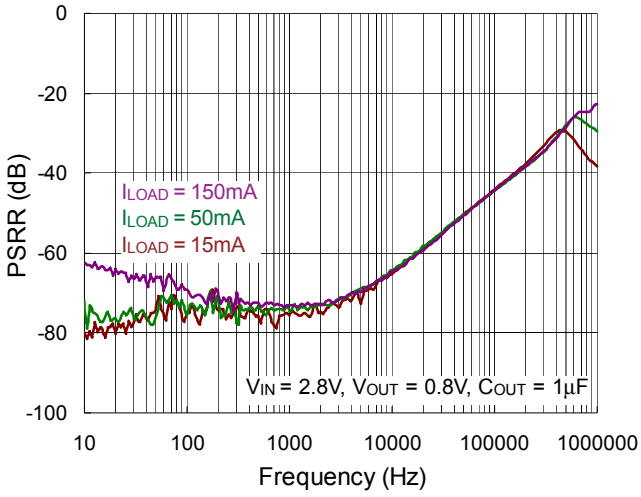
Output Current Limit Protection



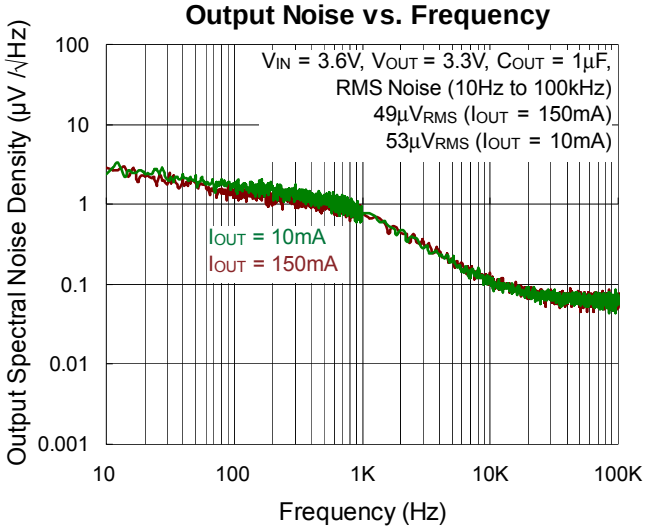
PSRR vs. Frequency



PSRR vs. Frequency



Output Noise vs. Frequency



Application Information

Like any low dropout linear regulator, the RT9078's external input and output capacitors must be properly selected for stability and performance. Use a 1μF or larger input capacitor and place it close to the IC's VIN and GND pins. Any output capacitor meeting the minimum 1mΩ ESR (Equivalent Series Resistance) and capacitance larger than 1μF requirement may be used. Place the output capacitor close to the IC's VOUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DROP} also can be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance $R_{DS(ON)}$. Thus the dropout voltage can be defined as ($V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED}$). For normal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + V_{DROP}$) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

Adjustable Output Voltage Setting

Because of the small input current at the SNS pin, the RT9078N with SNS pin also can work as an adjustable output voltage LDO. Figure 3 gives the connections for the adjustable output voltage application. The resistor divider from VOUT to SNS sets the output voltage when in regulation.

The voltage on the SNS pin sets the output voltage and is determined by the values of R1 and R2. The adjustable output voltage can be calculated using the formula given in equation 1 :

$$V_{OUT} = \frac{R1 + R2}{R2} \times V_{SNS} \quad (1)$$

where V_{SNS} is determined by the output voltage selections in the ordering information of the RT9078N (Ex : For the RT9078N-08GJ5, V_{SNS} is 0.8V).

The maximum adjustable output voltage can be as high as input voltage deducted by the dropout voltage. The Resistive divider total value of R1 and R2 are suggested not over 50kΩ.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For TSOT-23-5 package, the thermal resistance, θ_{JA}, is 230.6°C/W on a standard JEDEC 51-7 four-layer thermal test board. For ZQFN-4L 1x1 (ZDFN-4L 1x1) package, the thermal resistance, θ_{JA}, is 226°C/W on a two-layer Richtek evaluation board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (230.6°C/W) = 0.43W for TSOT-23-5 package

$P_{D(MAX)}$ = (125°C – 25°C) / (226°C/W) = 0.44W for ZQFN-4L 1x1 (ZDFN-4L 1x1) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

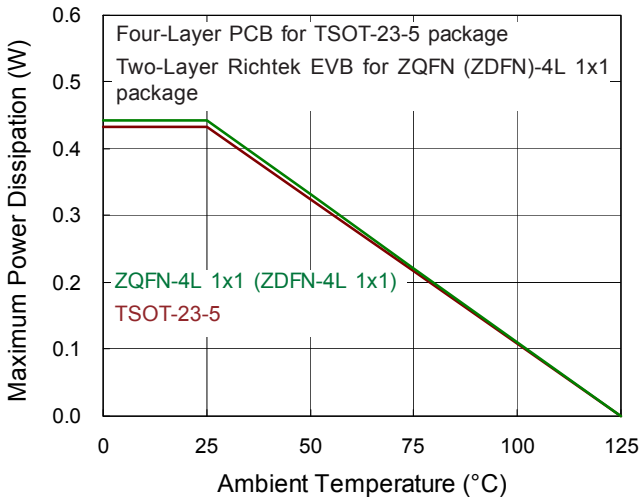


Figure 4. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RT9078, the PCB layout suggestions below are highly recommend :

- Input capacitor must be placed as close as possible to IC to minimize the power loop area.
- Minimize the power trace length and avoid using vias for the input and output capacitors connection.

Figure 5 and Figure 6 shows the examples for the layout reference which helps the inductive parasitic components minimization, load transient reduction and good circuit stability.

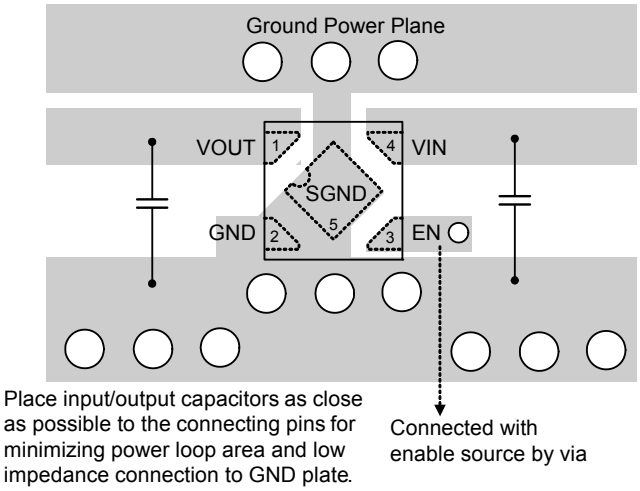


Figure 5. PCB Layout Guide for ZQFN-4L 1x1 package

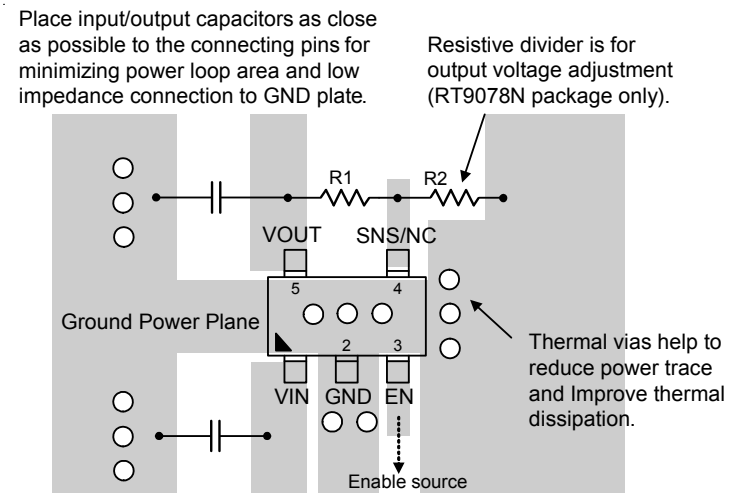
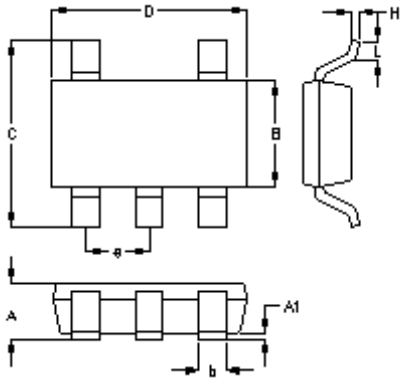


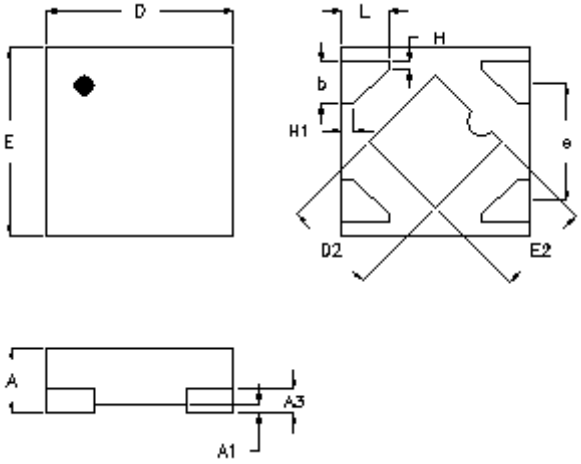
Figure 6. PCB Layout Guide for TSOT-23-5 package

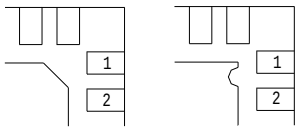
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-5 Surface Mount Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.300	0.400	0.012	0.016
A1	0.000	0.050	0.000	0.002
A3	0.117	0.162	0.005	0.006
b	0.175	0.275	0.007	0.011
D	0.900	1.100	0.035	0.043
D2	0.450	0.550	0.018	0.022
E	0.900	1.100	0.035	0.043
E2	0.450	0.550	0.018	0.022
e	0.625		0.025	
L	0.200	0.300	0.008	0.012
H	0.039		0.002	
H1	0.064		0.003	

Z-Type 4L QFN 1x1 Package

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