ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +4.0V
IN_+, IN_- to GND ....-0.3V to +4.0V
OUT+, OUT- to GND ....-0.3V to +4.0V
$\overline{PD}$, SEL to GND ....-1.4V to (V_{CC} + 1.4V)
Single-Ended and Differential Output
  Short-Circuit Duration (OUT+, OUT-) ....Continuous
Continuous Power Dissipation (T_A = +70°C)
  10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
  10-Lead Thin QFN (derate 24.4mW/°C above +70°C)..1951mW

Operating Temperature Range ....-40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
ESD Protection
  Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
  (IN_+, IN_-, OUT+, OUT-) ....±16kV
  IEC61000-4-2 Level 4 (R_D = 330Ω, C_S = 150pF)
  Contact Discharge (IN_+, IN_-, OUT+, OUT-)................±8 kV
  Air-Gap Discharge (IN_+, IN_-, OUT+, OUT-)................±15kV
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, R_L = 100Ω, $\overline{PD}$ = high, SEL = high or low, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, MAX9176 input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, MAX9177 input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, T_A = +25°C.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIFFERENTIAL INPUTS (IN_+, IN_-)							
Differential Input High Threshold	V_{TH}					+50	mV
Differential Input Low Threshold	V_{TL}			-50			mV
Input Current	I_{IN+}, I_{IN-}	Figure 1		-20		+20	µA
Power-Off Input Current	I_{INO+}, I_{INO-}	MAX9176	V_{CC} = 0 or open, Figure 1	-20		+20	µA
		MAX9177	V_{IN+} = 3.6V or 0, V_{IN-} = 3.6V or 0, V_{CC} = 0 or open, Figure 1				
Fail-Safe Input Resistors (MAX9176)	R_{IN1}	V_{CC} = 3.6V, 0 or open, Figure 1		60		108	kΩ
	R_{IN2}			200		394	
Input Resistors (MAX9177)	R_{IN3}	V_{CC} = 3.6V, 0 or open, Figure 1		212		450	kΩ
Input Capacitance	C_{IN}	IN_+ or IN_- to GND (Note 4)				4.5	pF
LVTTL/LVCMOS INPUTS (SEL, $\overline{PD}$)							
Input High Voltage	V_{IH}			2.0		V_{CC} + 1.0	V
Input Low Voltage	V_{IL}			-1.0		+0.8	V
Input Current	I_{IN}	-1.0V ≤ SEL, $\overline{PD}$ ≤ 0V		-1.5			mA
		0V ≤ SEL, $\overline{PD}$ ≤ V_{CC}		-20		+20	µA
		V_{CC} ≤ SEL, $\overline{PD}$ ≤ V_{CC} + 1.0V				+1.5	mA
LVDS OUTPUT (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Figure 2		250	393	475	mV
Change in Differential Output Voltage Between Logic States	ΔV_{OD}	Figure 2			1.0	15	mV
Offset Voltage	V_{OS}	Figure 3		1.125	1.25	1.375	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, R_L = 100Ω, $\overline{PD}$ = high, SEL = high or low, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, MAX9176 input common-mode voltage $V_{CM} = |V_{ID}/2|$ to $2.4V - |V_{ID}/2|$, MAX9177 input common-mode voltage $V_{CM} = |V_{ID}/2|$ to $V_{CC} - |V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, T_A = +25°C.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Change in Offset Voltage Between Logic States	ΔV_{OS}	Figure 3			4	15	mV
Fail-Safe Differential Output Voltage (MAX9176)	V_{OD}	Figure 2		250	393	475	mV
Differential Output Resistance	R_{DIFF}	V_{CC} = 3.6V or 0		95	123	146	Ω
Power-Down Single-Ended Output Current	I_{PD}	$\overline{PD}$ = low	V_{OUT+} = open, V_{OUT-} = 3.6V or 0	-1.0	±0.01	+1.0	µA
			V_{OUT-} = open, V_{OUT+} = 3.6V or 0				
Power-Off Single-Ended Output Current	I_{OFF}	$\overline{PD}$, SEL = low, V_{CC} = 0 or open	V_{OUT+} = open, V_{OUT-} = 3.6V or 0	-1.0	±0.01	+1.0	µA
			V_{OUT-} = open, V_{OUT+} = 3.6V or 0				
Output Short-Circuit Current	I_{OS}	V_{ID} = +50mV or -50mV, V_{OUT+} = 0 or V_{CC}		-15		+15	mA
		V_{ID} = +50mV or -50mV, V_{OUT-} = 0 or V_{CC}					
Differential Output Short-Circuit Current Magnitude	I_{OSD}	V_{ID} = +50mV or -50mV, V_{OD} = 0 (Note 4)				15	mA
Supply Current	I_{CC}	R_L = 100Ω, $\overline{PD}$ = V_{CC}, SEL = V_{CC} or 0			26	40	mA
Power-Down Supply Current	I_{CCPD}	R_L = 100Ω, $\overline{PD}$ = 0, other inputs open			0.5	20	µA
Output Capacitance	C_O	OUT+ or OUT- to GND (Note 4)				5.2	pF

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, R_L = 100Ω, C_L = 5pF, differential input voltage $|V_{ID}|$ = 0.15V to 1.2V, MAX9176 input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, MAX9177 input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, T_A = +25°C.) (Notes 5, 6, 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL INPUTS (IN_+, IN_-)						
High-to-Low Propagation Delay	t_{PHL}	Figures 4, 5	1.33	2.46	3.23	ns
Low-to-High Propagation Delay	t_{PLH}	Figures 4, 5	1.33	2.49	3.31	ns
Added Deterministic Jitter	t_{DJ}	Figures 4, 5 (Notes 8, 12)		68	80	$ps_{(P-P)}$
Added Random Jitter	t_{RJ}	Figures 4, 5 (Note 12)		0.7	1.0	$ps_{(RMS)}$
Pulse Skew $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SKP}	Figures 4, 5		27	142	ps
Part-to-Part Skew	t_{SKPP1}	Figures 4, 5 (Note 9)		0.4	1.3	ns
	t_{SKPP2}	Figures 4, 5 (Note 10)			2.0	
Rise Time	t_R	Figures 4, 5	217	320	383	ps
Fall Time	t_F	Figures 4, 5	157	340	360	ps
Select to Out Delay	t_{PSO}	Figure 6		2.0	2.7	ns
Power-Down Time	t_{PD}	Figures 7, 8			6.0	ns
Power-Up Time	t_{PU}	Figures 7, 8			35	µs
Maximum Data Rate	DR_{MAX}	Figures 4, 5, $\lvert V_{OD} \rvert \geq$ 250mV (Note 11)	800			Mbps
Maximum Switching Frequency	f_{MAX}	Figures 4, 5, $\lvert V_{OD} \rvert \geq$ 250mV (Note 11)	670			MHz
Switching Supply Current	I_{CCSW}	f_{IN} = 670MHz		38	58	mA
		f_{IN} = 155MHz		26	47	
PRBS Supply Current	I_{CCPR}	DR = 800Mbps, 2^{23} - 1 PRBS input		27	49	mA

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH}, V_{TL}, V_{ID}, V_{OD}, and ΔV_{OD}.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at T_A = +25°C.

Note 3: Tolerance on all external resistors (including figures) is ±1%.

Note 4: Guaranteed by design and characterization.

Note 5: AC parameters are guaranteed by design and characterization and not production tested. Limits are set at ±6 sigma.

Note 6: C_L includes scope probe and test jig capacitance.

Note 7: Pulse-generator output for differential inputs IN_+, IN_- (unless otherwise noted): f = 670MHz, 50% duty cycle, R_O = 50Ω, t_R = 500ps, and t_F = 500ps (0% to 100%). Pulse-generator output for single-ended inputs $\overline{PD}$, SEL: t_R = t_F = 1.5ns (0.2V_{CC} to 0.8V_{CC}), 50% duty cycle, V_{OH} = V_{CC} + 1.0V settling to V_{CC}, V_{OL} = -1.0V settling to zero.

Note 8: Pulse-generator output for t_{DJ}: V_{OD} = 0.15V, V_{OS} = 1.25V, bit rate = 800Mbps, 2^{23} - 1 PRBS, R_O = 50Ω, t_R = 500ps, and t_F = 500ps (0% to 100%).

Note 9: t_{SKPP1} is the magnitude of the difference of any differential propagation delays between devices operating under identical conditions.

Note 10: t_{SKPP2} is the magnitude of the difference of any differential propagation delays between devices operating over rated conditions.

Note 11: Meets all AC specifications.

Note 12: Input jitter subtracted from output jitter.

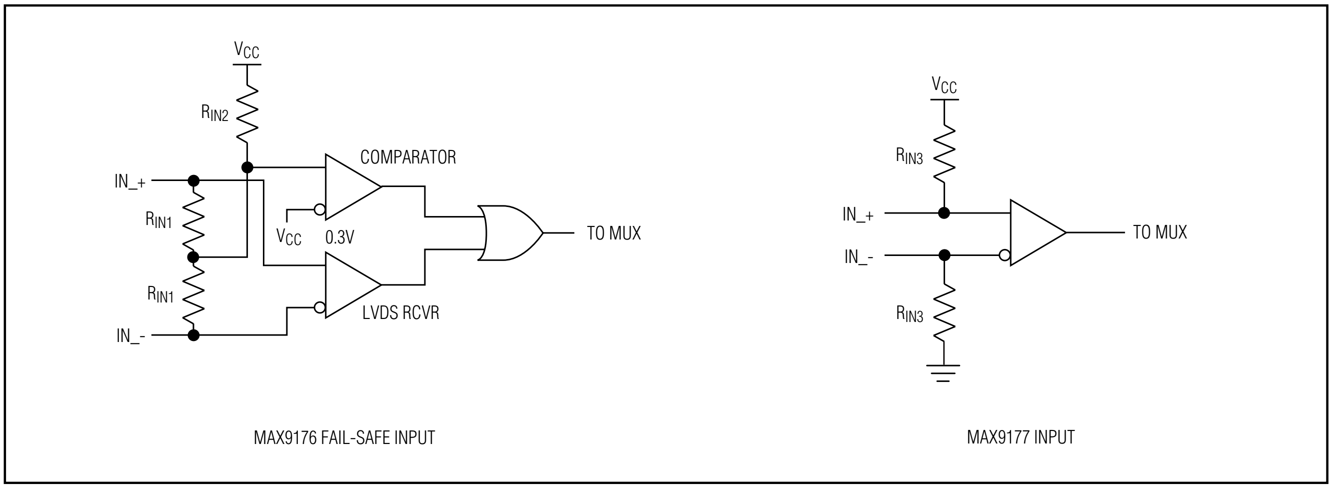


Figure 1. Input Structure

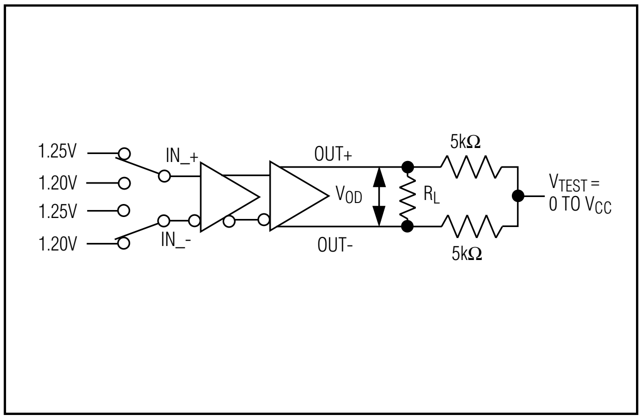


Figure 2. V_{OD} Test Circuit

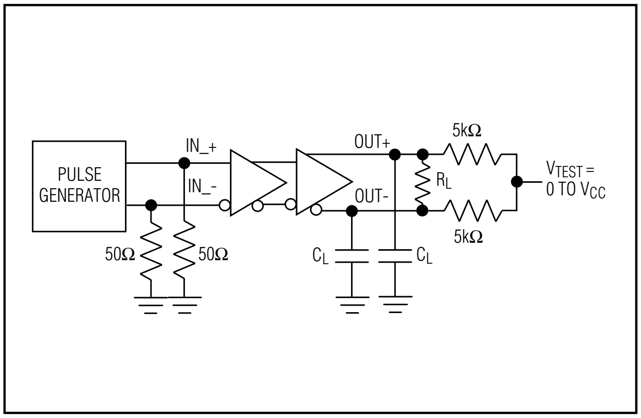


Figure 4. Transition Time and Propagation Delay Test Circuit

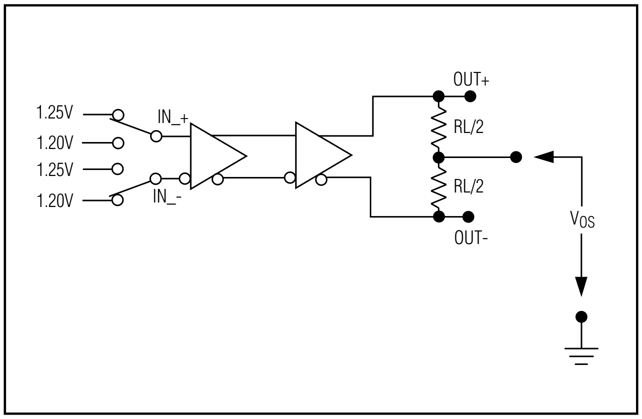


Figure 3. V_{OS} Test Circuit

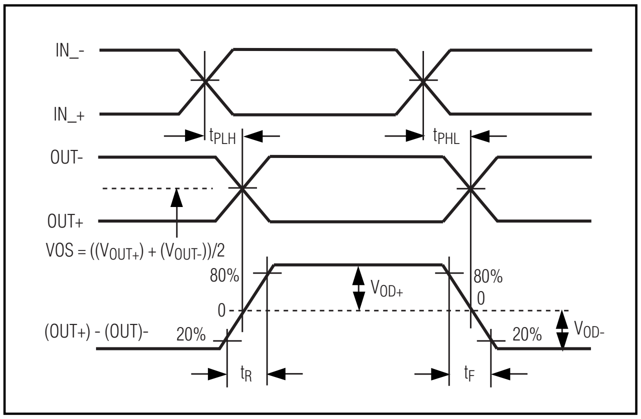


Figure 5. Transition Time and Propagation Delay Timing

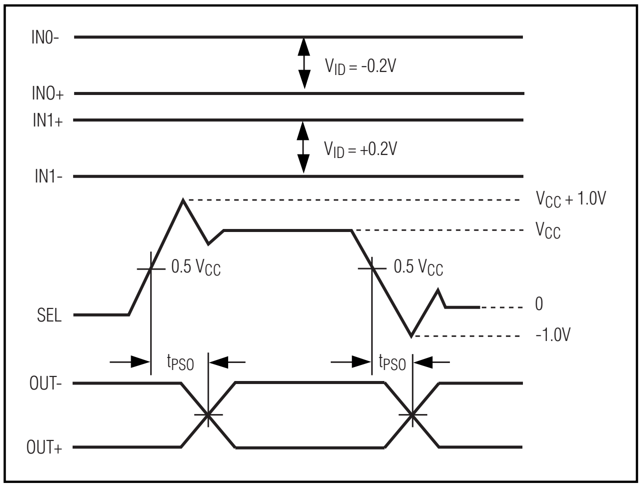


Figure 6. Select-to-Out Delay Timing

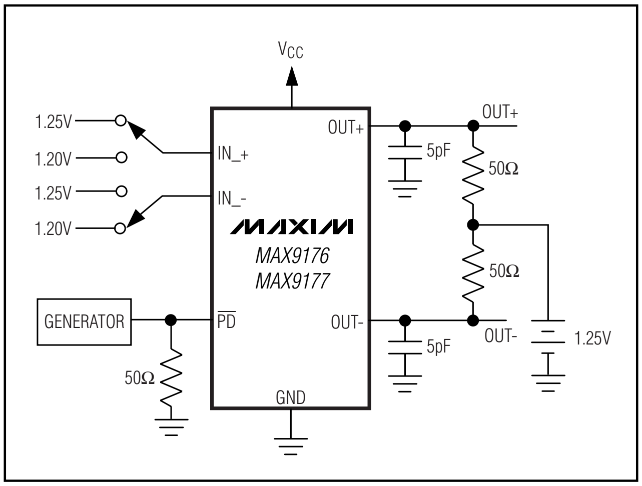


Figure 7. Power-Up/Down Delay Test Circuit

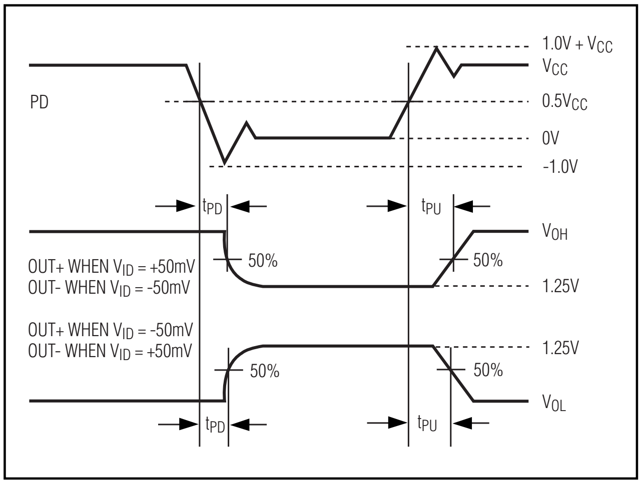
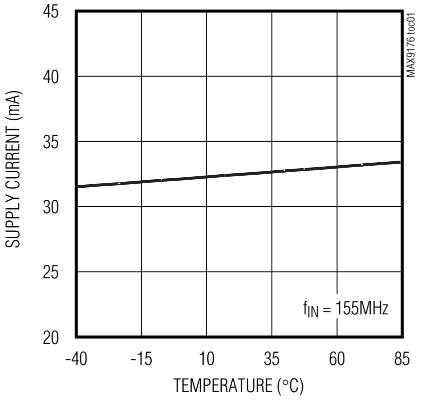


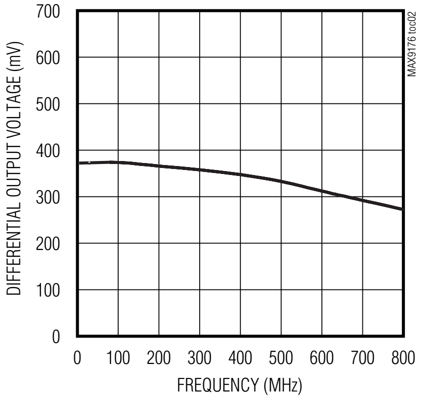
Figure 8. Power-Up/Down Delay Waveform

Typical Operating Characteristics

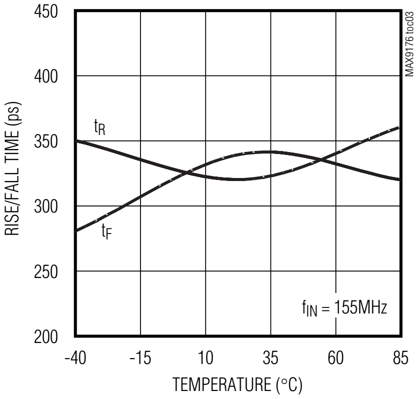
((MAX9176) V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, R_L = 100Ω, C_L = 5pf, $\overline{PD}$ = V_{CC}, SEL = 0V, IN1+, IN1- = open, T_A = +25°C, unless otherwise noted.)



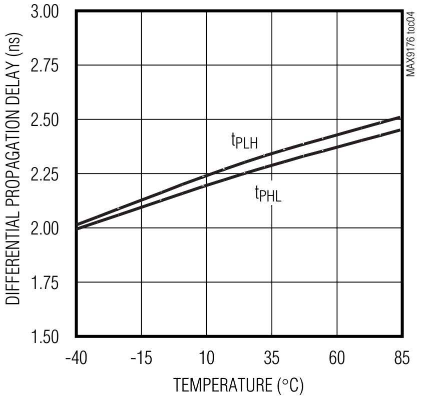
SUPPLY CURRENT vs. TEMPERATURE



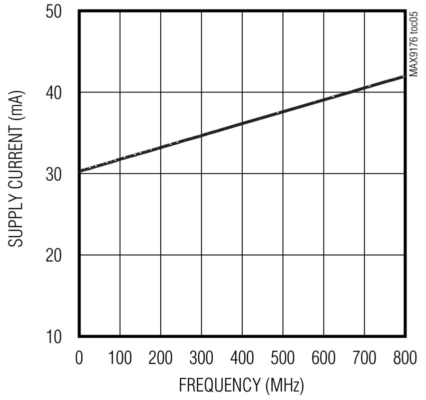
DIFFERENTIAL OUTPUT VOLTAGE vs. FREQUENCY



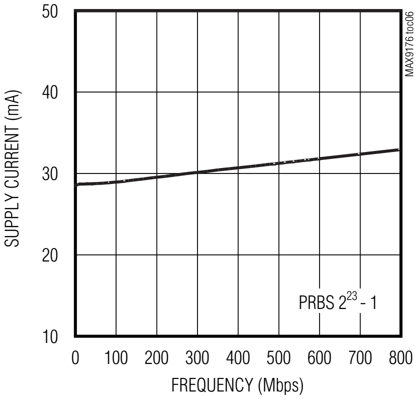
OUTPUT RISE/FALL TIME vs. TEMPERATURE



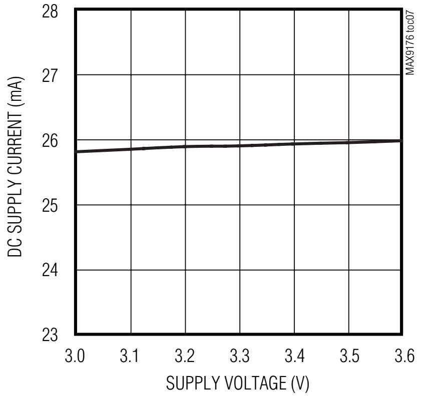
DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



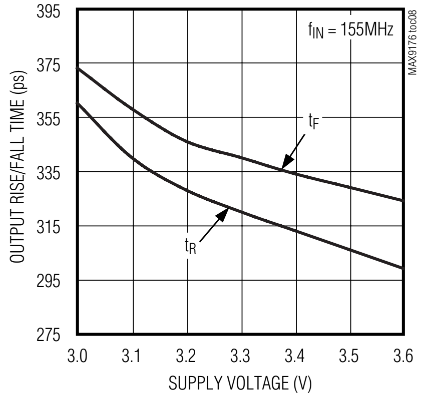
SUPPLY CURRENT vs. FREQUENCY



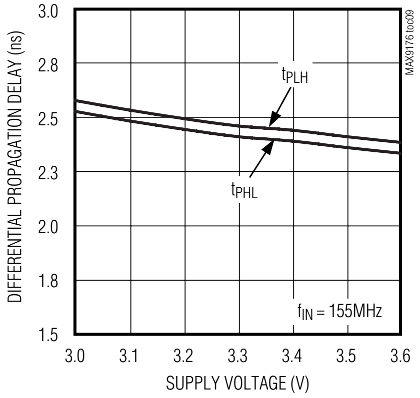
SUPPLY CURRENT vs. DATA RATE



DC SUPPLY CURRENT vs. SUPPLY VOLTAGE



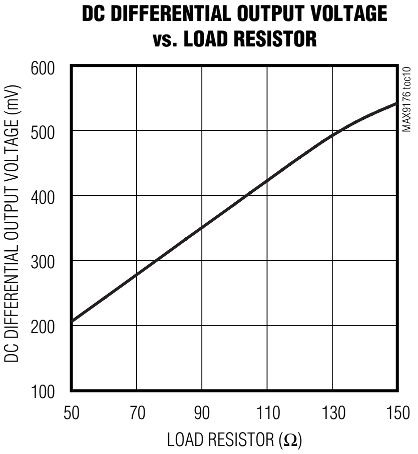
OUTPUT RISE/FALL TIME vs. SUPPLY VOLTAGE

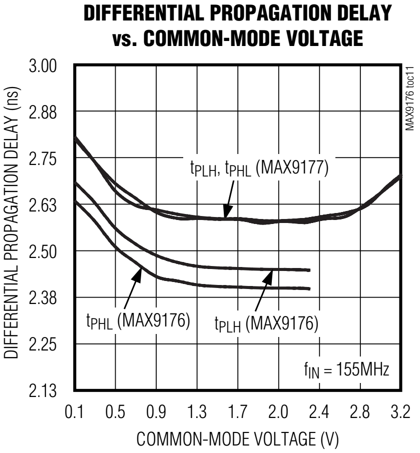


DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE

Typical Operating Characteristics (continued)

((MAX9176) V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.25V, R_L = 100Ω, C_L = 5pf, $\overline{PD}$ = V_{CC}, SEL = 0V, IN1+, IN1- = open, T_A = +25°C, unless otherwise noted.)





Pin Description

PIN		NAME	FUNCTION
µMAX	QFN		
1	1	IN0+	Noninverting Differential Input 0
2	2	IN0-	Inverting Differential Input 0
3	3	GND	Ground
4	4	IN1+	Noninverting Differential Input 1
5	5	IN1-	Inverting Differential Input 1
6	6	SEL	LVTTL/LVCMOS Input Select. SEL = high selects differential input 1. SEL = low selects differential input 0. Internal pulldown resistor to GND.
7	7	$\overline{PD}$	LVTTL/LVCMOS Input. Device is powered down when $\overline{PD}$ is low. Internal pulldown resistor to GND.
8	8	V_{CC}	Power Supply
9	9	OUT-	Inverting Differential Output
10	10	OUT+	Noninverting Differential Output
—	EP	Exposed Pad	Exposed Pad. Solder to ground.

Table 1. Function Table

INPUTS		OUTPUT
(IN_+) - (IN_-)		(OUT+) - (OUT-)
≥ +50mV		H
≤ -50mV		L
-50mV < V_{ID} < +50mV		Indeterminate
MAX9177	Open	H
MAX9176	Open, undriven short, or undriven parallel termination	

Table 2. Input Select and Power-Down Function Table

SEL	$\overline{PD}$	OUT+, OUT-
H	H	IN1+, IN1-
L or open	H	IN0+, IN0-
X	L or open	High impedance to ground and 123Ω (typ) differential output resistance

Detailed Description

The MAX9176/MAX9177 are 670MHz, low-jitter, low-skew 2:1 multiplexers ideal for protection switching, loopback, and clock distribution. The devices feature ultra-low 68ps$_{(P-P)}$ deterministic jitter that ensures reliable operation in high-speed links that are highly sensitive to timing error.

The MAX9176 has fail-safe LVDS inputs and an LVDS output. The MAX9177 has anything differential inputs (CML/LVDS/LVPECL) and an LVDS output. The output can be put into high impedance using the power-down input. The MAX9176 features fail-safe circuits that drive the output high when a selected input is open, undriven and shorted, or undriven and terminated. The MAX9177 has bias circuits that force the output high when a selected input is open. The mux select and power-down inputs are compatible with standard LVTTL/LVCMOS logic.

The select and power-down inputs tolerate undershoot of -1V and overshoot of V_{CC} + 1V. The MAX9176/MAX9177 are available in 10-pin µMAX and 10-lead thin QFN packages, and operate from a single 3.3V supply over the -40°C to +85°C temperature range.

Current-Mode LVDS Output

The LVDS output uses a current-steering configuration. This approach results in less ground bounce and less output ringing, enhancing noise margin and system speed performance.

A differential output voltage is produced by steering current through the parallel combination of the integrated differential output resistor and transmission line impedance/termination resistor. When driving a 100Ω load, a differential voltage of 250mV to 475mV is produced. For loads greater than 100Ω, the output voltage is larger, and for loads less than 100Ω, the output voltage is smaller. See the Differential Output Voltage vs. Load Resistance curve in *Typical Operating Characteristics* for more information. The output is short-circuit current limited for single-ended and differential shorts.

MAX9176 Input Fail-Safe

The fail-safe feature of the MAX9176 sets the output high when the differential input is:

- Open
- Undriven and shorted
- Undriven and terminated

Without a fail-safe circuit, when the selected input is undriven, noise at the input may switch the output and it may appear to the system that data is being sent. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when the driver output is in high impedance. A shorted input can occur because of a cable failure.

When the selected input is driven with a differential signal of $|V_{ID}|$ = 50mV to 1.2V within a voltage range of 0 to 2.4V, the fail-safe circuit is not activated. If the selected input is open, undriven and shorted, or undriven and terminated, an internal resistor in the fail-safe circuit pulls both inputs above V_{CC} - 0.3V, activating the fail-safe circuit and forcing the output high (Figure 1).

Overshoot and Undershoot Voltage Protection

The MAX9176/MAX9177 are designed to protect the select and power-down inputs (SEL and $\overline{PD}$) against latchup due to transient overshoot and undershoot voltage. If the input voltage goes above V_{CC} or below GND by up to 1V, an internal circuit limits input current to 1.5mA.

Applications Information

Power-Supply Bypassing

Bypass the V_{CC} pin with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to V_{CC}.

Differential Traces

Input and output trace characteristics affect the performance of the MAX9176/MAX9177. Use controlled-impedance differential traces (100Ω typical). To reduce radiated noise and ensure that noise couples as common mode, route the differential input and output signals within a pair close together. Reduce skew by matching the electrical length of the two signal paths that make up the differential pair. Excessive skew can result in a degradation of magnetic field cancellation. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Interconnect for LVDS typically has a controlled differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

The MAX9176/MAX9177 require external input and output termination resistors. For LVDS, connect an input termination resistor across each differential input and at the far end of the interconnect driven by the LVDS output. Place the input termination resistor as close to the receiver input as possible. Termination resistors should match the differential impedance of the transmission line. Use 1% surface-mount resistors.

The MAX9176/MAX9177 feature an integrated differential output resistor. This resistor reduces jitter by damping reflections produced by any mismatch between the transmission line and termination resistor at the far end of the interconnect.

Board Layout

Separate the differential and single-ended signals to reduce crosstalk. A four-layer printed circuit board with separate layers for power, ground, differential signals, and single-ended logic signals is recommended. Separate the differential signals from the logic signals with power and ground planes for best results.

IEC 61000-4-2 Level 4 ESD Protection

The IEC 61000-4-2 standard (Figure 10) specifies ESD tolerance for electronic systems. The IEC61000-4-2 model specifies a 150pF capacitor that is discharged into the device through a 330Ω resistor. The MAX9176/MAX9177 differential inputs and outputs are rated for IEC61000-4-2 level 4 (±8kV Contact Discharge and ±15kV Air-Gap Discharge). The Human Body Model (HBM, Figure 9) specifies a 100pF capacitor that is discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2 level 4 discharges higher peak current and more energy than the HBM due to the lower series resistance and larger capacitor.

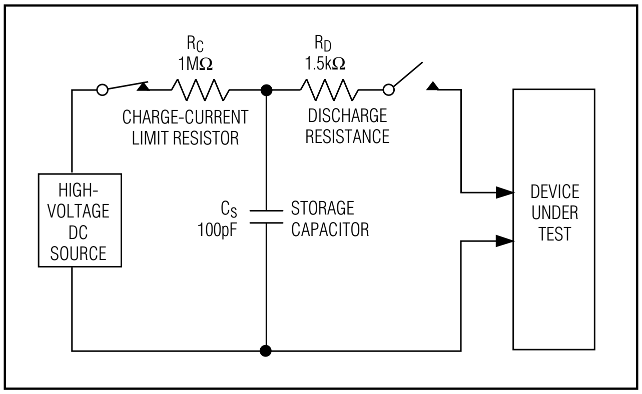


Figure 9. Human Body Test Model

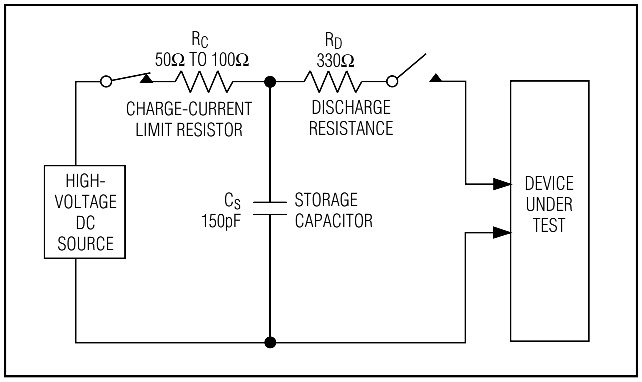
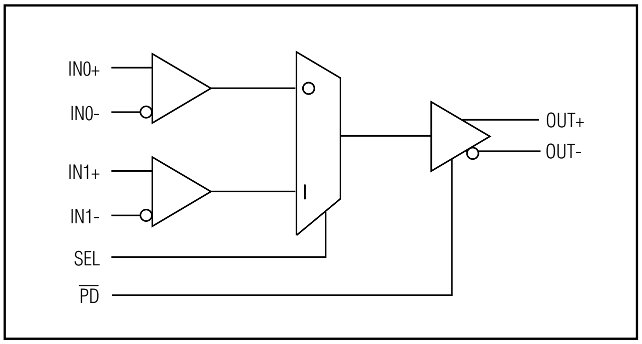


Figure 10. IEC 61000_4-2 Contact Discharge Test Model

Functional Diagram



Chip Information

TRANSISTOR COUNT: 744

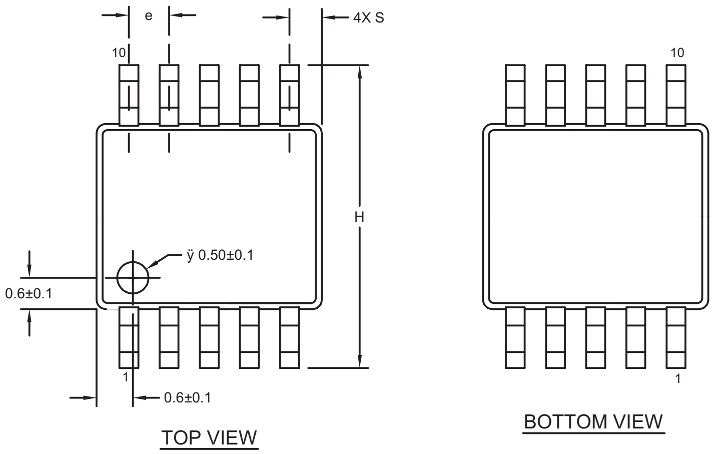
PROCESS: CMOS

670MHz LVDS-to-LVDS and Anything-to-LVDS 2:1 Multiplexers

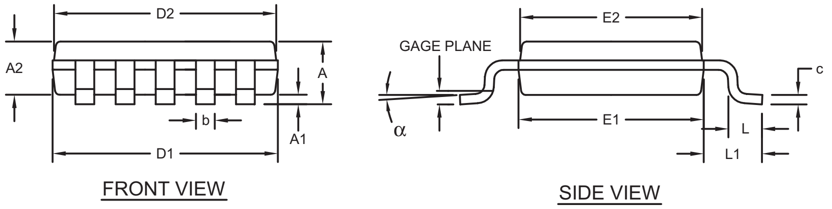
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞

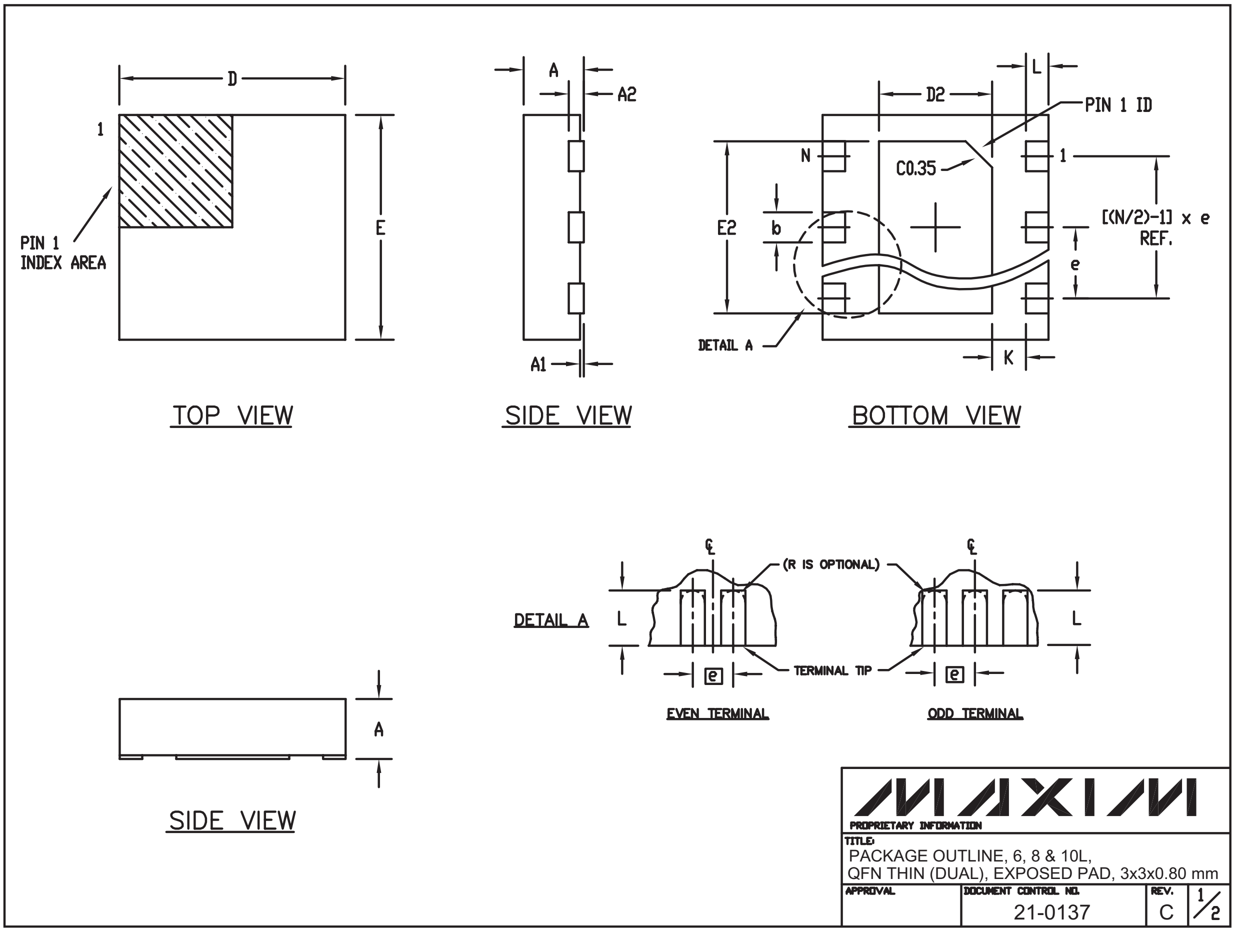


NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 10L uMAX/uSOP
APPROVAL
DOCUMENT CONTROL NO. 21-0061
REV. I
1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



PACKAGE OUTLINE, 6, 8 & 10L,
QFN THIN (DUAL), EXPOSED PAD, 3x3x0.80 mm

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6, 8, &10L, QFN THIN.EPS

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO220.

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, 6, 8 & 10L,
QFN THIN (DUAL), EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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