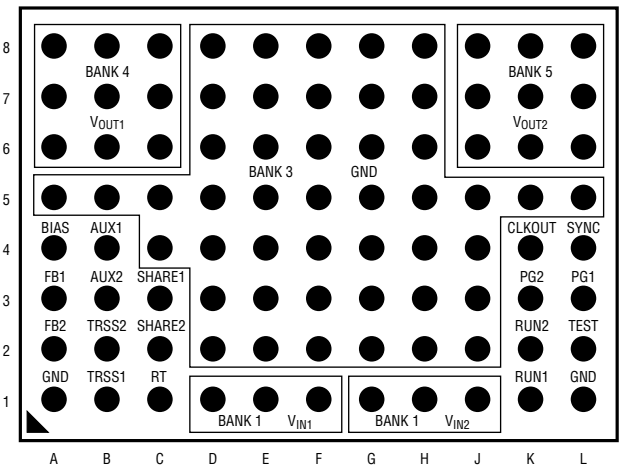
## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$, RUN, PG .....42V
$V_{OUT}$, BIAS .....10V
FB .....4V
TRSS.....3V
SYNC .....6V
Maximum Internal Temperature (Note 2) ..... 125°C
Storage Temperature ..... –55°C to 125°C
Peak Reflow Solder Body Temperature .....250°C

## PIN CONFIGURATION




BGA PACKAGE
88-PIN (11.25mm × 9mm × 3.32mm)

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 18.0°C/W, $\theta_{JCtop}$ = 10.0°C/W,
$\theta_{JB}$ = 4.5°C/W, WEIGHT = 1.0g
θ VALUES DETERMINED PER JESD 51-9, 51-12

## ORDER INFORMATION

| PART NUMBER | PAD OR BALL FINISH | PART MARKING* | | PACKAGE TYPE | MSL RATING | TEMPERATURE RANGE (SEE NOTE 2) |
|---|---|---|---|---|---|---|
| | | DEVICE | FINISH CODE | | | |
| LTM8024EY#PBF | SAC305 (RoHS) | LTM8024Y | e1 | BGA | 3 | –40°C to 125°C |
| LTM8024IY#PBF | | | | | | |

- Contact the factory for parts specified with wider operating temperature ranges.
- Device temperature grade is indicated by a label on the shipping container. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to:
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings



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## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating internal temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN1}$ = $V_{IN2}$ = 12V. RUN1 = RUN2 = 2V unless otherwise noted (Note 2).**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Minimum $V_{IN1}$ Input Voltage<br>Minimum $V_{IN2}$ Input Voltage | <br>$V_{IN1}$ = 3V | ●<br>● | | | 3.0<br>2.0 | V<br>V |
| Output DC Voltage | FB*n* open<br>FB*n* = 21.5kΩ | | | 0.8<br>10 | | V<br>V |
| Maximum Output DC Current | (Note 3) | | | | 6 | A |
| Quiescent Current into $V_{IN}$*n* | RUN1 = 0<br>BIAS = 5V, SYNC = 0V, No Load<br>BIAS = 5V, SYNC = 3.3V, No Load | | | <br>90<br>16 | 5 | µA<br>µA<br>mA |
| Current into BIAS | RUN*n* = 0, BIAS = 5V<br>BIAS = 5V, SYNC = 3.3V, No Load | | | | 0.5 | µA<br>mA |
| Line Regulation | 5.5V < $V_{IN}$*n* < 36V, $I_{OUT}$*n* = 1A | | | 0.2 | | % |
| Load Regulation | 12$V_{IN}$*n*, 0.1A < $I_{OUT}$*n* < 4A | | | 0.4 | | % |
| Output RMS Ripple | 3.3$V_{OUT}$*n*, $I_{OUT}$*n* = 4A | | | 10 | | mV |
| FB*n* Voltage | <br> | <br>● | <br>784 | 800 | <br>816 | mV<br>mV |
| Current out of FB*n* | $V_{OUT}$*n* = 1V, FB*n* = 0V | | | 4 | | µA |
| Minimum BIAS for Proper Operation | | | | | 3.2 | V |
| Switching Frequency | $R_T$ = 200kΩ<br>$R_T$ = 35.7kΩ<br>$R_T$ = 8.06kΩ | | | 200<br>1<br>3 | | kHz<br>MHz<br>MHz |
| RUN*n* Threshold | | | | 0.74 | | V |
| RUN*n* Input Current | RUN*n* = 0V | | | | 1 | µA |
| PG*n* Threshold at FB*n* | Lower Threshold<br>Upper Threshold | | | 740<br>860 | | mV<br>mV |
| PG*n* Output Sink Current | PG*n* = 0.1V | | 100 | | | µA |
| CLKOUT $V_{OL}$ | | | | 0.1 | | V |
| CLKOUT $V_{OH}$ | | | | 3.2 | | V |
| SYNC Input High Threshold | | | 1.5 | | | V |
| SYNC Input Low Threshold | | | | | 0.8 | V |
| SYNC Threshold to Enable Spread Spectrum | | | 2.8 | | 4.0 | V |
| SYNC Current | SYNC = 6V | | | 130 | | µA |
| TRSS*n* Source Current | TRSS*n* = 0V | | | 2 | | µA |
| TRSS*n* Pull-Down Resistance | Fault Condition, TRSS*n* = 0.1V | | | 200 | | Ω |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTM8024E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls.

The LTM8024I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

**Note 3:** The maximum current out of either channel may be limited by the internal temperature of the LTM8024. See output current derating curves for different $V_{IN}$, $V_{OUT}$ and $T_A$.



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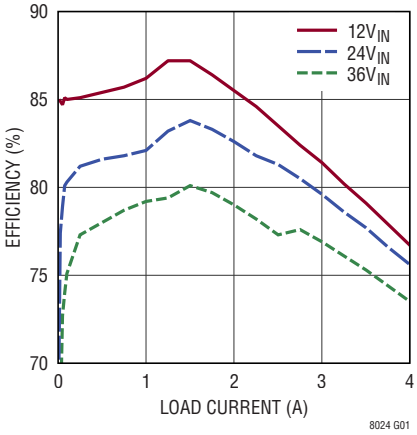
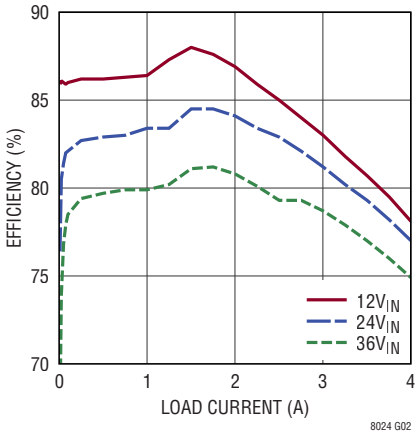
## TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C, operating per Table 1,unless otherwise noted.**

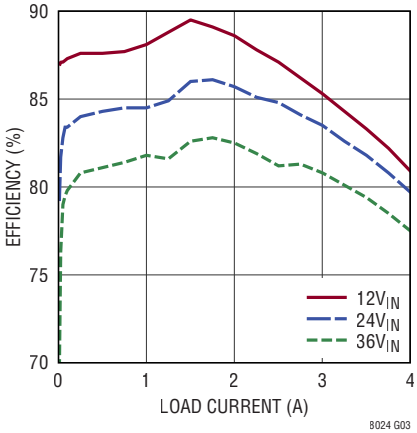
**Efficiency, $V_{OUT}$ = 1V**
**BIAS = 5V**



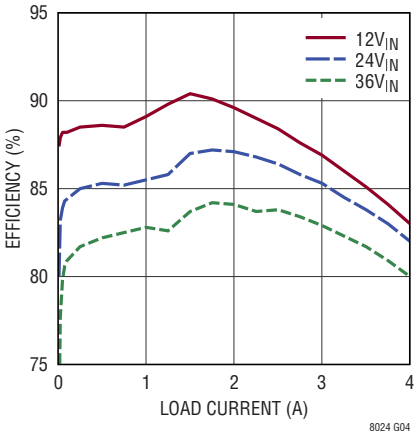

**Efficiency, $V_{OUT}$ = 1.2V**
**BIAS = 5V**



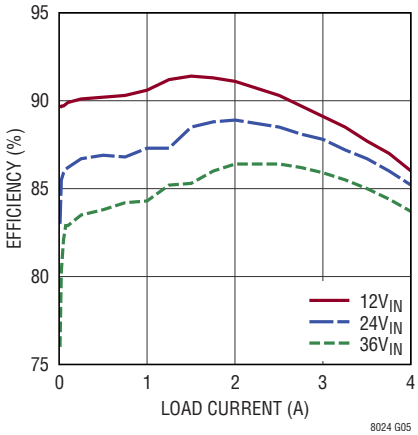

**Efficiency, $V_{OUT}$ = 1.5V**
**BIAS = 5V**



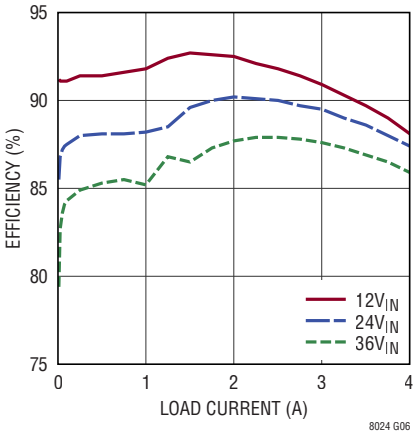

**Efficiency, $V_{OUT}$ = 1.8V**
**BIAS = 5V**



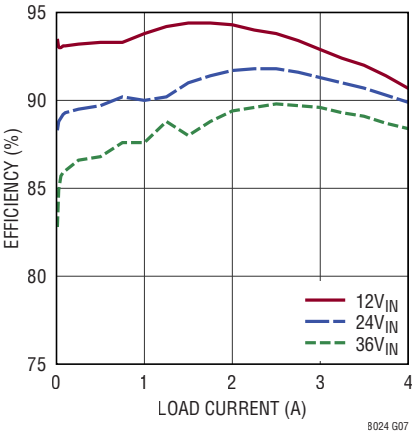

**Efficiency, $V_{OUT}$ = 2.5V**
**BIAS = 5V**



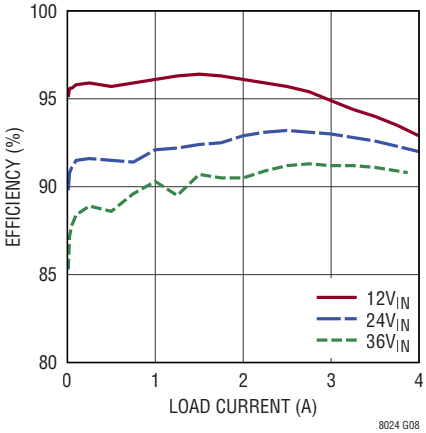

**Efficiency, $V_{OUT}$ = 3.3V**
**BIAS = 5V**



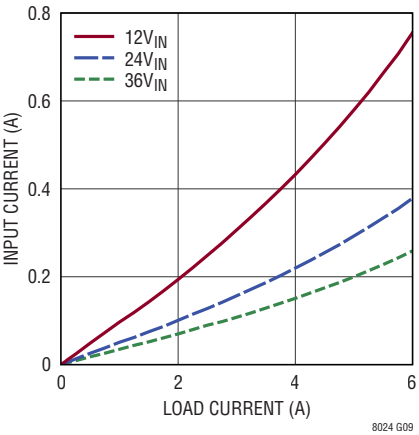

**Efficiency, $V_{OUT}$ = 5V**
**BIAS = 5V**




**Efficiency, $V_{OUT}$ = 8V**
**BIAS = 5V**




**Input vs Load Current, $V_{OUT}$ = 1V**



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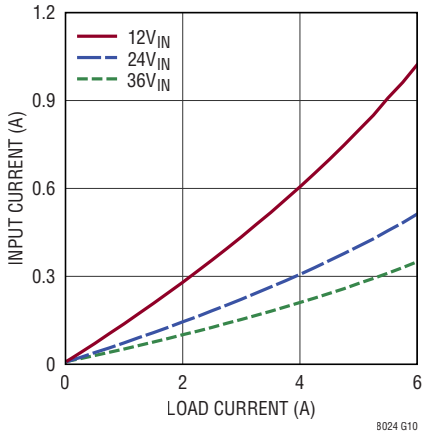
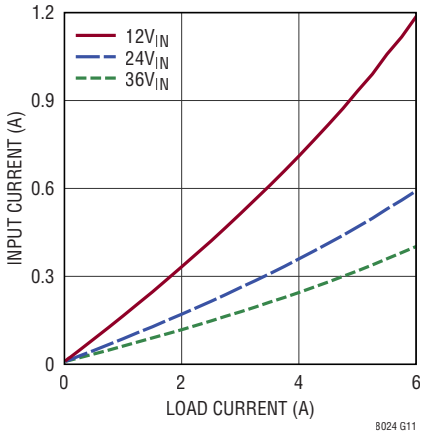
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, operating per Table 1,unless otherwise noted.

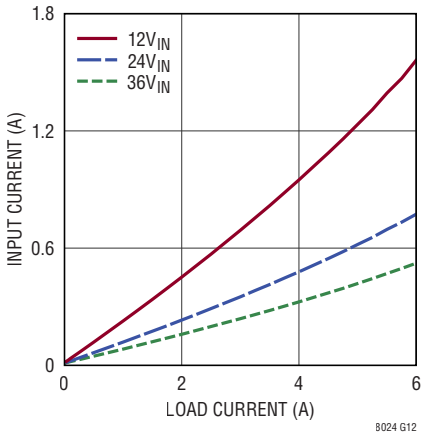
**Input vs Load Current, $V_{OUT}$ = 1.5V**



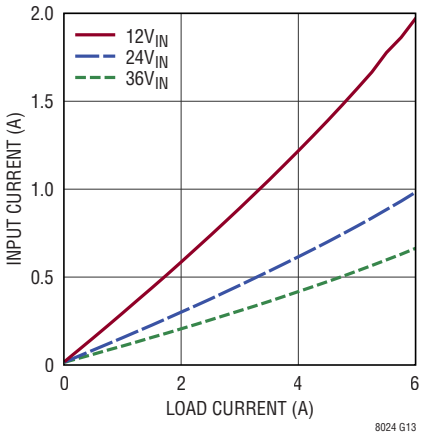

**Input vs Load Current, $V_{OUT}$ = 1.8V**



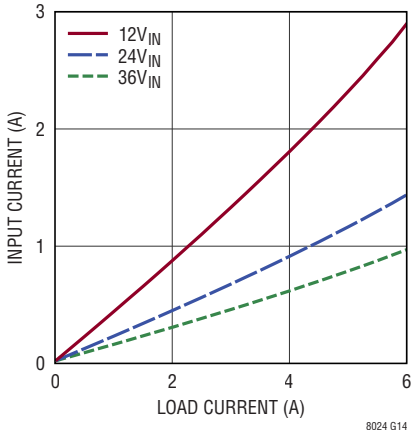

**Input vs Load Current, $V_{OUT}$ = 2.5V**



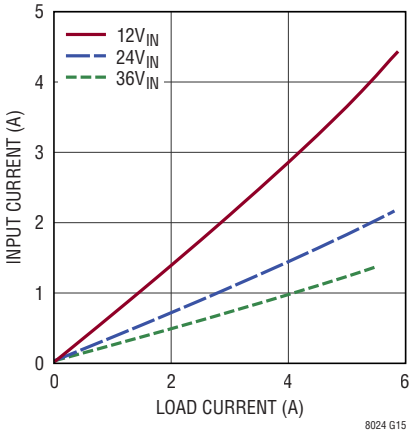

**Input vs Load Current, $V_{OUT}$ = 3.3V**



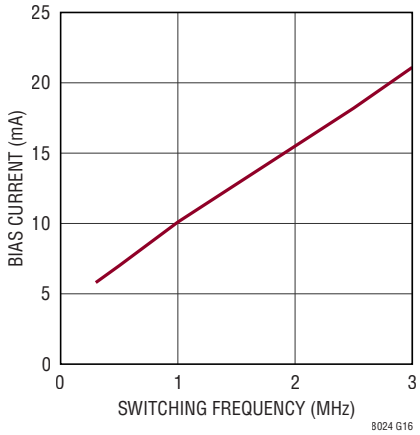

**Input vs Load Current, $V_{OUT}$ = 5V**



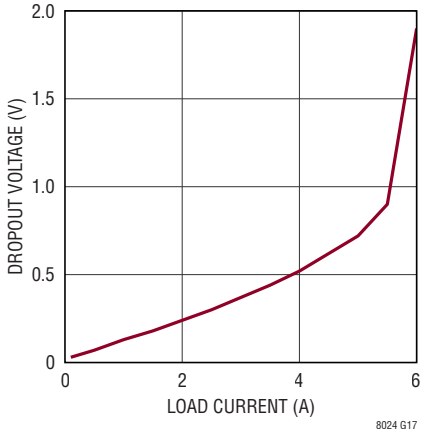

**Input vs Load Current, $V_{OUT}$ = 8V**



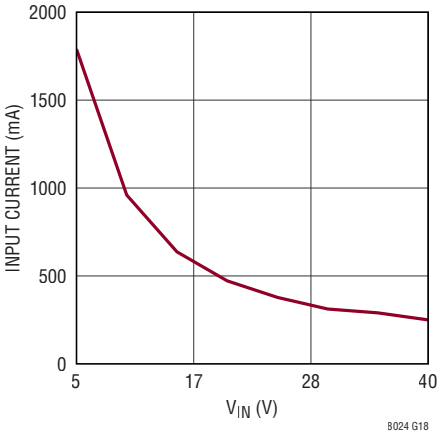

**BIAS Current vs Frequency $12V_{IN}$, $3.3V_{OUT}$, 1A Load SYNC Floating**




**Dropout Voltage vs Load Current**




**Input Current vs $V_{IN}$, $V_{OUT}$ Short Circuited**



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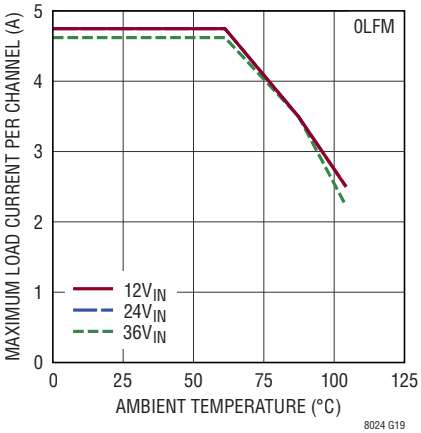
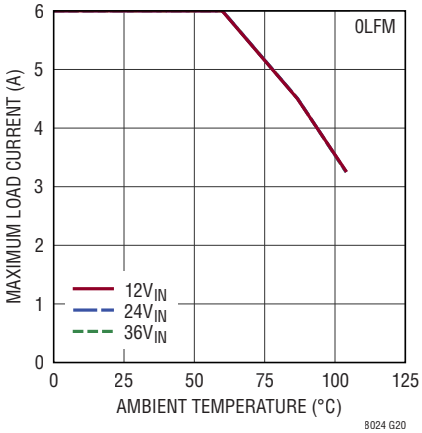
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, operating per Table 1,unless otherwise noted.

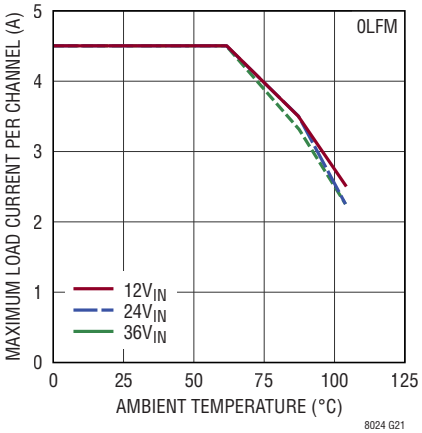
**Derating, $V_{OUT}$ = 1V, BIAS = 5V, DC1868A Demo Board Both Channels at Same Load**



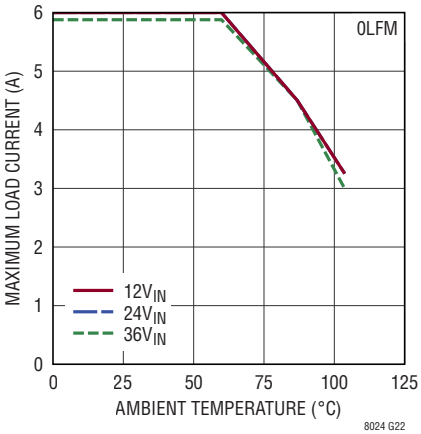

**Derating, $V_{OUT}$ = 1V, BIAS = 5V, DC1868A Demo Board Channel 2 Off**



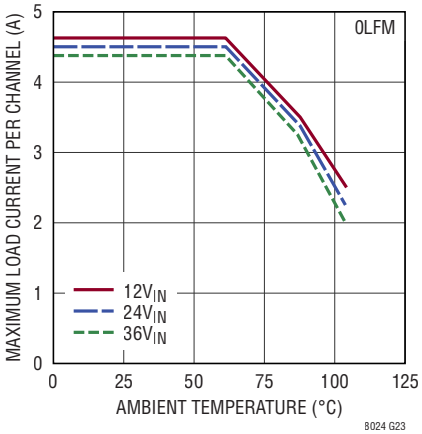

**Derating, $V_{OUT}$ = 1.2V, BIAS = 5V, DC1868A Demo Board Both Channels at Same Load**



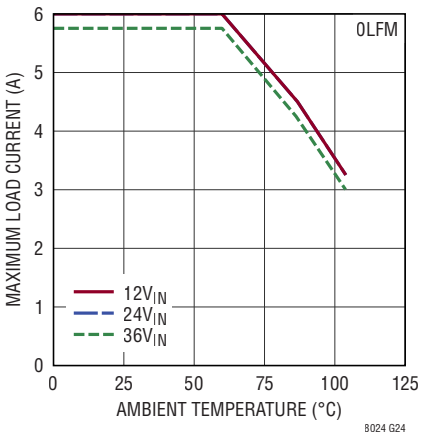

**Derating, $V_{OUT}$ = 1.2V, BIAS = 5V, DC1868A Demo Board Channel 2 Off**



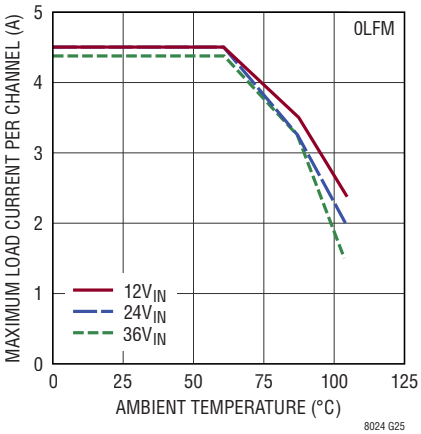

**Derating, $V_{OUT}$ = 1.5V, BIAS = 5V, DC1868A Demo Board Both Channels at Same Load**



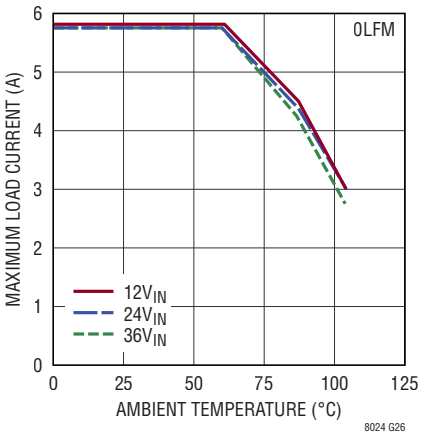

**Derating, $V_{OUT}$ = 1.5V, BIAS = 5V, DC1868A Demo Board Channel 2 Off**



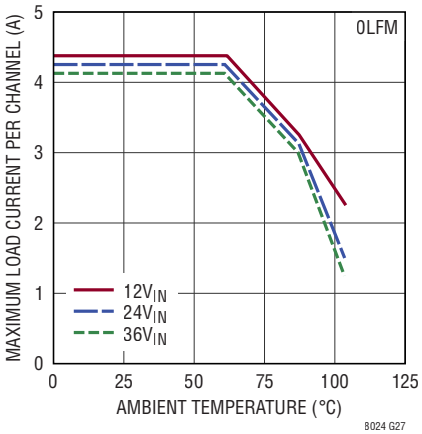

**Derating, $V_{OUT}$ = 1.8V, BIAS = 5V, DC1868A Demo Board Both Channels at Same Load**




**Derating, $V_{OUT}$ = 1.8V, BIAS = 5V, DC1868A Demo Board Channel 2 Off**




**Derating, $V_{OUT}$ = 2.5V, BIAS = 5V, DC1868A Demo Board Both Channels at Same Load**



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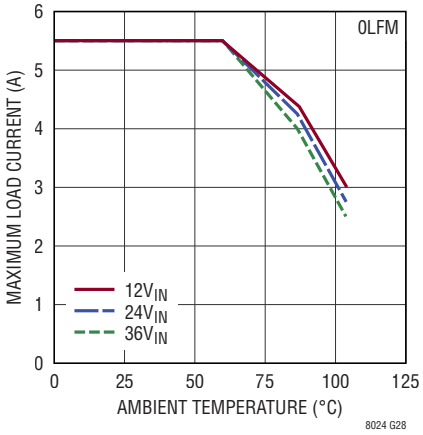
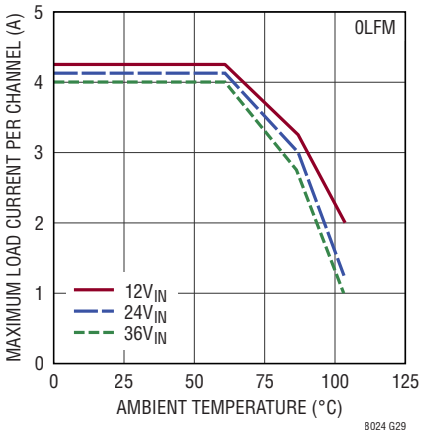
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, operating per Table 1,unless otherwise noted.

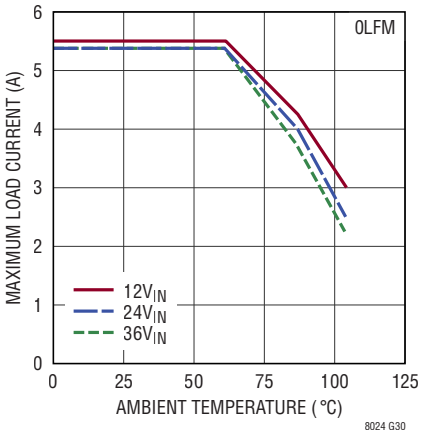
**Derating, $V_{OUT}$ = 2.5V, BIAS = 5V, DC1868A Demo Board Channel 2 Off**



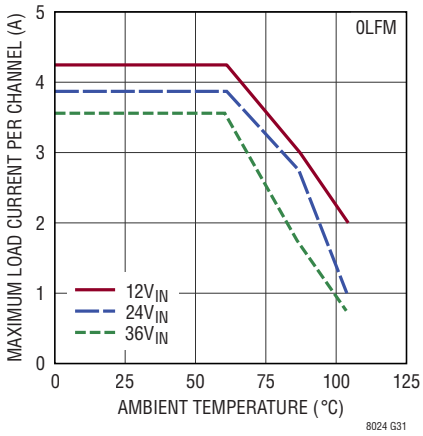

**Derating, $V_{OUT}$ = 3.3V, BIAS = 5V, DC1868A Demo Board Both Channels at Same Load**



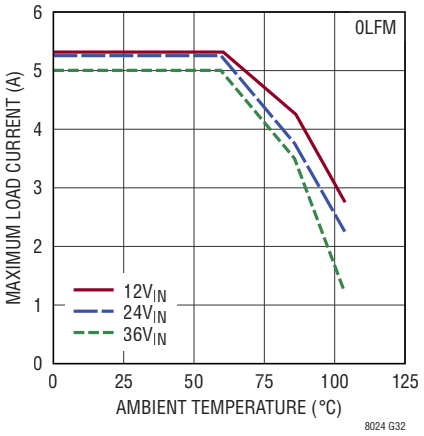

**Derating, $V_{OUT}$ = 3.3V, BIAS = 5V, DC1868A Demo Board Channel 2 Off**



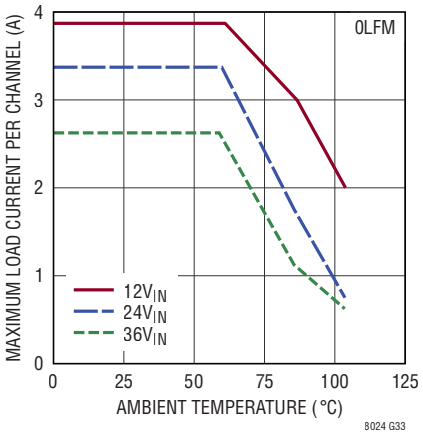

**Derating, $V_{OUT}$ = 5V, BIAS = 5V, DC1868A Demo Board Both Channels at Same Load**



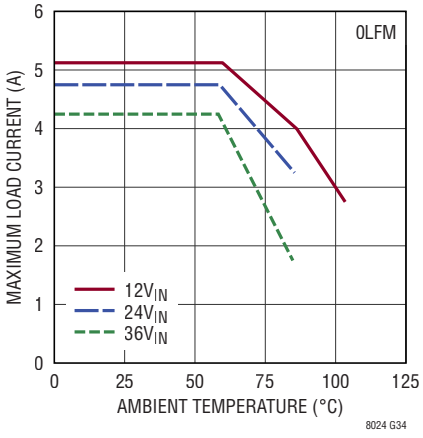

**Derating, $V_{OUT}$ = 5V, BIAS = 5V, DC1868A Demo Board Channel 2 Off**



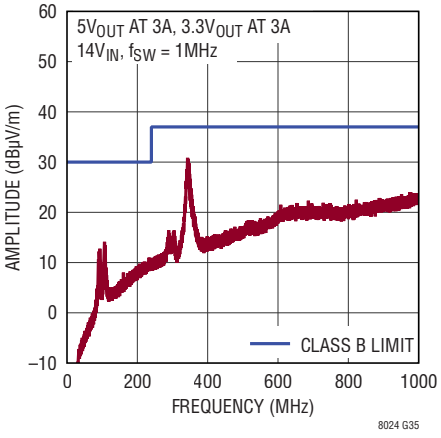

**Derating, $V_{OUT}$ = 8V, BIAS = 5V, DC1868A Demo Board Both Channels at Same Load**



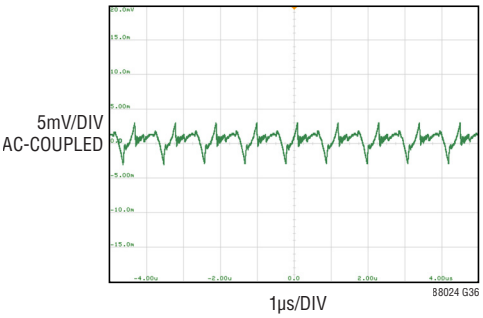

**Derating, $V_{OUT}$ = 8V, BIAS = 5V, DC1868A Demo Board Channel 2 Off**




**CISPR22 Class B Emissions DC1868A Demo Board Spread Spectrum On, No EMI Filter (C20 = 0.1µF, L1, FB1 Short) (C21, C22, C34-C37 Open)**




**Output Voltage Ripple DC1868A Demo Board**




$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V
$I_{OUT}$ = 3.5A, $f_{SW}$ = 900kHz



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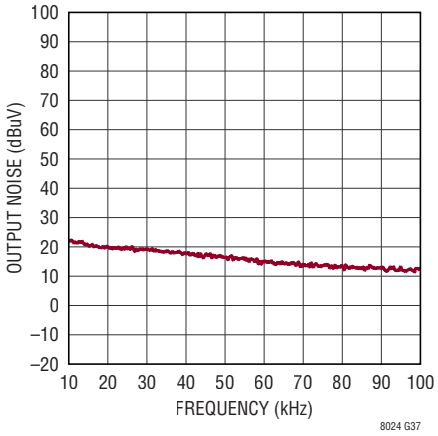
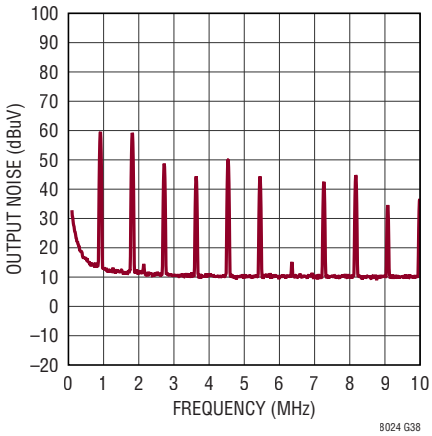
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, operating per Table 1,unless otherwise noted.

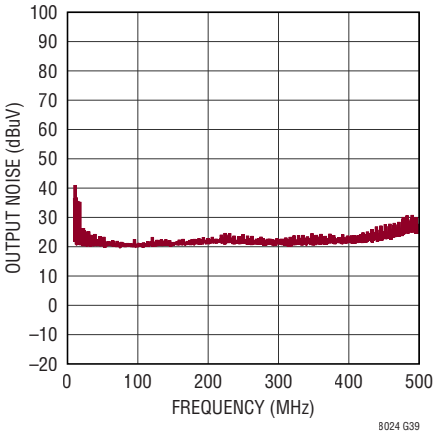
**Output Noise Sprectrum**
**DC1868A, 100kHz Span**
**$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V**
**$I_{OUT}$ = 3.5A, $F_{SW}$ = 900kHz**




**Output Noise Sprectrum**
**DC1868A, 10MHz Span**
**$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V**
**$I_{OUT}$ = 3.5A, $F_{SW}$ = 900kHz**

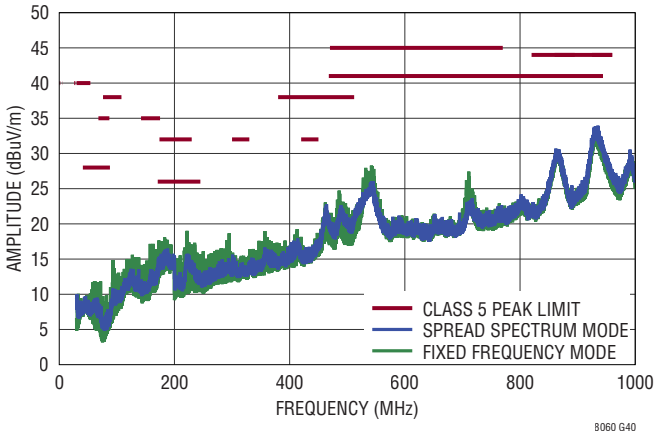



**Output Noise Sprectrum**
**DC1868A, 500MHz Span**
**$V_{IN}$ = 12V, $V_{OUT}$ = 3.3V**
**$I_{OUT}$ = 3.5A, $F_{SW}$ = 900kHz**

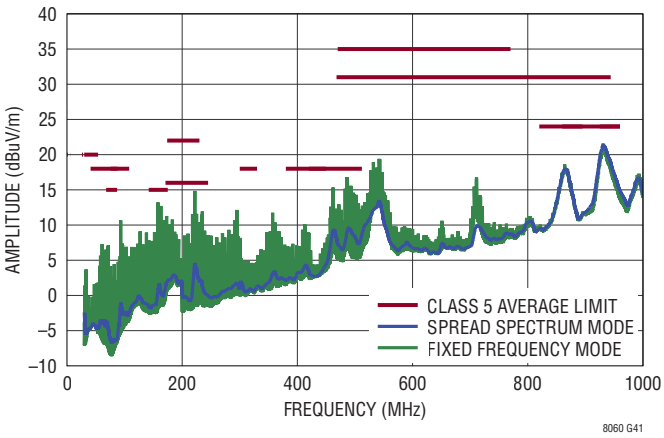



**CISPR25 Radiated Emission with Class 5 Average Limit DC1868A Demo Board, $V_{IN}$ = 12V, $V_{OUT}$ = 3.3V**
**Two Channels Paralleled, $I_{OUT}$ = 7A, $f_{SW}$ = 1MHz**

**Radiated Peak**




**Radiated Average**



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## PIN FUNCTIONS

**$V_{IN1}$ (Bank 1):** Input Power for the Channel 1 Regulator. The $V_{IN1}$ bank powers the internal control circuitry for both channels and is monitored by undervoltage lockout circuitry. Power must be applied to $V_{IN1}$ in order for either channel of the LTM8024 to operate. Decouple $V_{IN1}$ to ground with an external, low ESR capacitor. See Table 1 for recommended values.

**$V_{IN2}$ (Bank 2):** Input Power for the Channel 2 Regulator. The $V_{IN2}$ pin is monitored by undervoltage lockout circuitry. $V_{IN1}$ voltage must be greater than 3.0V for $V_{IN2}$ operation. Decouple $V_{IN2}$ to ground with an external, low ESR capacitor. See Table 1 for recommended values.

**$V_{OUT1}$/$V_{OUT2}$ (Banks 4 and 5):** Power Output for Channels 1 and 2, Respectively. Apply the output filter capacitor and the output load between these pins and GND pins.

**GND (Bank 3):** Tie these GND pins to a local ground plane below the LTM8024 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8024 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider ($R_{FB}$) to this net.

**FB1/FB2 (Pins A3, A2):** The LTM8024 regulates the FB*n* pin to 800mV. Connect the feedback resistor to this pin to set the output voltage.

**BIAS (Pin A4):** The internal regulator will draw current from BIAS instead of $V_{IN1}$ when BIAS is tied to a voltage higher than 3.2V. For output voltages of 3.3V and above this pin should be tied to $V_{OUT}$. If this pin is tied to a supply other than $V_{OUT}$ use a local bypass capacitor on this pin. If not used, tie this pin to GND.

**TRSS1/TRSS2 (Pin B1, B2):** Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during startup. A TRSS*n* voltage below 0.8V forces the LTM8024 to regulate the FB*n* pin to equal the TRSS*n* pin voltage. When TRSS*n* is above 0.8V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the soft-start feature is not being used.

**AUX1/AUX2 (Pins B4, B3):** Low Current Voltage Source for BIAS. In many designs, the BIAS pin is simply connected to $V_{OUT}$ by way of the AUX pin. The AUX pins are internally connected to $V_{OUT}$ and placed adjacent to the BIAS pin to ease printed circuit board routing. Although this pin is internally connected to $V_{OUT}$, it is not intended to deliver a high current, so do NOT connect this pin to the load. If this pin is not tied to BIAS, leave it floating.

**RT (Pin C1):** Connect a resistor between RT and ground to set the switching frequency. Do not drive this pin.

**SHARE1/SHARE2 (Pins C3, C2):** Channel 1/Channel 2 Sharing Control. Tie this to the SHARE*n* pin of another LTM8024 channel when paralleling outputs. Otherwise, leave these pins open.

**RUN1/RUN2 (Pins K1, K2):** The corresponding channel of the LTM8024 is shutdown when this pin is low and active when this pin is high. Tie to $V_{INn}$ if shutdown feature is not used. An external resistor divider from $V_{INn}$ can be used to program a $V_{INn}$ threshold below which the corresponding channel of the LTM8024 will shut down. Do not float this pin.

**CLKOUT (Pin K4):** Synchronization Output. When SYNC > 2.8V, the CLKOUT pin provides a waveform about 90 degrees out-of-phase with Channel 1. This allows synchronization with other regulators with up to four phases. When an external clock is applied to the SYNC pin, the CLKOUT pin will output a waveform with about the same phase, duty cycle, and frequency as the SYNC waveform. In Burst Mode® operation, the CLKOUT pin will be internally grounded. Float this pin if the CLKOUT function is not used. Do not drive this pin.



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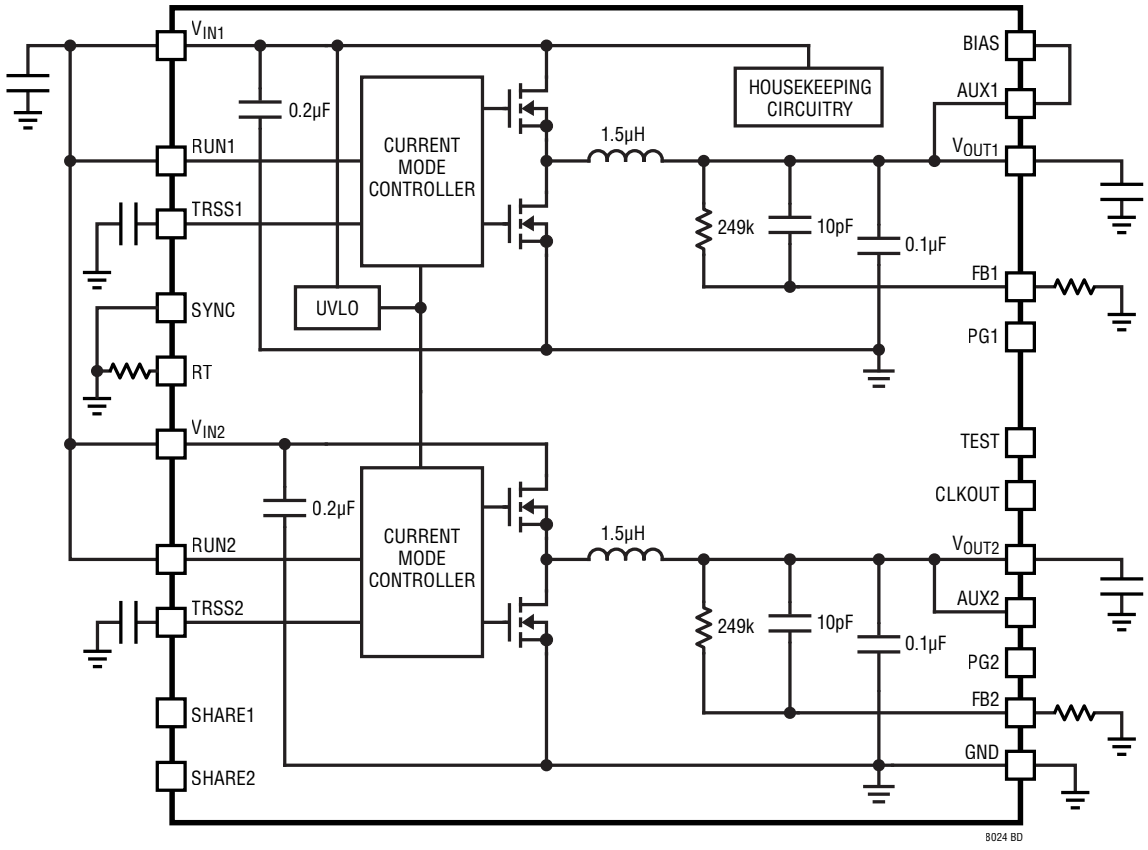
## PIN FUNCTIONS

**PG1/PG2 (Pins L3, K3):** The PG*n* pin is the open-drain output of an internal comparator. PG*n* remains low until the FB1 pin is within ±7.5% of the final regulation voltage, and there are no fault conditions. PG*n* is pulled low during $V_{IN1}$ UVLO, $V_{CC}$ UVLO, thermal shutdown, or when RUN1 or RUN2 are low.

**TEST (Pin L2):** This pin is used in LTM8024 production testing.

**SYNC (Pin L4):** External Clock Synchronization Input. Ground this pin for low ripple Burst Mode operation at low output loads; this will also disable the CLKOUT function. Apply a DC voltage between 2.8V and 4.0V for spread spectrum modulation. Float the SYNC pin for forced continuous operation without spread spectrum modulation. Apply a clock source to the SYNC pin for synchronization to an external frequency. The LTM8024 will be in forced continuous mode when an external frequency is applied.

## BLOCK DIAGRAM



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## OPERATION

The LTM8024 is a dual standalone non-isolated step-down switching DC/DC power supply that can deliver up to 6A (peak) per channel. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable via one external resistor from 0.8V to 8V. The input voltage range for channel 1 is 3V to 40V, while the input voltage range for channel 2 is 2V to 40V. $V_{IN1}$ must be 3V or above for either channel to operate.

Given that the LTM8024 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current. See simplified Block Diagram.

The LTM8024 contains current mode controllers, power switching elements, power inductors and a modest amount of input and output capacitance. The LTM8024 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT pin to GND.

An internal regulator provides power to the control circuitry. This bias regulator normally draws power from the $V_{IN1}$ pin, but if the BIAS pin is connected to an external voltage higher than 3.2V, bias power is drawn from the external source (typically the regulated output voltage). This improves efficiency. Tie BIAS to GND if it is not used.

To enhance efficiency, the LTM8024 automatically switches to Burst Mode operation in light or no load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to just a few µA.

The oscillator reduces the LTM8024's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the output current during start-up and overload.

The TRSS node acts as an auxiliary input to the error amplifier. The voltage at FB servos to the TRSS voltage until TRSS goes above 0.8V. Soft-start is implemented by generating a voltage ramp at the TRSS pin using an external capacitor which is charged by an internal constant current. Alternatively, driving the TRSS pin with a signal source or resistive network provides a tracking function. Do not drive the TRSS pin with a low impedance voltage source. See the Applications Information section for more details.

The LTM8024 contains a power good comparator which trips when the FB pin is at about 92% to 108% of its regulated value. The PG output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. The PG1 signal is valid when $V_{IN1}$ is above 3V. Similarly, the PG2 signal is valid when $V_{IN2}$ is above 2V.

The LTM8024 is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above the maximum temperature rating to avoid interfering with normal operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.



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## APPLICATIONS INFORMATION

For most applications, the design process is straightforward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended $C_{IN}$, $C_{OUT}$, $R_{FB}$ and $R_T$ values.
3. Connect BIAS as indicated.

When using the LTM8024 with two different output voltages, the higher frequency recommended by Table 1 will usually result in the best operation. While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant $R_T$ value) at which the LTM8024 should be allowed to switch is given in Table 1 in the Maximum $f_{SW}$ column, while the recommended frequency (and $R_T$ value) for optimal efficiency over the given input condition is given in the $f_{SW}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

### Capacitor Selection Considerations

The $C_{IN}$ and $C_{OUT}$ capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8024's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8024 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear.

**Table 1. Recommended Component Values and Configuration ($T_A$ = 25°C)**

| $V_{IN}$ (Note 1) | $V_{OUT}$ | $R_{FB}$ (Ω) | $C_{IN}$ (Note 2) | $C_{OUT}$ | BIAS | $f_{SW}$ | $R_T$ (Ω) | MAX $f_{SW}$ | MIN $R_T$ |
|---|---|---|---|---|---|---|---|---|---|
| 3V to 40V | 1V | 976k | 4.7µF 50V 1206 X5R | 2× 100µF 4V X5R 0805 | Up to 10V | 550kHz | 71.5k | 725kHz | 53.6k |
| 3V to 40V | 1.2V | 487k | 4.7µF 50V 1206 X5R | 2× 100µF 4V X5R 0805 | Up to 10V | 600kHz | 64.9k | 875kHz | 43.2k |
| 3V to 40V | 1.5V | 280k | 4.7µF 50V 1206 X5R | 2× 100µF 4V X5R 0805 | Up to 10V | 750kHz | 51.1k | 1MHz | 35.7k |
| 3V to 40V | 1.8V | 200k | 4.7µF 50V 1206 X5R | 100µF 4V X5R 0805 | Up to 10V | 750kHz | 51.1k | 1.3MHz | 26.7k |
| 3.5V to 40V | 2.5V | 115k | 4.7µF 50V 1206 X5R | 100µF 4V X5R 0805 | Up to 10V | 750kHz | 51.1k | 1.7MHz | 19.6k |
| 4.5V to 40V | 3.3V | 78.7k | 4.7µF 50V 1206 X5R | 100µF 4V X5R 0805 | Up to 10V | 900kHz | 41.2k | 2.2MHz | 13k |
| 6.7V to 40V | 5V | 47.5k | 4.7µF 50V 1206 X5R | 47µF 6.3V X5R 0805 | Up to 10V | 1.2MHz | 29.4k | 3MHz | 8.06k |
| 11V to 40V | 8V | 27.4k | 4.7µF 50V 1206 X5R | 47µF 10V X5R 1206 | Up to 10V | 1.2MHz | 29.4k | 3MHz | 8.06k |

**Note 1:** The LTM8024 may be capable of the operating at lower input voltages but may skip switching cycles.

**Note 2:** A bulk input capacitor is required.



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If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8024. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM8024 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

### Frequency Selection

The LTM8024 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 3MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of $R_T$ resistor values and their resultant frequencies. The resistors in the table are standard 1% E96 values.

**Table 2. Switching Frequency vs $R_T$ Value**

| $f_{SW}$ (MHz) | $R_T$ (kΩ) |
|---|---|
| 0.2 | 200 |
| 0.3 | 140 |
| 0.4 | 102 |
| 0.5 | 80.6 |
| 0.6 | 64.9 |
| 0.7 | 56.2 |
| 0.8 | 47.5 |
| 0.9 | 41.2 |
| 1.0 | 35.7 |
| 1.2 | 29.4 |
| 1.4 | 24.9 |
| 1.6 | 21.0 |
| 1.8 | 18.2 |
| 2.0 | 15 |
| 2.2 | 13 |
| 2.4 | 11.5 |
| 2.6 | 10.2 |
| 2.8 | 9.09 |

### Operating Frequency Trade-Offs

It is recommended that the user apply the optimal $R_T$ value given in Table 1 for the input and output operating condition. When using the LTM8024 with two different output voltages, the higher frequency recommended by Table 1 will usually result in the best operation. System level or other considerations, however, may necessitate another operating frequency. While the LTM8024 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8024 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

### BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate other internal circuitry. For proper operation, it must be powered by at least 3.2V. If the output voltage is programmed to 3.2V or higher, BIAS may be simply tied to $V_{OUT}$. If $V_{OUT}$ is less than 3.2V, BIAS can be tied to $V_{IN}$ or some other voltage source. If the BIAS pin voltage is too high, the efficiency of the LTM8024 may suffer. The optimum BIAS voltage is dependent upon many factors, such as load current, input voltage, output voltage and switching frequency. In all cases, ensure that the maximum voltage at the BIAS pin is less than 10V. If BIAS power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the pin. A 1µF ceramic capacitor works well. The BIAS pin may also be tied to GND at the cost of a small degradation in efficiency.

### Maximum Load

The maximum practical continuous load that the LTM8024 can drive per channel, while rated at 3.0A, actually depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM8024 in the case of overload or short-circuit. The internal temperature of the LTM8024



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depends upon operating conditions such as the ambient temperature, the power delivered, and the heat sinking capability of the system. For example, if channel 1 of the LTM8024 is configured to regulate at 1V, and channel 2 is turned off, channel 1 may continuously deliver 6A from $12V_{IN}$ if the ambient temperature is controlled to less than 60°C. This is quite a bit higher than the 3.5A continuous rating. Please see the "Derating, $1V_{OUT}$" curve in the Typical Performance Characteristics section. Similarly, if both channels of the LTM8024 are delivering $8V_{OUT}$ and the ambient temperature is 100°C, each channel will deliver at most 1A from $24V_{IN}$, which is less than the 3.5A continuous rating.

### Load Sharing

The two LTM8024 channels may be paralleled to produce higher currents. To do this, tie the $V_{IN}$, $V_{OUT}$, FB and SHARE pins of all the paralleled channels together. To ensure that paralleled channels start up together, the TRSS pins may be tied together, as well. If it is inconvenient to tie the TRSS pins together, make sure that the same value soft-start capacitors are used for each µModule regulator. An example of two LTM8024 channels configured for load sharing is given in the Typical Applications Section. When load sharing among *n* units and using a single $R_{FB}$ resistor, the value of the resistor is:

$$R_{FB} = \frac{199.2}{n(V_{OUT} - 0.8)}, \text{where } R_{FB} \text{ is in k}\Omega \qquad (1)$$

### Burst Mode Operation

To enhance efficiency at light loads, the LTM8024 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8024 delivers single cycle bursts of current to the output capacitor followed by sleep periods where most of the internal circuitry is powered off and energy is delivered to the load by the output capacitor. During the sleep time, $V_{IN}$ and BIAS quiescent currents are greatly reduced, so, as the load current decreases towards a no load condition, the percentage of time that the LTM8024 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher light load efficiency.

Burst Mode operation is enabled by tying SYNC to GND.

### Minimum Input Voltage

The LTM8024 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. Keep the input above 3V to ensure proper operation. Voltage transients or ripple valleys that cause the input to fall below 3V may turn off the LTM8024.

$V_{IN1}$ must be above 3V for either channel to operate. If $V_{IN1}$ is above 3V, channel 2 will operate as long as $V_{IN2}$ is above 2V.

### Output Voltage Tracking and Soft-Start

The LTM8024 allows the user to adjust its output voltage ramp rate by means of the TRSS pin. An internal 2µA pulls up the TRSS pin to about 2.4V. Putting an external capacitor on TRSS enables soft starting the output to reduce current surges on the input supply. During the soft-start ramp the output voltage will proportionally track the TRSS pin voltage. For output tracking applications, TRSS can be externally driven by another voltage source. From 0V to 0.8V, the TRSS voltage will override the internal 0.8V reference input to the error amplifier, thus regulating the FB pin voltage to that of the TRSS pin. When TRSS is above 0.8V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The TRSS pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the TRSS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the RUN pin transitioning low, $V_{IN}$ voltage falling too low, or thermal shutdown.



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### Pre-Biased Output

As discussed in the Output Voltage Tracking and Soft-Start section, the LTM8024 regulates the output to the FB voltage determined by the TRSS pin whenever TRSS is less than 0.8V. If the LTM8024 output is higher than the target output voltage, and SYNC is not held below 0.8V, the LTM8024 will attempt to regulate the output to the target voltage by returning a small amount of energy back to the input supply. If there is nothing loading the input supply, its voltage may rise. Take care that it does not rise so high that the input voltage exceeds the absolute maximum rating of the LTM8024. If SYNC is grounded, the LTM8024 will not return current to the input.

### Frequency Foldback

The LTM8024 is equipped with frequency foldback which acts to reduce the thermal and energy stress on the internal power elements during a short circuit or output overload condition. If the LTM8024 detects that the output has fallen out of regulation, the switching frequency is reduced as a function of how far the output is below the target voltage. This in turn limits the amount of energy that can be delivered to the load under fault. During the start-up time, frequency foldback is also active to limit the energy delivered to the potentially large output capacitance of the load. When a clock is applied to the SYNC pin, the SYNC pin is floated or held high, the frequency foldback is disabled, and the switching frequency will slow down only during overcurrent conditions.

### Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below about 0.8V (this can be ground or a logic low output). To synchronize the LTM8024 oscillator to an external frequency, connect a square wave (with about 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.8V and peaks above 1.5V.

The LTM8024 may be synchronized over a 200kHz to 3MHz range. The LTM8024 will not enter Burst Mode operation at light output loads while synchronized to an external clock. The $R_T$ resistor should be chosen to set the switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the $R_T$ should be selected for 500kHz or lower frequency.

The LTM8024 features spread spectrum operation to further reduce EMI/EMC emissions. To enable spread spectrum operation, apply between 2.8V and 4.0V to the SYNC pin. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by $R_T$ to about 20% higher than that value. The modulation frequency is about 3kHz. For example, when the LTM8024 is programmed to 2MHz, the frequency will vary from 2MHz to 2.4MHz at a 3kHz rate. When spread spectrum operation is selected, Burst Mode operation is disabled, and the part may run in forced continuous mode. Do not tie SYNC to GND when load sharing. Please see the load sharing section for details.

### Shorted Input Protection

Care needs to be taken in systems where the output is held high when the input to the LTM8024 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR'ed with the LTM8024's output. If the $V_{IN}$ pin is allowed to float and the RUN pin is held high (either by a logic signal or because it is tied to $V_{IN}$), then the LTM8024's internal circuitry pulls its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN pin, the internal current drops to essentially zero. However, if the $V_{IN}$ pin is grounded while the output is held high, parasitic diodes inside the LTM8024 can pull large currents from the output through the $V_{IN}$ pin. Figure 1 shows a circuit that runs only when the input voltage is present and that protects against a shorted or reversed input.



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### PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8024. The LTM8024 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified

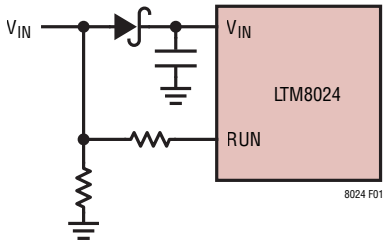


**Figure 1. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8024 Runs Only When the Input Is Present**

operation with a haphazard or poor layout. See Figure 2 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place the $R_{FB}$ and $R_T$ resistors as close as possible to their respective pins.
2. Place the $C_{IN}$ capacitor as close as possible to the $V_{IN}$ and GND connection of the LTM8024.
3. Place the $C_{OUT}$ capacitor as close as possible to the $V_{OUT}$ and GND connection of the LTM8024.
4. Place the $C_{IN}$ and $C_{OUT}$ capacitors such that their ground current flow directly adjacent to or underneath the LTM8024.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8024.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 2. The LTM8024 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

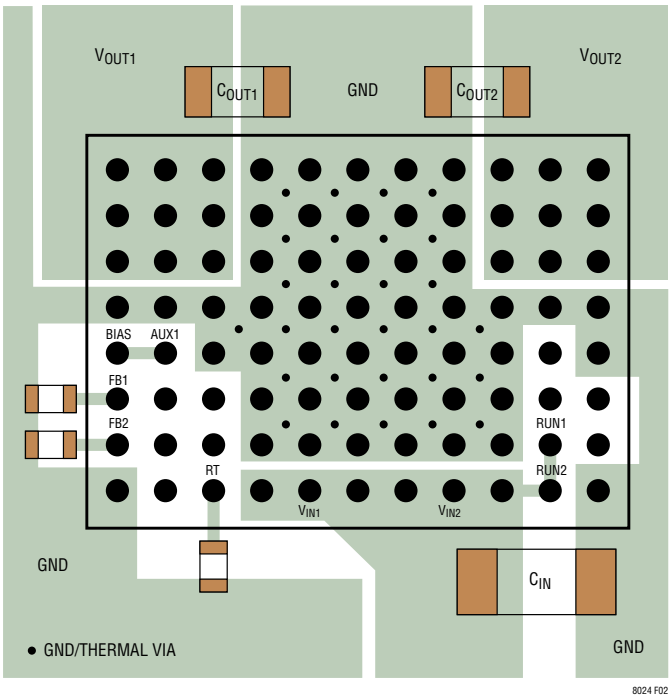


**Figure 2. Layout Showing Suggested External Components, GND Plane and Thermal Vias**



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## APPLICATIONS INFORMATION

### Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8024. However, these capacitors can cause problems if the LTM8024 is plugged into a live supply (see Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the $V_{IN}$ pin of the LTM8024 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8024's rating and damaging the part. If the input supply is poorly controlled or the LTM8024 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to $V_{IN}$, but the most popular method of controlling input voltage overshoot is add an electrolytic bulk cap to the $V_{IN}$ net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

### Thermal Considerations

The LTM8024 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The derating curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8024 mounted to a 77cm$^2$ 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA (Finite Element Analysis) or CFD (Computational Fluid Dynamics) to predict thermal performance. To that end, the Pin Configuration typically gives three dominant thermal coefficients:

1. $\theta_{JA}$ – Thermal resistance from junction to ambient
2. $\theta_{JCbot}$ – Thermal resistance from junction to the bottom of the product case
3. $\theta_{JCtop}$ – Thermal resistance from junction to top of the product case

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

1. $\theta_{JA}$ is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{JCbot}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user'sapplication.
3. $\theta_{JCtop}$ is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbot}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.



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## APPLICATIONS INFORMATION

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical approximation of these dominant thermal resistances is given in Figure 3. Some thermal resistance elements, such as heat flow out the side of the package, are not defined by the JEDEC standard, and are not shown. The blue resistances are contained within the µModule regulator, and the green are outside.

The die temperature of the LTM8024 must be lower than the maximum rating, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8024. The bulk of the heat flow out of the LTM8024 is through the bottom of the package and the pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

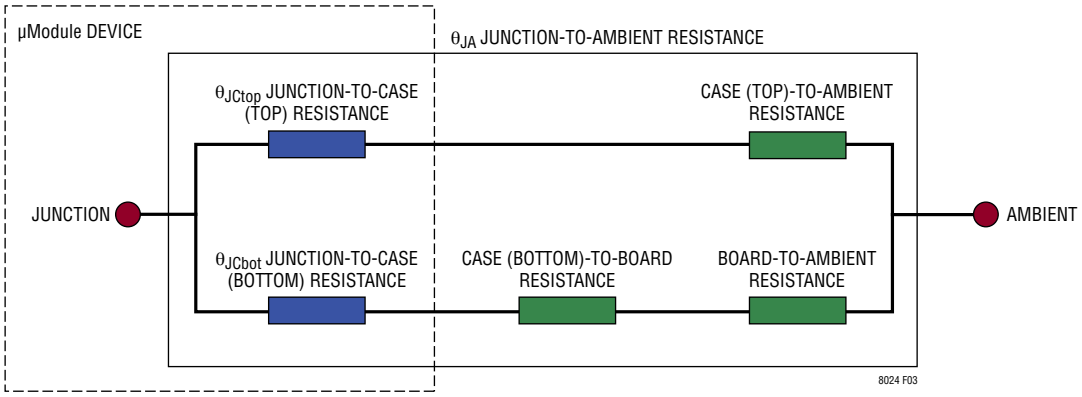


**Figure 3. Graphical Approximation of the Thermal Coefficients, Including JESD51-12 Terms**



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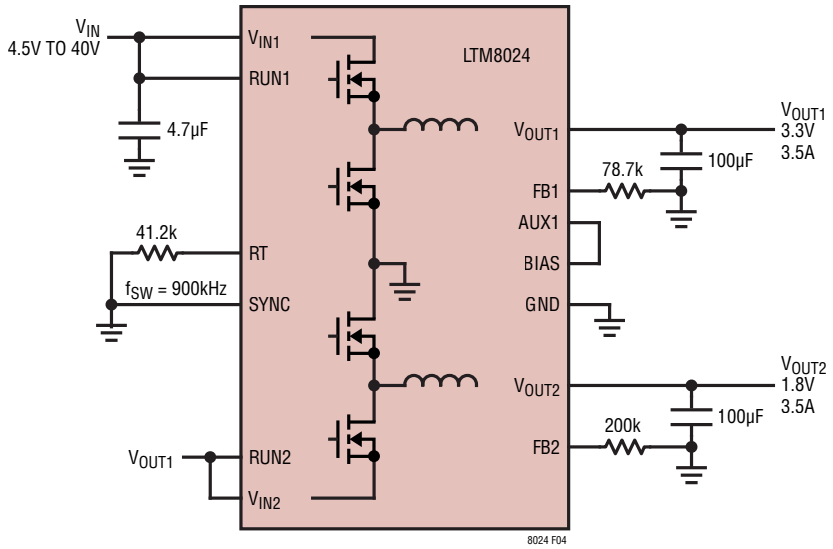
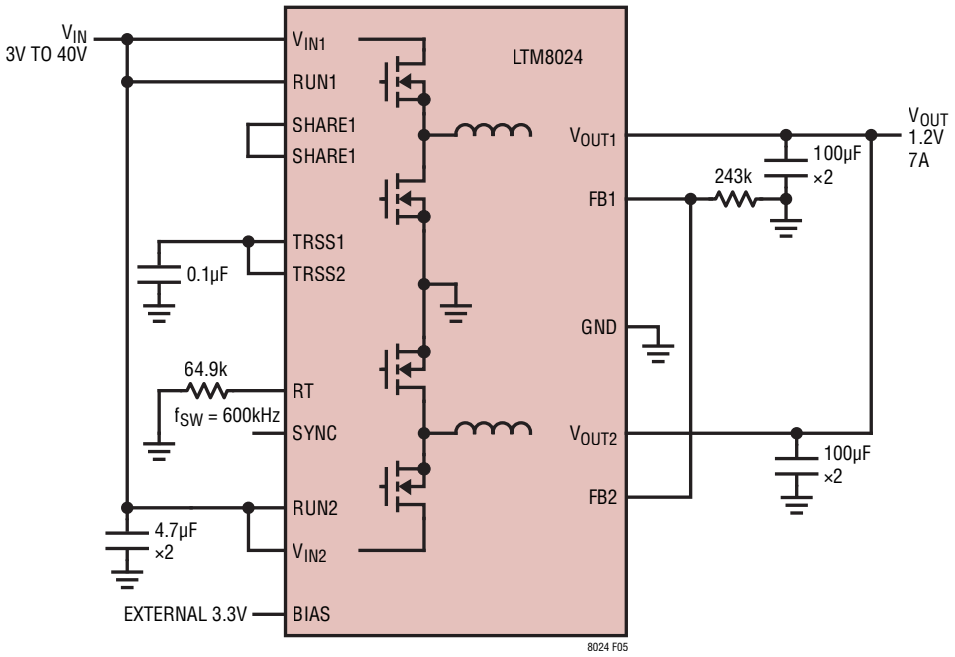
# TYPICAL APPLICATIONS




PINS NOT USED: TRSS1, TRSS2, SHARE1, SHARE2, PG1, PG2, TEST, CLKOUT

**Figure 4. 1.8V/3.5A and 3.3V/3.5A from 4.5V to 40$V_{IN}$. BIAS Is Connected to AUX1**




PINS NOT USED: PG1, PG2, TEST, CLKOUT, AUX1, AUX2

**Figure 5. Parallel Two Channels to Produce 1.2V/7A from 3V to 40$V_{IN}$. BIAS is Tied to External 3.3V**



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## TYPICAL APPLICATIONS

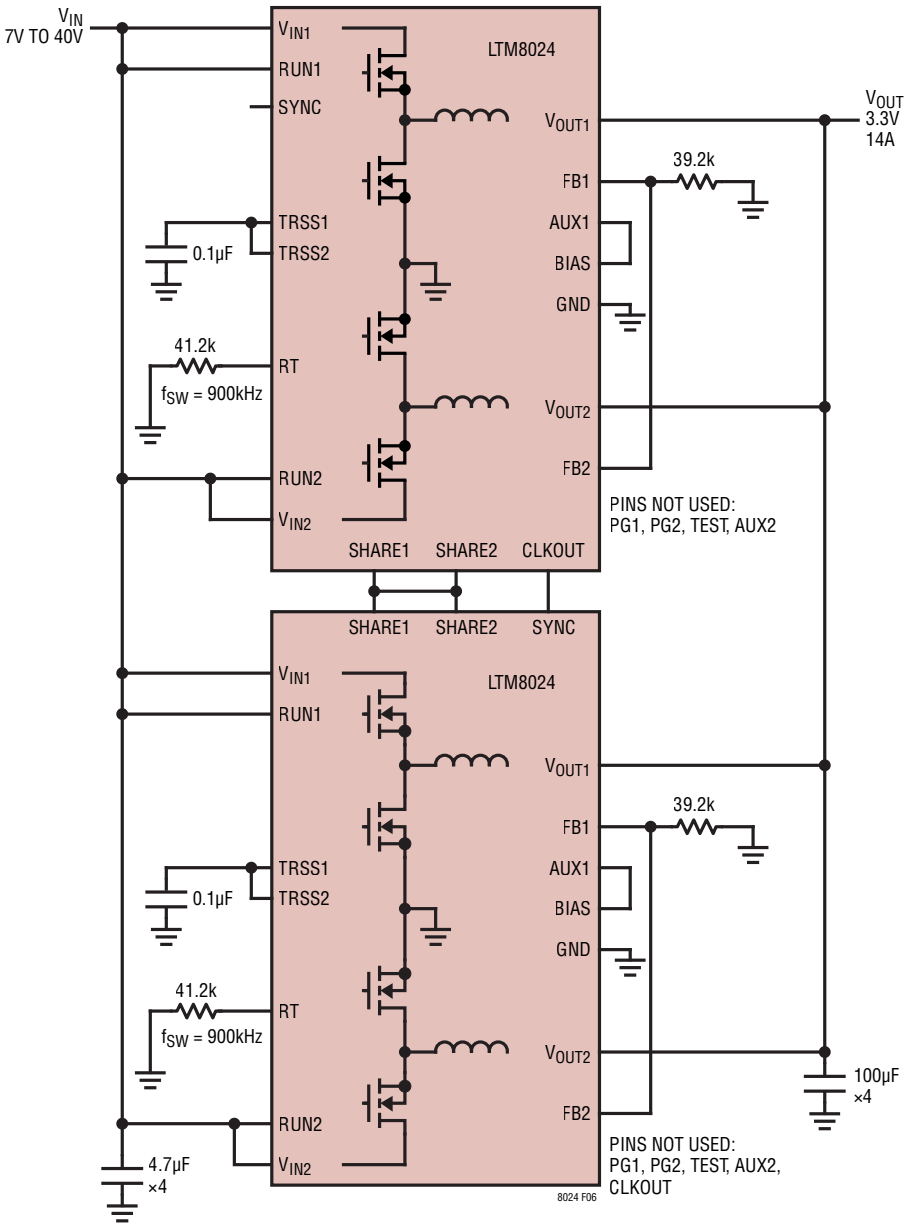


**Figure 6. Parallel Four Channels to Produce 3.3V/14A from 7V to 40$V_{IN}$. BIAS is Tied to AUX1**



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# PACKAGE DESCRIPTION

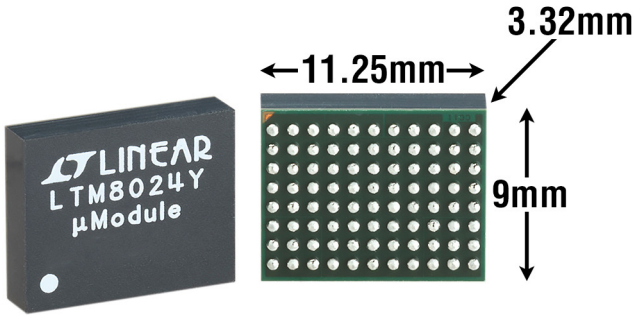
| | |
|---|---|
| 3.0 | 8.06 |

**Table 3. LTM8024 Pinout (Sorted by Pin Number)**

| PIN | PIN NAME | PIN | PIN NAME | PIN | PIN NAME | PIN | PIN NAME | PIN | PIN NAME | PIN | PIN NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | GND | B1 | TRSS1 | C1 | RT | D1 | VIN1 | E1 | VIN1 | F1 | VIN1 |
| A2 | FB2 | B2 | TRSS2 | C2 | SHARE2 | D2 | GND | E2 | GND | F2 | GND |
| A3 | FB1 | B3 | AUX2 | C3 | SHARE1 | D3 | GND | E3 | GND | F3 | GND |
| A4 | BIAS | B4 | AUX1 | C4 | GND | D4 | GND | E4 | GND | F4 | GND |
| A5 | GND | B5 | GND | C5 | GND | D5 | GND | E5 | GND | F5 | GND |
| A6 | $V_{OUT1}$ | B6 | $V_{OUT1}$ | C6 | $V_{OUT1}$ | D6 | GND | E6 | GND | F6 | GND |
| A7 | $V_{OUT1}$ | B7 | $V_{OUT1}$ | C7 | $V_{OUT1}$ | D7 | GND | E7 | GND | F7 | GND |
| A8 | $V_{OUT1}$ | B8 | $V_{OUT1}$ | C8 | $V_{OUT1}$ | D8 | GND | E8 | GND | F8 | GND |

| PIN | PIN NAME | PIN | PIN NAME | PIN | PIN NAME | PIN | PIN NAME | PIN | PIN NAME |
|---|---|---|---|---|---|---|---|---|---|
| G1 | $V_{IN2}$ | H1 | $V_{IN2}$ | J1 | $V_{IN2}$ | K1 | RUN1 | L1 | GND |
| G2 | GND | H2 | GND | J2 | GND | K2 | RUN2 | L2 | TEST |
| G3 | GND | H3 | GND | J3 | GND | K3 | PG2 | L3 | PG1 |
| G4 | GND | H4 | GND | J4 | GND | K4 | CLKOUT | L4 | SYNC |
| G5 | GND | H5 | GND | J5 | GND | K5 | GND | L5 | GND |
| G6 | GND | H6 | GND | J6 | $V_{OUT2}$ | K6 | $V_{OUT2}$ | L6 | $V_{OUT2}$ |
| G7 | GND | H7 | GND | J7 | $V_{OUT2}$ | K7 | $V_{OUT2}$ | L7 | $V_{OUT2}$ |
| G8 | GND | H8 | GND | J8 | $V_{OUT2}$ | K8 | $V_{OUT2}$ | L8 | $V_{OUT2}$ |

# PACKAGE PHOTOGRAPH





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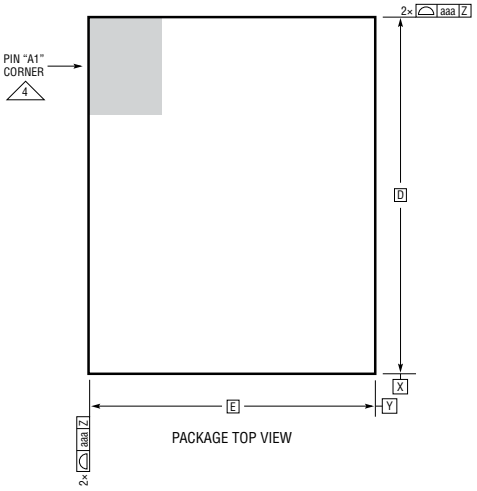
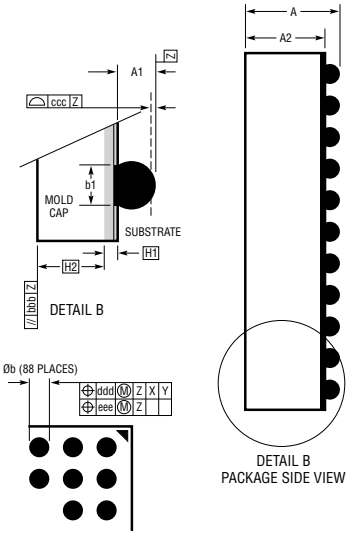
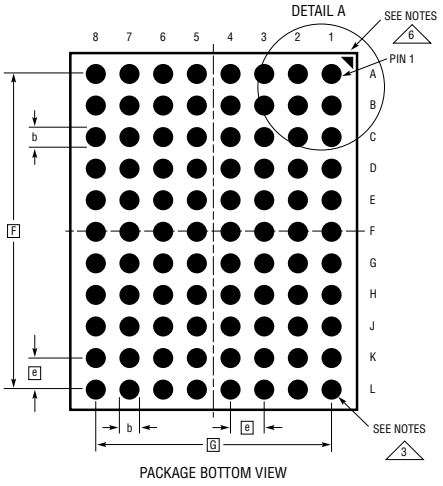
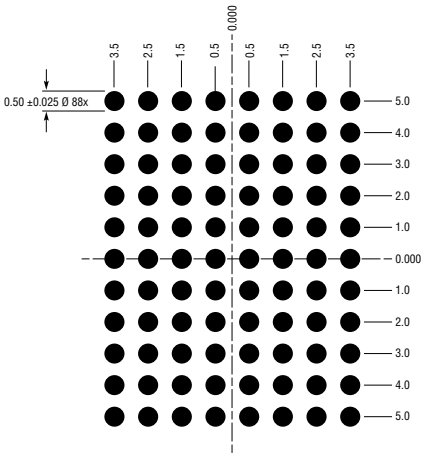
# PACKAGE DESCRIPTION

**BGA Package**
**88-Lead (11.25mm × 9mm × 3.32mm)**
(Reference LTC DWG # 05-08-1535 Rev A)



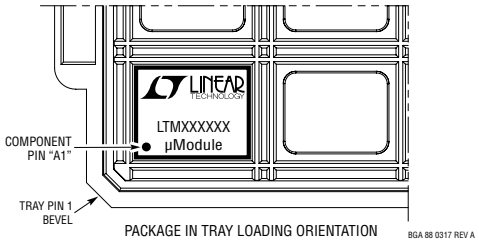




| DIMENSIONS | | | | |
|---|---|---|---|---|
| **SYMBOL** | **MIN** | **NOM** | **MAX** | **NOTES** |
| A | 3.12 | 3.32 | 3.52 | |
| A1 | 0.40 | 0.50 | 0.60 | BALL HT |
| A2 | 2.72 | 2.82 | 2.92 | |
| b | 0.50 | 0.60 | 0.70 | BALL DIMENSION |
| b1 | 0.47 | 0.50 | 0.53 | PAD DIMENSION |
| D | | 11.25 | | |
| E | | 9.00 | | |
| e | | 1.00 | | |
| F | | 10.00 | | |
| G | | 7.00 | | |
| H1 | | 0.32 | | SUBSTRATE THK |
| H2 | | 2.50 | | MOLD CAP HT |
| aaa | | | 0.15 | |
| bbb | | | 0.20 | |
| ccc | | | 0.20 | |
| ddd | | | 0.25 | |
| eee | | | 0.10 | |
| TOTAL NUMBER OF BALLS: 88 | | | | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



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# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 03/20 | Added Output Voltage Ripple DC1868A Demo Board Graph | 7 |
| | | Added Output Noise Spectrum DC1868A, 100kHz, 10MHz and 500MHz Span Performance Graphs | 8 |
| | | Added CISPR25 Radiated Emission with Class 5 Average Limit DC1868A Demo Board Graphs | 8 |



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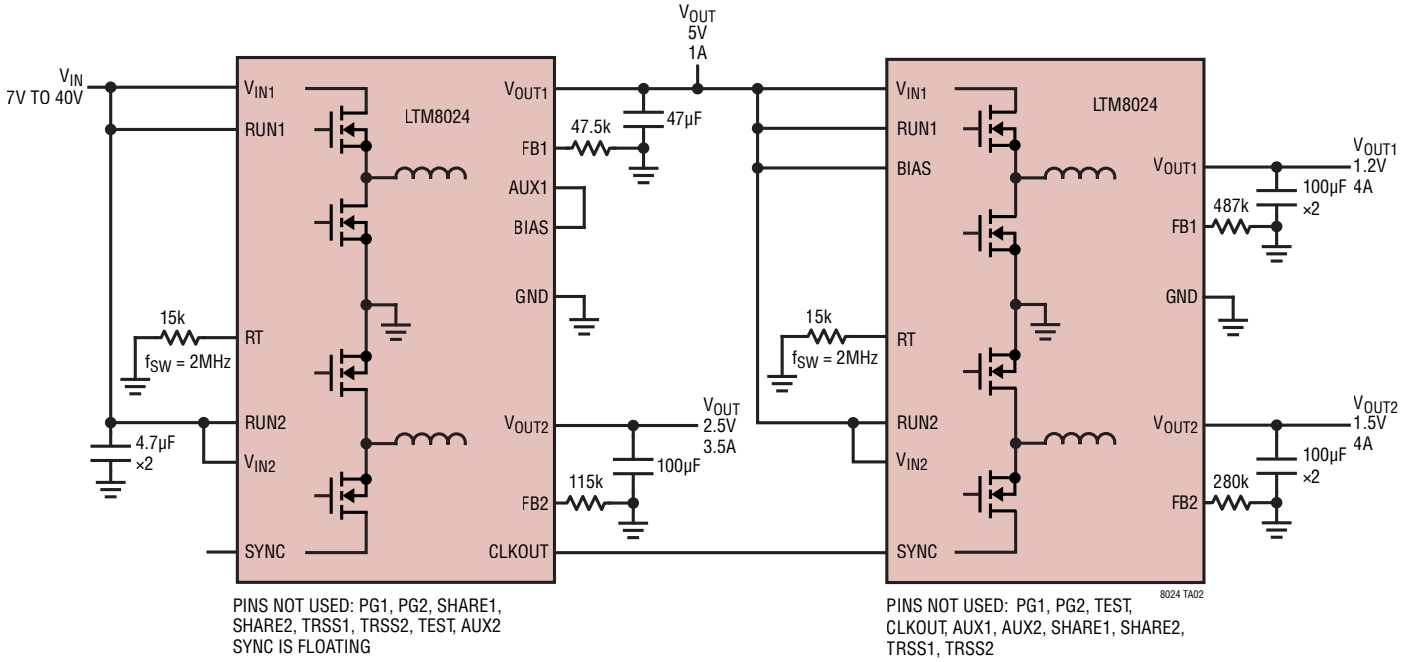
## TYPICAL APPLICATION

**5V/1A, 2.5V/3.5A, 1.5V/4A, 1.2V/4A from 7V to 40V$_{IN}$**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTM8033 | 36V, 3A Low EMI Step-Down µModule Regulator | 3.6V ≤ $V_{IN}$ ≤ 36V, 0.8V ≤ $V_{OUT}$ ≤ 24V, EN55022B Compliant |
| LTM8074 | 40V, 1.2A Silent Switcher Step-Down µModule Regulator | 3.2V ≤ $V_{IN}$ ≤ 40V, 0.8V ≤ $V_{OUT}$ ≤ 12V, 4mm × 4mm × 1.82mm BGA Package |
| LTM8063 | 40V, 2A Silent Switcher Step-Down µModule Regulator | 3.2V ≤ $V_{IN}$ ≤ 40V, 0.8V ≤ $V_{OUT}$ ≤ 15V, 6.25mm × 4mm × 2.22mm BGA Package |
| LTM8065 | 40V, 2.5A Silent Switcher Step-Down µModule Regulator | 3.4V ≤ $V_{IN}$ ≤ 40V, 0.97V ≤ $V_{OUT}$ ≤ 18V, 6.25mm × 6.25mm × 2.32mm BGA Package |
| LTM8053 | 40V, 3.5A Silent Switcher Step-Down µModule Regulator | 3.4V ≤ $V_{IN}$ ≤ 40V. 0.97V ≤ $V_{OUT}$ ≤ 15V. 6.25mm × 9mm × 3.32mm BGA Package |
| LTM8003 | 40V, 3.5A H-Grade (150°C Operation), FMEA Compliant Pinout | 3.4V ≤ $V_{IN}$ ≤ 40V, 0.97V ≤ $V_{OUT}$ ≤ 15V, $I_{OUT}$ = 3.5A, 6.25mm × 9mm × 3.32mm BGA Package |
| LTM8073 | 60V, 3A Silent Switcher Step-Down µModule Regulator | 3.4V ≤ $V_{IN}$ ≤ 60V, 0.8V ≤ $V_{OUT}$ ≤ 15V, 6.25mm × 9mm × 3.32mm BGA Package |
| LTM8071 | 60V, 5A Silent Switcher Step-Down µModule Regulator | 3.6V ≤ $V_{IN}$ ≤ 60V, 0.97V ≤ $V_{OUT}$ ≤ 15V, 9mm × 11.25mm × 3.32mm BGA Package |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