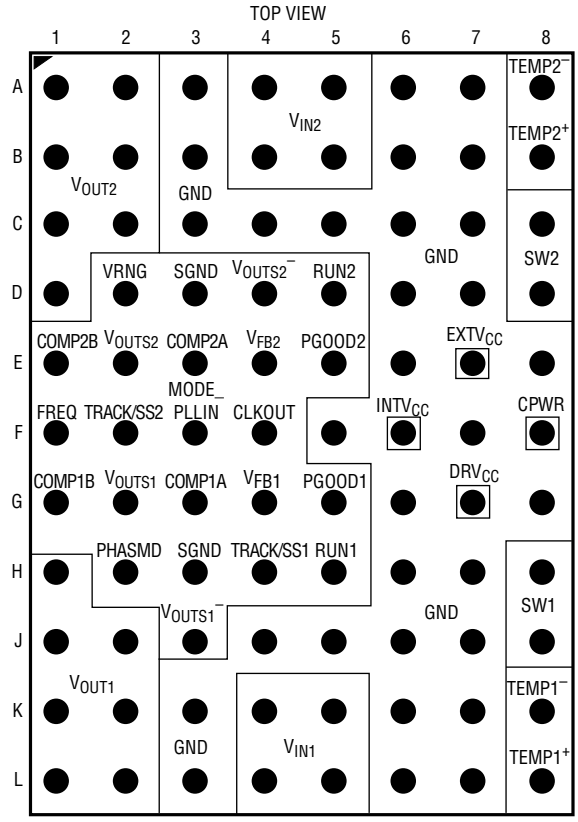
ABSOLUTE MAXIMUM RATINGS

(Note 1)

CPWR, V_{IN1}, V_{IN2} ..... –0.3V to 22V
V_{SW1}, V_{SW2} ..... –2V to 22V
PGOOD1, PGOOD2, RUN1, RUN2, DRV_{CC}, $INTV_{CC}$, $EXTV_{CC}$, V_{OUT1}, V_{OUT2}, V_{OUTS1}, V_{OUTS2} ..... –0.3V to 6V
TRACK/SS1, TRACK/SS2 ..... –0.3V to 5V
FREQ, VRNG, PHASMD, MODE_PLLIN ..... –0.3V to ($INTV_{CC}$+0.3)
V_{OUTS1}^- (Note 6) ..... –0.3V to V_{FB1}
V_{OUTS2}^-, V_{FB1} (Note 6) ..... –0.3V to ($INTV_{CC}$+0.3V)
COMP1A, COMP2A (Note 6) ..... –0.3V to 2.7V
COMP1B, COMP2B, V_{FB2} ..... –0.3V to 2.7V
DRV_{CC} Peak Output Current 100mA
Internal Operating Temperature Range (Note 2)
E- and I-Grade ..... –40°C to 125°C
MP-Grade ..... –55°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Package Body Temperature .... 245°C

PIN CONFIGURATION



BGA PACKAGE
88-LEAD (15mm × 11.25mm × 5.74mm)
T_{JMAX} = 125°C, θ_{JA} = 7°C/W, $\theta_{JCbottom}$ = 1.5°C/W, θ_{JCtop} = 3.7°C/W, θ_{JB} + θ_{BA} ≅ 7°C/W
θ VALUES DEFINED PER JESD51-12
WEIGHT = 2.2g

ORDER INFORMATION

PART NUMBER	BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4662EY#PBF	SAC305 (RoHS)	LTM4662Y	e1	BGA	3	–40°C to 125°C
LTM4662IY#PBF		LTM4662Y				–40°C to 125°C
LTM4662MPY#PBF		LTM4662Y				–55°C to 125°C
LTM4662IY	SnPb (63/37)	LTM4662Y	e0			–40°C to 125°C
LTM4662MPY		LTM4662Y				–55°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel. T_A = 25°C, V_{IN} = 12V and V_{RUN1}, V_{RUN2} at 5V unless otherwise noted. Per the typical application in Figure 20.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage	2.375V with 5V External Bias on CPWR, 4.5V Min without Bias	●	2.375		20	V
$V_{CPWR(DC)}$	Input Control Power Voltage	Input Range of Bias Normally Connected to V_{IN}		4.5		20	V
$V_{OUT1, 2(Range)}$	Output Voltage Range	(Note 8)	●	0.6		5.5	V
$V_{OUT1(DC)}$, $V_{OUT2(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 10µF ×4, C_{OUT} = 100µF ×4 Ceramic V_{OUT} = 1.5V	●	1.4775	1.5	1.5225	V
Input Specifications							
V_{RUN1}, V_{RUN2}	RUN Pin On/Off Threshold	RUN Rising		1.1	1.2	1.3	V
$V_{RUN1HYS}$, $V_{RUN2HYS}$	RUN Pin On Hysteresis				160		mV
R_{RUN1}, R_{RUN2}	RUN1, RUN2 Resistance	Pull-Down Resistance			100		kΩ
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	I_{OUT} = 0A, C_{IN} = 10µF ×4, C_{SS} = 0.01µF, C_{OUT} = 100µF ×4, V_{OUT1} = 1.5V, V_{OUT2} = 1.5V, V_{IN} = 12V			1		A
$I_{Q(VIN)}$	Input Supply Bias Current	I_{OUT} = 0.1A, f_{SW} = 1MHz, Pulse-Skipping Mode I_{OUT} = 0.1A, f_{SW} = 1MHz, Switching Continuous Shutdown, RUN = 0, V_{IN} = 12V			20 45 40		mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 4.5V, V_{OUT} = 1.5V, I_{OUT} = 15A V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 15A			5.9 2.15		A A
Output Specifications							
$I_{OUT1(DC)}$, $I_{OUT2(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V (Notes 7, 8)		0		15	A
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} from 4.5V to 20V I_{OUT} = 0A for Each Output	●		0.01	0.025	%/V
$\Delta V_{OUT1(LOAD)}/V_{OUT1}$ $\Delta V_{OUT2(LOAD)}/V_{OUT2}$	Load Regulation Accuracy	For Each Output, V_{OUT} = 1.5V, 0A to 15A V_{IN} = 12V (Note 7)	●		0.15	0.3	%
$V_{OUT1(AC)}$, $V_{OUT2(AC)}$	Output Ripple Voltage	For Each Output, I_{OUT} = 0A, C_{OUT} = 100µF ×4, V_{IN} = 12V, V_{OUT} = 1.5V, Frequency = 350kHz			15		mV_{P-P}
f_S (Each Channel)	Output Ripple Voltage Frequency	V_{IN} = 12V, V_{OUT} = 1.5V, R_{FREQ} = 115kΩ (Note 4)			350		kHz
$\Delta V_{OUTSTART}$ (Each Channel)	Turn-On Overshoot	C_{OUT} = 100µF ×4, V_{OUT} = 1.5V, I_{OUT} = 0A V_{IN} = 12V, C_{SS} = 0.01µF			10		mV
t_{START} (Each Channel)	Turn-On Time	C_{OUT} = 100µF ×4, No Load, TRACK/SS with 0.01µF to GND, V_{IN} = 12V			5		ms
$\Delta V_{OUT(LS)}$ (Each Channel)	Peak Deviation for Dynamic Load	Load: 0A to 6A to 0A C_{OUT} = 100µF ×4, V_{IN} = 12V, V_{OUT} = 1.5V			50		mV
t_{SETTLE} (Each Channel)	Settling Time for Dynamic Load Step	Load: 0A to 6A to 0A C_{OUT} = 100µF ×4, V_{IN} = 12V, V_{OUT} = 1.5V			20		µs
$I_{OUT(PK)}$ (Each Channel)	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.5V			22		A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel. T_A = 25°C, V_{IN} = 12V and V_{RUN1}, V_{RUN2} at 5V unless otherwise noted. Per the typical application in Figure 20.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Section							
V_{FB1}	Voltage at V_{FB1} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.592	0.600	0.608	V
V_{FB2}	Voltage at V_{FB2} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V V_{FB2} is Gained Back Up by 2× Internal to 0.6V	●	0.296	0.3	0.304	V
I_{FB1}, I_{FB2}		(Note 6)			0	±50	nA
V_{OVL1}, V_{OVL2}	Feedback Overvoltage Lockout	V_{FB1} Rising, V_{FB2} Rising	●	0.630 0.315	0.645 0.323	0.660 0.330	V V
$I_{TRACK/SS1}$, $I_{TRACK/SS2}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS1,TRACK/SS2 = 0V			1.0		µA
UVLO	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Falling V_{IN} (Note 6) $INTV_{CC}$ Rising V_{IN}		3.3	3.7 4.2	 4.5	V V
$t_{OFF(MIN)}$	Minimum Top Gate Off-Time	(Note 6)			90		ns
$t_{ON(MIN)}$	Minimum Top Gate On-Time	(Note 6)			30		ns
R_{FBHI1}, R_{FBHI2}	Resistor Between V_{OUTS1}, V_{OUTS2} and V_{FB1}, V_{FB2} Pins for Each Output			59.9	60.4	60.9	kΩ
V_{PGOOD1}, V_{PGOOD2} Low	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V		–2		2	µA
V_{PGOOD}	PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive			 –7.5 7.5		 % %
Internal Linear Regulator							
DRV_{CC}	Internal DRV_{CC} Voltage	6V < CPWR < 20V		5.0	5.3	5.6	V
DRV_{CC} Load Regulation	DRV_{CC} Load Regulation	I_{CC} = 0mA to 100mA			–1.3	–3.0	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.4	4.6	4.8	V
$V_{EXTVCC(DROP)}$	$EXTV_{CC}$ Dropout	I_{CC} = 20mA, V_{EXTVCC} = 5V			80	120	mV
$V_{EXTVCC(HYST)}$	$EXTV_{CC}$ Hysteresis				200		mV
Frequency and Clock Synchronization							
Frequency Nominal	Nominal Frequency	R_{FREQ} = 115kΩ		300	350	400	kHz
Frequency Low	Lowest Frequency	R_{FREQ} = 165kΩ (Note 5)			250		kHz
Frequency High	Highest Frequency	R_{FREQ} = 39.2kΩ		900	1000	1100	kHz
R_{MODE_PLLIN}	MODE_PLLIN Input Resistance	MODE_PLLIN to SGND			600		kΩ
Channel 2 Phase	V_{OUT2} Phase Relative to V_{OUT1}	PHASMD = SGND PHASMD = Float PHASMD = $INTV_{CC}$			180 180 240		Deg Deg Deg
CLKOUT Phase	Phase (Relative to V_{OUT1})	PHASMD = SGND PHASMD = Float PHASMD = $INTV_{CC}$			60 90 120		Deg Deg Deg
V_{PLLIN} High V_{PLLIN} Low	Clock Input High Level to MODE_PLLIN Clock Input Low Level to MODE_PLLIN			2		 0.5	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel. T_A = 25°C, V_{IN} = 12V and V_{RUN1}, V_{RUN2} at 5V unless otherwise noted. Per the typical application in Figure 20.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SYNC} (Each Channel)	Frequency Sync Capture Range	MODE_PLLIN Clock Duty Cycle = 50%		250		1000	kHz
VRNG I_{LIMIT}	SET Current Limit Per Channel	VRNG = $INTV_{CC}$, I_{OUT} to 15A, I_{LIMIT} ~22A VRNG = SGND, I_{OUT} to 7.5A, I_{LIMIT} ~11A			15 7.5		A A
$t_{D(PGOOD)}$	Delay from V_{FB} Fault (OV/UV) to PGOOD Falling	(Note 6)			50		µs
$t_{D(PGOOD)}$	Delay from V_{FB} Fault (OV/UV Clear) to PGOOD	(Note 6)			20		µs
V_{TEMP1}, V_{TEMP2}	TEMP Diode Voltage	I_{TEMP} = 100µA			0.598		V
T_C $V_{TEMP1,2}$	V_{TEMP} Temperature Coefficient				–2.0		mV/°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4662 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4662E is guaranteed to meet specifications from 0°C to 125°C internal temperature. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4662I is guaranteed over the full –40°C to 125°C internal operating temperature range. The LTM4662MP is tested and guaranteed over full –55°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: Two outputs are tested separately and the same testing condition is applied to each output.

Note 4: The switching frequency is programmable from 250kHz to 1000kHz.

Note 5: LTM4662 device is optimized to operate from 300kHz to 750kHz.

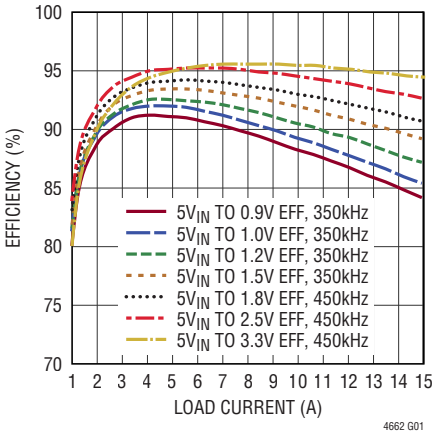
Note 6: These parameters are tested at wafer sort.

Note 7: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

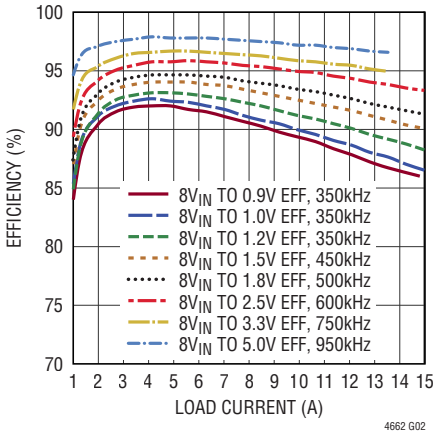
Note 8: For 6V ≤ V_{IN} ≤ 20V, the 3.3 to 5V output current needs to be limited to 13A/channel. All other input and output combinations are 15A/channel with recommended switching frequency included in the efficiency graphs. Derating curves and airflow apply.

TYPICAL PERFORMANCE CHARACTERISTICS

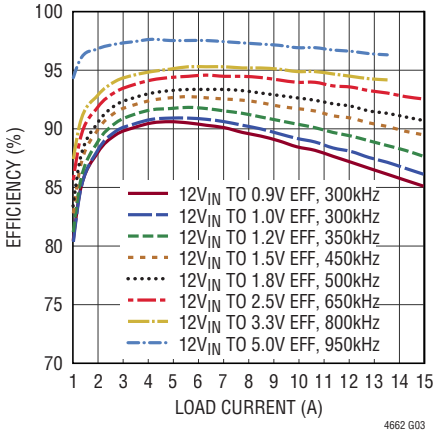
Efficiency vs Output Current, V_{IN} = 5V



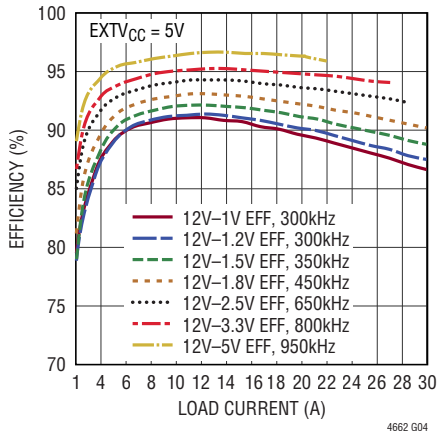
Efficiency vs Output Current, V_{IN} = 8V



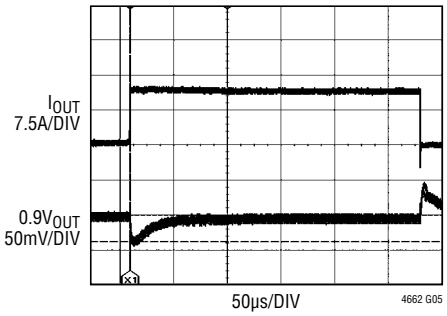
Efficiency vs Output Current, V_{IN} = 12V



Dual Phase Single Output Efficiency vs Output Current, V_{IN} = 12V

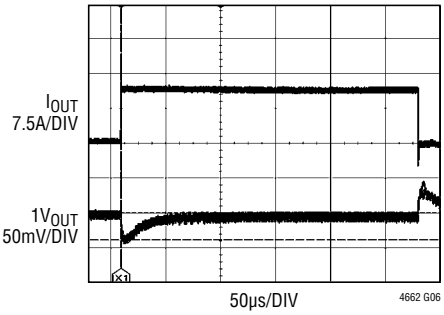


0.9V Single Phase Single Output Load Transient Response



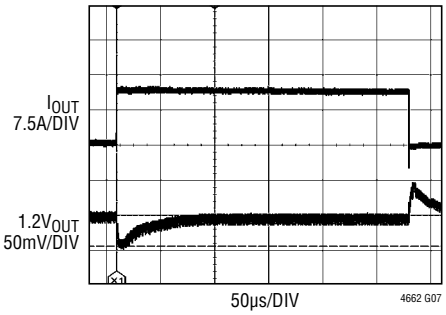
C_{OUT} = 470µF POSCAP, 5mΩ,
100µF ×4, CERAMIC
C_{COMP} = 100pF,
f = 350kHz

1V Single Phase Single Output Load Transient Response



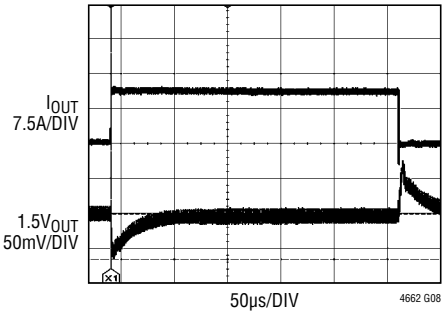
C_{OUT} = 470µF POSCAP, 5mΩ,
100µF ×4, CERAMIC
C_{COMP} = 100pF,
f = 350kHz

1.2V Single Phase Single Output Load Transient Response



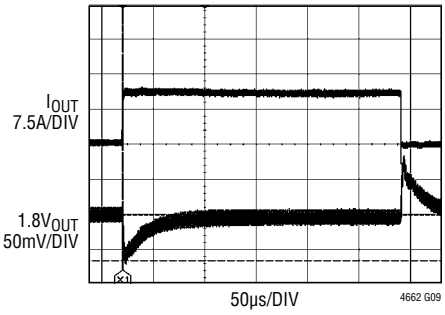
C_{OUT} = 470µF POSCAP, 5mΩ,
100µF ×4, CERAMIC
C_{COMP} = 100pF,
f = 350kHz

1.5V Single Phase Single Output Load Transient Response



C_{OUT} = 100µF ×3, CERAMIC
C_{COMP} = 100pF, C_{FF} = 47pF
f = 450kHz

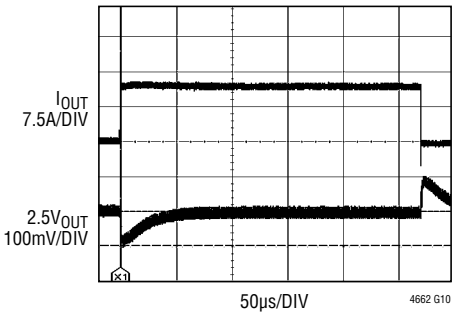
1.8V Single Phase Single Output Load Transient Response



C_{OUT} = 100µF ×3, CERAMIC
C_{COMP} = 100pF, C_{FF} = 47pF
f = 500kHz

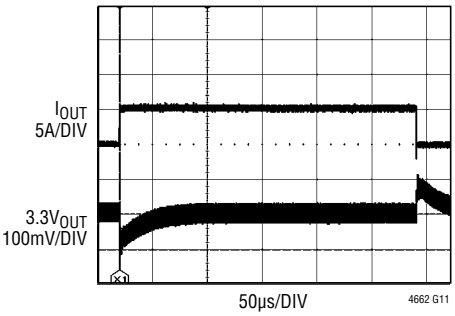
TYPICAL PERFORMANCE CHARACTERISTICS

2.5V Single Phase Single Output Load Transient Response



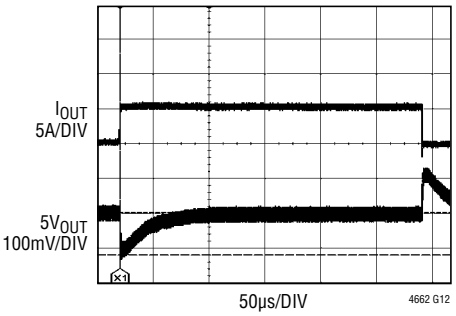
C_{OUT} = 100µF ×2, CERAMIC
C_{COMP} = 100pF, C_{FF} = 47pF
f = 500kHz

3.3V Single Phase Single Output Load Transient Response



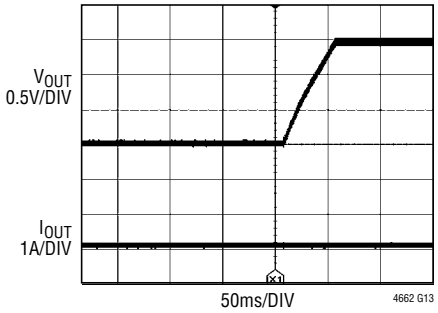
C_{OUT} = 100µF ×1, CERAMIC
C_{COMP} = 100pF, C_{FF} = 47pF
f = 750kHz

5V Single Phase Single Output Load Transient Response



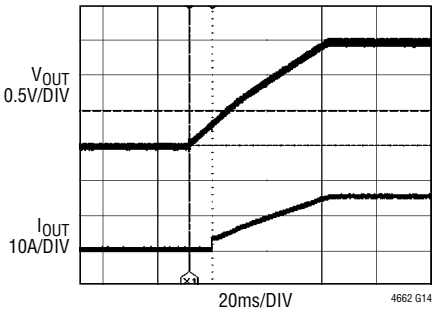
C_{OUT} = 100µF ×1, CERAMIC
C_{COMP} = 100pF, C_{FF} = 47pF
f = 950kHz

Single Phase Single Output Start-Up, No Load



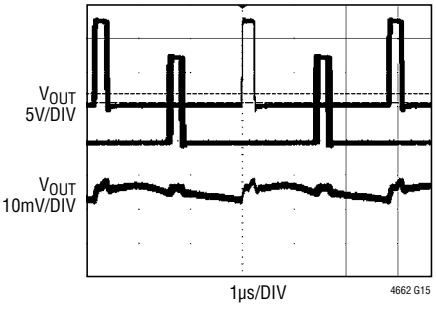
$12V_{IN}$, $1.5V_{OUT}$ AT NO LOAD
C_{OUT} = 470µF ×1, 2.5V, SANYO POSCAP,
100µF ×4, 6.3V, CERAMIC
SOFT-START CAPACITOR = 0.1µF
USE RUN PIN TO CONTROL START-UP

Single Phase Single Output Start-Up, 15A Load



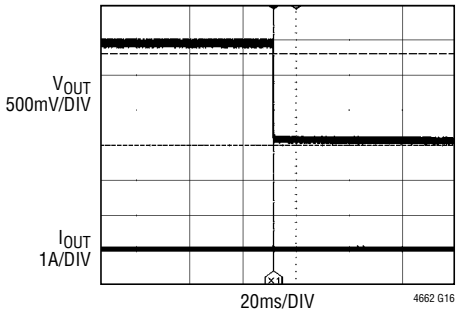
$12V_{IN}$, $1.5V_{OUT}$ AT 15A LOAD
C_{OUT} = 470µF ×1, 2.5V, SANYO POSCAP,
100µF ×4, 6.3V, CERAMIC
SOFT-START CAPACITOR = 0.1µF
USE RUN PIN TO CONTROL START-UP

Two-Phase Switching and Ripple



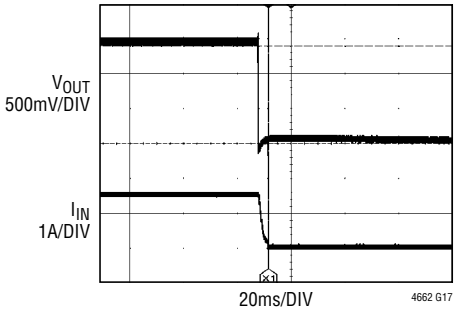
12V TO 1V AT 30A TWO-PHASE
12V TO 1V AT 350kHz
RIPPLE AT 30A LOAD
C_{OUT} = 330µF, 9mΩ, 100µF ×4, CERAMIC

Short-Circuit Protection, No Load



V_{IN} = 12V
V_{OUT} = 1.5V
I_{OUT} = NO LOAD

Short-Circuit Protection, 15A Load



V_{IN} = 12V
V_{OUT} = 1.5V
I_{OUT} = 15A

PIN FUNCTIONS (Recommended to Use Test Points to Monitor Signal Pin Connections.)

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{OUT1} (H1, J1-J2, K1-K2, L1-L2): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. There is a 49.9Ω resistor connected between V_{OUT1} and V_{OUTS1} to protect the output from an open V_{OUTS1}. Review Table 5. See Note 8 in the Electrical Characteristics section for output current guideline.

GND (A3, A6-A7, B3, B6-B7, C3-C7, D6-D7, E6, E8, F5, F7, G6, G8, H6-H7, J4-J7, K3, K6-K7, L3, L6-L7): Power Ground Pins for Both Input and Output Returns.

V_{OUT2} (A1-A2, B1-B2, C1-C2, D1): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. There is a 49.9Ω resistor connected between V_{OUT2} and V_{OUTS2} to protect the output from an open V_{OUTS2}. Review Table 5. See Note 8 in the Electrical Characteristics section for output current guideline.

V_{OUTS1}, V_{OUTS2} (G2, E2): These pins are connected to the top of the internal top feedback resistor for each output. Each pin can be directly connected to its specific output, or connected to the remote sense point of V_{OUT}. It is important to connect these pins to their designated outputs for proper regulation.

In paralleling modules, the V_{OUTS1} pin is left floating, and the V_{FB1} pin is connected to $INTV_{CC}$. This will disable channel 1's error amplifier and internally connect COMP1A to COMP2A. The PGOOD1 and TRACK/SS1 will be disabled in this mode. Channel 2's error amplifier will regulate the two channel single output. See V_{FB} pin description and Applications Information section.

FREQ (F1): Frequency Set Pin. A resistor from this pin to SGND sets the operating frequency. The Equation:

$$\frac{41550}{f(kHz)} - 2.2 = R_{FREQ}(k\Omega)$$

An external clock applied to MODE_PLLIN should be within ±30% of this programmed frequency to ensure frequency lock. See the Applications Information section.

SGND (D3, H3): Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See layout guidelines in Figure 19.

V_{FB1} (G4): This pin is the + input to a unity gain differential amplifier. This pin is connected to V_{OUTS1} with a 60.4k precision resistor internal. Different output voltages can be programmed with an additional resistor between V_{FB1} and V_{OUTS1}^- pins. The differential amplifier is feeding back the divided down output voltage from a remote sense divider network to compare to the internal 0.6V reference. In 2-phase single output operation, tie the V_{FB1} pin to $INTV_{CC}$. See Figure 1 and Applications Information section for details.

V_{FB2} (E4): This pin is the + input to a non-inverting gain of two amplifier utilizing three resistors in the feedback network to develop a remote sense divider network. This pin is connected to V_{OUTS2} with an internal 60.4k precision resistor. The V_{OUT2} voltage is divided down to 0.3V then gained back up to 0.6V to compare with the internal 0.6V reference. This technique provides for equivalent remote sensing on V_{OUT2}. See Figure 1 and Applications Information section for details.

TRACK/SS1,TRACK/SS2 (H4, F2): Output Voltage Tracking Pin and Soft-Start Inputs. Each channel has a 1.0µA pull-up current source. Each pin can be programmed with a soft-start ramp rate up to the 0.6V internal reference level, then beyond this point the internal 0.6V reference will control the feedback loop. When one channel is configured to be master of the two channels, then a capacitor from this pin to ground will set the soft-start ramp rate. The remaining channel can be set up as the slave, and have the master's output applied through a voltage divider to the slave output's track pin. This voltage divider is equal to the slave output's feedback divider for coincidental tracking. See the Applications Information section. (Recommended to use test points to monitor signal pin connections.)

DRV_{CC} (G7): Internal 5.3V regulator output used to source the power MOSFET drivers, and supply power to the $INTV_{CC}$ input. A 4.7µF ceramic capacitor is needed on this pin to GND.

PIN FUNCTIONS (Recommended to Use Test Points to Monitor Signal Pin Connections.)

CPWR (F8): Input Power to the Control IC, and Power to the DRV_{CC} Regulator. This pin is connected to V_{IN} for normal 4.5V to 20V operation. For lower voltage inputs below 4.5V, CPWR can be powered with an external 5V bias. See Application section.

COMP1A, COMP2A (G3, E3): Current Control Threshold. These pins are the output of the error amplifier and the switching regulator's compensation point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V.

COMP1B, COMP2B (G1, E1): Internal Compensation Network .These pins are to be connected to their respected COMPA pins. When Utilizing specific external compensation, then float these pins.

MODE_PLLIN (F3): Operation Mode Selection or External Clock Synchronization Input. When this pin is tied to $INTV_{CC}$, forced continuous mode operation is selected. Tying this pin to SGND allows discontinuous mode operation. When an external clock is applied at this pin, both channels operate in forced continuous mode and synchronize to the external clock. This pin has an internal 600k pull-down resistor to SGND. An external clock applied to MODE_PLLIN should be within ±30% of this programmed frequency to ensure frequency lock.

CLKOUT (F4): Clock output with phase control using the PHASMD pin to enable multiphase operation between devices. Its output level swings between $INTV_{CC}$ and SGND. If clock input is present at the MODE_PLLIN pin, it will be synchronized to the input clock, with phase set by the PHASMD pin. If no clock is present at MODE_PLLIN, its frequency will be set by the FREQ pin. To synchronize other controllers, it can be connected to their MODE_PLLIN pins. See the Applications Information section.

RUN1, RUN2 (H5, D5): Run Control Pins. A voltage above 1.3V will turn on each channel in the module. A voltage below 1.0V on the RUN pin will turn off the related channel. Each RUN pin has a 1.2µA pull-up current, once the RUN pin reaches 1.2V an additional 4.5µA pull-up current is added to this pin. A 100k resistor to ground is internal, and can be used with a pull-up resistor to V_{IN} to turn on the module using the external and internal resistor to program under voltage lockout. Otherwise, an external enable signal or source can drive these pins directly below the 6V max. Enabling either RUN pin will turn on the DRV_{CC}, and turn on the $INTV_{CC}$ path for operation. See Figure 1 and Applications section.

PHASMD (H2): Connect this pin to SGND, $INTV_{CC}$, or floating this pin to select the phase of CLKOUT and channel 2. See Electrical Characteristics table and Application section.

PGOOD1, PGOOD2 (G5, E5): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point. See Applications section.

$INTV_{CC}$ (F6): Supply Input for Internal Circuitry (Not Including Gate Drivers). This bias is derived from DRV_{CC} internally.

$EXTV_{CC}$ (E7): External Power Input. When $EXTV_{CC}$ exceeds the switchover voltage (typically 4.6V), an internal switch connects this pin to DRV_{CC} and shuts down the internal regulator so that $INTV_{CC}$ and gate drivers draw power from $EXTV_{CC}$. The V_{IN} pin still needs to be powered up but draws minimum current.

$TEMP1^+$,$TEMP1^-$ and $TEMP2^+$, $TEMP2^-$ (L8, K8 and B8, A8): Onboard temperature diode for monitoring each channel with differential connections for noise immunity.

V_{IN1} (K4-K5, L4-L5) and V_{IN2} (A4-A5, B4-B5): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUTS1}^- (J3): Differential Output Sense Amplifier (–) Input of channel 1. Connect this pin to the negative terminal of the output load capacitor of V_{OUT1}.

V_{OUTS2}^- (D4): Differential Output Sense Amplifier (–) Input of channel 2. Connect this pin to the negative terminal of the output load capacitor of V_{OUT2}.

SW1 (H8, J8) and SW2 (C8, D8): Switching node of each channel that is used for testing purposes. Also an R-C snubber network can be applied to reduce or eliminate switch node ringing, or otherwise leave floating. See the Applications Information section.

VRNG (D2): Current Limit Adjustment Range. Tying this pin to $INTV_{CC}$ sets full 15A current, or tying to SGND will lower the current limit to 7.5A. Default to $INTV_{CC}$.

BLOCK DIAGRAM

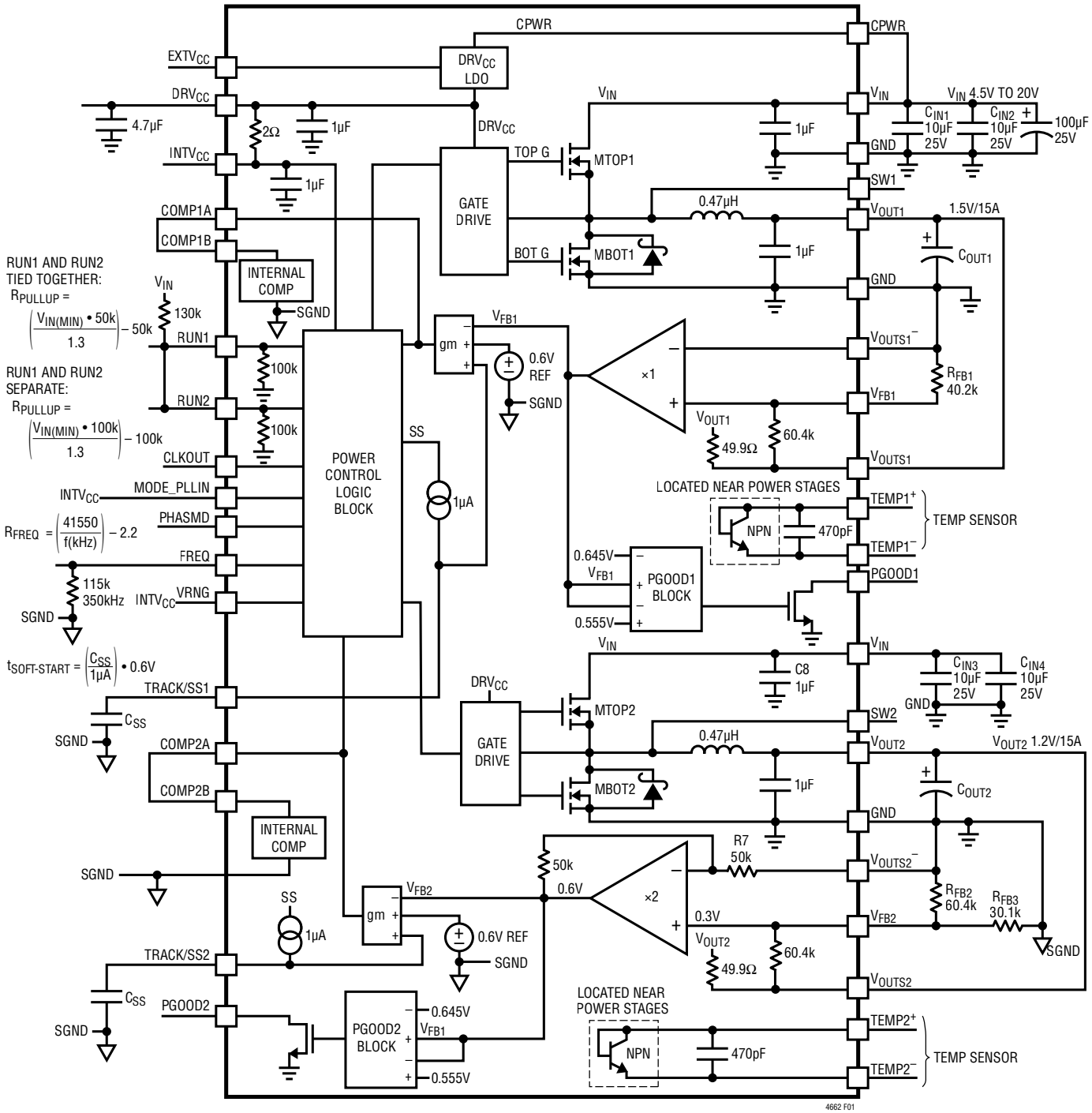


Figure 1. Simplified LTM4662 Block Diagram

DECOUPLING REQUIREMENTS T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN1}, C_{IN2} C_{IN3}, C_{IN4}	External Input Capacitor Requirement (V_{IN} = 4.5V to 20V, V_{OUT1} = 1.5V) (V_{IN} = 4.5V to 20V, V_{OUT2} = 1.5V)	 I_{OUT1} = 15A 10µF ×2 I_{OUT2} = 15A 10µF ×2 (Note 8)			20 20		µF µF
C_{OUT1} C_{OUT2}	External Output Capacitor Requirement (V_{IN} = 4.5V to 20V, V_{OUT1} = 1.5V) (V_{IN} = 4.5V to 20V, V_{OUT2} = 1.5V)	 I_{OUT1} = 15A I_{OUT2} = 15A (Note 8)			400 400		µF µF

OPERATION

Power Module Description

The LTM4662 is a dual-output standalone non-isolated switching mode DC/DC power supply. It can provide two 15A outputs with few external input and output capacitors and setup components. This module provides precisely regulated output voltages programmable via external resistors from $0.6V_{DC}$ to $5.5V_{DC}$ over 4.5V to 20V input voltages. The typical application schematic is shown in Figure 20. See Note 8 in the Electrical Characteristics section for output current guideline.

The LTM4662 has dual integrated controlled-on time current mode regulators and built-in power MOSFET devices with fast switching speed. The controlled on-time, valley current mode control architecture, allows for not only fast response to transients without clock delay, but also constant frequency switching at steady load condition. The typical switching frequency is 400kHz. For switching-noise sensitive applications, it can be externally synchronized from 250kHz to 1000kHz. A resistor can be used to program a free run frequency on the FREQ pin. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4662 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors. Optimized external compensation is supported by disconnecting the internal compensation.

Current mode control provides cycle-by-cycle fast current limit and foldback current limit in an overcurrent condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD outputs low if the output feedback voltage exits a ±7.5% window around the regulation point. As the output voltage exceeds 7.5% above regulation, the bottom MOSFET will turn on to clamp the output voltage. The top MOSFET will be turned off. This overvoltage protect is feedback voltage referred.

Pulling the RUN pins below 1.3V forces the regulators into a shutdown state, by turning off both MOSFETs. The TRACK/SS pins are used for programming the output voltage ramp and voltage tracking during start-up or used for soft-starting the regulator. See the Applications Information section. The LTM4662 is internally compensated to be stable over all operating conditions. Table 5 provides a guideline for input and output capacitances for several operating conditions. The LTpowerCAD® will be provided for transient and stability analysis. The V_{FB1} pin is used to program the channel 1 output voltage with a single external resistor to ground, and V_{FB2} pin requires two resistors to program the output. Both channel 1 and 2 have remote sense capability.

Multiphase operation can be easily employed with the MODE_PLLIN, PHASMD, and CLKOUT pins. Up to 6 phases can be cascaded to run simultaneously with respect to each other by programming the PHASMD pin to different levels. See the Applications Information section.

High efficiency at light loads can be accomplished with selectable pulse-skipping operation using the MODE_PLLIN. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section. Each channel has temperature diode included inside the module to monitor the temperature of the module. See the Applications Information section for details.

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The typical LTM4662 application circuit is shown in Figure 20. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 5 for specific external capacitor requirements for particular applications.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage. Each output of the LTM4662 is capable of a wide duty cycle that is limited by the minimum on-time $t_{ON(MIN)}$ of 30ns defined as $t_{ON(MIN)} < D/f_{SW}$ for narrow duty cycle, where D is duty cycle (V_{OUT}/V_{IN}) and f_{SW} is the switching frequency. The minimum off-time of 90ns $t_{OFF(MIN)} < 1 – D/f_{SW}$ is required for higher duty cycles. See Note 8 in the Electrical Characteristics section for output current guideline.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in Figure 1, a 60.4k internal feedback resistor connects between the V_{OUTS1} to V_{FB1} and V_{OUTS2} to V_{FB2}. It is very important that these pins be connected to their respective outputs for proper feedback regulation. Each channel has a 49.9Ω resistor connected from V_{OUTS1} and V_{OUTS2} to V_{OUT1} and V_{OUT2}, respectively. This is used to protect the output if V_{OUTSn} is open or left unconnected. The V_{OUT1} output voltage will default to 0.6V with no feedback resistor on V_{FB1}. Adding a resistor R_{FB1} from V_{FB1} pin to V_{OUTS1}^- programs the output voltage:

$$V_{OUT1} = 0.6V \bullet \frac{60.4k + R_{FB1}}{R_{FB1}}$$

The V_{OUT2} output voltage will default to 0.3V with no feedback resistor on V_{FB2}. Adding a resistor R_{FB2} from V_{FB2} pin to V_{OUTS2}^-, and the R_{FB3} resistor equal to (60.4k||R_{FB2}) from V_{FB2} to SGND programs the output voltage:

$$V_{OUT2} = 0.6V \bullet \frac{60.4k + R_{FB2}}{R_{FB2}}$$

$$R_{FB3} = 60.4k \,||\, R_{FB2} = \left(\frac{60.4k \bullet R_{FB2}}{60.4k + R_{FB2}} \right)$$

The Thevenin equivalent of the V_{OUT2} equation would be the 0.6V with a series resistance of (60.4k || R_{FB2}), thus R_{FB3} connected to the series resistance would be (60.4k || R_{FB2}) to equal the 0.3V reference.

Table 1. V_{FB1}, V_{FB2}, Resistor Table vs Various Output Voltages

V_{OUT1}	0.6V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5.0V
R_{FB1}	Open	90.9k	60.4k	40.2k	30.1k	19.1k	13.3k	8.25k
V_{OUT2}	0.3V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5.0V
R_{FB2}	Open	90.9k	60.4k	40.2k	30.1k	19.1k	13.3k	8.25k
R_{FB3}	Open	36.5k	30.1k	24.3k	20k	14.7k	11k	7.32k

Figure 2 shows the LTM4662 used in a 2-phase single output: Tie the V_{FB1} pin to $INTV_{CC}$, which will disable channel 1's error amplifier and internally connect COMP2 to COMP1. Tie any of the compensation components to the COMP2 pin. The COMP1 pin can be either left open or shorted to COMP2 externally as shown. The, V_{OUTS1}, TRACK/SS1 and PGOOD1 pins become non-operable and can be left open. To make a single-output converter of three or more phases, additional LTM4662 micro modules can be used. The first module should be tied the same way as the Figure 2. If only one more channel of an additional LTM4662 is needed, use channel 2 for the additional phase:

- Tie the COMP2 pin to the COMP2 pin of the first module.
- Tie the RUN2 pin to the RUN pins of the first module. Use 1/2 the value for R_{FB2} and R_{FB3}.
- Tie V_{OUTS2} of the additional channel to V_{OUTS2} of the first module then to remote sense point.
- Tie the V_{FB2} pin to the V_{FB2} pin of the first module.
- Tie the V_{OUTS2}^- pin to the V_{OUTS2}^- pin of the first module.
- Tie the TRACK/SS2 pin to the TRACK/SS2 pin of the first module.

If both channels are needed for four phases, the additional LTM4662 module should be tied the same way as the first as shown in Figure 2 to disable the second channel 1's EA:

- Tie the V_{FB1} pin to the module's own $INTV_{CC}$.
- Tie the COMP2 pin to the COMP2 pin of the first module.

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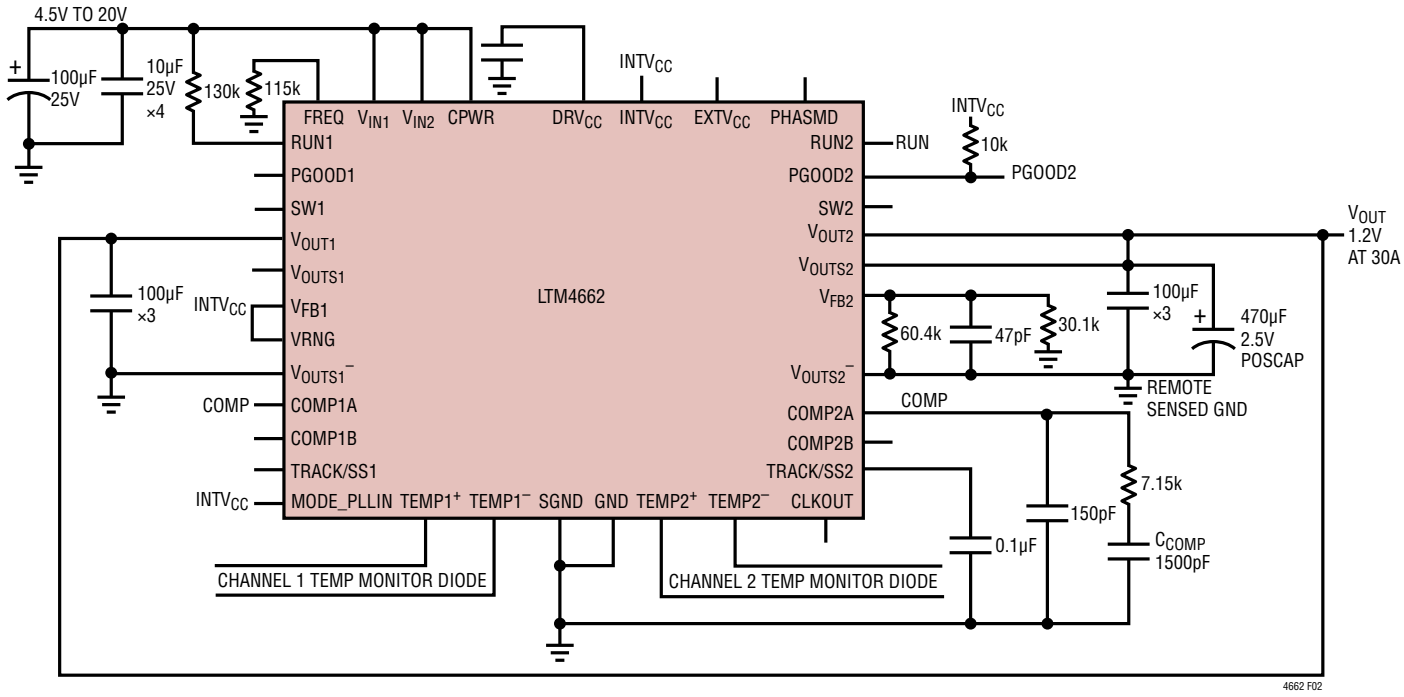

Figure 2. 2-Phase Parallel Configurations

- Tie the RUN pins to the RUN pins of the first module.
- Tie the V_{FB2} pin to the V_{FB2} pin of the first module. Use 1/2 the value for R_{FB2} and R_{FB3}.
- Tie the V_{OUTS2}^- pin to the V_{OUTS2}^- pin of the first module.
- Tie V_{OUTS2} of both modules together then to the remote sense output.
- Tie the TRACK/SS2 pin to the TRACK/SS2 pin of the first module.

See Figure 22 for an example.

Input Capacitors

The LTM4662 module should be connected to a low AC impedance DC source. For the regulator input, four 10µF input ceramic capacitors are used for RMS ripple current. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance.

This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, $\eta\%$ is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated aluminum electrolytic capacitor, polymer capacitor.

The LTM4662 is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, low ESR polymer capacitor or

APPLICATIONS INFORMATION

ceramic capacitor. The typical output capacitance range for each output is from 200µF to 470µF. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 5 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 7.5A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 5 matrix, and LTpowerCAD will be provided for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. LTpowerCAD can calculate the output ripple reduction as the number of implemented phases increases by N times.

Continuous and Discontinuous Mode Operation

If the MODE_PLLIN pin is tied to $INTV_{CC}$ or an external clock is applied to MODE_PLLIN, the LTM4662 will be forced to operate in continuous mode. With load current less than one-half of the full load peak-to-peak ripple, the inductor current valley can drop to zero or become negative. This allows constant-frequency operation but at the cost of low efficiency at light loads.

If the MODE_PLLIN pin is left open or connected to signal ground, the channel will transition into discontinuous mode operation, where a current reversal comparator shuts off the bottom MOSFET as the inductor current approaches zero, thus preventing negative inductor current and improving light-load efficiency. In this mode, both switches can remain off for extended periods of time. As the output capacitor discharges by load current and the output voltage droops lower, EA will eventually move the ITH voltage above the zero current level (0.8V) to initiate another switching cycle.

Multiphase Operation

For output loads that demand more than 15A of current, two outputs in LTM4662 or even multiple LTM4662s can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripple. The MODE_PLLIN pin allows the LTM4662 to synchronize to an external clock (between 250kHz and 1000kHz) and the internal phase-locked loop allows the LTM4662 to lock onto an incoming clock phase as well. The CLKOUT signal can be connected to the MODE_PLLIN pin of the following stage to line up both the frequency and the phase of the entire system. Tying the PHASMD pin to $INTV_{CC}$, SGND, or floating the pin will select V_{OUT2} and CLKOUT phases relative to V_{OUT1}.

Up to of 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHASMD pin of each LTM4662 channel to different levels. Figure 3 shows a 2-phase design, 4-phase design and a 6-phase design example for clock phasing with the PHASMD table.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage).

The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design. The LTM4662 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Figure 21 shows an example of parallel operation and pin connection.

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 4 shows this graph.

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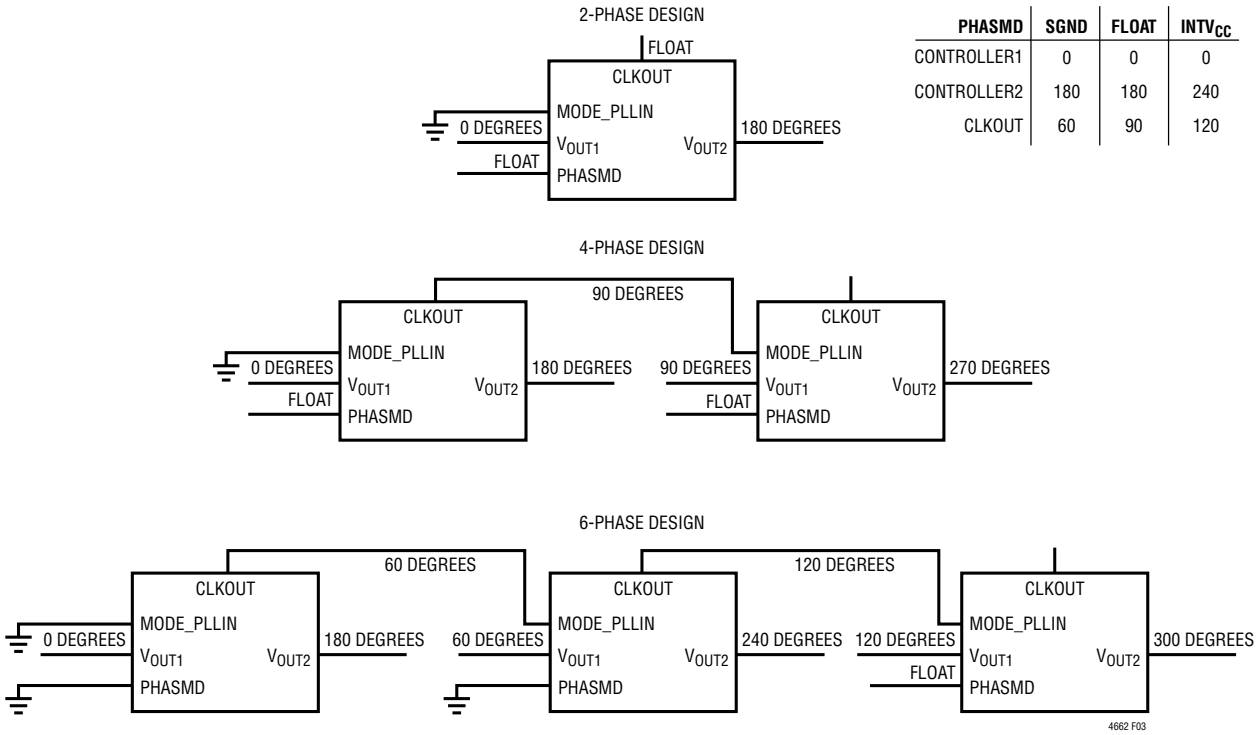

PHASMD	SGND	FLOAT	$INTV_{CC}$
CONTROLLER1	0	0	0
CONTROLLER2	180	180	240
CLKOUT	60	90	120

Figure 3. Examples of 2-Phase, 4-Phase, and 6-Phase Operation with PHASMD Table

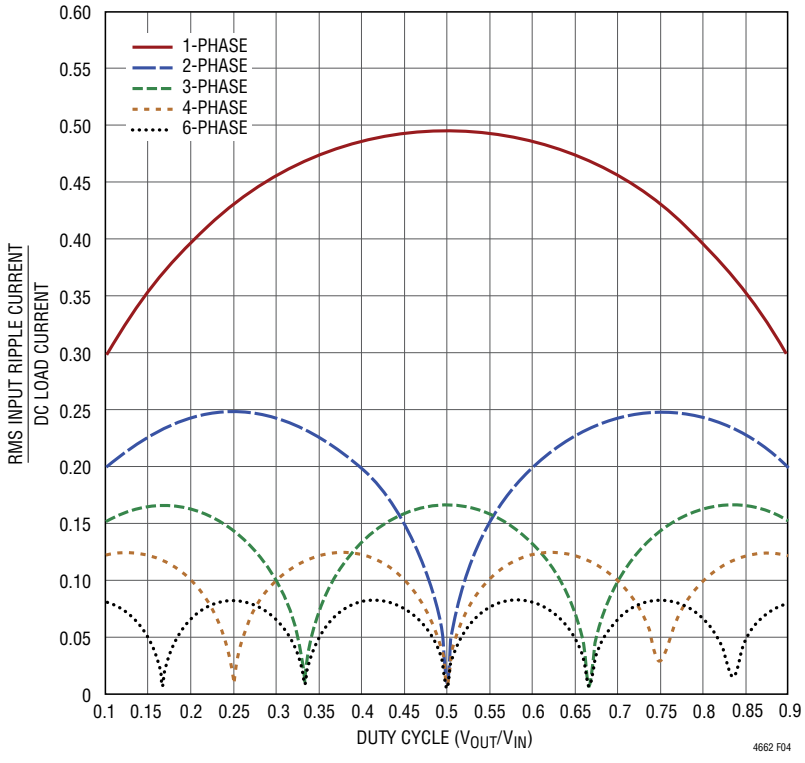

Figure 4. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

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Frequency Selection and Phase-Locked Loop (MODE_PLLIN and f_{SET} Pins)

The LTM4662 device is operated over a range of frequencies to improve power conversion efficiency . It is recommended to operate the lower output voltages or lower duty cycle conversions at lower frequencies to improve efficiency by lowering power MOSFET switching losses. Higher output voltages or higher duty cycle conversions can be operated at higher frequencies to limit inductor ripple current. The efficiency graphs will show an operating frequency chosen for that condition An internal oscillator (clock generator) provides phase interleaved internal clock signals for individual channels to lock up to. The switching frequency and phase of each switching channel is independently controlled by adjusting the top MOSFET turn-on time (on-time) through the one-shot timer. This is achieved by sensing the phase relationship between a top MOSFET turn-on signal and its internal reference clock through a phase detector, and the time interval of the one-shot timer is adjusted on a cycle-by-cycle basis, so that the rising edge of the top MOSFET turn-on is always trying to synchronize to the internal reference clock signal for the respective channel.

The frequency of the internal oscillator can be programmed from 250kHz to 1MHz by connecting a resistor, R_T , from the FREQ pin to signal ground (SGND). The FREQ pin is regulated to 1.2V internally. The value of this resistor can be chosen according to the formula:

$$R_T(k\Omega) = \frac{41550}{f(kHz)} - 2.2$$

For applications with stringent frequency or interference requirements, an external clock source connected to the MODE_PLLIN pin can be used to synchronize the internal clock signals through a clock phase-locked loop (Clock PLL). The LTM4662 operates in forced continuous mode of operation when it is synchronized to the external clock. The external clock frequency has to be within ±30% of the internal oscillator frequency for successful synchronization.

The clock input levels should be no less than 2V for “high” and no greater than 0.5V for “low”. The MODE_PLLIN pin has an internal 600k pull-down resistor.

During dynamic transient conditions either in the line voltage or load current (e.g., load step or release), the top switch will turn on more or less frequently in response to achieve faster transient response. This is the benefit of the LTM4662’s controlled on-time, valley current mode architecture. However, this process may understandably lose phase and even frequency lock momentarily. For relatively slow changes, phase and frequency lock can still be maintained. For large load current steps with fast slew rates, phase lock will be lost until the system returns back to a steady-state condition . It may take up to several hundred microseconds to fully resume the phase lock, but the frequency lock generally recovers quickly, long before phase lock does.

Minimum On-Time and Minimum Off-Time

Minimum on-time t_{ON} is the smallest time duration that the LTM4662 is capable of turning on the top MOSFET on either channel. It is determined by internal timing delays, and the gate charge required to turn on the top MOSFET. The LTM4662 has a minimum on time of ~30ns, and far lower than what would be a concern based on the maximum operating frequency of 1MHz .

The below equation can be checked against the V_{IN} , V_{OUT}, and (FREQ) frequency of operation to insure the minimum on time $t_{ON(MIN)}$ is above 30ns.

$$\frac{V_{OUT}}{V_{IN} \bullet FREQ} > t_{ON(MIN)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple will increase. The on-time can be increased by lowering the switching frequency. The below equation can be checked against the V_{IN} , V_{OUT}, and (FREQ) frequency of operation to insure the minimum off time $t_{OFF(MIN)}$ is above 90ns.

$$\frac{V_{OUT(MAX)}}{V_{IN(MAX)}} = D_{MAX} \qquad D_{MAX} = 1 - FREQ \bullet t_{OFF(MIN)}$$

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Output Voltage Soft Starting and Tracking

Output voltage tracking can be programmed externally using the TRACK/SS pins. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider for to implement coincident tracking. The LTM4662 uses an accurate 60.4k resistor internally for the top feedback resistor for each channel. Figure 5 shows an example of coincident tracking.

$$SLAVE = \left(1 + \frac{60.4k}{R_{TB}}\right) \bullet V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's track pin. V_{TRACK} has a control range of 0V to 0.6V, or the internal reference voltage. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point. Voltage tracking is disabled when $V_{TRACK/SS}$ is more than 0.6V. R_{TB} in Figure 5 will be equal to the R_{FB} for coincident tracking. Figure 6 shows the coincident tracking waveforms.

The TRACK/SS pins can be controlled by a capacitor placed on the regulator TRACK/SS pin to ground. A 1.0µA current source will charge the TRACK/SS pin up to the voltage reference and then proceed up to $INTV_{CC}$. After the 0.6V ramp, the TRACK/SS pin will no longer be in control, and the internal voltage reference will control output regulation from the feedback divider. Foldback current limit is disabled during this sequence of turn-on during tracking or soft-starting. The TRACK/SS pins are pulled low when the RUN pin is below 1.2V. The total soft-start time can be calculated as:

$$t_{SOFT\text{-}START} = \left(\frac{C_{SS}}{1.0\mu A}\right) \bullet 0.6V$$

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's TRACK/SS pin. As mentioned above, the TRACK/SS pin has a control range from 0 to 0.6V. The master's TRACK/SS pin slew rate is directly equal to the master's output slew rate in Volts/second. The equation:

$$\frac{MR}{SR} \bullet 60.4k = R_{TA}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/second. When coincident tracking is desired, then MR and SR are equal, thus R_{TA} is equal the 60.4k. R_{TB} is derived from equation:

$$R_{TB} = \frac{0.6V}{\frac{V_{FB}}{60.4k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_{TA}}}$$

where V_{FB} is the feedback voltage reference of the regulator, and $V_{TRACK/SS}$ is 0.6V. Since R_{TA} is equal to the 60.4k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R_{TB} is equal to R_{FB} with $V_{FB} = V_{TRACK/SS}$. In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R_{TB} can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach its final value before the master output For example, MR = 20V/s, and SR = 15V/s. Then R_{TA} = 80.6k. Solve for R_{TB} to equal to 80.6k.

Each of the TRACK/SS pins will have a 1.0µA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK/SS pin input. Smaller values resistors with the same ratios as the resistor value calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK/SS pin offset to a negligible value.

Power Good

Each PGOOD pin is connected to an internal open-drain N-channel MOSFET. An external resistor or current source can be used to pull this pin up to 6V (e.g., $V_{OUT1,2}$ or DRV_{CC}). Overvoltage or undervoltage comparators (OV, UV) turn on the MOSFET and pull the PGOOD pin low when the feedback voltage is outside the ±7.5% window of the reference voltage. The PGOOD pin is also pulled low when the channel's RUN pin is below the 1.2V threshold

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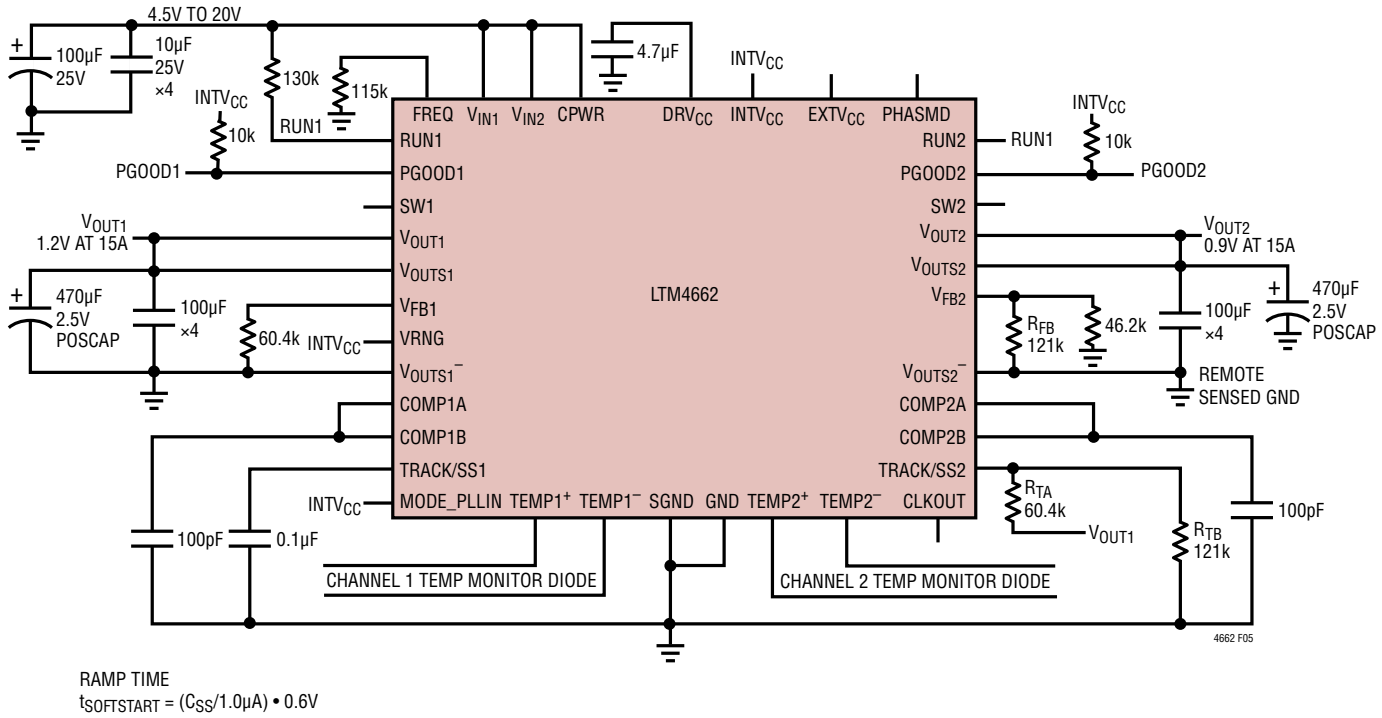

Figure 5. Example of Output Tracking Application Circuit

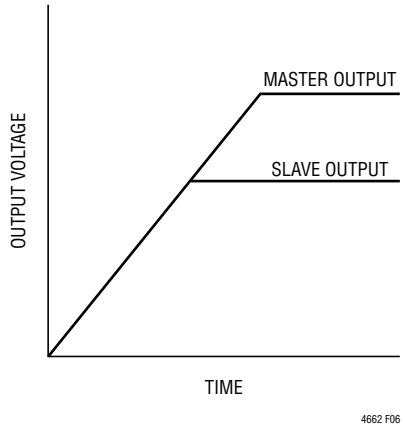

Figure 6. Output Coincident Tracking Waveform

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(hysteresis applies), or in undervoltage lockout (UVLO). In an overvoltage (OV) condition, MT is turned off and MB is turned on immediately without delay and held on until the overvoltage condition clears. This happens regardless of any other condition as long as the RUN pin is enabled. For example, upon enabling the RUN1 pin, if V_{OUT} is prebiased at more than 7.5% above the programmed regulated voltage, the OV stays triggered and BG forced on until V_{OUT} is pulled a ~2.5% hysteresis below the 7.5% OV threshold.

Stability Compensation

The module has already been internally compensated for all output voltages. Table 5 is provided for most application requirements. LTpowerCAD will be provided for other control loop optimization. Use LTpowerCAD when tying output in parallel for higher current. External compensation may be necessary.

Run Enable

The RUN pins have an enable threshold of 1.3V maximum, typically 1.2V with 160mV of hysteresis. They control the turn on each of the channels and DRV_{CC} and $INTV_{CC}$. A 100k resistor to ground is internal, and can be used with a pull-up resistor to V_{IN} to turn on the module using the external and internal resistor to program under voltage lock out. Otherwise an external enable signal or source can drive these pins directly below the 6V max. The RUN pins can also be used for output voltage sequencing. In parallel operation the RUN pins can be tie together and controlled from a single control. See the Typical Application circuits in Figure 23.

DRV_{CC}, $INTV_{CC}$, and $EXTV_{CC}$

The LTM4662 module has an internal 5.3V low dropout regulator (DRV_{CC}) that is derived from the input voltage through the CPWR (control power) pin. This regulator is used to power the $INTV_{CC}$ control circuitry and the power MOSFET drivers. This regulator can source up to 100mA, and typically uses ~50mA for powering the device at the maximum frequency. This internal 5.3V supply is enabled by either RUN1 or RUN2.

$EXTV_{CC}$ allows an external 5V supply to power the LTM4662 and reduce power dissipation from the internal low dropout 5V regulator. The power loss savings can be calculated by:

$$(CPWR - 5V) \bullet 50mA = P_{LOSS}$$

$EXTV_{CC}$ has a threshold of 4.7V for activation, and a maximum rating of 6V. When using a 5V input, connect this 5V input to $EXTV_{CC}$ also to maintain a 5V gate drive level. $EXTV_{CC}$ must sequence on after CPWR, and $EXTV_{CC}$ must sequence off before CPWR.

CPWR (Control Power)

The LTM4662 module has a CPWR pin that is biased with a supply voltage minimum of 4.5V, and up to V_{IN} maximum in normal operation. When operating at lower input voltages below the 4.5V minimum, this pin can biased with an alternate source to power the controller section while operating down to the 2.375V minimum.

For example, if 3.3V is supplied to V_{IN}, and a 5V bias with a 50mA capability was used to source the CPWR pin, then 3.3V input power conversion can be implemented. Even though the CPWR can operate from 4.5V to 20V, a lower bias will lower the power loss if the module. See Figure 23 for an example.

Output Remote Sense

The LTM4662's differential output sensing schemes are distinct from conventional schemes where the regulated output and its ground reference are directly sensed with a difference amplifier whose output is then divided down with an external resistor divider and fed into the error amplifier input. This conventional scheme is limited by the common mode input range of the difference amplifier and typically limits differential sensing to the lower range of output voltages.

The LTM4662 allows for seamless differential output sensing by sensing the resistively divided feedback voltage differentially. This allows for differential sensing in the full output range from 0.6V to 5.5V. Channel 1's difference amplifier (DIFFAMP) has a bandwidth of around 8MHz, and channel 2's feedback amplifier has a bandwidth of around 4MHz, both high enough so as to not affect main loop compensation and transient behavior.

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The LTM4662 differential output sensing can correct for up to ±300mV of common-mode deviation in the output's power and ground lines on channel 1, and ±200mV on channel 2.

To avoid noise coupling into the feedback voltages, the resistor dividers should be placed close to the V_{OUTS1} and V_{OUTS1}^-, or V_{OUTS2} and V_{OUTS2}^- pins. Remote output and ground traces should be routed together as a differential pair to the remote output. For best accuracy, these traces to the remote output and ground should be connected as close as possible to the desired regulation point. Review the parallel schematics in Figure 22.

OUTPUT CURRENT RANGE PIN (VRNG)

Tying the VRNG pin to SGND will set the output current to 7.5A, and ~10A current limit. Tying the VRNG pin to $INTV_{CC}$ will set the output current to 15A, and ~20A current limit.

SW Pins

The SW pins are generally for testing purposes by monitoring these pins. These pins can also be used to dampen out switch node ringing caused by LC parasitic in the switched current paths. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing.

If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance. First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated:

$$Z(L) = 2\pi fL$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by: $Z(C) = 1/(2\pi fC)$. These values are a good place to start with. Modification to these components should be made to attenuate the ringing with the least amount of power loss.

Temperature Monitoring (TEMP1 and TEMP2)

A diode connected NPN transistor is used for temperature monitoring. Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage and temperature described by the classic diode equation:

$$I_D = I_S \bullet e\left(\frac{V_D}{\eta \bullet V_T}\right)$$

or

$$V_D = \eta \bullet V_T \bullet \ln\frac{I_D}{I_S}$$

where I_D is the diode current, V_D is the diode voltage, η is the ideality factor (typically close to 1.0) and I_S (saturation current) is a process dependent parameter. V_T can be broken out to:

$$V_T = \frac{k \bullet T}{q}$$

where T is the diode junction temperature in Kelvin, q is the electron charge and k is Boltzmann's constant. V_T is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The I_S term in the equation above is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The I_S term varies from process to process, varies with temperature, and by definition must always be less than I_D. Combining all of the constants into one term:

$$K_D = \frac{\eta \bullet k}{q}$$

where K_D = 8.62 – 5, and knowing $\ln(I_D/I_S)$ is always positive because I_D is always greater than I_S, leaves us with the equation that:

$$V_D = T(KELVIN) \bullet K_D \bullet \ln\frac{I_D}{I_S}$$

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where V_D appears to increase with temperature. It is common knowledge that a silicon diode biased with a current source has an approximate –2mV/°C temperature relationship (Figure 7), which is at odds with the equation term, increases with temperature, reducing the $\ln(I_D/I_S)$ absolute value yielding an approximate –2mV/°C composite diode voltage slope.

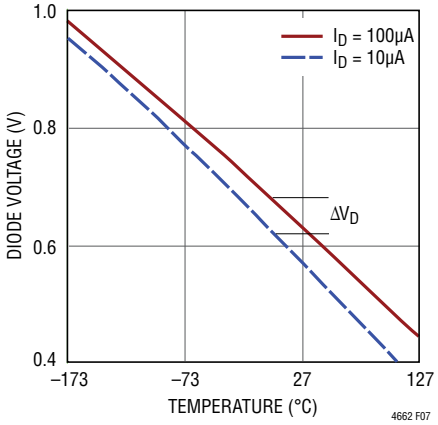

Figure 7. Diode Voltage V_D vs Temperature T(°C) for Different Bias Currents

To obtain a linear voltage proportional to temperature, we cancel the I_S variable in the natural logarithm term to remove the I_S dependency from the following equation. This is accomplished by measuring the diode voltage at two currents I_1, and I_2, where $I_1 = 10 \bullet I_2$.

Subtracting we get:

$$\Delta V_D = T(KELVIN) \bullet K_D \bullet \ln\frac{I_1}{I_S} - T(KELVIN) \bullet K_D \bullet \ln\frac{I_2}{I_S}$$

Combining like terms, then simplifying the natural log terms yields:

$$\Delta V_D = T(KELVIN) \bullet K_D \bullet \ln(10)$$

and redefining constant

$$K'_D = K_D \bullet \ln(10) = 198\mu V/k$$

yields

$$\Delta V_D = K'_D \bullet T(KELVIN)$$

Solving for temperature:

$$T(KELVIN) = \frac{\Delta V_D}{K'_D},$$

$$T(KELVIN) = [°C] + 273.15,$$

$$[°C] = T(KELVIN) - 273.15$$

means that if we take the difference in voltage across the diode measured at two currents with a ratio of 10, the resulting voltage is 198µV per Kelvin of the junction with a zero intercept at 0 Kelvin. The diode connected NPN transistor at the TEMP+, TEMP– pins can be used to monitor the internal temperature of the LTM4662. A general temperature monitor can be implemented by connecting a resistor between TEMP+ and V_{IN} to set the current to 100µA, grounding the TEMP– pin and then monitoring the diode voltage drop with temperature. A more accurate temperature monitor can be achieved with a circuit injecting two currents that are at a 10:1 ratio. See LTC®2997 data sheet.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule® package mounted to a hardware test board.

The motivation for providing these thermal coefficients is found in JESD51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”). Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application. The

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Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a 95mm × 76mm PCB with four layers.

2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package.

A graphical representation of the aforementioned thermal resistances is given in Figure 8; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

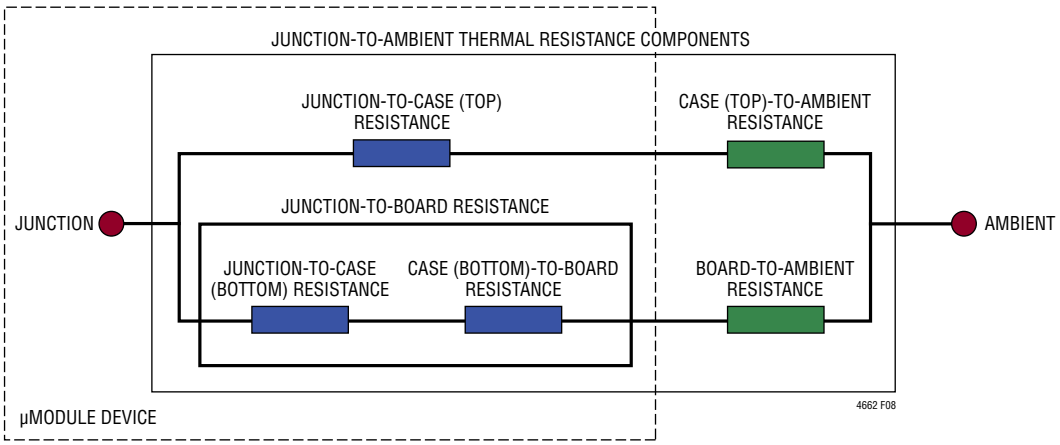

Figure 8. Graphical Representation of JESD51-12 Thermal Coefficients

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Within the LTM4662, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4662 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4662 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory tests have been performed, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the LTM4662 model with no airflow or heat sinking in a define chamber. This θ_{JB} + θ_{BA} value should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink. Each system has its own thermal characteristics, therefore thermal analysis must be performed by the user in a particular system. The LTM4662 has been designed to effectively remove heat from both the top and bottom of the package. The bottom substrate material has very low thermal resistance to the printed circuit board. An external heat sink can be applied to the top of the device for excellent heat sinking with airflow . Basically all power dissipating devices are mounted directly to the substrate and the top exposed metal. This provides two low thermal resistance paths to remove heat.

Figure 9 shows a temperature plot of the LTM4662 with 400LFM airflow. Figure 10 shows a temperature plot of the LTM4662 with 400LFM airflow. These plots equate to a paralleled 1V at 30A and 5V at 22A design operating at 87% and 95% efficiency.

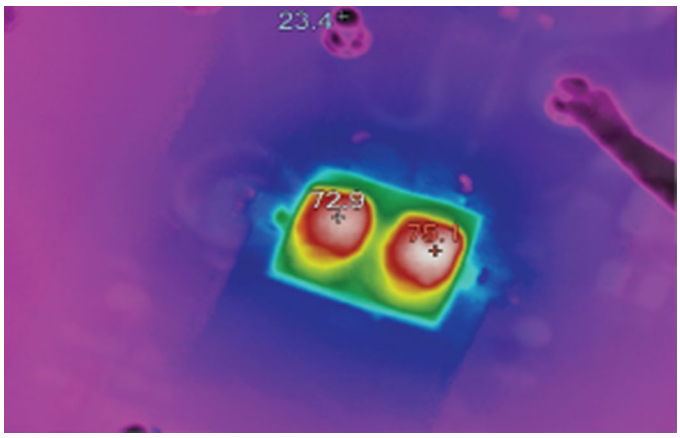

Figure 9. LTM4662 12V to 1V at 30A with 400LFM, 30°C Ambient, 30W

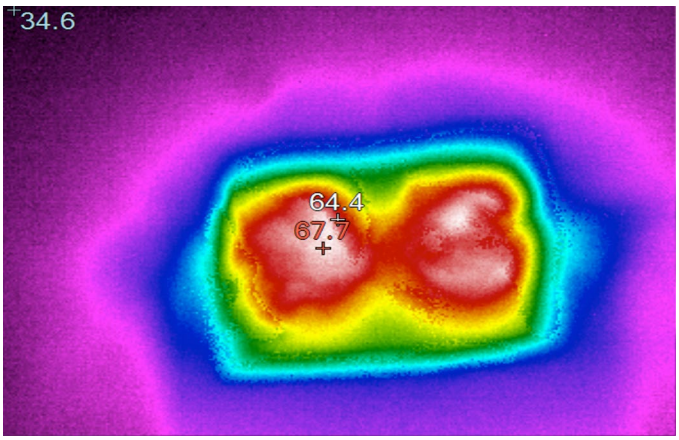

Figure 10. LTM4662 12V to 5V at 22A with 400LFM, 30°C Ambient, 110W

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Power Derating

The 5V, 8V and 12V power loss curves in Figures 11 through 13 can be used in coordination with the load current derating curves in Figures 14 to 18 for calculating an approximate θ_{JA} thermal resistance for the LTM4662 with airflow conditions. The power loss curves are taken at room temperature, and are increased with a 1.35 to 1.4 multiplicative factor at 125°C. These factors come from the fact that the power loss of the regulator increases about 45% from 25°C to 150°C, thus a 50% spread over 125°C delta equates to ~0.35%/°C loss increase. A 125°C maximum junction minus 25°C room temperature equates to a 100°C increase. This 100°C increase multiplied by 0.35%/°C equals a 35% power loss increase at the 125°C junction, thus the 1.35 multiplier.

The derating curves are plotted with V_{OUT1} and V_{OUT2} in parallel single output operation starting at 30A of load with low ambient temperature. The output voltages are 1V, 2.5V and 5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis.

The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at ~120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased.

The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much temperature rise can be allowed. As an example in Figure 14, the load current is derated to ~22.5A at ~80°C with no air or heat sink and the power loss for the 12V to 1.0V at 22.5A output is a ~4.05W loss. The 4.05W loss is calculated with the ~3.0W room temperature loss from the 12V to 1.0V power loss curve at 22.5A, and the 1.35 multiplying factor at 125°C ambient. If the 80°C ambient temperature is subtracted from the 125°C junction temperature, then the difference of 45°C divided by 4.05W equals a 11°C/W θ_{JA} thermal resistance. Table 2 specifies a 11°C/W value which is pretty close. The airflow graphs are more accurate due to the fact that the ambient temperature environment is controlled better with airflow. As an example in Figure 15, the load current is derated to ~24A at ~88°C with 200LFM of airflow and the power loss for the 12V to 1.0V at 24A output is a ~4.35W loss.

The 4.35W loss is calculated with the ~3.2W room temperature loss from the 12V to 1.0V power loss curve at 24A, and the 1.35 multiplying factor at 125°C ambient. If the 88°C ambient temperature is subtracted from the 125°C junction temperature, then the difference of 37°C divided by 4.35W equals a 8.5°C/W θ_{JA} thermal resistance. Table 2 specifies a 8.5°C/W value which is pretty close. Table 2 through Table 4 provide equivalent thermal resistances for 2.5V and 5V outputs with and without airflow and heat sinking.

The derived thermal resistances in Table 2 through Table 4 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the power loss curves and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers.

Safety Considerations

The LTM4662 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage, thus the internal bottom MOSFET will turn on indefinitely trying to protect the load. Under this fault condition, the input voltage will source very large currents to ground through the failed internal top MOSFET and enabled

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Table 2. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	BGA θ_{JA} (°C/W)
Figures 14, 15	5, 12	Figure 11, 13	0	None	11
Figures 14, 15	5, 12	Figure 11, 13	200	None	8.5
Figures 14, 15	5, 12	Figure 11, 13	400	None	8

Table 3. 2.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	LGA θ_{JA} (°C/W)	BGA θ_{JA} (°C/W)
Figures 16, 17	5, 12	Figure 11, 13	0	None	6.5 to 7	11
Figures 16, 17	5, 12	Figure 11, 13	200	None	5.5 to 6	8,5
Figures 16, 17	5, 12	Figure 11, 13	400	None	4.5	8

Table 4. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	BGA θ_{JA} (°C/W)
Figures 18	12	Figure 13	0	None	11
Figures 18	12	Figure 13	200	None	8,5
Figures 18	12	Figure 13	400	None	8

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Aavid Thermalloy	375424B00034G	www.aavid.com
Cool Innovations	4-050503P to 4-050508P	www.coolinnovations.com

Table 5. Capacitor Matrix (All Parameters Are Typical and Dependent on Board Layout)

VENDORS	VALUE	PART NUMBER	VENDORS	VALUE	PART NUMBER
Taiyo Yuden	22µF, 25V	C3216X7S0J226M	Panasonic SP	470µF, 2.5V	EEFGX0E471R
Murata	22µF, 25V	GRM31CR61C226KE15L	Panasonic POSCAP	470µF, 2.5V	2R5TPD470M5
Murata	100µF, 6.3V	GRM32ER60J107M	Panasonic POSCAP	470µF, 6.3V	6TPD470M
AVX	100µF, 6.3V	18126D107MAT	Panasonic	100µF, 20V	20SEP100M

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)**	C_{OUT1} (CERAMIC)	C_{OUT2} (CERAMIC/BULK)	C_{FF} (pF)	C_{COMP} (pF)	V_{IN} (V)	DROOP (mV)	P-P DEVIATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)	FREQ (kHz)
0.9	22µF ×4	100µF	100µF ×4	470µF ×2		100	5,12	39	78	30	7.5	350
1	22µF ×4	100µF	100µF ×4	470µF ×2		100	5,12	39	78	30	7.5	350
1.2	22µF ×4	100µF	100µF ×4	470µF ×2		100	5,12	44	88	30	7.5	350
1.5	22µF ×4	100µF	100µF ×3	None	47	100	5,12	65	130	25	7.5	450
1.8	22µF ×4	100µF	100µF ×3	None	47	100	5,12	65	130	25	7.5	500
2.5	22µF ×4	100µF	100µF ×2	None	47	100	5,12	80	160	25	7.5	650
3.3	22µF ×4	100µF	100µF ×1	None	47	100	5,12	100	200	20	5	750
5	22µF ×4	100µF	100µF ×1	None	47	100	5,12	100	280	20	5	950

**Bulk capacitance is optional if V_{IN} has very low input impedance.

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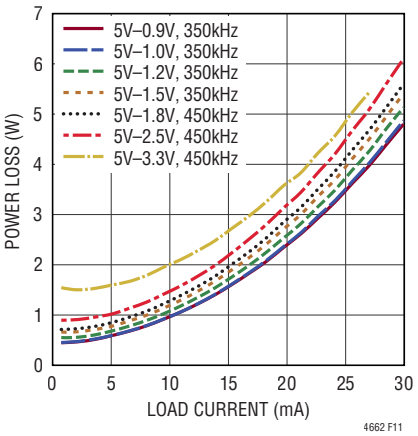


Figure 11. $5V_{IN}$ Power Loss Curve

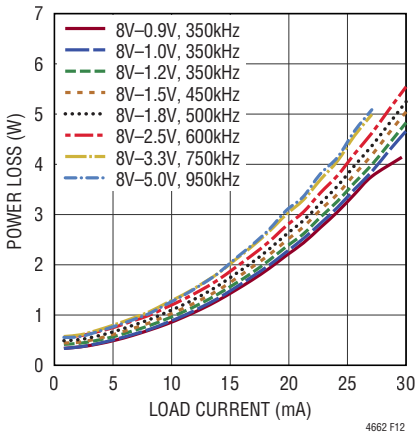


Figure 12. $8V_{IN}$ Power Loss Curve

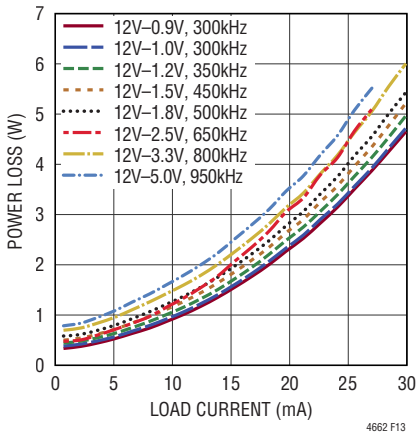


Figure 13. $12V_{IN}$ Power Loss Curve

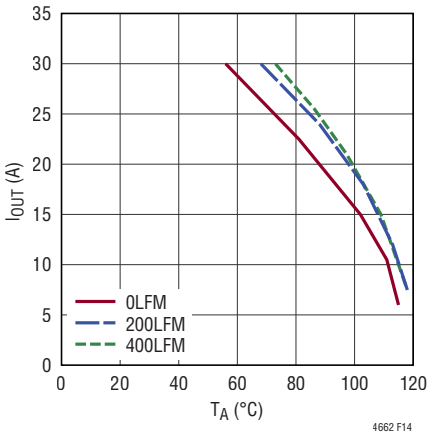


Figure 14. 5V to 1V Derating Curve, No Heat Sink

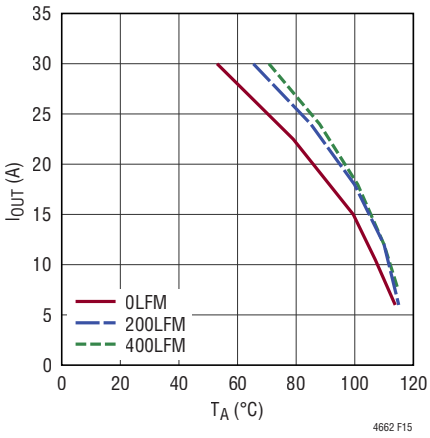


Figure 15. 12V to 1V Derating Curve, No Heat Sink

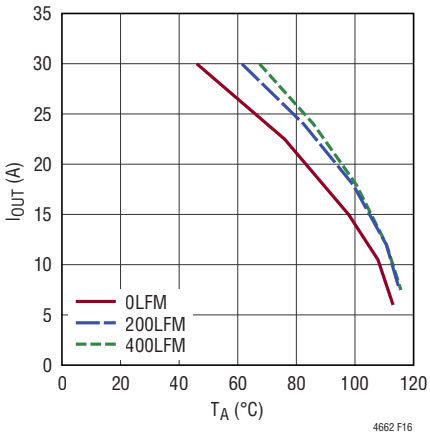


Figure 16. 5V to 2.5V Derating Curve, No Heat Sink

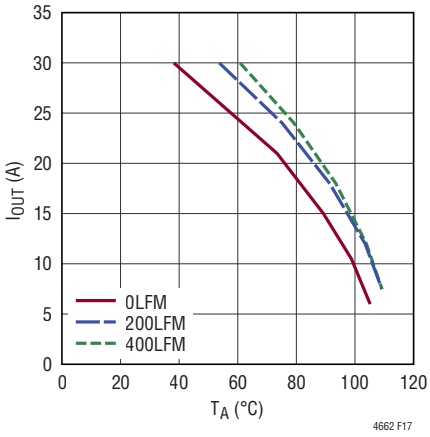


Figure 17. 12V to 2.5V Derating Curve, No Heat Sink

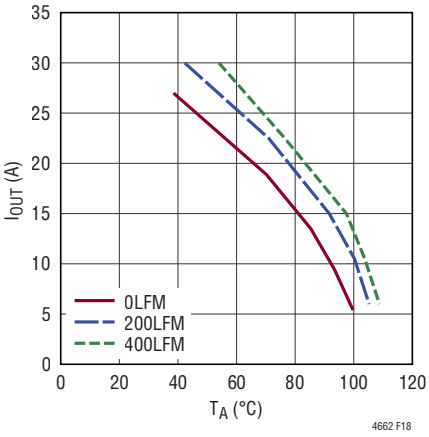


Figure 18. 12V to 5V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation.

The device does support over current protection. Temperature diodes are provided for monitoring internal temperature, and can be used to detect the need for thermal shutdown that can be done by controlling the RUN pin.

Layout Checklist/Example

The high integration of LTM4662 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pads, unless they are capped or plated over.

Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.

- For parallel modules, tie the V_{OUT}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK/SS pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figures 19a and 19b give a good example of the recommended layout.

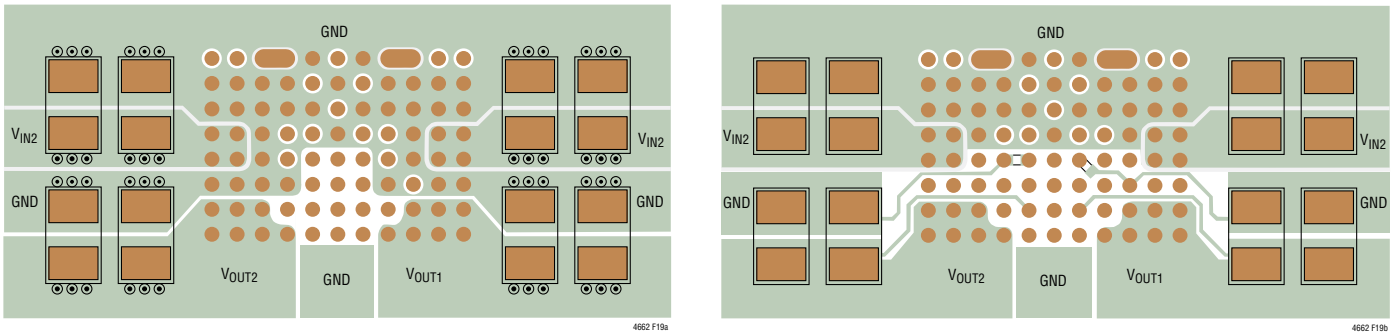


Figure 19. Recommended PCB Layout

TYPICAL APPLICATIONS

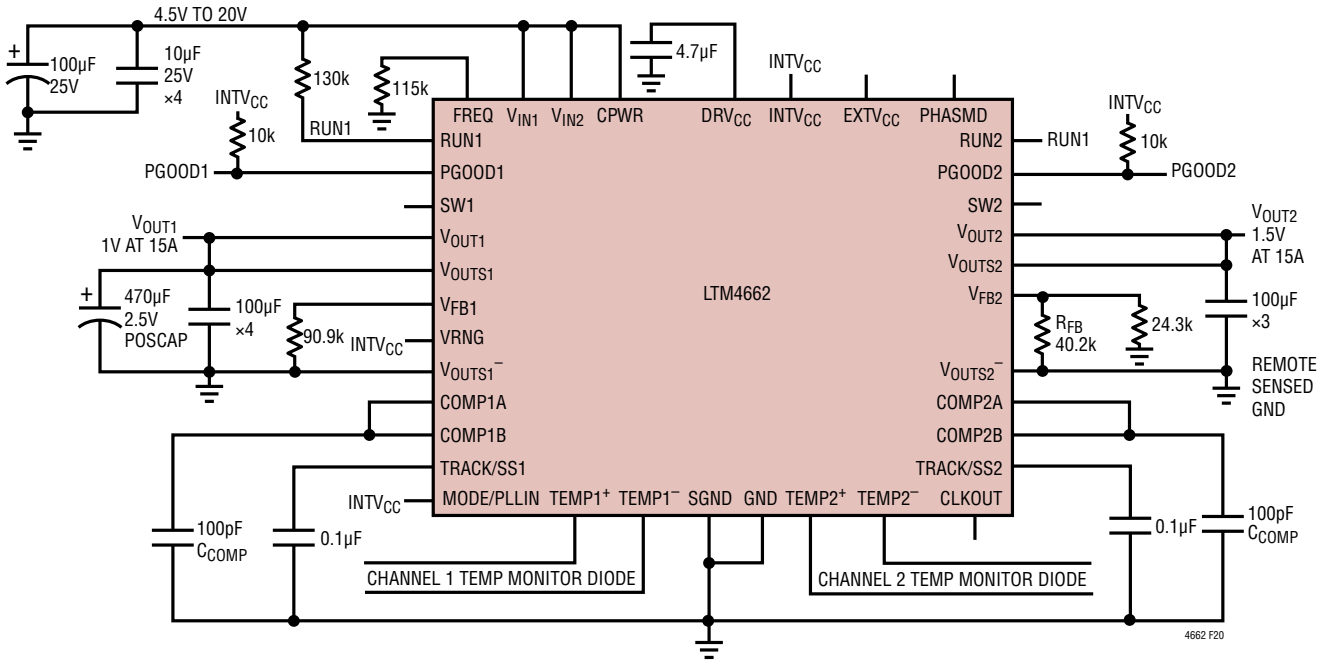


Figure 20. 4.5V to 20V Input to 1.0V and 1.5V at 15A Each

TYPICAL APPLICATIONS

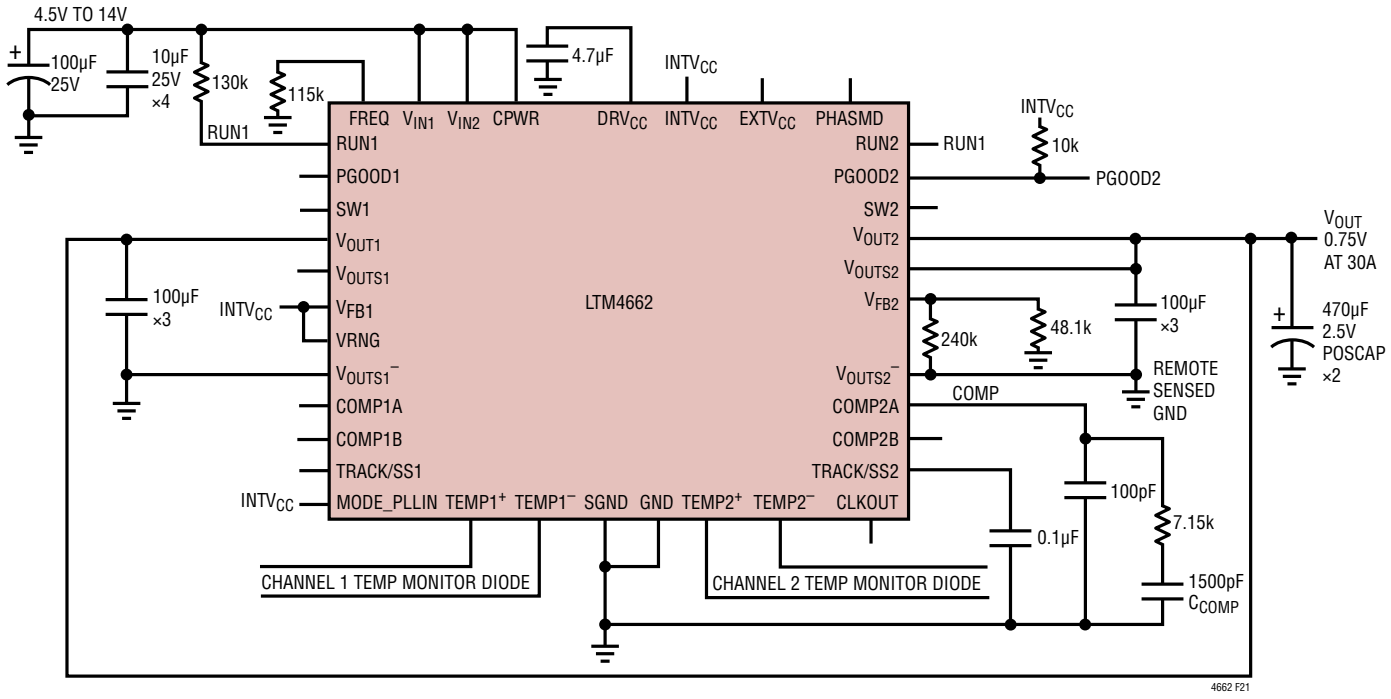


Figure 21. 12V Input to 0.75V at 30A Two Phase

TYPICAL APPLICATIONS

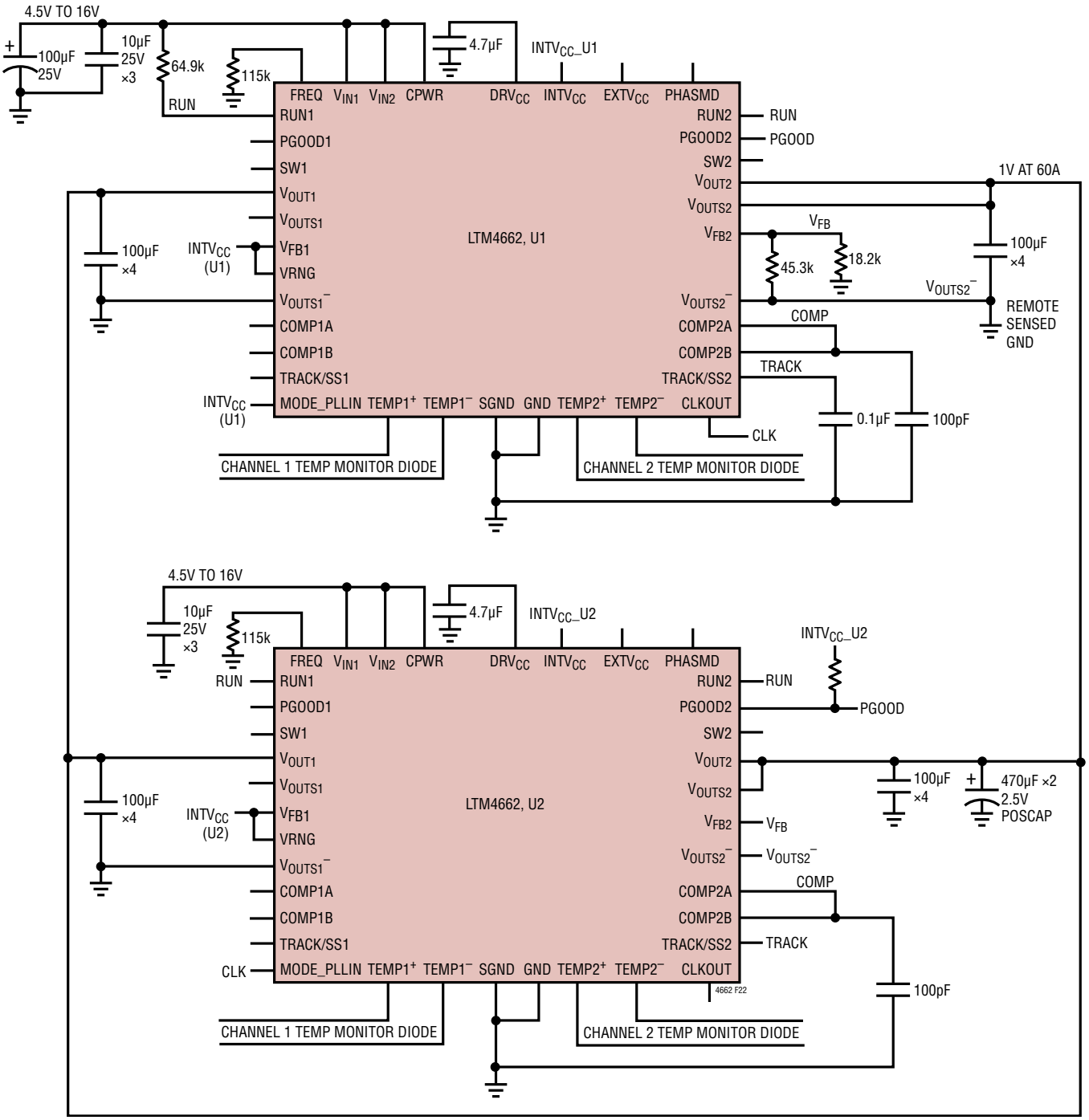


Figure 22. Four Phase Design 1V at 60A

TYPICAL APPLICATIONS

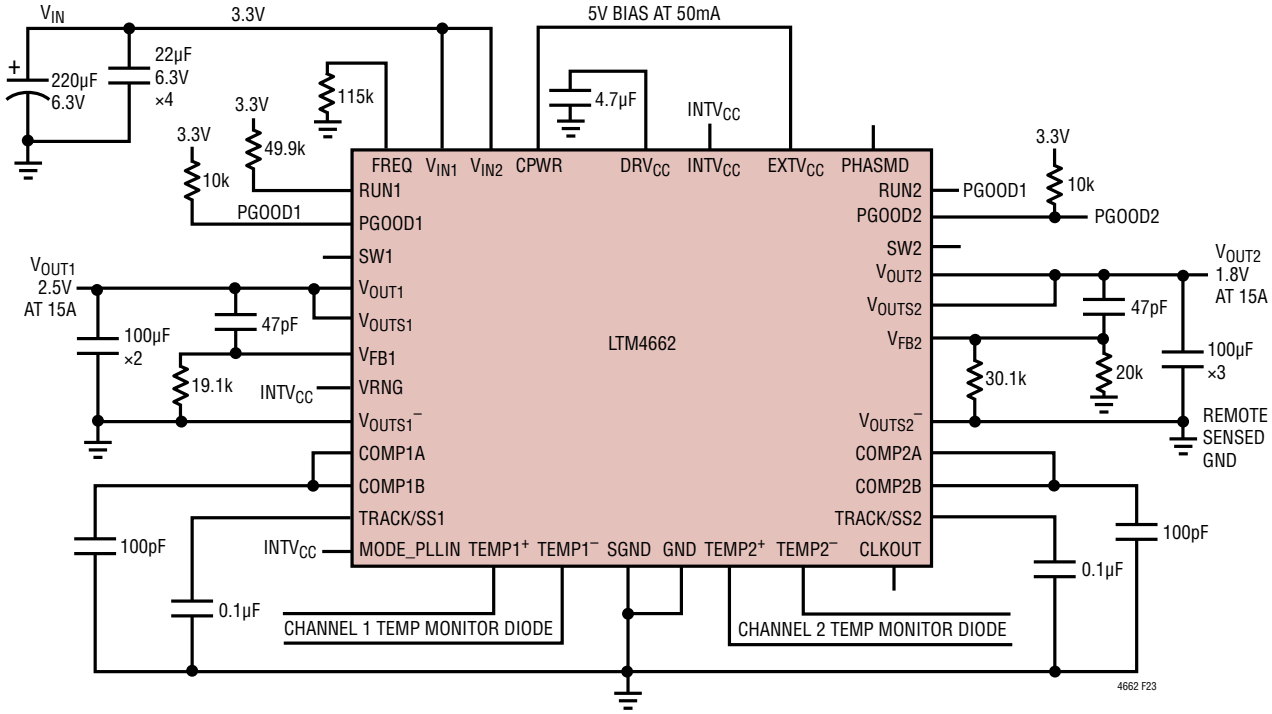


Figure 23. 3.3V to 1.8V, and 2.5V at 15A each with PGOOD Power Up Sequencing

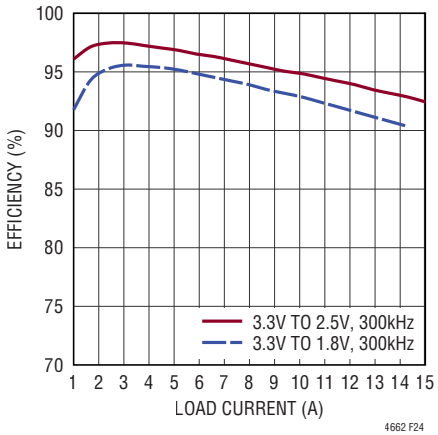


Figure 24. Efficiency, 3.3V_{IN}

TYPICAL APPLICATIONS

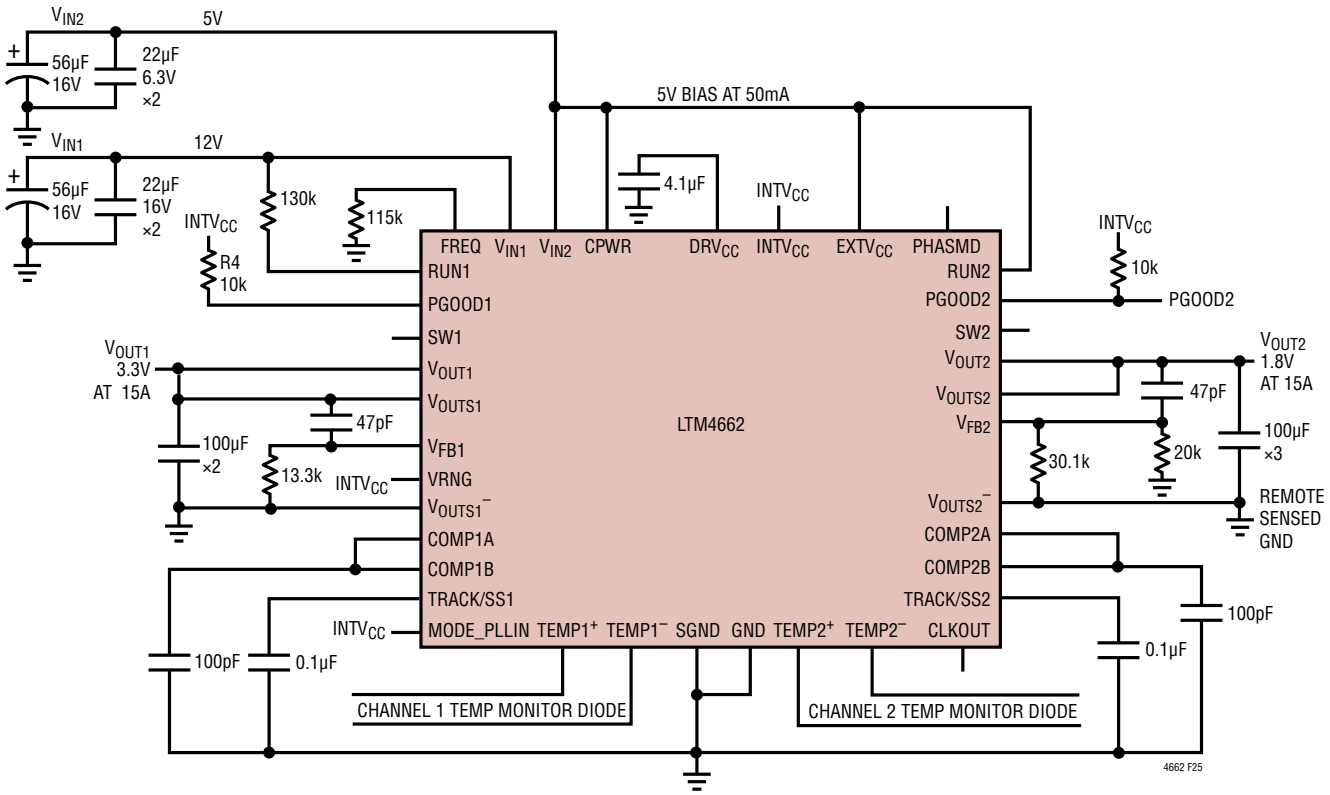


Figure 25. 12V to 3.3V at 15A, 5V to 1.8V at 15A

PACKAGE DESCRIPTION

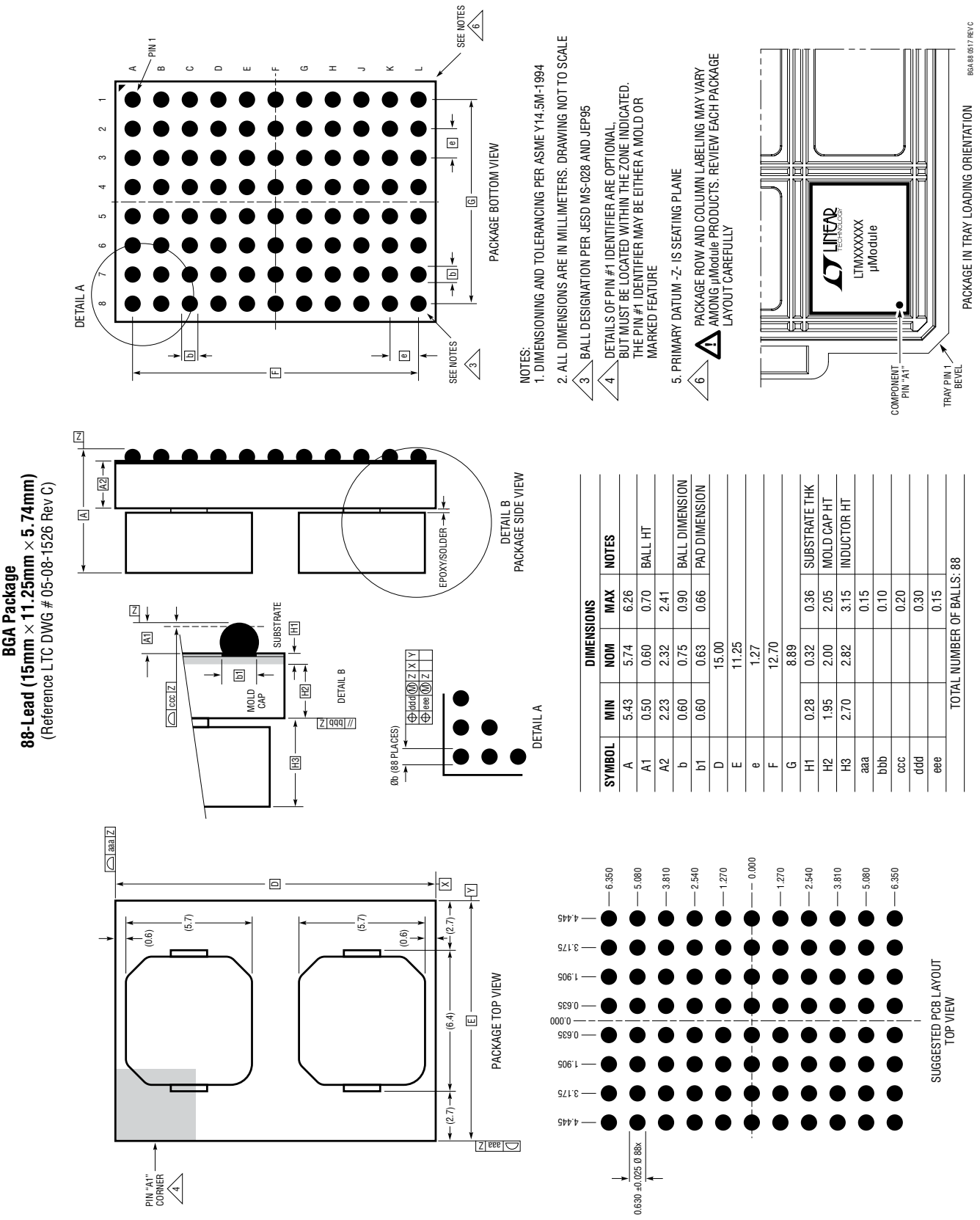
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

LTM4662 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT2}	B1	V_{OUT2}	C1	V_{OUT2}	D1	V_{OUT2}	E1	COMP2B	F1	FREQ
A2	V_{OUT2}	B2	V_{OUT2}	C2	V_{OUT2}	D2	VRNG	E2	V_{OUTS2}	F2	TRACK/SS2
A3	GND	B3	GND	C3	GND	D3	SGND	E3	COMP2A	F3	MODE_PLLIN
A4	V_{IN2}	B4	V_{IN2}	C4	GND	D4	V_{OUTS2}^-	E4	V_{FB2}	F4	CLKOUT
A5	V_{IN2}	B5	V_{IN2}	C5	GND	D5	RUN2	E5	PGOOD2	F5	GND
A6	GND	B6	GND	C6	GND	D6	GND	E6	GND	F6	$INTV_{CC}$
A7	GND	B7	GND	C7	GND	D7	GND	E7	$EXTV_{CC}$	F7	GND
A8	$TEMP2^-$	B8	$TEMP2^+$	C8	SW2	D8	SW2	E8	GND	F8	CPWR

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION		
G1	COMP1B	H1	V_{OUT1}	J1	V_{OUT1}	K1	V_{OUT1}	L1	V_{OUT1}		
G2	V_{OUTS1}	H2	PHASMD	J2	V_{OUT1}	K2	V_{OUT1}	L2	V_{OUT1}		
G3	COMP1A	H3	SGND	J3	V_{OUTS1}^-	K3	GND	L3	GND		
G4	V_{FB1}	H4	TRACK/SS1	J4	GND	K4	V_{IN1}	L4	V_{IN1}		
G5	PGOOD1	H5	RUN1	J5	GND	K5	V_{IN1}	L5	V_{IN1}		
G6	GND	H6	GND	J6	GND	K6	GND	L6	GND		
G7	DRV_{CC}	H7	GND	J7	GND	K7	GND	L7	GND		
G8	GND	H8	SW1	J8	SW1	K8	$TEMP1^-$	L8	$TEMP1^+$		

PACKAGE DESCRIPTION



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	5.43	5.74	6.26	
A1	0.50	0.60	0.70	BALL HT
A2	2.23	2.32	2.41	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		15.00		
E		11.25		
e		1.27		
F		12.70		
G		8.89		
H1	0.28	0.32	0.36	SUBSTRATE THK
H2	1.95	2.00	2.05	MOLD CAP HT
H3	2.70	2.82	3.15	INDUCTOR HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 88				

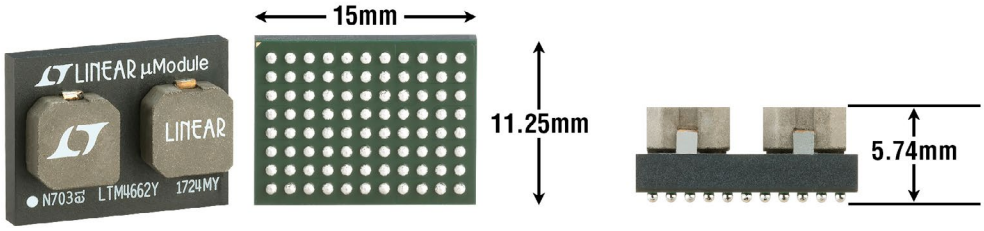
Rev. B

REVISION HISTORY

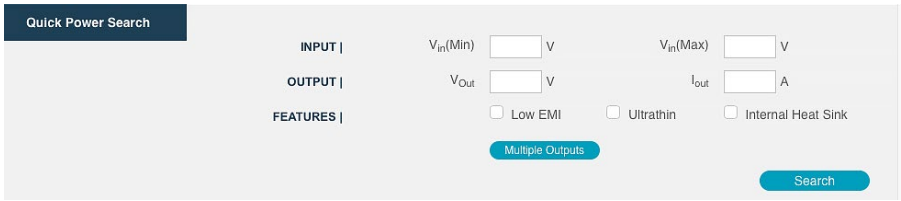
REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/18	Changed Absolute Maximum voltage of V_{FBI} from "–0.3V to 2.7V" to "–0.3V to ($INTV_{CC}$ to 0.3V)."	2
		Changed R_{FBHI1}, R_{FBHI2} from 60.5 (min) and 60.75 (max) to 59.9 (min) and 60.9 (max).	4
		Corrected run enable hysteresis from 100mV to 160mV.	19
B	09/21	Added MP-grade option to the Ordering Information table.	2

PACKAGE PHOTO

BGA



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4646	Pin-Compatible, Lower Current version of the LTM4662	Dual 10A, Single 20A Step-Down µModule Regulator 4.5V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V. 11.25mm × 15mm × 5.01mm BGA
LTM4628	Dual 8A or Single 16A Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 26.5V, 0.6V ≤ V_{OUT} ≤ 5.5V. 15mm × 15mm × 4.32mm LGA 15mm × 15mm × 4.92mm BGA
LTM4620A	Dual 13A or Single 26A Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 5.3V, 15mm × 15mm × 4.41mm LGA, 15mm × 15mm × 5.01mm BGA
LTM4630A	Dual 18A or Single 36A Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 5.3V. 16mm × 16mm × 4.41mm LGA, 16mm × 16mm × 5.01mm BGA
LTM4644	Quad 4A Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 14V, 0.6V ≤ V_{OUT} ≤ 5.5V. 9mm × 15mm × 5.01mm BGA
LTM4637	Single 20A Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V. 15mm × 15mm × 4.32mm LGA, 15mm × 15mm × 4.92mm BGA
LTM4645	Single 25A Step-Down µModule Regulator	4.7V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 1.8V. 9mm × 15mm × 3.51mm BGA
LTM4647	Single 30A Step-Down µModule Regulator	4.7V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 1.8V. 9mm × 15mm × 5.01mm BGA
LTM4636	Single 40A Step-Down µModule Regulator	4.7V V_{IN} 15V, 0.6V ≤ V_{OUT} ≤ 3.3V. 16mm × 16mm × 7.07mm BGA.