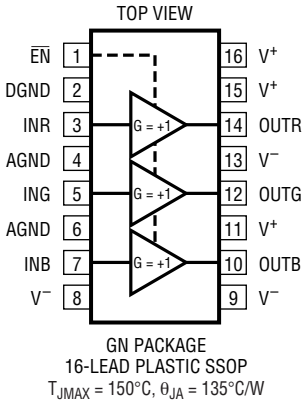
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 13.2V
Input Current (Note 2) ..... ±10mA
Output Current (Continuous) ..... ±70mA
$\overline{EN}$ to DGND Voltage (Note 2) 5.5V
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) ... –40°C to 85°C
Specified Temperature Range (Note 5) .... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 135°C/W

ORDER PART NUMBER
LT6554CGN LT6554IGN
GN PART MARKING
6554 6554I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, R_L = 1k, C_L = 1.5pF, $V_{\overline{EN}}$ = 0.4V, V_{AGND}, V_{DGND} = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Offset Voltage	V_{IN} = 0V, V_{OS} = V_{OUT}	 ●		11	±35 ±70	mV mV
I_{IN}	Input Current		●		–17	±50	µA
e_n	Output Noise Voltage	f = 100kHz			20		nV√Hz
i_n	Input Noise Current	f = 100kHz			3.5		pA√Hz
R_{IN}	Input Resistance	V_{IN} = ±1V	●	150	400		kΩ
C_{IN}	Input Capacitance	f = 100kHz			1		pF
PSRR	Power Supply Rejection Ratio	V_S (Total) = 4.5V to 12V (Note 6)	●	51	65		dB
I_{PSRR}	Input Current Power Supply Rejection	V_S (Total) = 4.5V to 12V (Note 6)	●		1	±5	µA/V
A_V ERR	Gain Error	V_{OUT} = ±2V	●	–2.5	–0.6	0	%
A_V MATCH	Gain Matching	Any One Channel to Another			±0.03		%
V_{OUT}	Maximum Output Voltage Swing		●	±3.75	±3.85		V
I_S	Supply Current, Per Amplifier	R_L = ∞ R_L = ∞	 ●		8	10 13	mA mA
	Supply Current, Disabled, Total	$V_{\overline{EN}}$ = 4V $V_{\overline{EN}}$ = Open	● ●		22 0.5	100 100	µA µA
$I_{\overline{EN}}$	Enable Pin Current	$V_{\overline{EN}}$ = 0.4V $V_{\overline{EN}}$ = V^+	● ●	–200	–95 0.5	 50	µA µA
I_{SC}	Output Short-Circuit Current	R_L = 0Ω, V_{IN} = ±2V	●	±50	±105		mA
SR	Slew Rate	4V_{P-P} Output Step (Note 9)		1700	2500		V/µs
–3dB BW	Small Signal –3dB Bandwidth	V_{OUT} = 200mV_{P-P}			650		MHz
0.1dB BW	Gain Flatness ±0.1dB Bandwidth	V_{OUT} = 200mV_{P-P}			100		MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V, R_L = 1k, C_L = 1.5pF, $V_{\overline{EN}}$ = 0.4V, V_{AGND}, V_{DGND} = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LSBW	Large Signal Bandwidth	V_{OUT} = $2V_{P-P}$ (Note 7) V_{OUT} = $4V_{P-P}$ (Note 7)		270	400 200		MHz MHz
	All-Hostile Crosstalk	f = 10MHz, V_{OUT} = $2V_{P-P}$ f = 100MHz, V_{OUT} = $2V_{P-P}$			–90 –60		dB dB
t_S	Settling Time	0.1% of V_{FINAL}, V_{STEP} = 2V			6		ns
t_R, t_F	Small-Signal Rise and Fall Time	10% to 90%, V_{OUT} = $200mV_{P-P}$			550		ps
dG	Differential Gain	(Note 8)			0.022		%
dP	Differential Phase	(Note 8)			0.006		Deg
HD2	2nd Harmonic Distortion	f = 10MHz, V_{OUT} = $2V_{P-P}$			–82		dBc
HD3	3rd Harmonic Distortion	f = 10MHz, V_{OUT} = $2V_{P-P}$			–96		dBc

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: This parameter is guaranteed to meet specified performance through design and characterization. It is not production tested.

Note 3: As long as output current and junction temperature are kept below the Absolute Maximum Ratings, no damage to the part will occur. Depending on the supply voltage, a heat sink may be required.

Note 4: The LT6554C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 5: The LT6554C is guaranteed to meet specified performance from 0°C to 70°C. The LT6554C is designed, characterized and expected to meet specified performance from –40°C and 85°C but is not tested or QA sampled at these temperatures. The LT6554I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: The two supply voltage settings for power supply rejection are shifted from the typical $\pm V_S$ points for ease of testing. The first measurement is taken at V^+ = 3V, V^- = –1.5V to provide the required 3V headroom for the enable circuitry to function with $\overline{EN}$, DGND, AGND and all inputs connected to 0V. The second measurement is taken at V^+ = 8V, V^- = –4V.

Note 7: Large signal bandwidth is calculated from the slew rate:

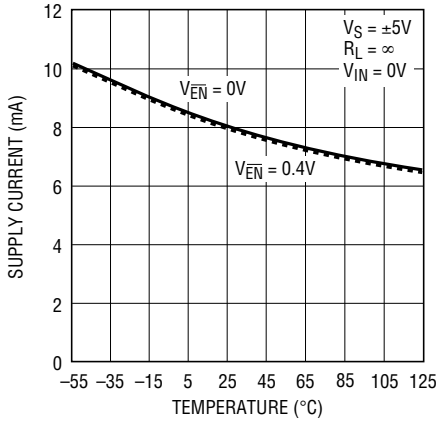
$$LSBW = SR/(\pi \bullet V_{P-P})$$

Note 8: Differential gain and phase are measured using a Tektronix TSG120YC/NTSC signal generator and a Tektronix 1780R video measurement set. The resolution of this equipment is better than 0.05% and 0.05°. Nine identical amplifier stages were cascaded giving an effective resolution of better than 0.0056% and 0.0056°.

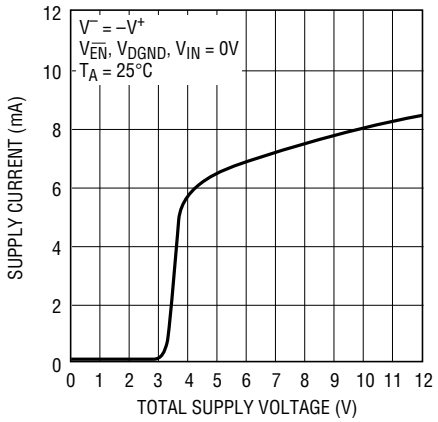
Note 9: Slew rate is 100% production tested on the G channel. Slew rate of the R and B channels is guaranteed through design and characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

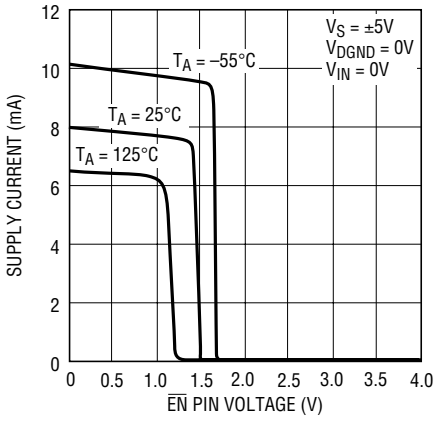
Supply Current per Amplifier vs Temperature



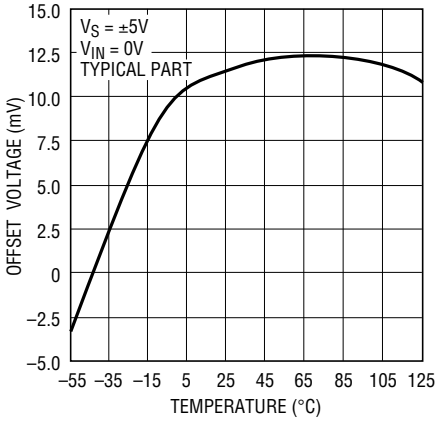
Supply Current per Amplifier vs Supply Voltage



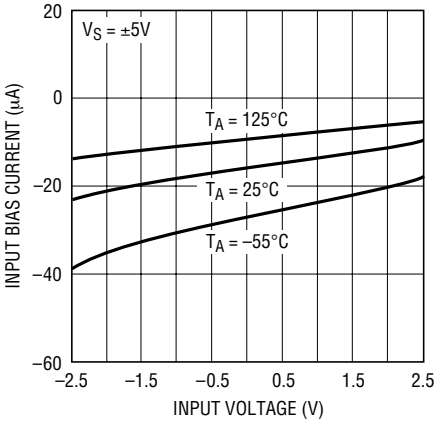
Supply Current per Amplifier vs EN Pin Voltage



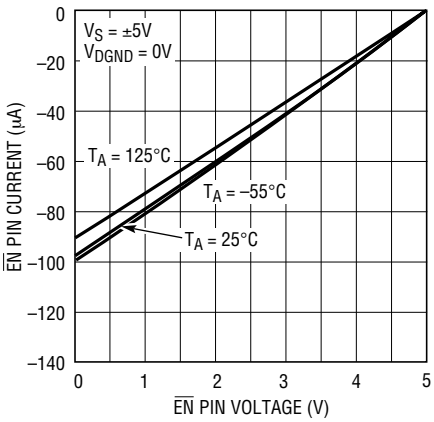
Offset Voltage vs Temperature



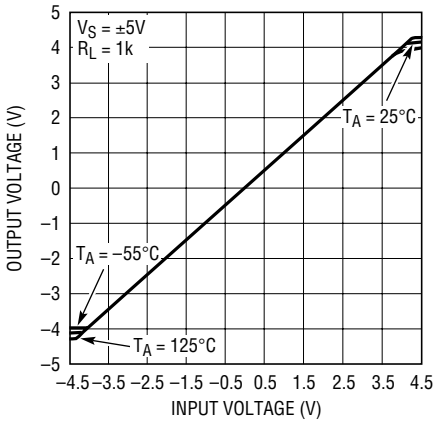
Input Bias Current vs Input Voltage



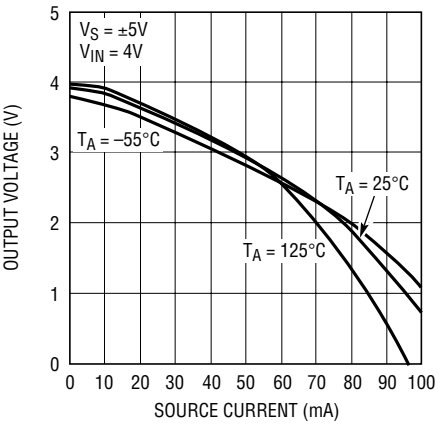
EN Pin Current vs EN Pin Voltage



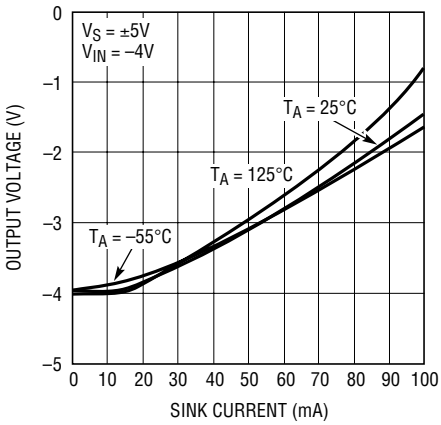
Output Voltage vs Input Voltage



Output Voltage Swing vs I_{LOAD} (Output High)

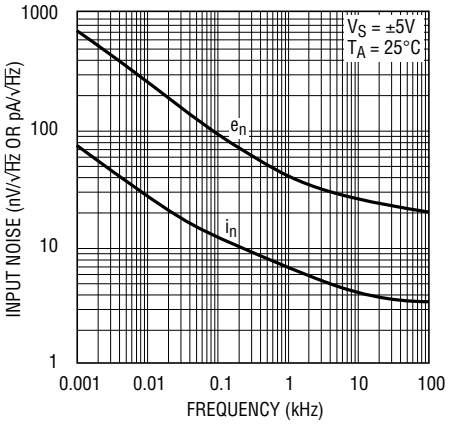


Output Voltage Swing vs I_{LOAD} (Output Low)

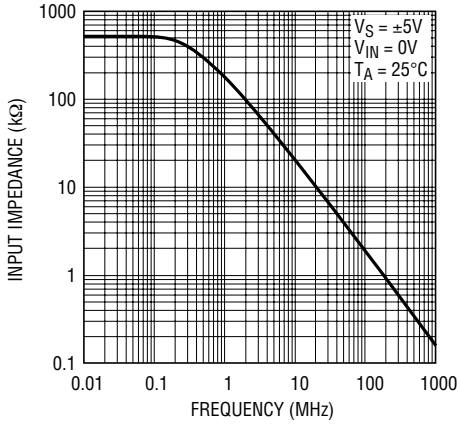


TYPICAL PERFORMANCE CHARACTERISTICS

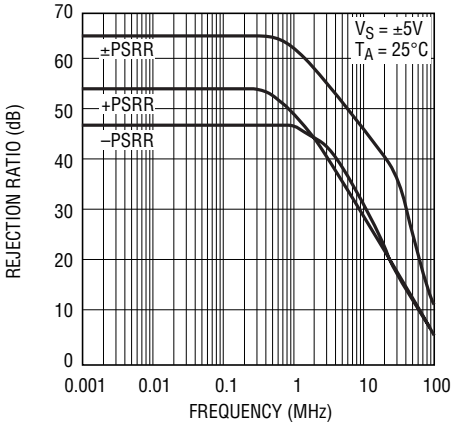
Input Noise Spectral Density



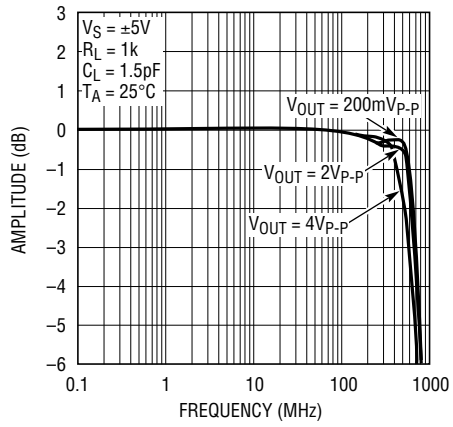
Input Impedance vs Frequency



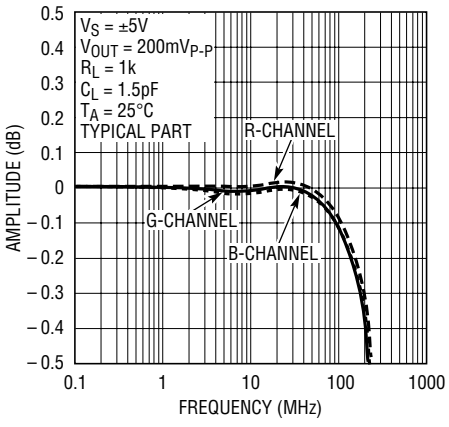
PSRR vs Frequency



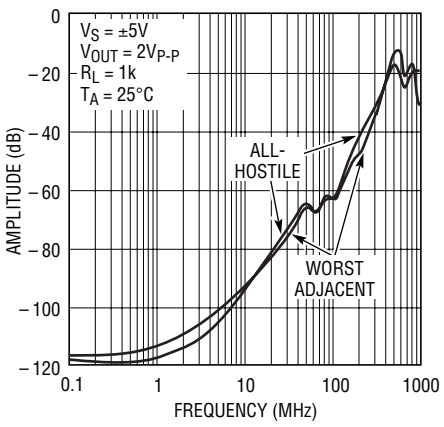
Frequency Response



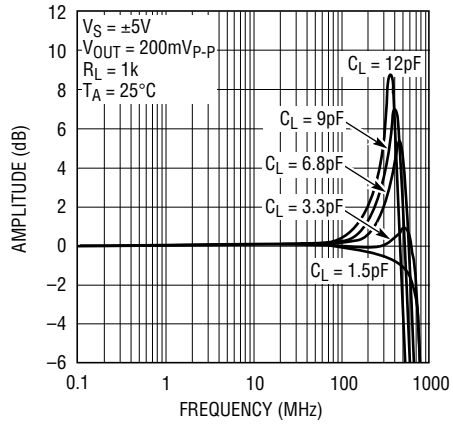
Gain Flatness vs Frequency



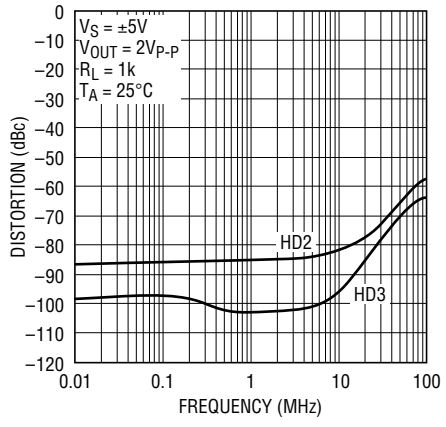
Crosstalk vs Frequency



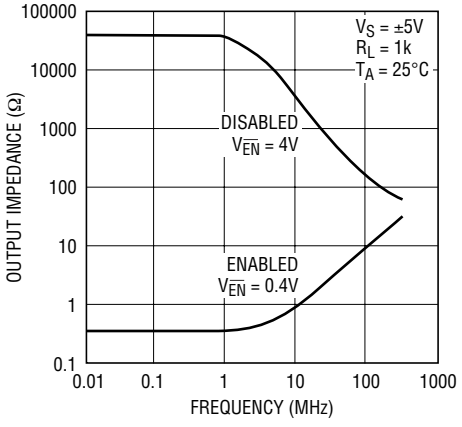
Frequency Response with Capacitive Loads



Harmonic Distortion vs Frequency

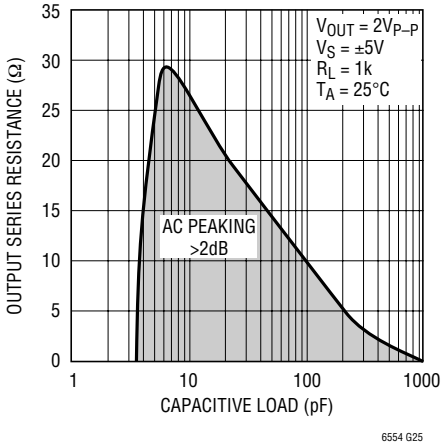


Output Impedance vs Frequency

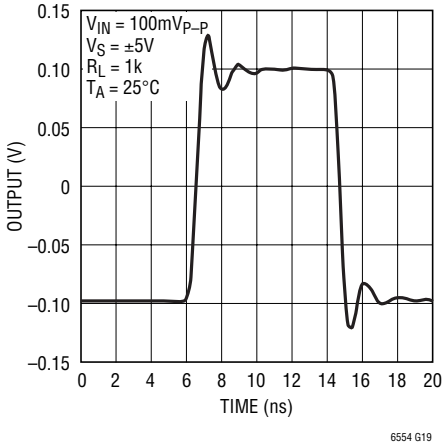


TYPICAL PERFORMANCE CHARACTERISTICS

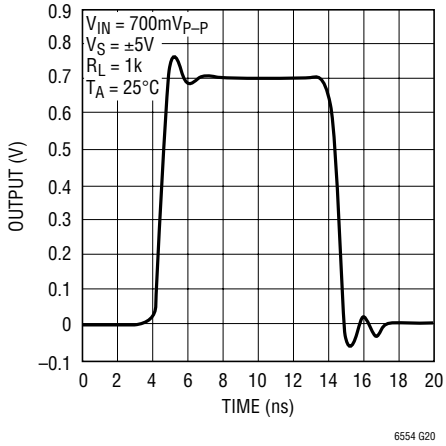
Maximum Capacitive Load vs Output Series Resistor



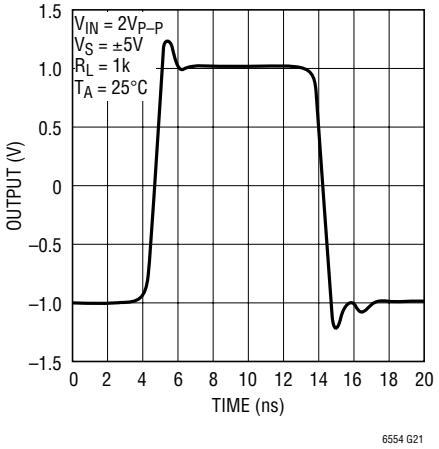
Small Signal Transient Response



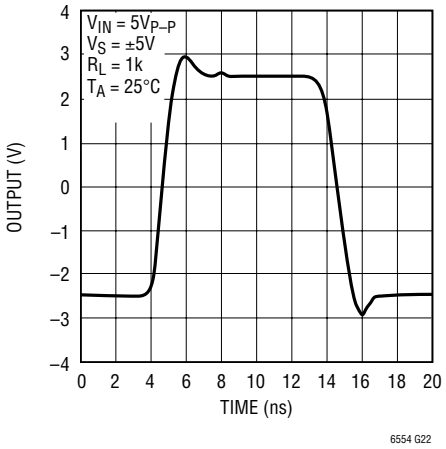
Video Amplitude Transient Response



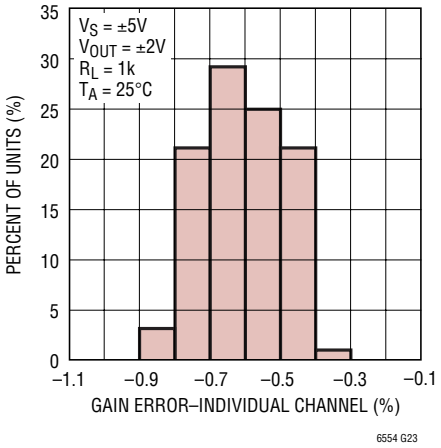
Large Signal Transient Response



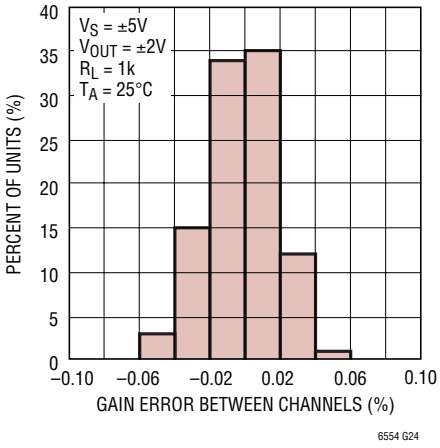
Large Signal Transient Response



Gain Error Distribution



Gain Error Matching Distribution



PIN FUNCTIONS

$\overline{EN}$ (Pin 1): Enable Control Pin. An internal pull-up resistor of 46k defines the pin's impedance and will turn the part off if the pin is unconnected. When the pin is pulled low, the part is enabled.

DGND (Pin 2): Digital Ground Reference for Enable Pin. This pin is normally connected to ground.

INR (Pin 3): Red Channel Input. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

AGND (Pin 4): Analog Ground for Isolation Between Red and Green Channel Inputs. The AGND pins have ESD protection and therefore should not be connected to potentials outside the power supply range.

ING (Pin 5): Green Channel Input. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

AGND (Pin 6): Analog Ground for Isolation Between Green and Blue Channel Inputs. The AGND pins have ESD protection and therefore should not be connected to potentials outside the power supply range.

INB (Pin 7): Blue Channel Input. This pin has a nominal impedance of 400kΩ and does not have any internal termination resistor.

V^- (Pin 8): Negative Supply Voltage. V^- pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

V^- (Pin 9): Negative Supply Voltage for Blue Channel Output Stage. V^- pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUTB (Pin 10): Blue Channel Output. It is the buffered output of the blue channel input.

V^+ (Pin 11): Positive Supply Voltage for Blue and Green Channel Output Stages. V^+ pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUTG (Pin 12): Green Channel Output. It is the buffered output of the green channel input.

V^- (Pin 13): Negative Supply Voltage for Green and Red Channel Output Stages. V^- pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

OUTR (Pin 14): Red Channel Output. It is the buffered output of the red channel input.

V^+ (Pin 15): Positive Supply Voltage for Red Channel Output Stage. V^+ pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

V^+ (Pin 16): Positive Supply Voltage. V^+ pins are not internally connected to each other, and must all be connected externally. Proper supply bypassing is necessary for best performance. See the Applications Information section.

APPLICATIONS INFORMATION

Power Supplies

The LT6554 is optimized for ±5V supplies but can be operated on as little as ±2.25V or a single 4.5V supply and as much as ±6V or a single 12V supply. Internally, each supply is independent to improve channel isolation. **Do not leave any supply pins disconnected!**

Enable/Shutdown

The LT6554 has a TTL compatible shutdown mode controlled by the $\overline{EN}$ pin and referenced to the DGND pin. If the amplifier will be enabled at all times, the $\overline{EN}$ pin can be connected directly to DGND. If the enable function is desired, either driving the pin above 2V or allowing the internal 46k pull-up resistor to pull the $\overline{EN}$ pin to the top rail will disable the amplifier. When disabled, the output will become very high impedance. Supply current into the amplifier in the disabled state will be primarily through V^+ and approximately equal to $(V^+ – V_{\overline{EN}})/46k$.

It is important that the two following constraints on the DGND pin and the $\overline{EN}$ pin are always followed:

$$V^+ – V_{DGND} \geq 3V$$
$$V_{\overline{EN}} – V_{DGND} \leq 5.5V$$

Split supplies of ±3V to ±5.5V will satisfy these requirements with DGND connected to 0V.

In single supply applications above 5.5V, an additional resistor may be needed from the $\overline{EN}$ pin to DGND if the pin is ever allowed to float. For example, on a 12V single supply, a 33k resistor to ground would protect the pin from floating too high while still allowing the internal pull-up resistor to disable the part.

On dual ±2.25V supplies, connecting the $\overline{EN}$ and DGND pins to $V^–$ is the easiest way of ensuring that $V^+ – V_{DGND}$ is more than 3V.

The DGND pin should not be pulled above the $\overline{EN}$ pin since doing so will turn on an ESD protection diode. If the $\overline{EN}$ pin voltage is forced a diode drop below the DGND pin, current should be limited to 10mA or less.

The enable/disable times of the LT6554 are fast when driven with a logic input. Turn on (from 50% $\overline{EN}$ input to 50% output) typically occurs in less than 50ns. Turn off is slower, but is nonetheless below 300ns.

Input Considerations

The LT6554 input voltage range is from $V^–$ + 1V to V^+ – 1V and is therefore larger than the output swing. The inputs can be driven beyond the point at which the output clips so long as input currents are limited to below ±10mA.

Layout and Grounding

It is imperative that care is taken in PCB layout in order to utilize the very high speed and very low crosstalk of the LT6554. Separate power and ground planes are highly recommended and trace lengths should be kept as short as possible. If input traces must be run over a distance of several centimeters, they should use a controlled impedance with either series or shunt terminations (nominally 50Ω or 75Ω) to maintain signal fidelity.

Care should be taken to minimize capacitance on the LT6554's output traces by increasing spacing between traces and adjacent metal and by eliminating metal planes in underlying layers. To drive cable or traces longer than several centimeters, using the LT6553 with its fixed gain of +2 in conjunction with series and load termination resistors may provide better results.

A plot of LT6554 performance driving a 1k load with various trace lengths is shown in Figure 1. All data is from a 4-layer board with 2oz copper, 18mil of board layer thickness to the ground plane, a trace width of 12mils and spacing to adjacent metal of 18mils. The 0.2cm output trace places the 1k resistor as close to the part as possible, while the other curves show the load resistor consecutively further away. The worst case, 4cm, trace has almost 10pF of parasitic capacitance.

In order to counteract any peaking in the frequency response from driving a capacitive load, a series resistance can be inserted in the line at the output of the part to flatten the response. Figure 2 shows the frequency response with the same 4cm trace from Figure 1, now with a 10Ω series resistor inserted near the output pin of the LT6554. Note that using a 10Ω series resistor with a 1k load only decreases the output amplitude by 0.1dB or 1% and has a minimal effect on the bandwidth of the system. See the graph labeled "Maximum Capacitive Load vs Output Series Resistor" in the Typical Performance Characteristics section for more information.

APPLICATIONS INFORMATION

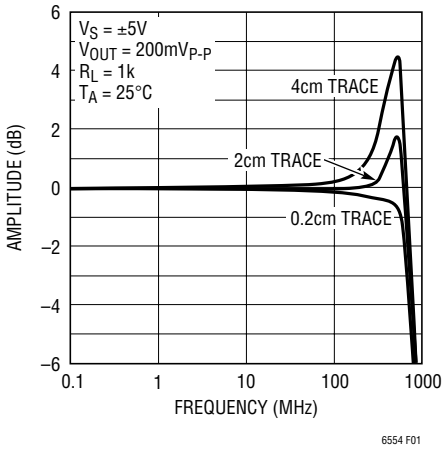


Figure 1. Response vs Output Trace Length

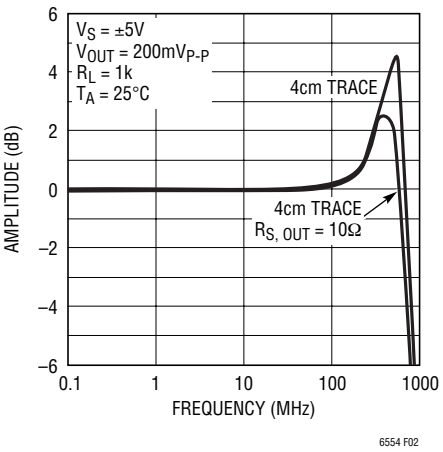


Figure 2. Response vs Series Output Resistance

While the AGND pins on the LT6554 are not connected to the amplifier circuitry, tying them to ground or another "quiet" node significantly increases channel isolation and is always recommended. The AGND pins do have ESD protection and therefore should not be connected to potentials outside the power supply range.

Low ESL/ESR bypass capacitors should be placed as close to the positive and negative supply pins as possible. One 4700pF ceramic capacitor is recommended for both V^+ and V^-. Additional 470pF ceramic capacitors with minimal trace length on each supply pin will further improve AC and transient response as well as channel isolation. For high current drive and large-signal transient applications, additional 1µF to 10µF tantalums should be added on each supply. The smallest value capacitors should be placed closest to the package.

To maintain the LT6554's channel isolation, it is beneficial to shield parallel input and output traces using a ground plane or power supply traces. Vias between topside and backside metal are recommended to maintain a low inductance ground, especially between closely spaced signal traces.

Single Supply Operation

Figure 3 illustrates how to use the LT6554 with a single supply ranging from 4.5V to 12V. Since the output range is comparable to the input range, the DC bias point at the input can be set anywhere between the supplies that will prevent the AC-coupled signal from running into the output range limits. As shown, the DC input level is mid-supply.

The only additional power dissipation in the single supply configuration is through the resistor bias string at the input and through any load resistance at the output. In many cases, the output can be used to directly drive other single supply devices without additional coupling and without any resistive load.

ESD Protection

The LT6554 has reverse-biased ESD protection diodes on all pins. If any pins are forced a diode drop above the positive supply or a diode drop below the negative supply, large currents may flow through these diodes. If the current is kept below 10mA, no damage to the device will occur.

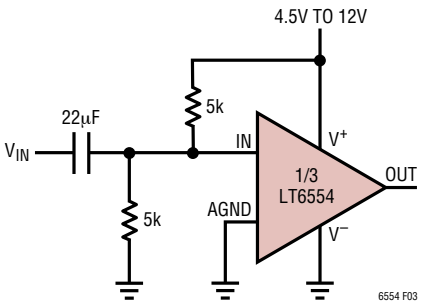


Figure 3. Single Supply Configuration, One Channel Shown

TYPICAL APPLICATION

RGB Buffer Demo Board

The DC794 Demo Board illustrates optimal routing, bypassing and termination using the LT6554 as an RGB video buffer. The schematic is shown in Figure 4. All inputs and outputs are routed to have a characteristic impedance of 75Ω. The 75Ω input shunt and output series terminations are connected as close to the part as possible. While the 75Ω back termination resistors at the outputs of the LT6554 minimize signal reflections in the output traces and isolate the part from any capacitive loading in those traces, they also contribute to gain error if the output is not terminated with high impedance. For example, if the output is terminated with a 1k load, the 75Ω back termination will cause a 7% gain error. Decreasing the value of the back termination resistors will decrease the signal attenuation but may compromise the AC response. However, connecting the LT6554 outputs to the output traces on the DC794 board without some series resistance is not recommended; 10Ω to 20Ω is generally sufficient.

A fourth signal trace is provided at the bottom of the DC794 demo board with dimensions identical to the combined input and output of the other channels. This trace can be used for calibrating the effects of electrical delay and impedance mismatching and is not necessary in an end-user application. Jumpers and additional connectors are also included to allow for evaluation of the enable feature and single supply operation.

RGB Video Selector/Cable Driver

A video multiplexer can be implemented using the $\overline{EN}$ pins of parallel LT6554s as shown in Figure 5. In this application, the corresponding outputs are connected together and one LT6554 is switched on while the other is switched off. A fast inverter provides a complementary signal to ensure that only one set of R, G and B channels is buffered at any time.

Since the output impedance of a disabled LT6554 is very high, adding additional channels will not resistively load an enabled output. However, since the disabled LT6554 has around 6pF of capacitance, it may be desirable to resistively isolate the outputs of each channel to maintain flat frequency response as shown in the graph labeled “Maximum Capacitive Load vs Output Series Resistor” in the Typical Performance Characteristics section.

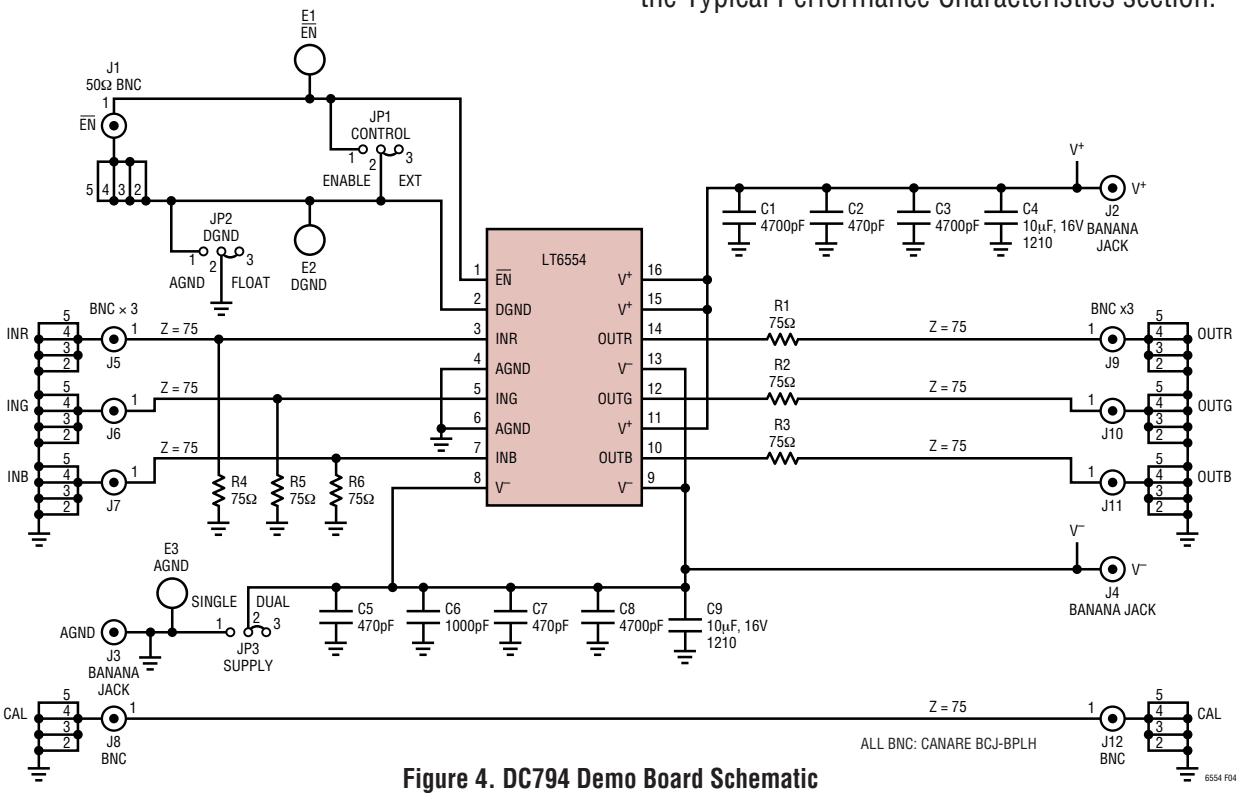
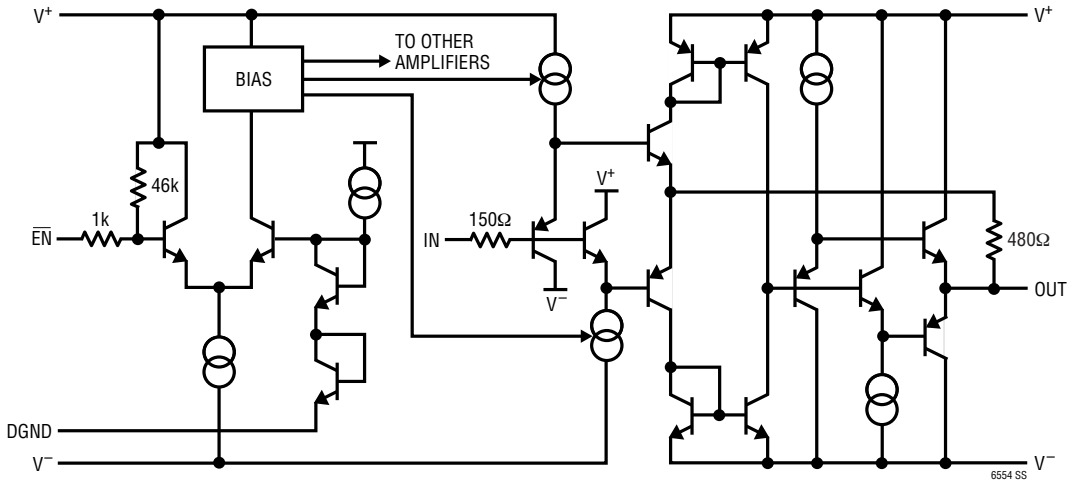


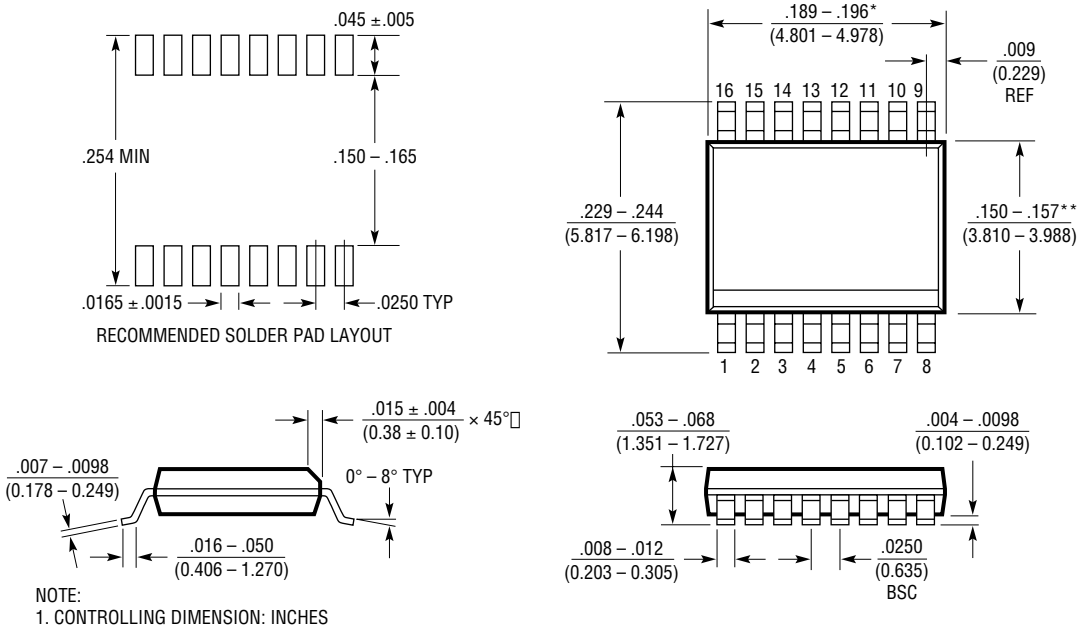
Figure 4. DC794 Demo Board Schematic

SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

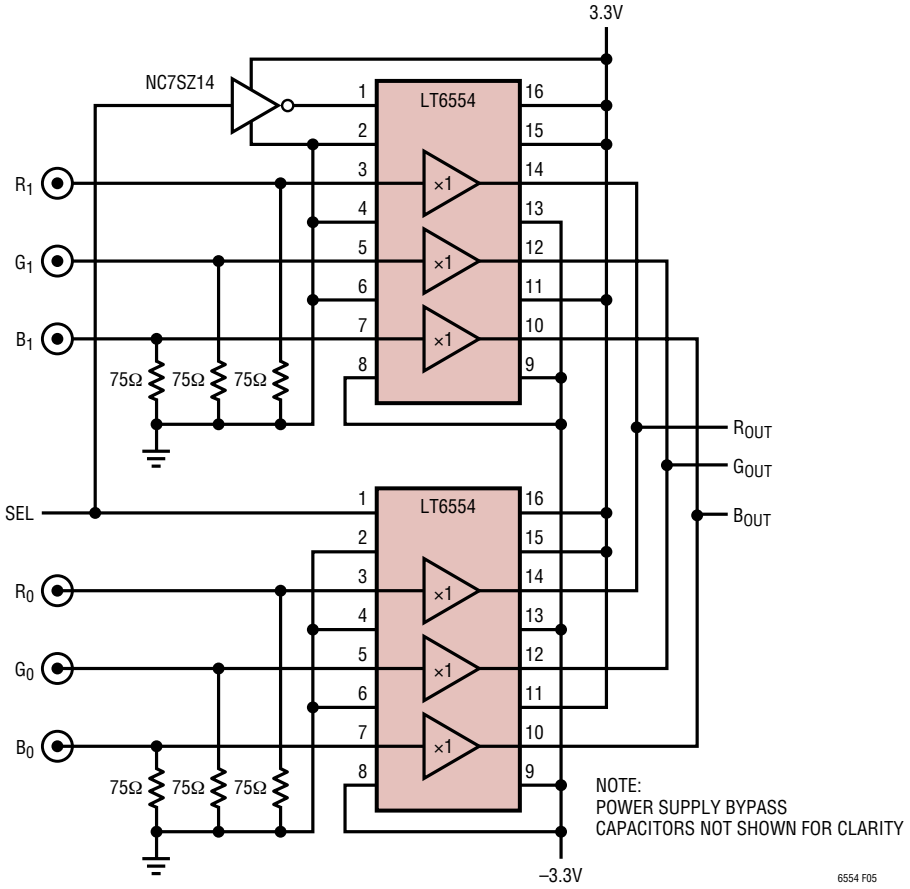


Figure 5. RGB Video Selector and A/D Driver

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1259/LT1260	Dual/Triple 130MHz Current Feedback Amplifiers	Shutdown, Operates to ±15V
LT1395/LT1396/LT1397	Single/Dual/Quad 400MHz Current Feedback Amplifiers	800V/µs Slew Rate
LT1398/LT1399	Dual/Triple 300MHz Current Feedback Amplifiers	0.1dB Gain Flatness to 150MHz, Shutdown
LT1675/LT1675-1	250MHz, Triple and Single RGB Multiplexer with Current Feedback Amplifiers	100MHz Pixel Switching, –3dB Bandwidth: 250MHz, 1100V/µs Slew Rate
LT1809/LT1810	Single/Dual, 180MHz, Rail-to-Rail Input and Output Amplifiers	350V/µs Slew Rate, Shutdown, Low Distortion –90dBc at 5MHz
LT6550/LT6551	3.3V Triple and Quad Video Buffers	110MHz Gain of 2 Buffers in MSOP Package
LT6553	650MHz, Gain of 2, Triple Video Amplifier	Same Pinout as LT6554

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