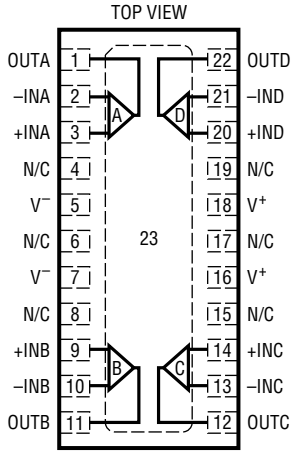
ABSOLUTE MAXIMUM RATINGS

(Note 1)

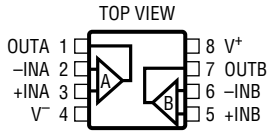
Supply Voltage (V^+ to V^-).....60V, –50V
Input Differential Voltage .....±80V
Input Voltage (Note 2).....80V, –25V
Input Current (Note 2).....±10mA
Output Short Circuit Duration
(Note 3).....Continuous

Temperature Range (Notes 4, 5)
LT6015I/LT6016I/LT6017I.....–40°C to 85°C
LT6015H/LT6016H/LT6017H.....–40°C to 125°C
LT6015MP/LT6016MP/LT6017MP
($T_{JUNCTION}$).....–55°C to 150°C
Storage Temperature Range .....–65°C to 150°C
Maximum Junction Temperature ..... 150°C
Lead Temperature (Soldering, 10sec).....300°C

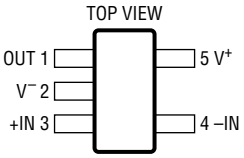
PIN CONFIGURATION



DJC PACKAGE
22-LEAD (6mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 31.8°C/W, θ_{JC} = 4.3°C/W
UNDERSIDE METAL INTERNALLY CONNECTED TO V^-



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 273°C/W, θ_{JC} = 45°C/W



S5 PACKAGE
5-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT6015IS5#PBF	LT6015IS5#TRPBF	LTGJG	5-Lead Plastic TSOT-23	–40°C to 85°C
LT6015HS5#PBF	LT6015HS5#TRPBF	LTGJG	5-Lead Plastic TSOT-23	–40°C to 125°C
LT6015MPS5#PBF	LT6015MPS5#TRPBF	LTGJG	5-Lead Plastic TSOT-23	–55°C to 150°C
LT6016IMS8#PBF	LT6016IMS8#TRPBF	LTGFK	8-Lead Plastic MSOP	–40°C to 85°C
LT6016HMS8#PBF	LT6016HMS8#TRPBF	LTGFK	8-Lead Plastic MSOP	–40°C to 125°C
LT6016MPMS8#PBF	LT6016MPMS8#TRPBF	LTGFK	8-Lead Plastic MSOP	–55°C to 150°C
LT6017IDJC#PBF	LT6017IDJC#TRPBF	6017	22-Lead Plastic DFN	–40°C to 85°C
LT6017HDJC#PBF	LT6017HDJC#TRPBF	6017	22-Lead Plastic DFN	–40°C to 125°C
LT6017MPDJC#PBF	LT6017MPDJC#TRPBF	6017	22-Lead Plastic DFN	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H–grade parts, otherwise specifications are at T_A = 25°C, V_S = 5V, V_{CM} = V_{OUT} = mid-supply.

SYMBOL	PARAMETER	CONDITIONS		I-, H-GRADE MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	0 < V_{CM} < V^+ – 1.75V MS8 Package		–50	±25	50	µV
		0 < V_{CM} < V^+ – 1.75V SOT-23, DJC22 Packages		–80	±45	80	µV
		V_{CM} = 5V		–125	±50	125	µV
		V_{CM} =76V		–135	±50	135	µV
		0 < V_{CM} < V^+ – 1.75V	●	–250	±45	250	µV
		V_{CM} = 5V to V_{CM} = 76V	●	–350	±50	350	µV
$\frac{\Delta V_{OS}}{\Delta TEMP}$	Input Offset Voltage Drift				0.75		µV/°C
$\frac{\Delta V_{OS}}{\Delta TIME}$	Long Term Voltage Offset Stability				0.75		µV/Mo
I_B	Input Bias Current	0.25V < V_{CM} < V^+ – 1.75V		–5	±2	5	nA
		V_{CM} = 0V		–60	–16.5	0	nA
		V_{CM} = 5V to 76V		11	14	17.5	µA
		0.25V < V_{CM} < V^+ – 1.75V	●	–15	±2	15	nA
		V_{CM} = 0V	●	–150	–16.5	0	nA
		V_{CM} = 5V to 76V	●	7	14	23	µA
		V_S = 0V, V_{CM} = 0V to 76V	●		0.001	1	µA
I_{OS}	Input Offset Current	0.25V < V_{CM} < V^+ – 1.75V		–5	±2	5	nA
		V_{CM} = 0V		–5	±2	5	nA
		V_{CM} = 5V to 76V (Note 6)		–500	±50	500	nA
		0.25V < V_{CM} < V^+ – 1.75V	●	–15	±2	15	nA
		V_{CM} = 0V	●	–15	±2	15	nA
		V_{CM} = 5V to 76V (Note 6)	●	–500	±50	500	nA
VCMR	Common Mode Input Range		●	0		76	V
C_{IN}	Differential Input Capacitance				5		pF
R_{IN}	Differential Input Resistance	0 < V_{CM} < V^+ – 1.75V			1		MΩ
		V_{CM} > V^+			3.7		kΩ
R_{INCM}	Common Mode Input Resistance	0 < V_{CM} < V^+ – 1.75V			>1		GΩ
		V_{CM} > V^+			>100		MΩ
e_n	Input Referred Noise Voltage Density	f = 1kHz V_{CM} < V^+ – 1.75V			18		nV/√Hz
		V_{CM} > V^+			25		nV/√Hz
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz V_{CM} < V^+ – 1.75V			0.5		$µV_{P-P}$
i_n	Input Referred Noise Current Density	f = 1kHz V_{CM} < V^+ – 1.75V			0.1		pA/√Hz
		V_{CM} > V^+			11.5		pA/√Hz
A_{VOL}	Open Loop Gain	R_L = 10kΩ ΔV_{OUT} = 3V	●	300	3000		V/mV
PSRR	Supply Rejection Ratio	V_S = ±1.65V to ±15V V_{CM} = V_{OUT} = Mid-Supply	●	110	126		dB
CMRR	Input Common Mode Rejection Ratio	V_{CM} = 0V to 3.25V	●	100	126		dB
		V_{CM} = 5V to 76V	●	126	140		dB
V_{OL}	Output Voltage Swing Low	V_S = 5V, No Load	●		3	55	mV
		V_S = 5V, 5mA	●		280	500	mV
V_{OH}	Output Voltage Swing High	V_S = 5V, No Load	●		450	700	mV
		V_S = 5V, 5mA	●		1000	1250	mV
I_{SC}	Short-Circuit Current	V_S = 5V, 50Ω to V^+	●	10	25		mA
		V_S = 5V, 50Ω to $V^–$	●	10	25		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H–grade parts, otherwise specifications are at T_A = 25°C, V_S = 5V, V_{CM} = V_{OUT} = mid-supply.

SYMBOL	PARAMETER	CONDITIONS		I-, H-GRADE MIN	TYP	MAX	UNITS
GBW	Gain Bandwidth Product	f_{TEST} = 100kHz		2.85	3.2		MHz
			●	2.5	3.2		MHz
SR	Slew Rate	ΔV_{OUT} = 3V		0.55	0.75		V/µs
			●	0.45	0.75		V/µs
t_S	Settling Time Due to Input Step ΔV_{OUT} = ±2V	0.1% Settling			3.5		µs
V_S	Supply Voltage			3		50	V
			●	3.3		50	V
	Reverse Supply (Note 7)	I_S < –25µA/Amplifier	●		–65	–50	V
I_S	Supply Current Per Amplifier	SOT-23 Package			315	345	µA
		MS8, DJC22 Packages			315	335	µA
			●		315	500	µA
R_O	Output Impedance	ΔI_O = ±5mA			0.15		Ω

The ● denotes the specifications which apply over the specified temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H–grade parts, otherwise specifications are at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = mid-supply.

SYMBOL	PARAMETER	CONDITIONS		I-, H-GRADE MIN	TYP	MAX	UNITS
V_{OSI}	Input Offset Voltage			–80	±55	80	µV
			●	–250	±55	250	µV
		V_S = ±25V		–110	±75	110	µV
		V_S = ±25V	●	–250	±75	250	µV
$\frac{\Delta V_{OSI}}{\Delta TEMP}$	Input Offset Voltage Drift				0.75		µV/°C
I_B	Input Bias Current			–5	±2	5	nA
			●	–15	±2	15	nA
I_{OS}	Input Offset Current			–5	±2	5	nA
			●	–15	±2	15	nA
VCMR	Common Mode Input Range		●	–15		61	V
C_{IN}	Differential Input Capacitance				5		pF
R_{IN}	Differential Input Resistance	0 < V_{CM} < V^+ – 1.75V			1		MΩ
		V_{CM} > V^+			3.7		kΩ
R_{INCM}	Common Mode Input Resistance	0 < V_{CM} < V^+ – 1.75V			>1		GΩ
		V_{CM} > V^+			>100		MΩ
e_n	Input Referred Noise Voltage Density	f = 1kHz					
		V_{CM} < V^+ – 1.75V			18		nV/√Hz
		V_{CM} > V^+			25		nV/√Hz
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz			0.5		μV_{P-P}
		V_{CM} < V^+ – 1.25V					
i_n	Input Referred Noise Current Density	f = 1kHz					
		V_{CM} < V^+ – 1.75V			0.1		pA/√Hz
		V_{CM} > V^+			11.5		pA/√Hz
A_{VOL}	Open Loop Gain	R_L = 10kΩ	●	200	1000		V/mV
		ΔV_{OUT} = 27V					
PSRR	Supply Rejection Ratio	V_S = ±2.5V to ±25V	●	114	126		dB
		V_{CM} = V_{OUT} = 0V					
CMRR	Input Common Mode Rejection Ratio	V_{CM} = –15V to 13.25V	●	110	126		dB
V_{OL}	Output Voltage Swing Low	V_S = ±15V, No Load	●		3	55	mV
		V_S = ±15V, 5mA	●		280	500	mV
V_{OH}	Output Voltage Swing High	V_S = ±15V, No Load	●		450	700	mV
		V_S = ±15V, 5mA	●		1000	1250	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, –40°C < T_A < 85°C for I-grade parts, –40°C < T_A < 125°C for H–grade parts, otherwise specifications are at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = mid-supply.

SYMBOL	PARAMETER	CONDITIONS		I-, H-GRADE MIN	TYP	MAX	UNITS
I_{SC}	Short-Circuit Current	V_S = ±15V, 50Ω to GND	●	10	30		mA
		V_S = ±15V, 50Ω to GND	●	10	32		mA
GBW	Gain Bandwidth Product	f_{TEST} = 100kHz		2.9	3.3		MHz
			●	2.55	3.3		MHz
SR	Slew Rate	ΔV_{OUT} = 3V		0.6	0.8		V/µs
			●	0.5	0.8		V/µs
t_S	Settling Time Due to Input Step	0.1% Settling ΔV_{OUT} = ±2V			3.5		µs
V_S	Supply Voltage			3		50	V
			●	3.3		50	V
	Reverse Supply	I_S = –25µA/Amplifier	●		–65	–30	V
I_S	Supply Current Per Amplifier	SOT-23 Package			325	360	µA
		MS8, DJC22 Packages			325	350	µA
			●		325	525	µA
		V_S = ±25V, SOT-23 Package			340	370	µA
		V_S = ±25V, MS8, DJC22 Package			340	360	µA
		V_S = ±25V	●		340	550	µA
R_O	Output Impedance	ΔI_O = ±5mA			0.15		Ω

The ● denotes the specifications which apply over the specified temperature range, –55°C < $T_{JUNCTION}$ < 150°C for MP-grade parts, otherwise specifications are at T_A = 25°C, V_S = 5V, V_{CM} = V_{OUT} = mid-supply.

SYMBOL	PARAMETER	CONDITIONS		MP-GRADE MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	0 < V_{CM} < V^+ – 1.75V					µV
		MS8 Package		–50	±25	50	µV
		0 < V_{CM} < V^+ – 1.75V					
		DJC22 Package		–80	±45	80	µV
		V_{CM} = 5V		–125	±50	125	µV
		V_{CM} = 76V		–135	±50	135	µV
		0 < V_{CM} < V^+ –1.75V	●	–500	±45	500	µV
		V_{CM} = 5V to V_{CM} = 76V	●	–600	±50	600	µV
$\frac{\Delta V_{OS}}{\Delta TEMP}$	Input Offset Voltage Drift				0.75		µV/°C
$\frac{\Delta V_{OS}}{\Delta TIME}$	Long Term Voltage Offset Stability				0.75		µV/Mo
I_B	Input Bias Current	0.25V < V_{CM} < V^+ – 1.75V		–5	±2	5	nA
		V_{CM} = 0V		–60	–16.5	0	nA
		V_{CM} = 5V to 76V		11	14	17.5	µA
		0.25V < V_{CM} < V^+ – 1.75V	●	–100	±2	100	nA
		V_{CM} = 0V	●	–500	–16.5	0	nA
		V_{CM} = 5V to 76V	●	6.5	14	24	µA
		V_S = 0V, V_{CM} = 0V to 76V	●		0.001	4	µA
I_{OS}	Input Offset Current	0.25V < V_{CM} < V^+ – 1.75V		–5	±2	5	nA
		V_{CM} = 0V		–5	±2	5	nA
		V_{CM} = 5V to 76V (Note 6)		–500	±50	500	nA
		0.25V < V_{CM} < V^+ – 1.75V	●	–50	±2	50	nA
		V_{CM} = 0V	●	–200	±2	200	nA
		V_{CM} = 5V to 76V (Note 6)	●	–500	±150	500	nA
VCMR	Common Mode Input Range		●	0		76	V
C_{IN}	Differential Input Capacitance				5		pF
R_{IN}	Differential Input Resistance	0 < V_{CM} < V^+ – 1.75V			1		MΩ
		V_{CM} > V^+			3.7		kΩ
R_{INCM}	Common Mode Input Resistance	0 < V_{CM} < V^+ – 1.75V			>1		GΩ
		V_{CM} > V^+			>100		MΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, –55°C < $T_{JUNCTION}$ < 150°C for MP-grade parts, otherwise specifications are at T_A = 25°C, V_S = 5V, V_{CM} = V_{OUT} = mid-supply.

SYMBOL	PARAMETER	CONDITIONS		MP-GRADE MIN	MP-GRADE TYP	MP-GRADE MAX	UNITS
e_n	Input Referred Noise Voltage Density	f = 1kHz V_{CM} < V^+ – 1.75V V_{CM} > V^+			18 25		nV/√Hz nV/√Hz
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz V_{CM} < V^+ – 1.75V			0.5		μV_{P-P}
i_n	Input Referred Noise Current Density	f = 1kHz V_{CM} < V^+ – 1.75V V_{CM} > V^+			0.1 11.5		pA/√Hz pA/√Hz
A_{VOL}	Open Loop Gain	R_L = 10kΩ ΔV_{OUT} = 3V	●	200	3000		V/mV
PSRR	Supply Rejection Ratio	V_S = ±1.65V to ±15V V_{CM} = V_{OUT} = Mid-Supply	●	106	126		dB
CMRR	Input Common Mode Rejection Ratio	V_{CM} = 0V to 3.25V V_{CM} = 5V to 76V	● ●	90 120	126 140		dB dB
V_{OL}	Output Voltage Swing Low	V_S = 5V, No Load V_S = 5V, 5mA	● ●		3 280	75 550	mV mV
V_{OH}	Output Voltage Swing High	V_S = 5V, No Load V_S = 5V, 5mA	● ●		450 1000	750 1300	mV mV
I_{SC}	Short-Circuit Current	V_S = 5V, 50Ω to V^+ V_S = 5V, 50Ω to $V^–$	● ●	8 8	25 25		mA mA
GBW	Gain Bandwidth Product	f_{TEST} = 100kHz	 ●	2.85 2.4	3.2 3.2		MHz MHz
SR	Slew Rate	ΔV_{OUT} = 3V	 ●	0.55 0.4	0.75 0.75		V/µs V/µs
t_S	Settling Time Due to Input Step	0.1% Settling ΔV_{OUT} = ±2V			3.5		µs
V_S	Supply Voltage Reverse Supply (Note 7)	 I_S < –25VµA/Amplifier	 ● ●	3 3.3	 –63	50 50 –50	V V V
I_S	Supply Current Per Amplifier	SOT-23 Package MS8, DJC22 Packages 	 ●		315 315 315	345 335 540	µA µA µA
R_O	Output Impedance	ΔI_O = ±5mA			0.15		Ω

The ● denotes the specifications which apply over the specified temperature range, –55°C < $T_{JUNCTION}$ < 150°C for MP-grade parts, otherwise specifications are at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = mid-supply.

SYMBOL	PARAMETER	CONDITIONS		MP-GRADE MIN	MP-GRADE TYP	MP-GRADE MAX	UNITS
V_{OSI}	Input Offset Voltage	 V_S = ±25V V_S = ±25V	 ● ●	–80 –500 –110 –500	±55 ±55 ±75 ±75	80 500 110 500	µV µV µV µV
$\frac{\Delta V_{OSI}}{\Delta TEMP}$	Input Offset Voltage Drift				0.75		µV/°C
I_B	Input Bias Current		 ●	–5 –300	±2 ±2	5 300	nA nA
I_{OS}	Input Offset Current		 ●	–5 –50	±2 ±2	5 50	nA nA
VCMR	Common Mode Input Range		●	–15		61	V
C_{IN}	Differential Input Capacitance				5		pF
R_{IN}	Differential Input Resistance	0 < V_{CM} < V^+ – 1.75V V_{CM} > V^+			1 3.7		MΩ kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, –55°C < $T_{JUNCTION}$ < 150°C for MP-grade parts, otherwise specifications are at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = Mid-Supply.

SYMBOL	PARAMETER	CONDITIONS		MP-GRADE MIN	MP-GRADE TYP	MP-GRADE MAX	UNITS
R_{INCM}	Common Mode Input Resistance	0 < V_{CM} < V^+ – 1.75V V_{CM} > V^+			>1 >100		GΩ MΩ
e_n	Input Referred Noise Voltage Density	f = 1kHz V_{CM} < V^+ – 1.75V V_{CM} > V^+			 18 25		 nV/√Hz nV/√Hz
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz V_{CM} < V^+ – 1.75V			0.5		μV_{P-P}
i_n	Input Referred Noise Current Density	f = 1kHz V_{CM} < V^+ – 1.75V V_{CM} > V^+			 0.1 11.5		 pA/√Hz pA/√Hz
A_{VOL}	Open Loop Gain	R_L = 10kΩ ΔV_{OUT} = 27V	●	100	1000		V/mV
PSRR	Supply Rejection Ratio	V_S = ±2.5V to ±25V V_{CM} = V_{OUT} = 0V	●	106	126		dB
CMRR	Input Common Mode Rejection Ratio	V_{CM} = –15V to 13.25V	●	100	126		dB
V_{OL}	Output Voltage Swing Low	V_S = ±15V, No Load V_S = ±15V, 5mA	● ●		3 280	75 550	mV mV
V_{OH}	Output Voltage Swing High	V_S = ±15V, No Load V_S = ±15V, 5mA	● ●		450 1000	750 1300	mV mV
I_{SC}	Short-Circuit Current	V_S = ±15V, 50Ω to GND V_S = ±15V, 50Ω to GND	● ●	8 8	30 32		mA mA
GBW	Gain Bandwidth Product	f_{TEST} = 100kHz	 ●	2.9 2.45	3.3 3.3		MHz MHz
SR	Slew Rate	ΔV_{OUT} = 3V	 ●	0.6 0.45	0.8 0.8		V/µs V/µs
t_S	Settling Time Due to Input Step	0.1% Settling ΔV_{OUT} = ±2V			3.5		µs
V_S	Supply Voltage Reverse Supply	 I_S = –25µA/Amplifier	 ● ●	3 3.3	 –65	50 50 –30	V V V
I_S	Supply Current Per Amplifier	SOT-23 Package MS8, DJC22 Packages V_S = ±25V, SOT-23 Package V_S = ±25V, MS8, DJC22 Package V_S = ±25V	 ● ●		325 325 325 340 340 340	360 350 575 370 360 600	µA µA µA µA µA µA
R_O	Output Impedance	ΔI_O = ±5mA			0.15		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Voltages applied are with respect to $V^–$. The inputs are tested to the Absolute Maximum Rating by applying –25V (relative to $V^–$) to each input for 10ms. In general, faults capable of sinking current from either input should be current limited to under 10mA. See the Applications Information section for more details.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted.

Note 4: The LT6015I/LT6016I/LT6017I are guaranteed functional over the operating temperature range of –40°C to 85°C. The LT6015H/LT6016H/LT6017H are guaranteed functional over the operating temperature range of –40°C to 125°C. The LT6015MP/LT6016MP/LT6017MP are guaranteed functional over the junction temperature range of –55°C to 150°C. Junction temperatures greater than 125°C will promote accelerated aging. The LT6015/LT6016/LT6017 has a demonstrated typical performance beyond 1000 hours at T_J = 150°C.

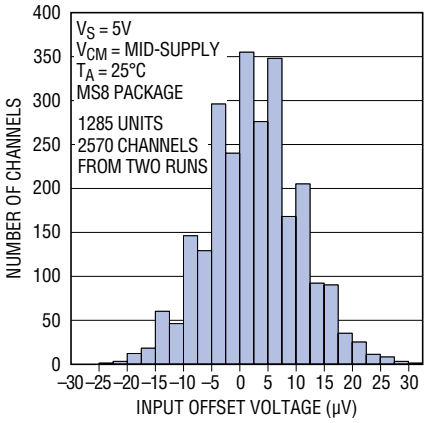
Note 5: The LT6015I/LT6016I/LT6017I are guaranteed to meet specified performance from –40°C to 85°C. The LT6015H/LT6016H/LT6017H are guaranteed to meet specified performance from –40°C to 125°C. The LT6015MP/LT6016MP/LT6017MP are guaranteed to meet specified performance with junction temperature ranging from –55°C to 150°C.

Note 6: Test accuracy is limited by high speed test equipment repeatability. Bench measurements indicate the input offset current in the Over-The-Top configuration is typically controlled to under ±50nA at 25°C and ±150nA over temperature.

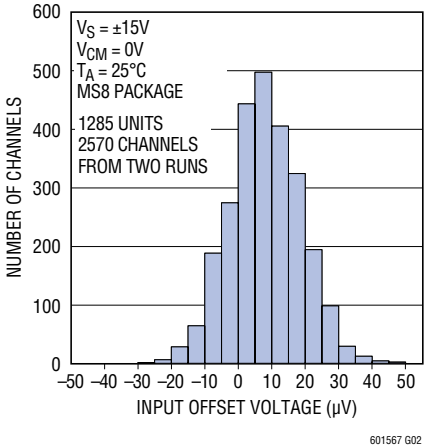
Note 7: The Reverse Supply voltage is tested by pulling 25µA/Amplifier out of the V^+ pin while measuring the V^+ pin's voltage with both inputs and $V^–$ grounded, verifying V^+ < –50V.

TYPICAL PERFORMANCE CHARACTERISTICS

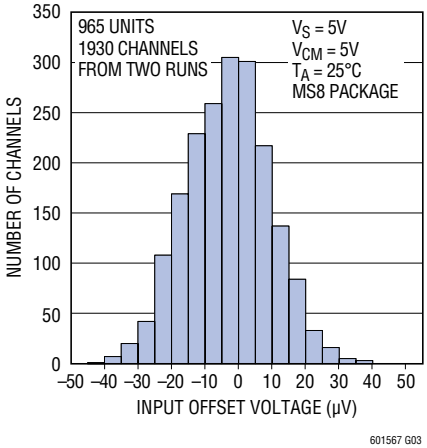
Typical Distribution of Input Offset Voltage



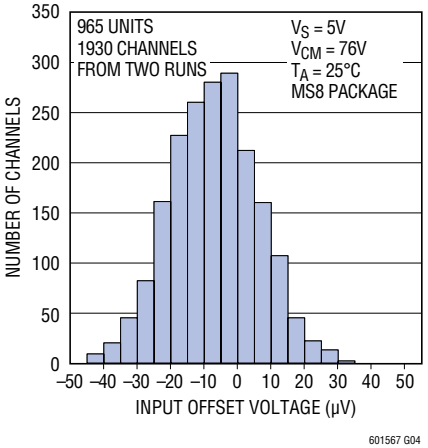
Typical Distribution of Input Offset Voltage



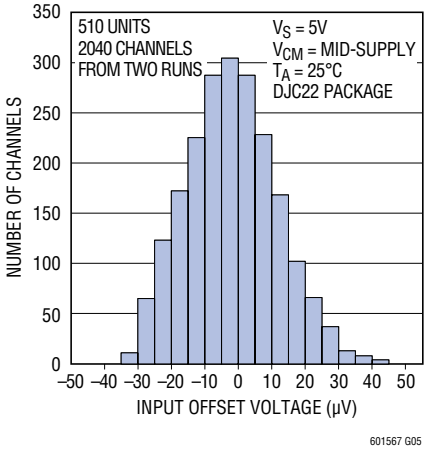
Typical Distribution of Over-The-Top Input Offset Voltage



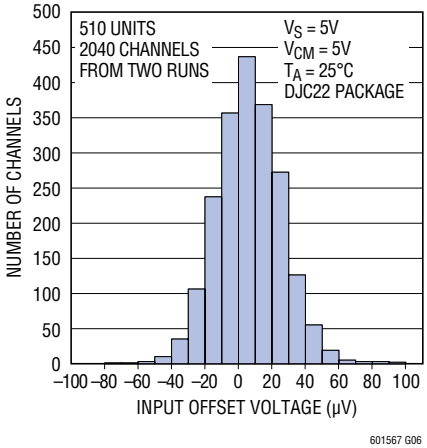
Typical Distribution of Over-The-Top Input Offset Voltage



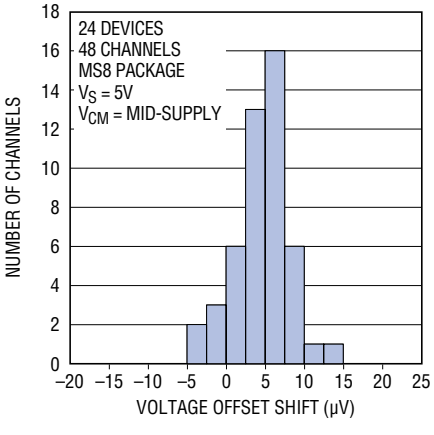
Typical Distribution of Input Offset Voltage



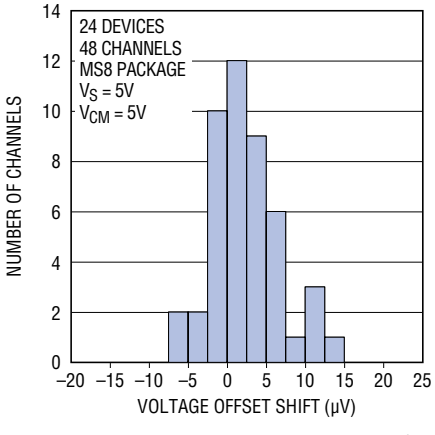
Typical Distribution of Over-The-Top Input Offset Voltage



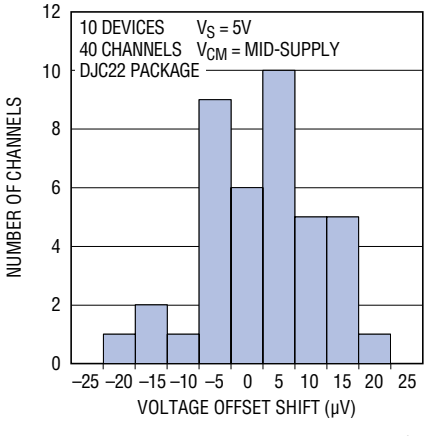
Voltage Offset Shift vs Lead Free IR Reflow



Over-The-Top Voltage Offset Shift vs Lead Free IR Reflow

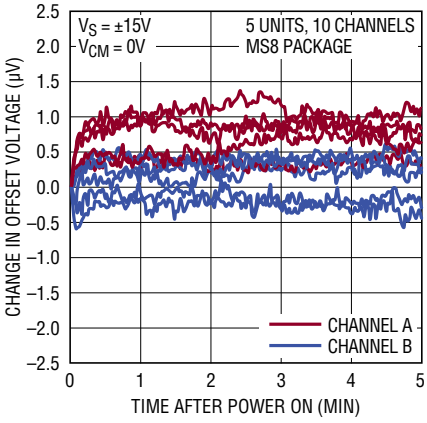


Voltage Offset Shift vs Lead Free IR Reflow

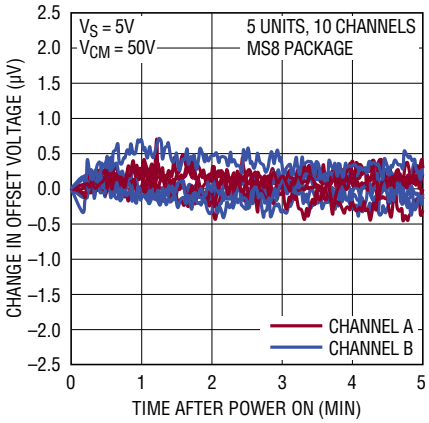


TYPICAL PERFORMANCE CHARACTERISTICS

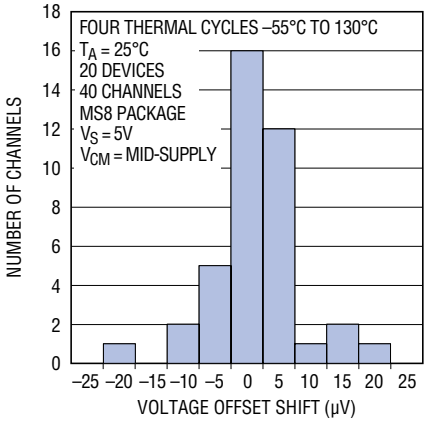
Warm-Up Drift



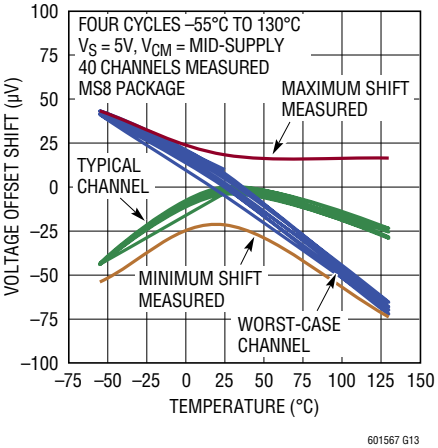
Over-The-Top Warm-Up Drift



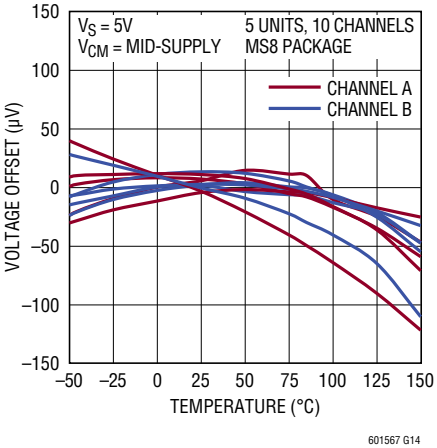
Voltage Offset Shift vs Thermal Cycling



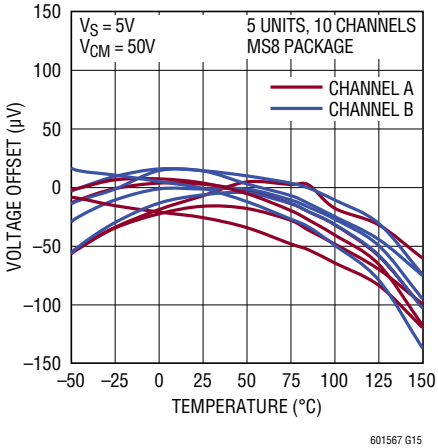
Voltage Offset Shift vs Temperature Cycling



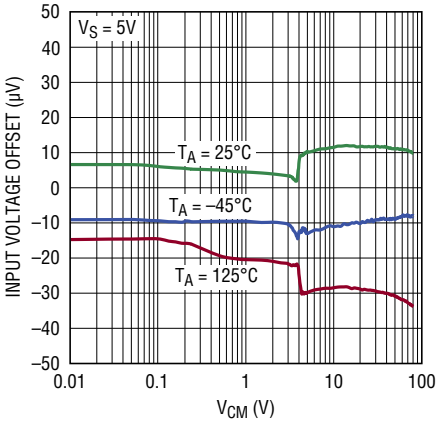
Voltage Offset vs Temperature



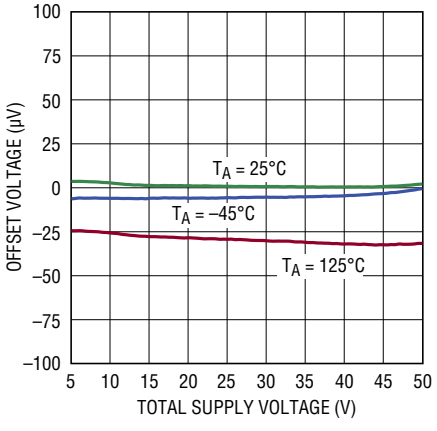
Over-The-Top Voltage Offset vs Temperature



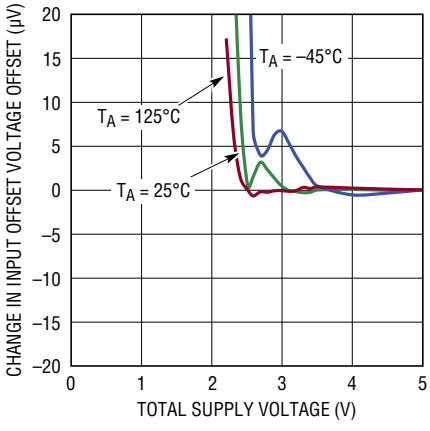
Voltage Offset vs Input Common Mode Voltage



Voltage Offset vs Supply Voltage

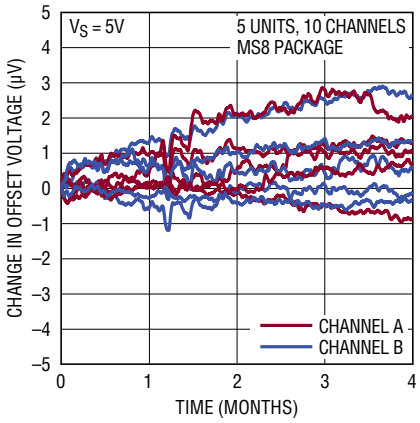


Minimum Supply Voltage



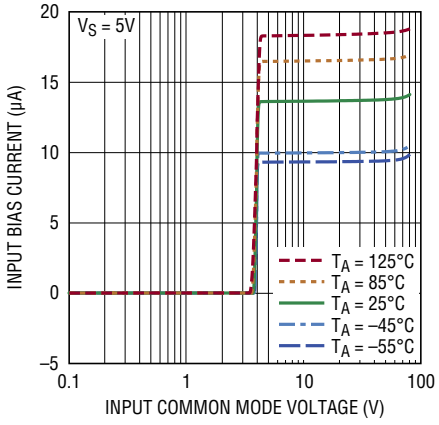
TYPICAL PERFORMANCE CHARACTERISTICS

Long Term Stability of Five Representative Units



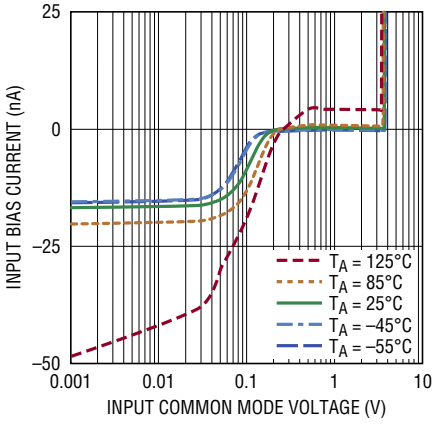
601567 G19

Input Bias Current vs Input Common Mode Voltage



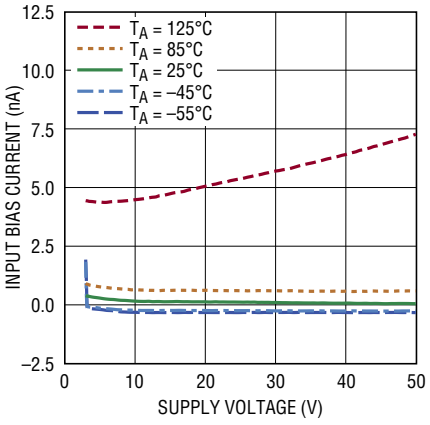
601567 G20

Input Bias Current vs Input Common Mode Voltage



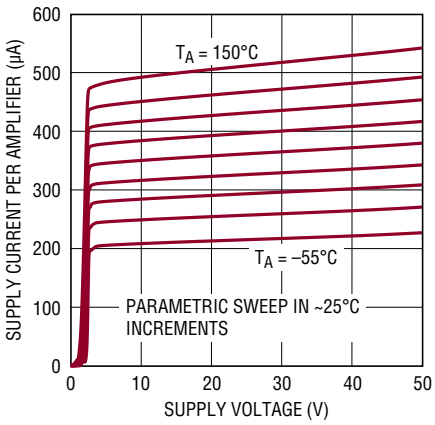
601567 G21

Input Bias Current vs Supply Voltage



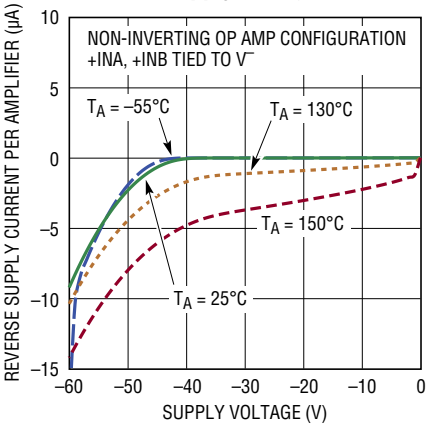
601567 G22

Supply Current vs Supply Voltage



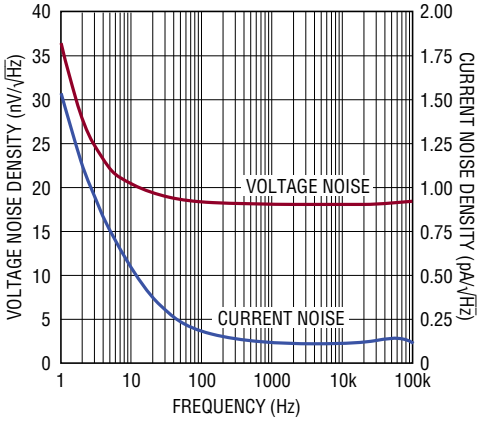
601567 G23

Reverse Supply Current vs Reverse Supply Voltage



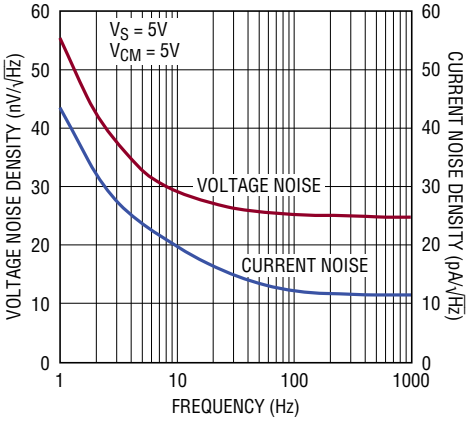
601567 G24

Noise Density vs Frequency



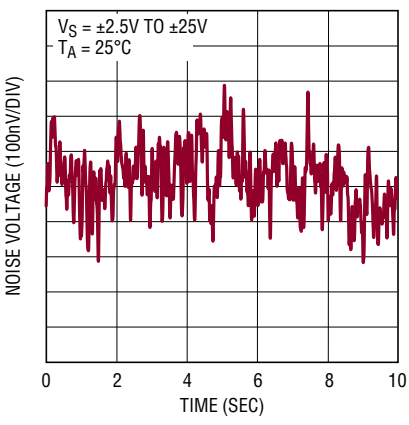
601567 G25

Over-The-Top Noise Density vs Frequency



601567 G26

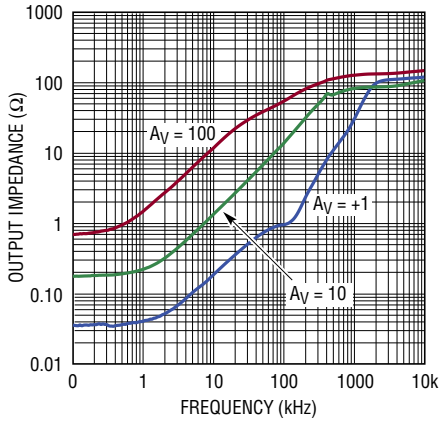
0.1Hz to 10Hz Noise



601567 G27

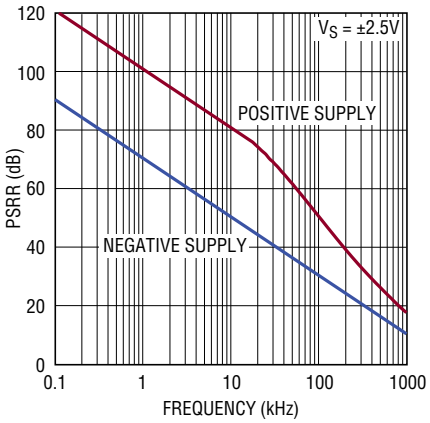
TYPICAL PERFORMANCE CHARACTERISTICS

Output Impedance vs Frequency



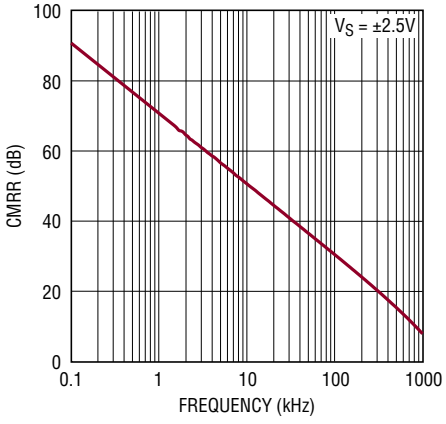
601567 G28

PSRR vs Frequency



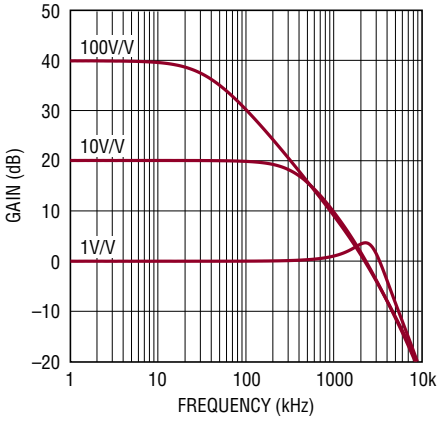
601567 G29

CMRR vs Frequency



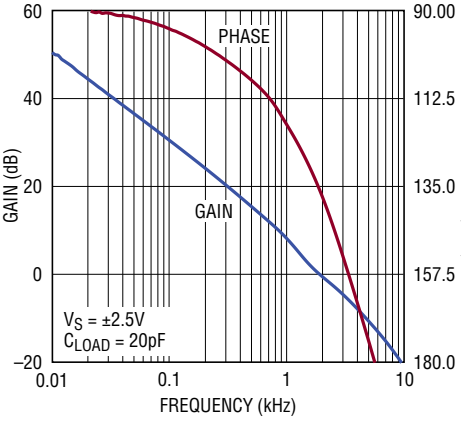
601567 G30

Closed-Loop Small Signal Frequency Response



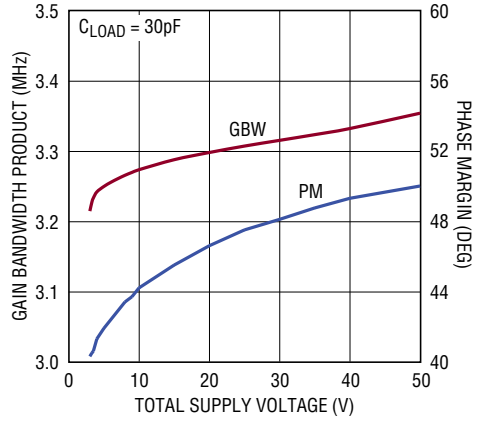
601567 G31

Gain and Phase Shift vs Frequency



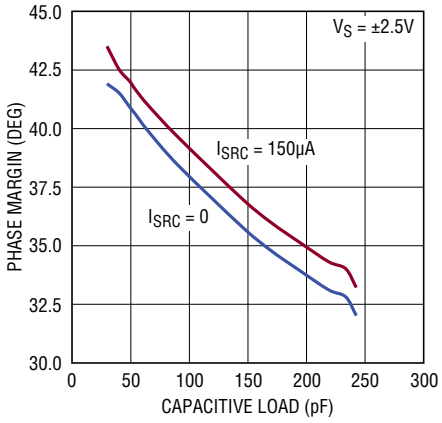
601567 G32

Gain Bandwidth Product and Phase Margin vs Supply Voltage



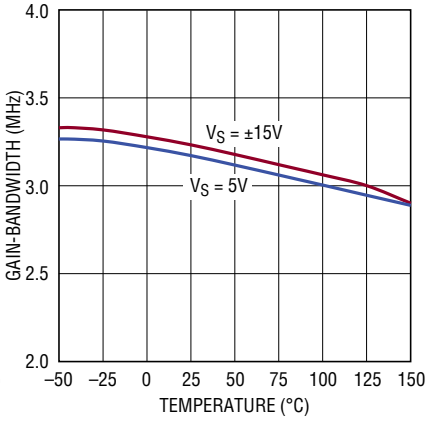
601567 G33

Phase Margin vs Capacitive Load



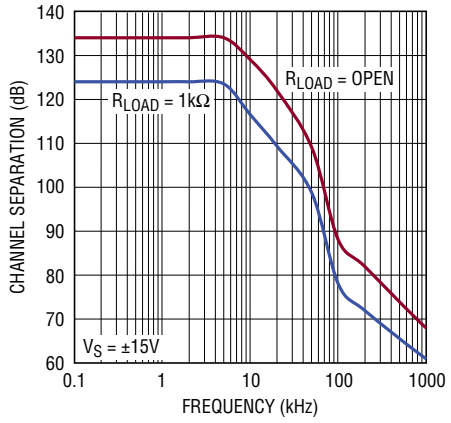
601567 G34

Gain-Bandwidth vs Temperature



601567 G35

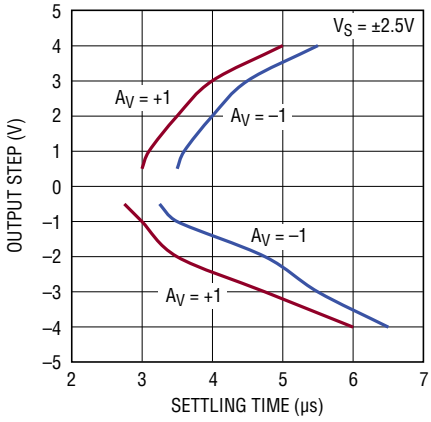
Channel Separation vs Frequency



601567 G36

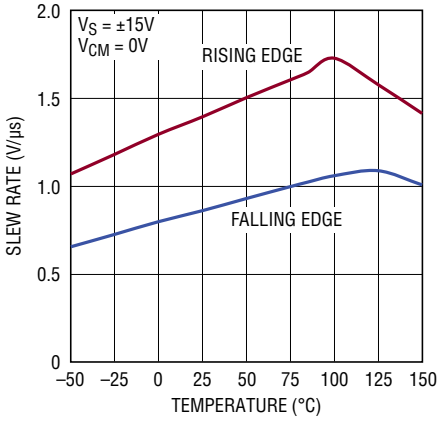
TYPICAL PERFORMANCE CHARACTERISTICS

Settling Time to 0.1% vs Output Step



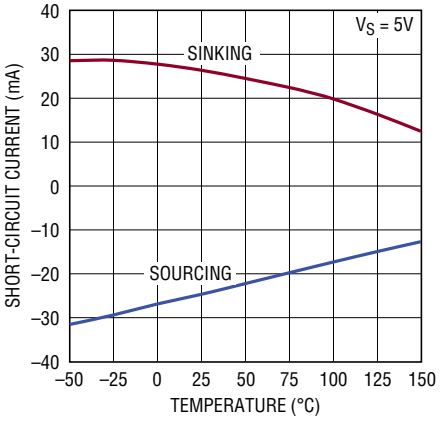
601567 G37

Slew Rate vs Temperature



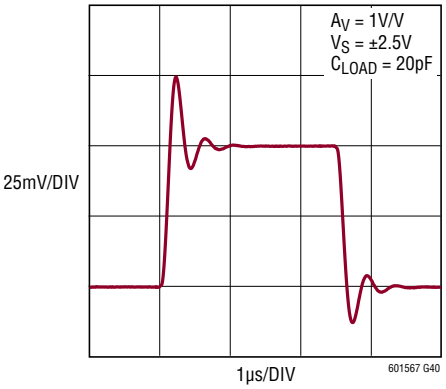
601567 G38

Short-Circuit vs Temperature



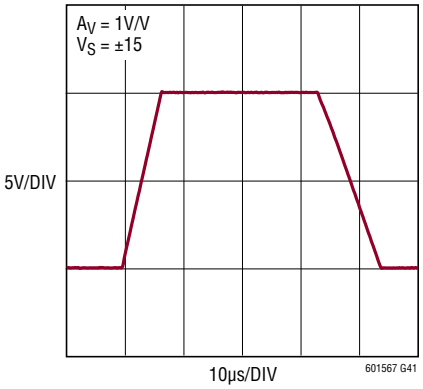
601567 G39

Small Signal Transient Response



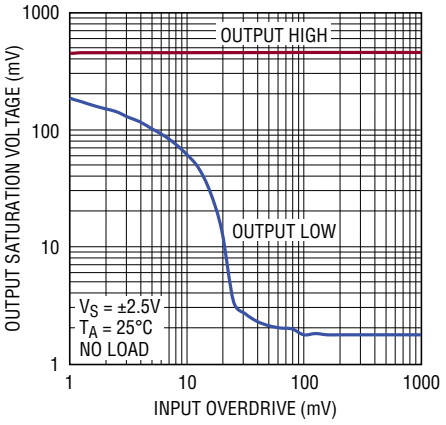
601567 G40

Large Signal Transient Response



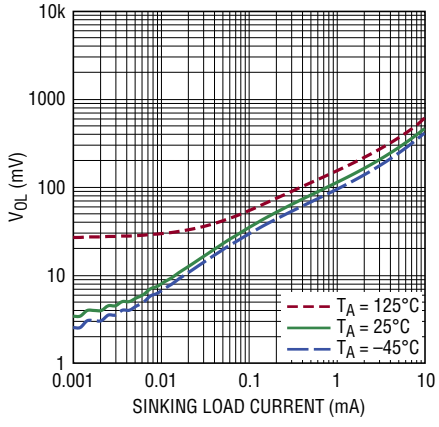
601567 G41

Output Saturation Voltage vs Input Overdrive



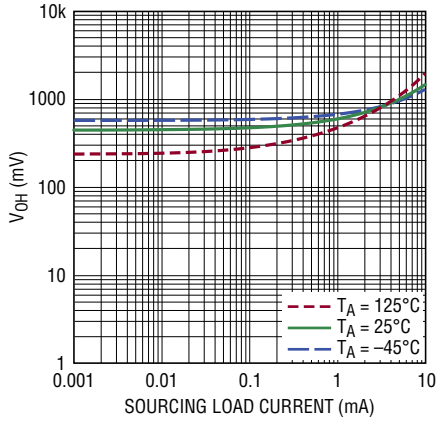
601567 G42

Output Saturation Voltage (V_{OL}) vs Load Current



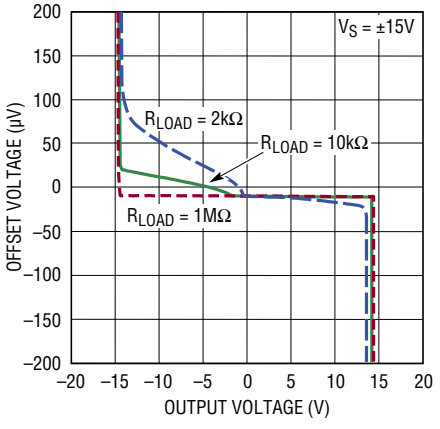
601567 G43

Output Saturation Voltage (V_{OH}) vs Load Current



601567 G44

Open-Loop Gain



601567 G45

APPLICATIONS INFORMATION

Supply Voltage

The positive supply pin of the LT6015/LT6016/LT6017 should be bypassed with a small capacitor (typically 0.1µF) as close to the supply pins as possible. When driving heavy loads an additional 4.7µF electrolytic capacitor should be added. When using split supplies, the same is true for the V^- supply pin.

The LT6017 consists of two dual amplifier dice assembled in a single DFN package which share a common substrate (V^-). While the V^- pins of the quad (pins 5 and 7) must always be tied together and to the exposed pad underneath, the V^+ power supply pins (pins 16 and 18) may be supplied independently. The B and C channel amplifiers are supplied through V^+ by pin 16, and the A and D channel amplifiers are supplied by pin 18. If pin 16 and pin 18 are not tied together and are biased independently, each V^+ pin should have their own dedicated supply bypass to ground.

Shutdown

While there are no dedicated shutdown pins for the LT6015/LT6016/LT6017, the amplifiers can effectively be shut down into a low power state by removing V^+. In this condition the input bias current is typically less than 1nA with the inputs biased between V^- and 76V above V^-, and if the inputs are taken below V^-, they appear as a diode in series with 1k of resistance. The output may be pulled up to 50V above the V^+ power supply in this condition (See Figure 1). Pulling the output pin below V^- will produce unlimited current and can damage the part.

Reverse Battery

The LT6015/LT6016/LT6017 are protected against reverse battery voltages up to 50V. In the event a reverse battery condition occurs, the supply current is typically less than 5µA (assuming the inputs are biased within a diode drop from V^-). For typical single supply applications with ground referred loads and feedback networks, no other precautions are required. If the reverse battery condition results in a negative voltage at the input pins, the current into the pin should be limited by an external resistor to less than 10mA.

Inputs

Referring to the Simplified Schematic, the LT6015/LT6016/LT6017 has two input stages: a common emitter differential input stage consisting of PNP transistors Q1 and Q2 which operate when the inputs are biased between V^- and 1.5V below V^+, and a common base input stage consisting of PNP transistors Q3 to Q6 which operate when the common mode input is biased greater than V^+ –1.5V. This results in two distinct operating regions as shown in Figure 2.

For common mode input voltages approximately 1.5V or more below the V^+ supply (Q1 and Q2 active), the common emitter PNP input stage is active and the input bias current is typically under ±2nA. When the common mode input is within approximately 1V of the V^+ supply or higher

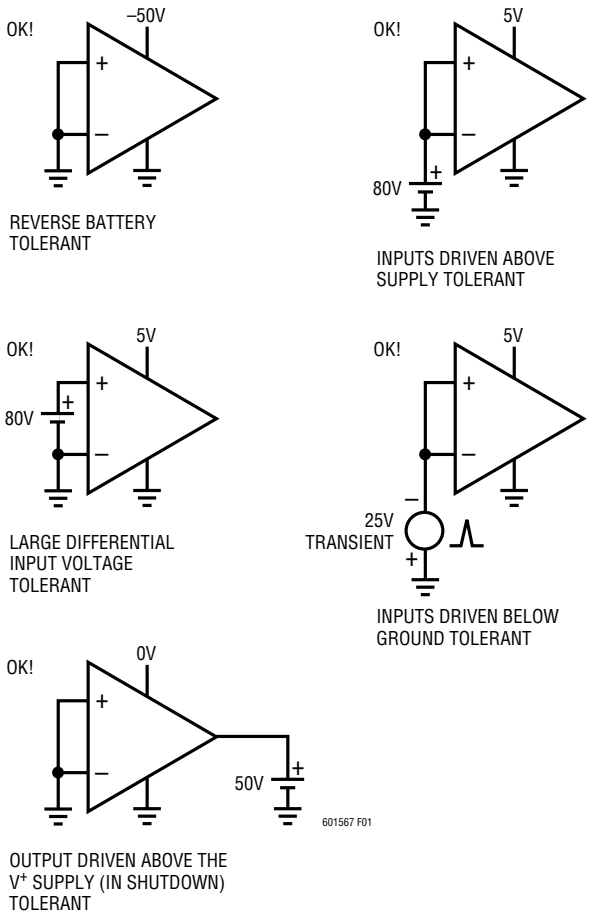


Figure 1. LT6015/LT6016/LT6017 Fault Tolerant Conditions

APPLICATIONS INFORMATION

(Over-The-Top operation), Q9 begins to turn on diverting bias current away from the common emitter differential input pair to the current mirror consisting of Q11 and Q12. The current from Q12 will bias the common base differential input pair consisting of Q3 to Q6. Because the Over-The-Top input pair is operating in a common base configuration, the input bias current will increase to about 14µA. Both input stages have their voltage offsets trimmed tightly and are specified in the Electrical Characteristics table.

The inputs are protected against temporary excursions to as much as 25V below V^- by internal 1k resistor in series with each input and a diode from the input to the negative supply. Adding additional external series resistance will extend the protection beyond 25V below V^-. The input stage of the LT6015/LT6016/LT6017 incorporates phase reversal protection to prevent the output from phase reversing for inputs below V^-.

There are no clamping diodes between the inputs. The inputs may be over-driven differentially to 80V without damage, or without drawing appreciable input current. Figure 1 summarizes the kind of faults that may be applied to the LT6015/LT6016/LT6017 without damage.

Over-The-Top Operation Considerations

When the input common mode of the LT6015/LT6016/LT6017 is biased near or above the V^+ supply, the amplifier is said to be operating in the Over-The-Top configuration. The differential input pair which control amplifier operation is common base pair Q3 to Q6 (refer to the Simplified Schematic). If the input common mode is biased between V^- and approximately 1.5V below V^+, the amplifier is said to be operating in the normal configuration. The differential input pair which control amplifier operation is common emitter pair Q1 and Q2.

A plot of the Over-The-Top Transition region vs Temperature (the region between normal operation and Over-The-Top operation) on a 5V single supply is shown in Figure 2.

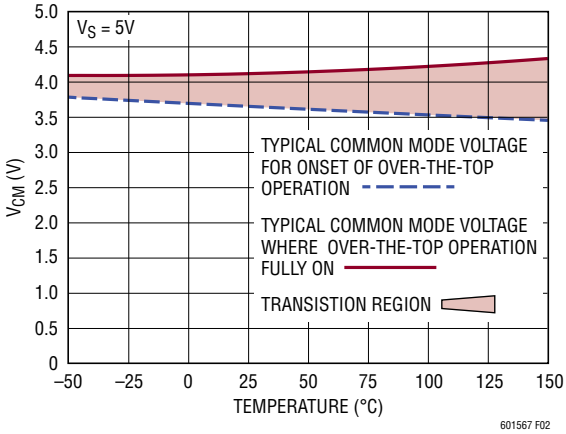


Figure 2. LT6016/LT6017 Over-The-Top Transition Region vs Temperature

Some implications should be understood about Over-The-Top operation. The first, and most obvious is the input bias currents change from under ±2nA in normal operation to 14µA in Over-The-Top operation as the input stage transitions from common emitter to common base. Even though the Over-The-Top input bias currents run around 14 µA, they are very well matched and their offset is typically under ±100nA.

The second and more subtle change to amplifier operation is the differential input impedance which decreases from 1MΩ in normal operation, to approximately 3.7kΩ in Over-The-Top operation (specified as R_{IN} in the Electrical Characteristics table). This resistance appears across the summing nodes in Over-The-Top operation and is due to the common base input stage configuration. Its value is easily derived from the specified input bias current flowing into the op amp inputs and is equal to 2 • k • T/(q • Ib) (k-Boltzmann's constant, T – operating temperature, Ib-operating input bias current of the amplifier in the Over-The-Top region). And because the inputs are biased proportional to absolute temperature, it is relatively constant with temperature. The user may think this effective resistance is relatively harmless because it appears across the summing nodes which are forced

APPLICATIONS INFORMATION

to 0V differential by feedback action of the amplifier. However, depending on the configuration of the feedback around the amplifier, this input resistance can boost noise gain, lower overall amplifier loop gain and closed loop bandwidth, raise output noise, with one benevolent effect in increasing amplifier stability.

In the normal mode of operation (where $V^- < V_{CM} < V^+ -1.5V$), R_{IN} is typically large compared to the value of the input resistor used, and R_{IN} can be ignored (refer to Figure 3). In this case the noise gain is defined by the equation:

$$\text{NOISE GAIN} \approx 1+\frac{R_F}{R_I}$$

However, when the amplifier transitions into Over-The-Top mode with the input common mode biased near or above the the V^+ supply, R_{IN} should be considered. The noise gain of the amplifier changes to:

$$\text{NOISE GAIN} = 1+\frac{R_F}{R_I \,||\, (R_{IN}+R_I \,||\, R_F)}$$

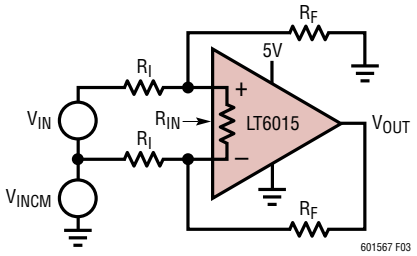


Figure 3. Difference Amplifier Configured for Both Normal and Over-The-Top Operation

While it is true that the DC closed loop gain will remain mostly unaffected ($= \frac{R_F}{R_I}$), the loop gain of the amplifier has decreased from $\frac{A_{OL}}{1+\frac{R_F}{R_I}}$ to $\frac{A_{OL}}{1+\frac{R_F}{R_I \,||\, (R_{IN}+R_I \,||\, R_F)}}$

Likewise the closed loop bandwidth of the amplifier will change going from normal mode operation to Over-The-Top operation:

Normal mode: $BW_{CLOSED-LOOP} \approx \frac{GBW}{1+\frac{R_F}{R_I}}$

Over-The-Top mode:

$$BW_{CLOSED-LOOP} \approx \frac{GBW}{1+\frac{R_F}{R_I \,||\, (R_{IN}+R_I \,||\, R_F)}}$$

And output noise is negatively impacted going from normal mode to Over-The-Top:

Normal mode: (neglecting resistor noise)

$$e_{no} \approx e_{ni} \bullet \left(1+\frac{R_F}{R_I}\right)$$

Over-The-Top mode: (neglecting resistor noise)

$$e_{no} \approx e_{ni} \bullet \left(1+\frac{R_F}{R_I \,||\, (R_{IN}+R_I \,||\, R_F)}\right)$$

Output

The output of the LT6015/LT6016/LT6017 can swing within a Schottky diode drop (~0.4V) of the V^+ supply, and within 5mV of the negative supply with no load. The output is capable of sourcing and sinking approximately 25mA.

The LT6015/LT6016/LT6017 are internally compensated to drive at least 200pF of capacitance under any output loading conditions. For larger capacitive loads, a 0.22µF capacitor in series with a 150Ω resistor between the output and ground will compensate these amplifiers to drive capacitive loads greater than 200pF.

APPLICATIONS INFORMATION

Distortion

There are two main contributors of distortion in op amps: output crossover distortion as the output transitions from sourcing to sinking current and distortion caused by nonlinear common mode rejection. If the op amp is operating in an inverting configuration there is no common mode induced distortion. If the op amp is operating in the noninverting configuration within the normal input common mode range (V^- to V^+ –1.5V) the CMRR is very good, typically over 120dB. When the LT6015/LT6016/LT6017 transitions input stages going from the normal input stage to the Over-The-Top input stage or vice-versa, there will be a significant degradation in linearity due to the change in input circuitry.

Lower load resistance increases distortion due to a net decrease in loop gain, and greater voltage swings internal to the amp necessary to drive the load, but has no effect on the input stage transition distortion. The lowest distortion can be achieved with the LT6015/LT6016/LT6017 sourcing in class-A operation in an inverting configuration, with the input common mode biased mid-way between the supplies.

Power Dissipation Considerations

Because of the ability of the LT6015/LT6016/LT6017 to operate on power supplies up to ±25V and to drive heavy loads, there is a need to ensure the die junction temperature does not exceed 150°C. The LT6015 is housed in a 5-lead TSOT-23 package (θ_{JA} = 250°C/W). The LT6016 is housed in an 8-lead MSOP package (θ_{JA} = 273°C/W). The LT6017 is housed in a 22 pin leadless DFN package (DJC22, θ_{JA} = 31.8°C/W).

In general, the die junction temperature (T_J) can be estimated from the ambient temperature T_A, and the device power dissipation P_D:

$$T_J = T_A + P_D \bullet \theta_{JA}$$

The power dissipation in the IC is a function of supply voltage and load resistance. For a given supply voltage, the worst-case power dissipation $P_{D(MAX)}$ occurs at the maximum supply current with the output voltage at half of either supply voltage (or the maximum swing is less than one-half the supply voltage). $P_{D(MAX)}$ is given by:

$$P_{D(MAX)} = (V_S \bullet I_{S(MAX)}) + (V_S/2)^2/R_{LOAD}$$

Example: An LT6016 in a MSOP package mounted on a PC board has a thermal resistance of 273°C/W. Operating on ±25V supplies with both amplifiers simultaneously driving 2.5kΩ loads, the worst-case IC power dissipation for the given load occurs when driving $12.5V_{PEAK}$ and is given by:

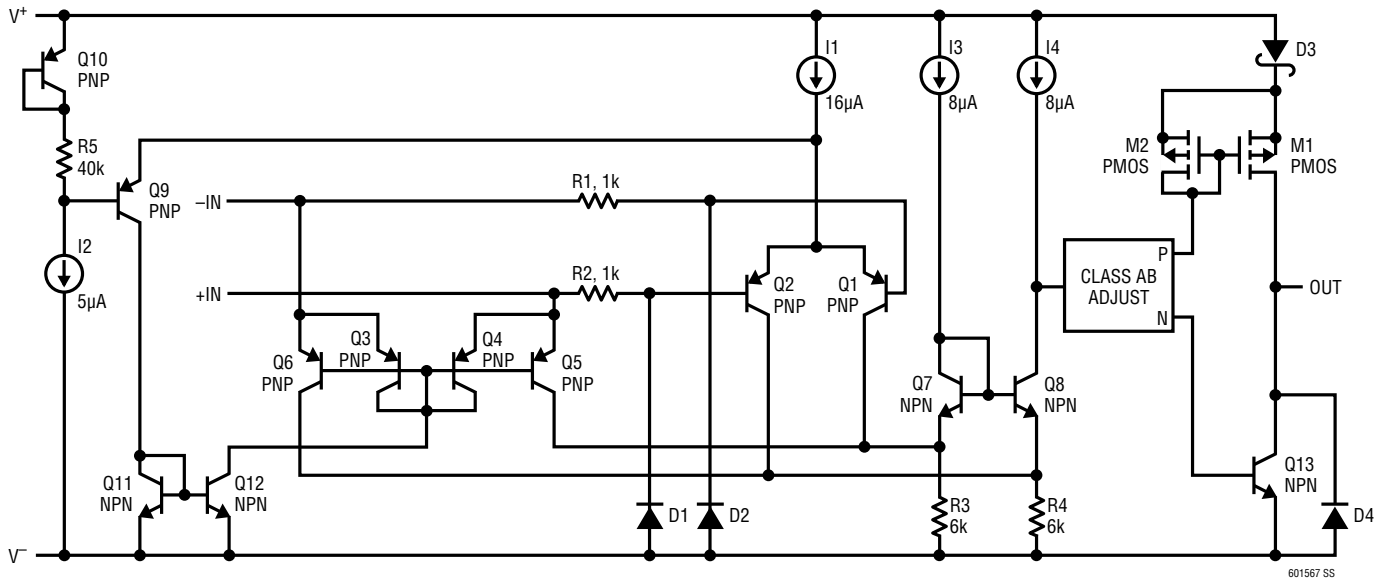
$$P_{D(MAX)} = 2 \bullet 50 \bullet 0.6mA + 2 \bullet (12.5)^2/2500 = 0.185W$$

With a thermal resistance of 273°C/W, the die temperature will experience approximately a 50°C rise above ambient. This implies the maximum ambient temperate the LT6016 should ever operate under the assumed conditions:

$$T_A = 150°C – 50°C = 100°C$$

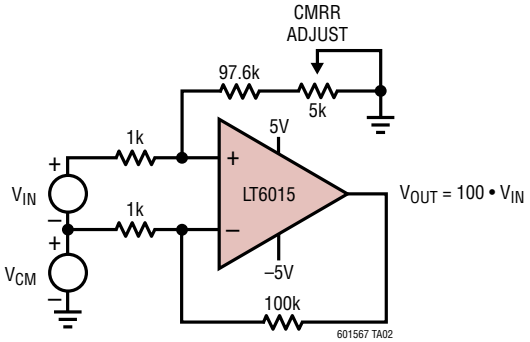
To operate to higher ambient temperatures, use two channels of the LT6017 quad which has lower thermal resistance θ_{JA} = 31.8°C/W, and an exposed pad which may be soldered down to a copper plane (connected to V^-) to further lower the thermal resistance below θ_{JA} = 31.8°C/W.

SIMPLIFIED SCHEMATIC

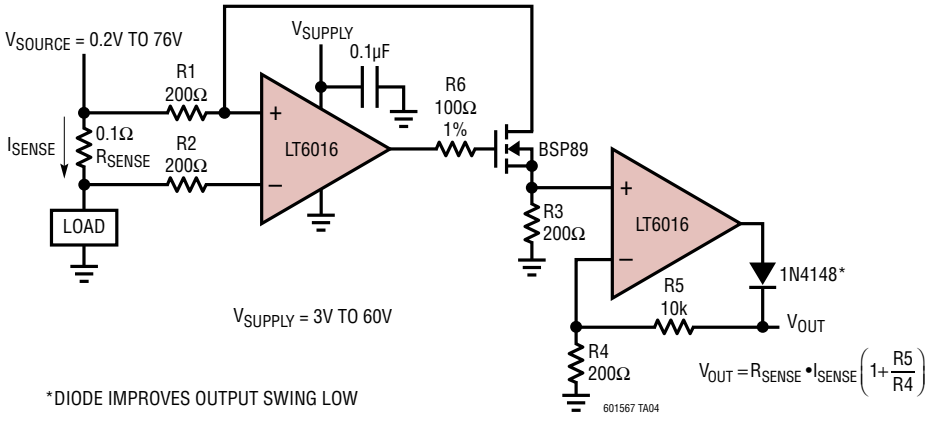


TYPICAL APPLICATIONS

Gain of 100 High Voltage Difference Amplifier with –5V/75V Common Mode Range



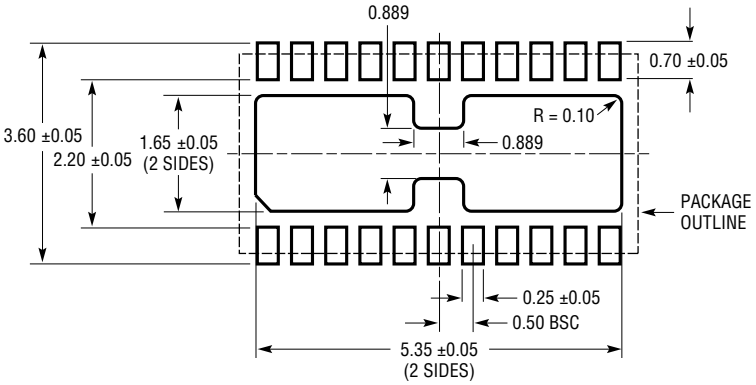
Wide Input Range Current Sense Amp Goes Hi-Z When V_{SUPPLY} Removed



PACKAGE DESCRIPTION

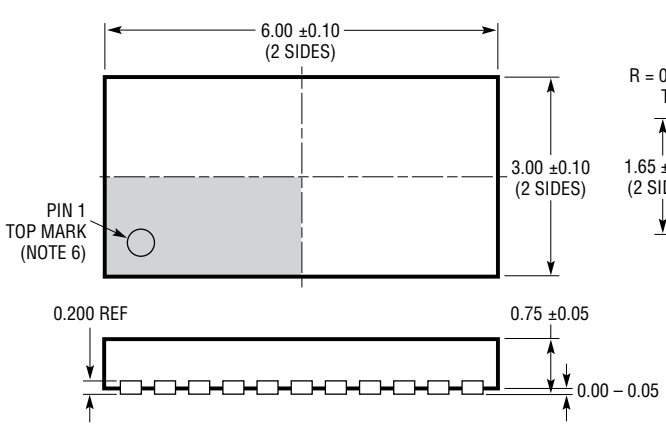
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

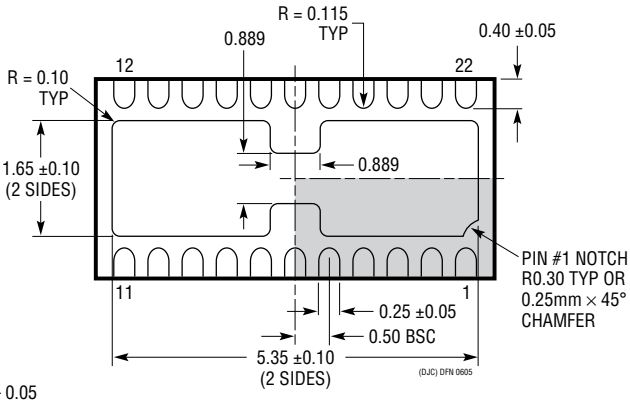
DJC Package
22-Lead Plastic DFN (6mm × 3mm)
(Reference LTC DWG # 05-08-1714 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. APPLY SOLDER MASK TO AREAS THAT
   ARE NOT SOLDERED
3. DRAWING IS NOT TO SCALE





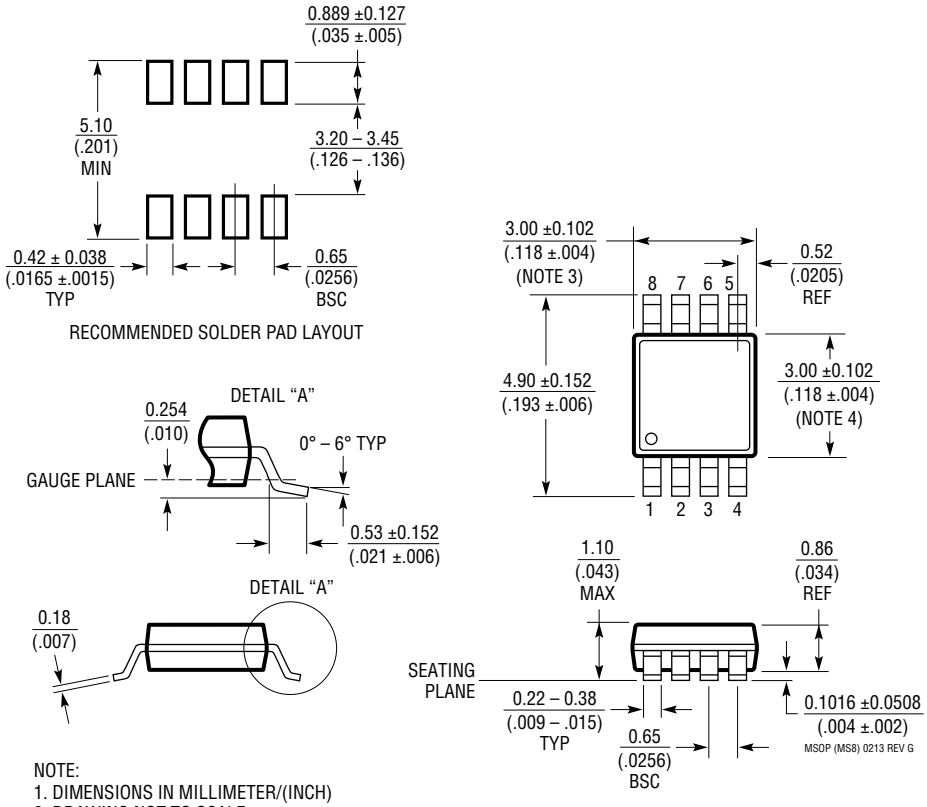
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX)
   IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)

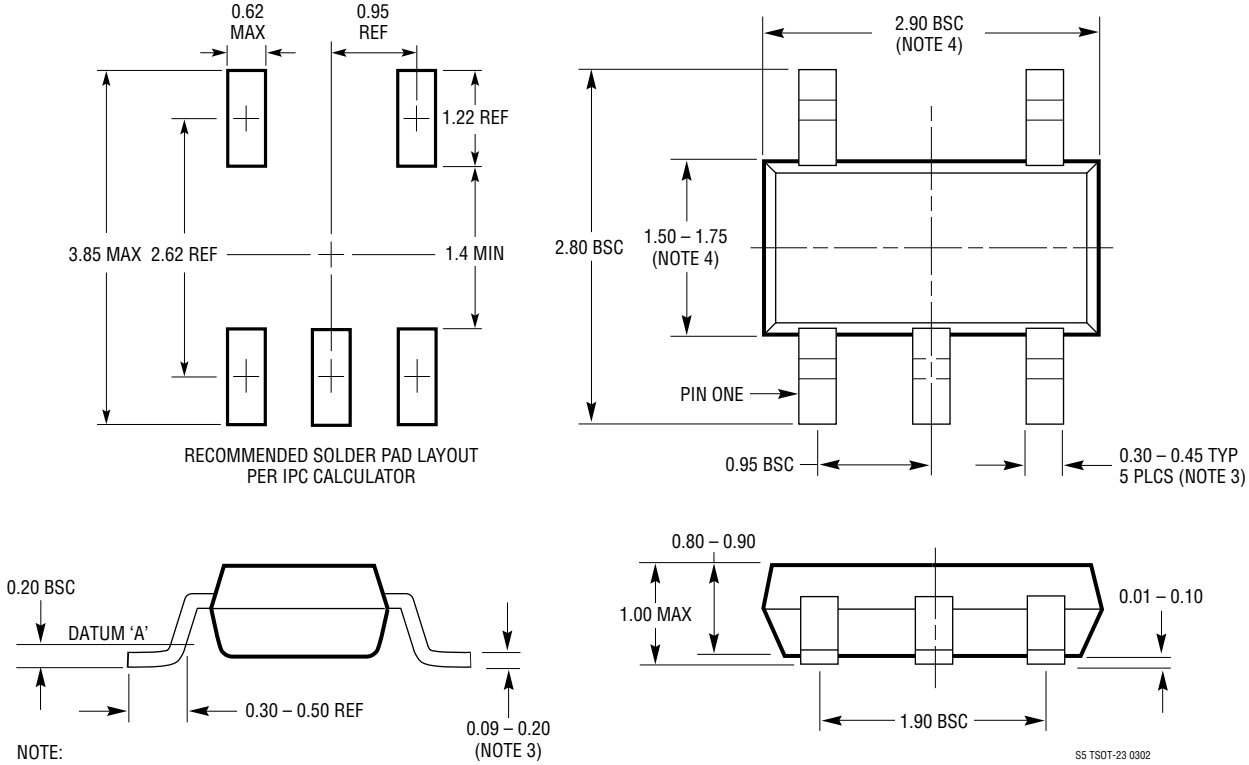


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)



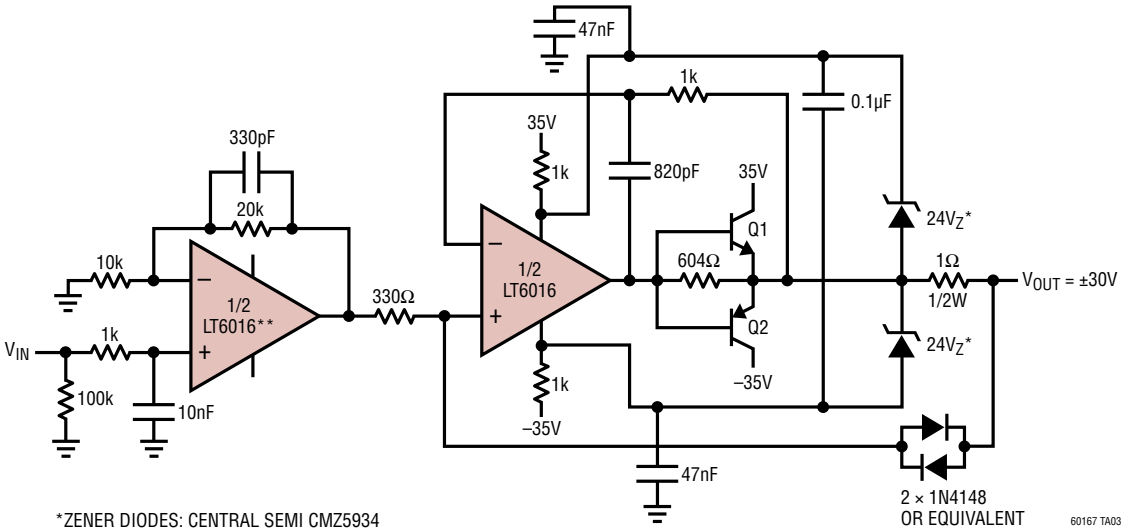
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/13	Corrected Block Diagram Q7 and Q8	17
B	06/13	Added LT6015 Single Amplifier	All
		Changed MIN I_B at V_{CM} = 0V to –60nA, changed GBW test condition to f_{TEST} = 100kHz	3-7
		Added Wide Input Range Current Sense Amp circuit	17

TYPICAL APPLICATION

Extended Supply Current Boosted Gain of Three Amplifier Drives 100Ω Load to ±30V, with 600mA Current Limit



*ZENER DIODES: CENTRAL SEMI CMZ5934
Q1, Q2: ON-SEMI D44VH10 NPN, D45VH10 PNP WITH HEAT SINK
**BOTH HALVES OF LT6016 ON SAME SUPPLY

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1490A/LT1491A	Dual and Quad Micropower Rail-to-Rail Input and Output Op amp	Over-The-Top Inputs, 50µA/Amplifier, Reverse Battery Protection to 18V
LT1638/LT1639	1.2MHz, 0.4V/µs Over-The-Top Rail-to-Rail Input and Output Op Amp	Over-The-Top Inputs, 230µA/Amplifier, 1.2MHz GBW, 0.4V/µs Slew Rate
LT1494/LT1495/LT1496	1.5µA Max, Single, Dual, and Quad, Over-The-Top Precision Rail-to-Rail Input and Output Op Amps	Over-The-Top Inputs, 1.5µA/Amplifier, 375µV Voltage Offset
LT1112/LT1114	Dual/Quad Low Power Precision, pA Input Op Amp	60µV Offset Voltage, 400µA/Amplifier
LT1013/LT1014	Dual/Quad Precision Op Amp	150µV Offset Voltage, 500µA/Amplifier