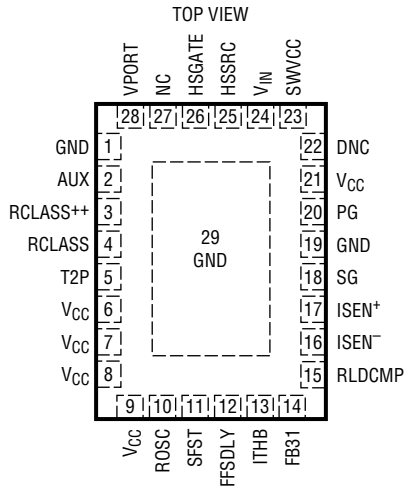
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

VPORT, HSSRC, V_{IN} Voltages ..... –0.3V to 100V
HSGATE Current..... ±20mA
V_{CC} Voltage..... –0.3V to 8V
RCLASS, RCLASS++
Voltages..... –0.3V to 8V (and ≤ VPORT)
SFST, FFSDLY, ITHB, T2P Voltages ... –0.3V to V_{CC}+0.3V
$ISEN^+$, $ISEN^-$ Voltages .....±0.3V
FB31 Voltage.....+12V/–30V
RCLASS/RCLASS++ Current ..... –50mA
AUX Current..... ±1.4mA
ROSC Current ..... ±100µA
RLDCMP Current .....±500µA
T2P Current.....–2.5mA
Operating Junction Temperature Range (Note 3)
LT4295I.....–40°C to 85°C
LT4295H .....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4295IUFD#PBF	LT4295IUFD#TRPBF	4295	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LT4295HUFD#PBF	LT4295HUFD#TRPBF	4295	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{VPORT} = V_{HSSRC} = V_{VIN} = 40V, V_{VCC} = VCCREG, ROSC, PG, and SG Open, R_{FFSDLY} = 5.23kΩ to GND. AUX connected to GND unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	VPORT, HSSRC, V_{IN} Operating Voltage	At VPORT Pin	●			60	V
V_{SIG}	VPORT Detection Signature Range	At VPORT Pin	●	1.5		10	V
V_{CLASS}	VPORT Classification Signature Range	At VPORT Pin	●	12.5		21	V
V_{MARK}	VPORT Mark Event Range	At VPORT Pin, After 1st Classification Event	●	5.6		10	V
	VPORT AUX Range	At VPORT Pin, V_{AUX} ≥ 6.45V	●	8		60	V
	Detect/Class Hysteresis Window		●	1.0			V
	Reset Threshold		●	2.6		5.6	V
V_{HSON}	Hot Swap Turn-On Voltage		●		35	37	V
V_{HSOFF}	Hot Swap Turn-Off Voltage		●	30	31		V
	Hot Swap On/Off Hysteresis Window		●	3			V
Supply Current							
	VPORT, HSSRC and V_{IN} Supply Current	V_{VPORT} = V_{HSSRC} = V_{VIN} = 60V	●			2	mA
	VPORT Supply Current During Classification	V_{VPORT} = 17.5V, RCLASS, RCLASS++ Open	●	0.7	1.0	1.3	mA
	VPORT Supply Current During Mark Event	V_{VPORT} = V_{MARK} after 1st Classification Event	●	0.4		2.2	mA
Detection and Classification Signature							
	Detection Signature Resistance	V_{SIG} (Note 4)	●	23.6	24.4	25.5	kΩ
	Resistance During Mark Event	V_{MARK} (Note 4)	●	5.2	8.3	11.4	kΩ
	RCLASS/RCLASS++ Voltage	–10mA ≥ I_{RCLASS} ≥ –36mA, V_{CLASS}	●	1.36	1.40	1.43	V
	Classification Signature Stability Time	V_{VPORT} Step GND to 17.5V, 35.7Ω from RCLASS to GND	●			2	ms
Digital Interface							
V_{AUXT}	AUX Threshold	V_{PORT} = 17.5V, V_{IN} = V_{HSSRC} = 18.5V	●	6.05	6.25	6.45	V
I_{AUXH}	AUX Pin Current	V_{AUX} = 6.05V, V_{PORT} = 17.5V, V_{IN} = 9V, V_{CC} = 0V	●	3.3	5.3	7.3	µA
	T2P Output High	V_{VCC} - V_{T2P}, –1mA Load	●			0.3	V
	T2P Leakage	V_{T2P} = 0V	●	–1		1	µA
Hot Swap Control							
I_{GPU}	HSGATE Pull Up Current	V_{HSGATE} - V_{HSSRC} = 5V (Note 5)	●	–27	–22	–18	µA
	HSGATE Voltage	–10µA Load, with Respect to HSSRC	●	10		14	V
	HSGATE Pull Down Current	V_{HSGATE} - V_{HSSRC} = 5V	●	400			µA
V_{CC} Supply							
VCCREG	V_{CC} Regulation Voltage		●	7.2	7.6	8.0	V
Feedback Amplifier							
V_{FB}	FB31 Regulation Voltage		●	3.11	3.17	3.23	V
	FB31 Pin Bias Current	RLDCMP Open			-0.1		µA
gm	Feedback Amplifier Average Trans-Conductance	Time Average, –2µA < I_{ITHB} < 2µA	●	–52	–40	–26	µA/V
I_{SINK}	ITHB Average Sink Current	Time Average, V_{FB31} = 0V	●	4.4	8.0	13.4	µA
Soft-Start							
I_{SFST}	Charging Current	V_{SFST} = 0.5V, 3.0V	●	–49	–42	–36	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{VPORT} = V_{HSSRC} = V_{VIN} = 40V, V_{VCC} = VCCREG, ROSC, PG, and SG Open, R_{FFSDLY} = 5.23kΩ to GND. AUX connected to GND unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Outputs							
	PG, SG Output High Level	I = –1mA	●	V_{CC} –0.1			V
	PG, SG Output Low Level	I = 1mA	●			1	V
	PG Rise Time, Fall Time	PG = 1000pF			15		ns
	SG Rise Time, Fall Time	SG = 400pF			15		ns
Current Sense/Overcurrent							
V_{FAULT}	Overcurrent Fault Threshold	$V_{ISEN+} – V_{ISEN–}$	●	125	140	155	mV
$\Delta V_{SENSE}/\Delta V_{ITHB}$	Current Sense Comparator Threshold with Respect to V_{ITHB}		●	–130	–111	–92	mV/V
$V_{ITHB(OS)}$	V_{ITHB} Offset		●	3.03	3.17	3.33	V
Timing							
f_{OSC}	Default Switching Frequency	ROSC Pin Open	●	200	214	223	kHz
	Switching Frequency	45.3kΩ from ROSC to GND	●	280	300	320	kHz
f_{T2P}	T2P Signal Frequency				f_{SW}/256		
	T2P Duty Cycle in PoE Operation (Note 7)	After 4-Event Classification After 5-Event Classification ($R_{CLASS++}$ Has Resistor to GND)			50 25		% %
	T2P Duty Cycle in Auxiliary Supply Operation (Note 7)	$V_{(AUX)} > V_{AUXT}$, and $R_{CLASS++}$ Has Resistor to GND			25		%
t_{MIN}	Minimum PG On Time		●	175	250	330	ns
D_{MAX}	Maximum PG Duty Cycle		●	63	66	70	%
$t_{PGDELAY}$	PG Turn-On Delay-Flyback PG Turn-On Delay-Forward	5.23kΩ from FFSDLY to GND 52.3kΩ from FFSDLY to GND 10.5kΩ from FFSDLY to V_{CC} 52.3kΩ from FFSDLY to V_{CC}			45 171 92 391		ns ns ns ns
t_{FBDLY}	Feedback Amp Enable Delay Time				350		ns
t_{FB}	Feedback Amp Sense Interval				550		ns
t_{PGSG}	PG Falling to SG Rising Delay Time-Flyback PG Falling to SG Falling Delay Time-Forward	Resistor from FFSDLY to GND 10.5kΩ from FFSDLY to V_{CC} 52.3kΩ from FFSDLY to V_{CC}			20 67 301		ns ns ns
t_{START}	Start Timer (Note 6)	Delay After Power Good	●	80	86	93	ms
t_{FAULT}	Fault Timer (Note 6)	Delay After Overcurrent Fault	●	80	86	93	ms
I_{MPS}	MPS Current		●	10	12	14	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All voltages with respect to GND unless otherwise noted. Positive currents are into pins; negative currents are out of pins unless otherwise noted.

Note 3. This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature can exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4. Detection signature resistance specifications do not include resistance added by the external diode bridge which can add as much as 1.1kΩ to the port resistance.

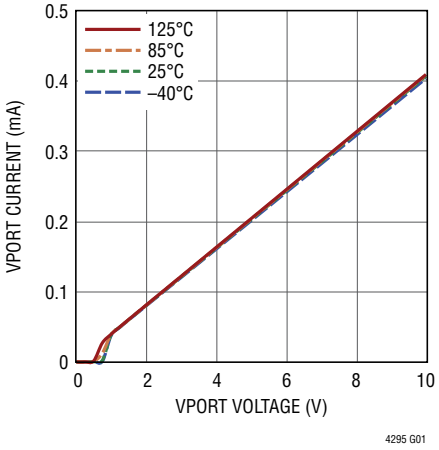
Note 5. I_{GPU} available in PoE powered operation. That is, available after $V_{(VPORT)} > V_{HSON}$ and $V_{(AUX)} < V_{AUXT}$, over the range where $V_{(VPORT)}$ is between V_{HSOFF} and 60V.

Note 6. Guaranteed by design, not subject to test.

Note 7. Specified as the percentage of the period which T2P is low impedance with respect to V_{CC}.

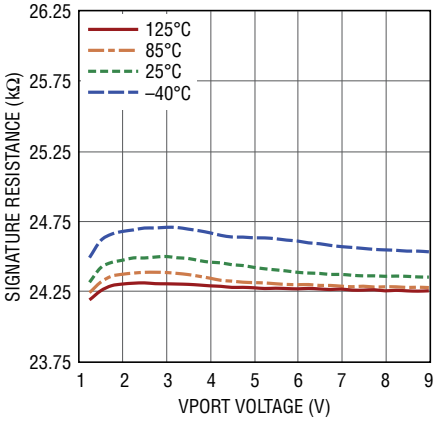
TYPICAL PERFORMANCE CHARACTERISTICS

Input Current vs Input Voltage 25k Detection Signature Range



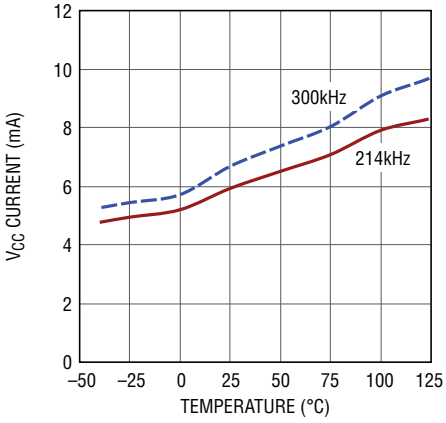
4295 G01

Detection Signature Resistance vs Input Voltage



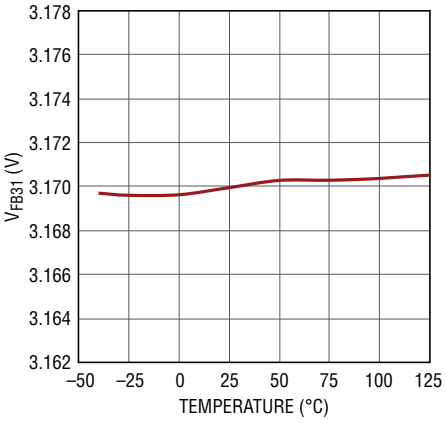
4295 G02

V_{CC} Current vs Temperature



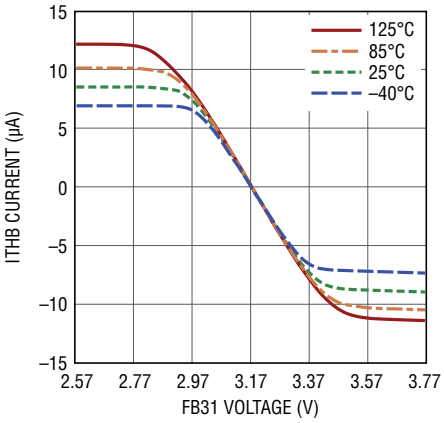
4295 G03

V_{FB31} vs Temperature



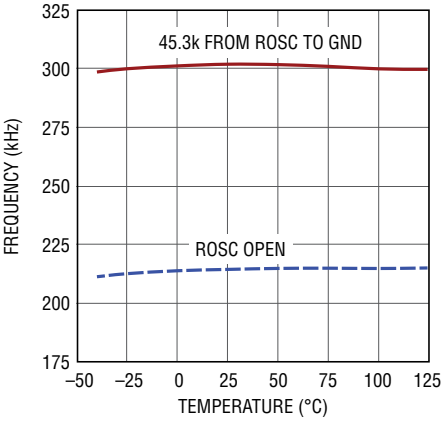
4295 G04

Feedback Amplifier Output Current vs V_{FB31}



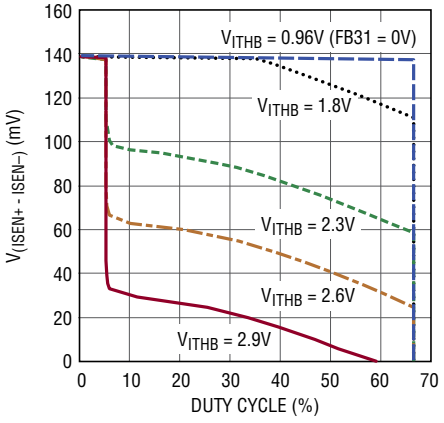
4295 G05

Switching Frequency vs Temperature



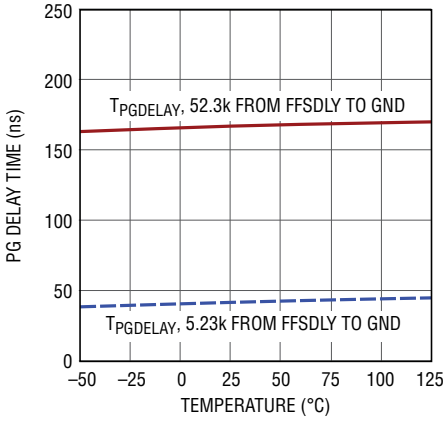
4295 G06

Current Sense Voltage vs Duty Cycle, I_{THB}



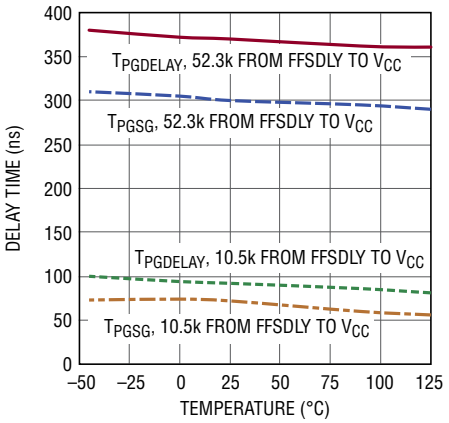
4295 G07

PG Delay Time vs Temperature in Flyback Mode



4295 G08

PG, SG Delay Time vs Temperature in Forward Mode



4295 G09

PIN FUNCTIONS

GND(Pins 1, 19, Exposed Pad Pin 29): Device Ground. Exposed Pad must be electrically and thermally connected to pins 1, 19 and PCB GND.

AUX (Pin 2): Auxiliary Sense. Assert AUX via a resistive divider from the auxiliary power input to set the voltage at which the auxiliary supply takes over. Asserting AUX pulls down HSGATE, disconnects the detection signature resistor and disables classification signature. The AUX pin sinks I_{AUXH} when below its threshold voltage, of V_{AUXT}, to provide hysteresis. Connect to GND if not used.

RCLASS++ (Pin 3): Class Select Input. Connect a resistor between RCLASS++ to GND per Table 1.

RCLASS (Pin 4): Class Select Input. Connect a resistor between RCLASS and GND per Table 1.

T2P (Pin 5): PSE Type Indicator. Open drain with respect to V_{CC}. See the T2P Output section for pin behavior.

V_{CC} (Pins 6, 7, 8, 9, 21): Switching Regulator Controller Supply Voltage. Connect a local ceramic capacitor from V_{CC} pin 21 to GND pin 19 as close as possible to LT4295 as shown in Table 3.

ROSC (Pin 10): Programmable Frequency Adjustment. Resistor to GND programs operating frequency. Leave open for default frequency of 214kHz.

SFST (Pin 11): Soft-Start. Capacitor to GND sets soft-start timing.

FFSDLY (Pin 12): Forward/Flyback Select and Primary Gate Delay Adjustment. Resistor to GND adjusts gate drive delay for a flyback topology. Resistor to V_{CC} adjusts gate drive delay for a forward topology.

ITHB (Pin 13): Current Threshold Control. The voltage on this pin corresponds to the peak current of the external primary FET. Note that the voltage gain from ITHB to the input of the current sense comparator (V_{SENSE}) is negative.

FB31 (Pin 14): Feedback Input. In flyback mode, connect external resistive divider from the third winding feedback. Reference voltage is 3.17V. Connect to GND in forward mode.

RLDCMP (Pin 15): Load Compensation Adjustment. Optional resistor to GND controls output voltage set point as a function of peak switching current. Leave RLDCMP open if load compensation is not needed.

$ISEN^-$ (Pin 16): Current Sense, Negative Input. Route as a dedicated trace to the return side of the current sense resistor.

$ISEN^+$ (Pin 17): Current Sense, Positive Input. Route as a dedicated trace to the sense side of the current sense resistor.

SG (Pin 18): Secondary (Synchronous) Gate Drive Output.

PG (Pin 20): Primary Gate Drive Output.

DNC (Pin 22): Do Not Connect. Leave pin open.

SWVCC (Pin 23): Switch Driver for V_{CC}'s Buck Regulator. This pin drives the base of a PNP in a buck regulator to generate V_{CC}.

V_{IN} (Pin 24): Buck Regulator Supply Voltage. Usually separated from HSSRC by a pi filter.

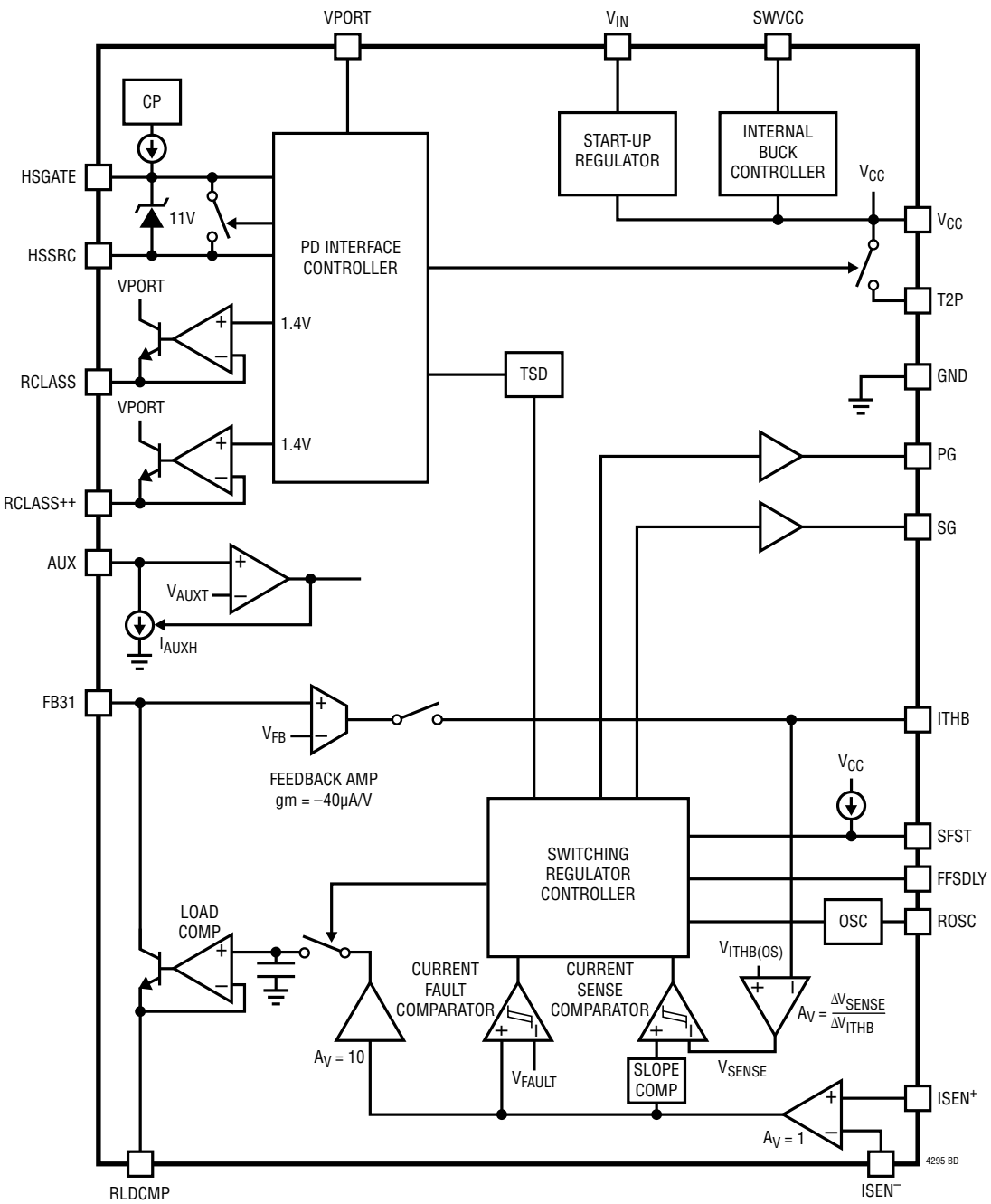
HSSRC (Pin 25): External Hot Swap MOSFET Source. Connect to source of the external MOSFET.

HSGATE (Pin 26): External Hot Swap MOSFET Gate Control Output. Capacitance to GND determines inrush time.

NC (Pin 27): No Connection. Not internally connected.

VPORT (Pin 28): PD Interface Supply Voltage and External Hot Swap MOSFET Drain Connection.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet (PoE) continues to gain popularity as products take advantage of the combination of DC power and high speed data available from a single RJ45 connector. The LT4295 is IEEE 802.3bt-compliant and allows up to 71.3 Watt operation while maintaining backwards compatibility with existing PSE systems. The LT4295 combines a PoE PD interface controller and a switching regulator controller capable of either flyback or forward isolated power supply operation.

SIGNIFICANT DIFFERENCES FROM PREVIOUS PRODUCTS

The LT4295 has several significant differences from previous Analog Devices products. These differences are briefly summarized below.

IEEE 802.3bt vs LTPoE++ Available PD Power

The LT4295 supports IEEE 802.3bt PD power levels up to 71.3 Watts. A PD requiring more than 71.3 Watts is beyond the allowable power levels of IEEE 802.3bt.

The LT4293, LT4275A and LT4276A are available to support PD power levels up to 90W under the LTPoE++ standard. See the Related Parts section for a list of LTPoE++ PSEs and PDs.

ITHB Is Inverted from the Usual ITH pin

The ITHB pin voltage has an inverse relationship to the current sense comparator threshold, V_{SENSE}. Furthermore, the ITHB pin offset voltage, $V_{ITHB(OS)}$, is 3.17V. See Figure 1.

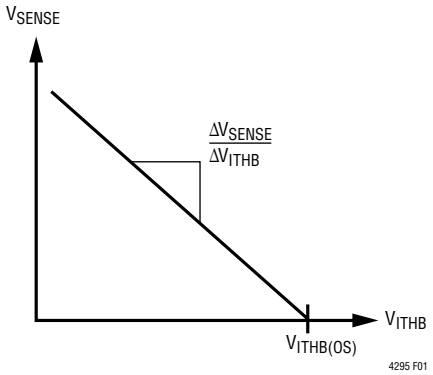


Figure 1. V_{SENSE} vs. V_{ITHB}

Duty-Cycle Based Soft-Start

The LT4295 uses a duty cycle ramp soft-start that injects charge into ITHB. This allows startup without appreciable overshoot using inexpensive external components.

The Feedback Pin FB31 is 3.17V Rather Than 1.25V

The error amp feedback voltage V_{FB} is 3.17V.

Flyback/Forward Mode Is Pin Selectable

The LT4295 operates in flyback mode if FFSDLY is pulled down by a resistor to GND. It operates in forward mode if FFSDLY is pulled up by a resistor to V_{CC}. The value of this resistor determines the $t_{PGDELAY}$ and t_{PGSG}.

T2P Pin Response

The T2P pin outputs high impedance to V_{CC}, low impedance to V_{CC}, 50% duty cycle, or 25% duty cycle, responsive to the number of class/mark event and responsive to

Table 1. Single-Signature Classification, Power Levels and Resistor Selection

PD REQUESTED CLASS	PD REQUESTED POWER	PD TYPE	NOMINAL CLASS CURRENT	RESISTOR (1%)	
				R_{CLS}	R_{CLS}++
0	13W	Type 1	2.5mA	1.00kΩ	Open
1	3.84W	Type 1 or 3	10.5mA	150Ω	Open
2	6.49W	Type 1 or 3	18.5mA	80.6Ω	Open
3	13W	Type 1 or 3	28mA	52.3Ω	Open
4	25.5W	Type 2 or 3	40mA	35.7Ω	Open
5	40W	Type 3	40mA/2.5mA	1.00kΩ	37.4Ω
6	51W	Type 3	40mA/10.5mA	150Ω	47.5Ω
7	62W	Type 4	40mA/18.5mA	80.6Ω	64.9Ω
8	71.3W	Type 4	40mA/28mA	52.3Ω	118Ω

APPLICATIONS INFORMATION

PoE or auxiliary power operation. See T2P Output section in the Applications Information.

V_{CC} Is Powered by Internally Driven Buck Regulator

The LT4295 includes a buck regulator controller that must be used to generate the V_{CC} supply voltage.

POE MODES OF OPERATION

The LT4295 has several modes of operation, depending on the input voltage sequence applied to the VPORT pin.

Detection Signature

During detection, the PSE looks for a 25kΩ detection signature resistor which identifies the device as a PD. The LT4295 detection signature resistor is smaller than 25k to compensate for the additional series resistance introduced by the IEEE required diode bridge or the LT4321-based ideal diode bridge.

IEEE 802.3bt Single-Signature vs Dual-Signature PDs

IEEE 802.3bt defines two PD topologies: single-signature and dual-signature. The LT4295 primarily targets single-signature PD topologies, eliminating the need for a second PD controller. All PD descriptions and IEEE 802.3 standard references in this data sheet are limited in scope to single-signature PDs.

The LT4295 may be deployed in dual-signature PD applications. For more information, contact Analog Devices Applications.

Classification Signature and Mark

The class/mark process varies depending on the PSE type. A PSE, after a successful detection, may apply a classification probe voltage of 15.5V to 20.5V and measure the PD classification signature current. Once the PSE applies a classification probe voltage, the PSE returns the PD voltage into the mark voltage range before applying another classification probe voltage, or powering up the PD.

An example of 1-Event classification is shown in Figure 2. In 2-Event classification, a PSE probes for power classification twice as shown in Figure 3. An IEEE 802.3bt PSE may apply as many as 5 events before powering up the PD.

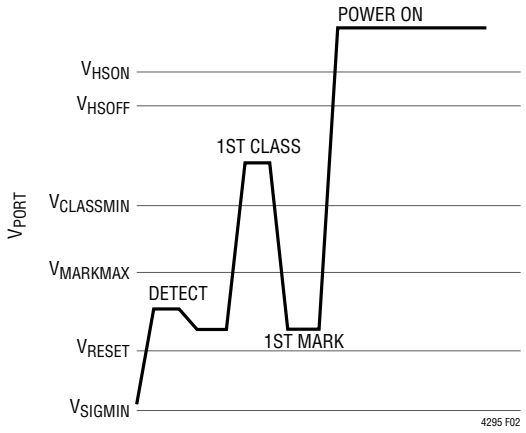


Figure 2. Type 3 or Type 4 PSE, 1-Event Class Sequence

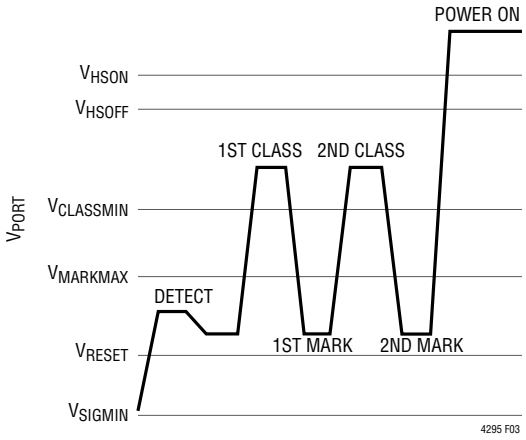


Figure 3. Type 2 PSE, 2-Event Class Sequence

IEEE 802.3bt Physical Classification and Demotion

IEEE 802.3bt defines physical classification to allow a PD to request a power allocation from the connected PSE and to allow the PSE to inform the PD of the PSE's available power. Demotion is provided if the PD Requested Power level is not available at the PSE. If demoted, the PD must operate in a lower power state.

IEEE 802.3bt provides nine PD classes and four PD types, as shown in Table 1. The LT4295 class is configured by setting the R_{CLS} and R_{CLS}++ resistor values.

The number of class/mark events issued by the PSE directly indicates the power allocated to the PD and is summarized in Table 2.

APPLICATIONS INFORMATION

Table 2. PSE Allocated Power

PD REQUESTED CLASS	NUMBER OF PSE CLASS/MARK EVENTS				
	1	2	3	4	5
0	13W				
1	3.84W				
2	6.49W				
3	13W				
4	**13W**	25.5W			
5	**13W**	**25.5W**		40W	
6	**13W**	**25.5W**		51W	
7	**13W**	**25.5W**		**51W**	62W
8	**13W**	**25.5W**		**51W**	71.3W

Note: Bold indicates the PD has been demoted.

IEEE 802.3bt PSEs present a single classification event (see Figure 2) to Class 0 through 3 PDs. A Class 0 through 3 PD presents its class signature to the PSE and is then powered on if sufficient power is available. Power limited IEEE 802.3bt PSEs may issue a single event to Class 4 and higher PDs in order to demote those PDs to Class 3 (13W).

IEEE 802.3bt PSEs present up to three classification events depending on type to Class 4 PDs (see Figure 4). Class 4 PDs present a class signature 4 on all events. This third event differentiates a Class 4 PD from a higher class PD. Power limited IEEE 802.3bt PSEs may issue three events to Class 5 and higher PDs in order to demote those PDs to Class 4 (25.5W).

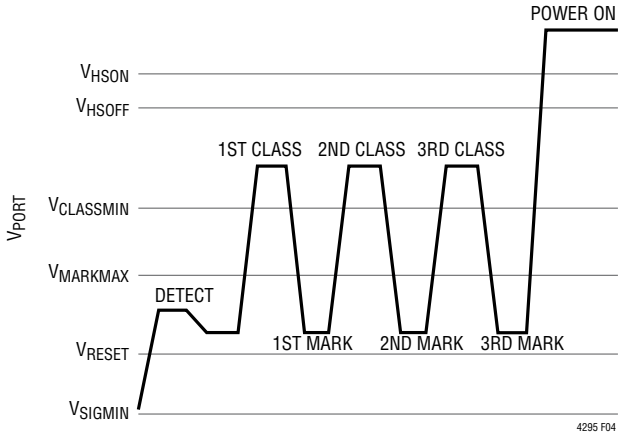


Figure 4. Type 3 or Type 4 PSE, 3-Event Class Sequence

IEEE 802.3bt PSEs present four classification events (see Figure 5) to Class 5 and 6 PDs. Class 5 and 6 PDs present a class signature 4 on the first two events. Class 5 and 6 PDs present a class signature 0 or 1, respectively, on the remaining events. Power limited IEEE 802.3bt PSEs may issue four events to Class 7 and higher PDs in order to demote those PDs to Class 6 (51W).

IEEE 802.3bt PSEs present five classification events (see Figure 6) to Class 7 and 8 PDs. Class 7 and 8 PDs present a class signature 4 on the first two events. Class 7 and 8 PDs present a class signature 2 or 3 respectively, on the remaining events.

The PD must monitor the number of classification/mark events, which is communicated through the LT4295 T2P pin.

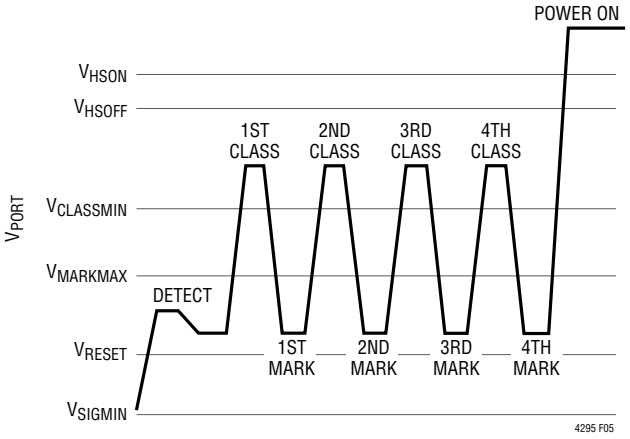


Figure 5. Type 3 or Type 4 PSE, 4-Event Class Sequence

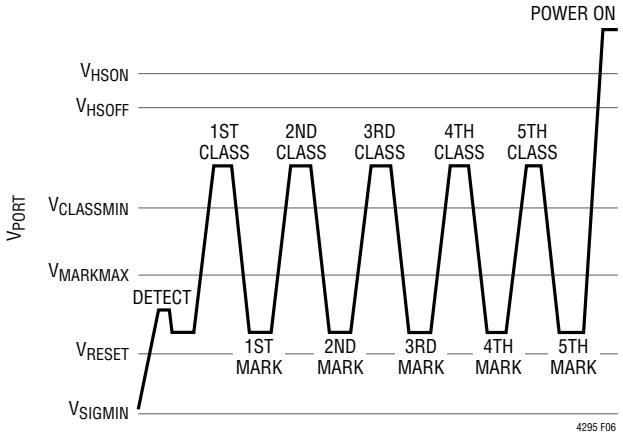


Figure 6. Type 4 PSE, 5-Event Class Sequence

APPLICATIONS INFORMATION

Classification Resistors (R_{CLS} and R_{CLS++})

The R_{CLS} and R_{CLS++} resistors set the classification currents corresponding to the PD power classification. Select the value of R_{CLS} and R_{CLS++} from Table 1 and connect the 1% resistor between the RCLASS, RCLASS++ pin and GND.

Detection Signature Corrupt During Mark Event

During the mark event, the LT4295 presents <11kΩ to the port as required by the IEEE 802.3 specification.

Inrush and Powered On

After the PSE detects and optionally classifies the PD, the PSE then powers on the PD. When the PD port voltage rises above the V_{HSON} threshold, it begins to source I_{GPU} out of the HSGATE pin. This current flows into an external capacitor C_{GATE} in Figure 7 and causes a voltage to ramp up the gate of the external MOSFET. The external MOSFET acts as a source follower and ramps the voltage up on the output bulk capacitor, C_{PORT}, thereby determining the inrush current, I_{INRUSH}. Design I_{INRUSH} to be ~100mA.

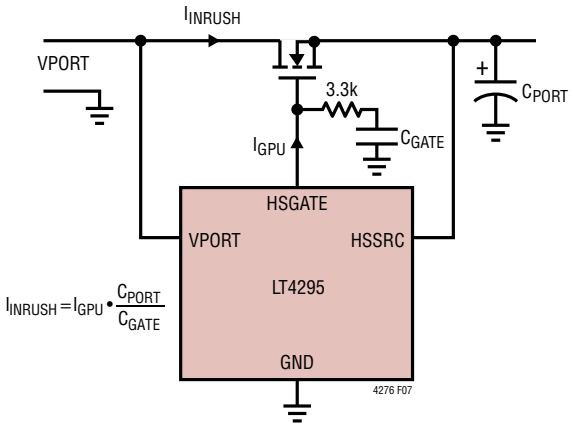


Figure 7. Programming I_{INRUSH}

The LT4295 internal charge pump enables an N-channel MOSFET solution, replacing a larger and more costly P-channel FET. The low $R_{DS(ON)}$ MOSFET also maximizes power delivery and efficiency, reduces power and heat dissipation, and eases thermal design.

DELAY START

After the HSGATE charges up to approximately 7V above HSSRC, fully enhancing the external hot swap MOSFET, the switching regulator controller operates after a delay of t_{START}.

EXTERNAL V_{CC} SUPPLY

The external V_{CC} supply must be configured as a buck regulator shown in Figure 8. To optimize the buck regulator, use the external component values in Table 3 corresponding to the V_{IN} operating range. This buck regulator runs in discontinuous mode with the inductor peak current considerably higher than average load current on V_{CC}. Thus, the saturation current rating of the inductor must exceed the values shown in Table 3. Place the capacitor, C, as close as possible to V_{CC} pin 21 and GND pin 19. For optimal performance, place these components as close as possible to the LT4295.

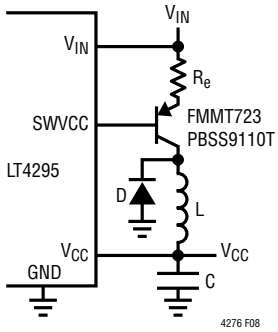


Figure 8. V_{CC} Buck Regulator

Table 3. Buck Regulator Component Selection

V_{IN}	C	L	I_{SAT}	R_e	D
9V-57V	22µF	22µH	≥1.2A	1Ω	Schottky
PoE	10µF	100µH	≥300mA	20Ω	Ultrafast Diode

AUXILIARY SUPPLY OVERRIDE

If the AUX pin is held above V_{AUXT}, the LT4295 enters auxiliary power operation. In this mode the detection signature resistor is disconnected, classification is disabled, and HSGATE is pulled down.

The AUX pin allows for setting the auxiliary supply turn on (V_{AUXON}) and turn off (V_{AUXOFF}) voltage thresholds. The auxiliary supply hysteresis voltage, V_{AUXHYS}, is set by sinking current, I_{AUXH}, only when the AUX pin voltage is less than V_{AUXT}. Use the following equations to set

APPLICATIONS INFORMATION

V_{AUXON} and V_{AUXOFF} via R1 and R2 in Figure 9. Note that an internal 6.5V Zener limits the voltage on the AUX pin.

A capacitor up to 1000pF may be placed between the AUX pin and GND to improve noise immunity. V_{AUXON} must be lower than V_{HSOFF}.

$$R1 = \frac{V_{AUXON} - V_{AUXOFF}}{I_{AUXH}} = \frac{V_{AUXHYS}}{I_{AUXH}}$$

$$R2 = \frac{R1}{\left(\frac{V_{AUXOFF}}{V_{AUXT}} - 1\right)}$$

$$R1 \geq \frac{V_{AUX(MAX)} - V_{AUXT}}{1.4mA}$$

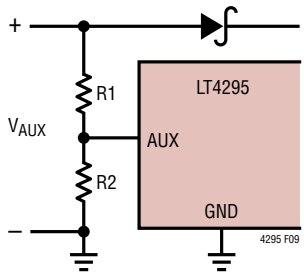


Figure 9. AUX Threshold and Hysteresis Calculation

T2P Output

The LT4295 communicates the PSE allocated power to the PD application via the T2P pin. The T2P pin state is determined by the AUX pin, the R_{CLASS}++ pin, and the number of classification events. The LT4295 uses a 4-state encoding for the T2P output. T2P state and the associated PSE allocated power are shown in Table 4.

The highest priority input is the AUX pin. AUX is asserted to enter the auxiliary power state and deasserted to enter the PoE state. In the auxiliary power state, the T2P pin indicates the highest available power, based on PD Requested Class. The auxiliary power supply must be sized to provide at least the PD Requested Power.

Second, PD Requested Class and PD Requested Power are configured using the R_{CLASS} and R_{CLASS}++ pins. The R_{CLASS}++ pin alone can be used to determine if the PD Class is 0–4 or 5–8, as shown in Table 1.

Last, the number of classification events determines the amount of power allocated by the PSE as described in Table 2.

Table 4. T2P Response to Determine PSE Allocated Power

STATE	PD REQUESTED CLASS	NUMBER OF CLASSIFICATION EVENTS	T2P*	PSE ALLOCATED POWER
Auxiliary	0–4	N/A	Low-Z	Aux. Power
	5-8	N/A	25%	Aux. Power
PoE	0–4	1	Hi-Z	Min (PD Requested Power, 13W)
		≥ 2	Low-Z	25.5W
	5–8	1	Hi-Z	13W
		2 or 3	Low-Z	25.5W
		4	50%	Min (PD Requested Power, 51W)
		5	25%	Min (PD Requested Power, 71.3W)

* Specified as the percentage of the period which T2P is low impedance with respect to V_{CC}.

Interoperability Across Various PSEs and Auxiliary Power Source

Table 5 summarizes the expected T2P response, the PSE allocated power, and the number of classification events. The result is a function of PD Requested Class and power source—Auxiliary or PoE.

SWITCHING REGULATOR CONTROLLER OPERATION

The switching regulator controller portion of the LT4295 is a current mode controller capable of implementing either a flyback or a forward power supply. When used in flyback mode, no opto-isolator is required for feedback because the output voltage is sensed via the transformer's third winding.

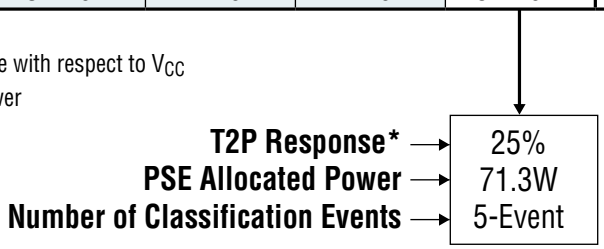
Table 5. LT4295 Interoperability {T2P Response*, PSE Allocated Power, Number of Classification Events}

PD REQUESTED CLASS (PD REQUESTED POWER)	PSE TYPE, CLASS (POWER)							AUXILIARY POWER SOURCE**
	IEEE 802.3 Type 1	IEEE 802.3 Type 2	IEEE 802.3 Type 3			IEEE 802.3 Type 4		
	Class 3 (13W)	Class 4 (25.5W)	Class 4 (25.5W)	Class 5 (40W)	Class 6 (51W)	Class 7 (62W)	Class 8 (71.3W)	
Class 0-3 (up to 13W)	Hi-Z up to 13W 1-Event	Hi-Z up to 13W 1-Event	Hi-Z up to 13W 1-Event	Hi-Z up to 13W 1-Event	Hi-Z up to 13W 1-Event	Hi-Z up to 13W 1-Event	Hi-Z up to 13W 1-Event	Low-Z Aux. Power N/A
Class 4 (25.5W)	Hi-Z 13W 1-Event	Low-Z 25.5W 2-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	Low-Z Aux. Power N/A
Class 5 (40W)	Hi-Z 13W 1-Event	Low-Z 25.5W 2-Event	Low-Z 25.5W 3-Event	50% 40W 4-Event	50% 40W 4-Event	50% 40W 4-Event	50% 40W 4-Event	25% Aux. Power N/A
Class 6 (51W)	Hi-Z 13W 1-Event	Low-Z 25.5W 2-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	50% 51W 4-Event	50% 51W 4-Event	50% 51W 4-Event	25% Aux. Power N/A
Class 7 (62W)	Hi-Z 13W 1-Event	Low-Z 25.5W 2-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	50% 51W 4-Event	25% 62W 5-Event	25% 62W 5-Event	25% Aux. Power N/A
Class 8 (71.3W)	Hi-Z 13W 1-Event	Low-Z 25.5W 2-Event	Low-Z 25.5W 3-Event	Low-Z 25.5W 3-Event	50% 51W 4-Event	50% 51W 4-Event	25% 71.3W 5-Event	25% Aux. Power N/A

Note 1. Shade of blue indicates the PD has been demoted

* Specified as the percentage of the period which T2P is low impedance with respect to V_{CC}

** Auxiliary Power Supply must be sized to provide PD Requested Power



APPLICATIONS INFORMATION

Flyback Mode

The LT4295 is programmed into flyback mode by placing a resistor R_{FFSDLY} from the FFSDLY pin to GND. This resistor must be in the range of 5.23kΩ to 52.3kΩ. If using a potentiometer to adjust R_{FFSDLY}, ensure the adjustment of the potentiometer does not exceed 52.3kΩ.The value of R_{FFSDLY} determines $t_{PGDELAY}$ according to the following equations:

$$t_{PGDELAY} \approx 2.69ns / k\Omega \bullet R_{FFSDLY} + 30ns$$

$$t_{PGSG} \approx 20ns$$

The SG pin must be connected to the secondary side MOSFET through a gate drive transformer as shown in Figure 11. Add a Schottky diode from PG to GND as shown in Figure 11 to prevent PG from going negative.

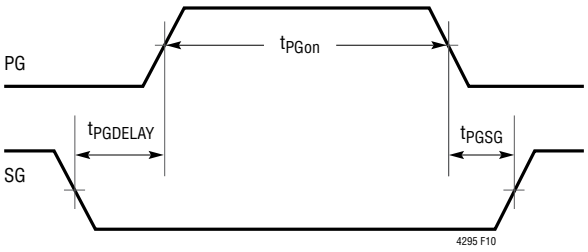


Figure 10. PG and SG Timing Relationship in Flyback Mode

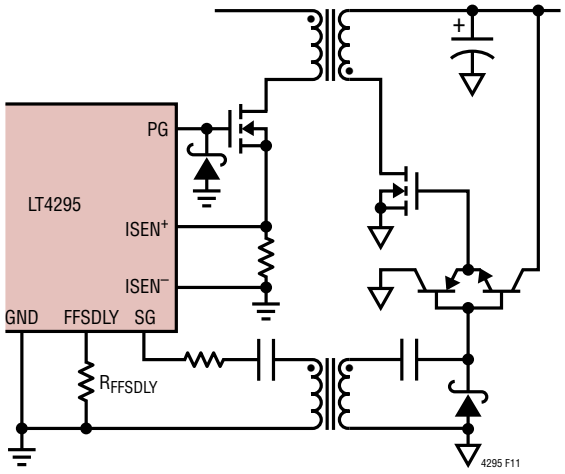


Figure 11. Example PG and SG Connections in Flyback Mode

Forward Mode

The LT4295 is programmed into forward mode by placing a resistor R_{FFSDLY} from the FFSDLY pin to V_{CC}. The R_{FFSDLY} resistor must be in the range of 10.5kΩ to 52.3kΩ. If using a potentiometer to adjust R_{FFSDLY} ensure the adjustment of the potentiometer does not exceed 52.3kΩ.

The value of R_{FFSDLY} determines $t_{PGDELAY}$ and t_{PGSG} according to the following equations:

$$t_{PGDELAY} \approx 7.16ns/k\Omega \bullet R_{FFSDLY} + 17ns$$

$$t_{PGSG} \approx 5.60ns/k\Omega \bullet R_{FFSDLY} + 7.9ns$$

The PG and SG relationships in forward mode are shown in Figure 12.

In forward mode, the SG pin has the correct polarity to drive the active clamp P-channel MOSFET through a simple level shifter as shown in Figure 13. Add a Schottky diode from the PG to GND as shown in Figure 13 to prevent PG from going negative.

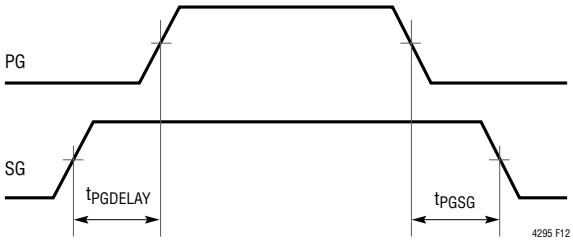


Figure 12. PG and SG Timing Relationship in Forward Mode

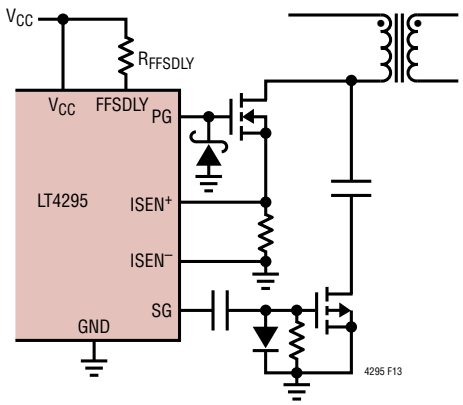


Figure 13. Example PG and SG Connections in Forward Mode

APPLICATIONS INFORMATION

Feedback Amplifier

In the flyback mode, the feedback amplifier senses the output voltage through the transformer's third winding as shown in Figure 14. The amplifier is enabled only during the fixed interval, t_{FB}, as shown in Figure 15. This eliminates the opto-isolator in isolated designs, thus greatly improving the dynamic response and stability over lifetime. Since t_{FB} is a fixed interval, the time-averaged transconductance, gm, varies as a function of the user-selected switching frequency.

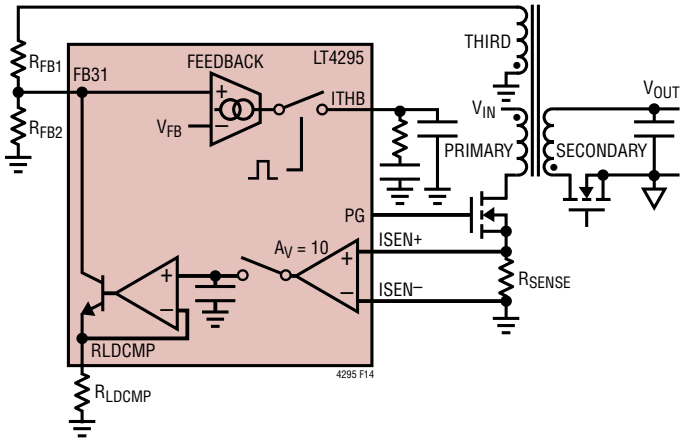


Figure 14. Feedback and Load Compensation Connection

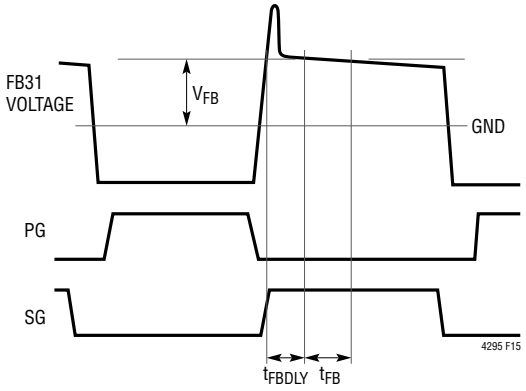


Figure 15. Feedback Amplifier Timing Diagram

FEEDBACK AMPLIFIER OUTPUT, ITHB

As shown in the Block Diagram, V_{SENSE} is the input of the Current Sense Comparator. V_{SENSE} is derived from the output of a linear amplifier whose input is the voltage on the ITHB pin, V_{ITHB}.

This linear amplifier inverts its input, V_{ITHB}, with a gain, $\Delta V_{SENSE}/\Delta V_{ITHB}$, and with an offset voltage of $V_{ITHB(OS)}$ to yield its output, V_{SENSE}. This relationship is shown graphically in Figure 1. Note the slope $\Delta V_{SENSE}/\Delta V_{ITHB}$ is a negative number and is provided in the electrical characteristics table.

$$V_{ITHB} = V_{ITHB(OS)} + V_{SENSE} \bullet \left(\frac{\Delta V_{SENSE}}{\Delta V_{ITHB}}\right)^{-1}$$

The block diagram shows V_{SENSE} is compared against the voltage across the current sense resistor, $V(ISEN^+)$-$V(ISEN^-)$ modified by the internal slope compensation voltage discussed subsequently.

LOAD COMPENSATION

As can be seen in Figure 15, the voltage on the FB31 pin droops slightly during the flyback period. This is mostly caused by resistances of components of the secondary side such as: the secondary winding, $R_{DS(ON)}$ of the synchronous MOSFET, ESR of the output capacitor, etc. These resistances cause a feedback error that is proportional to the current in the secondary loop at the time of feedback sample window. To compensate for this error, the LT4295 places a voltage proportional to the peak current in the primary winding on the RLDCMP pin.

Determining Feedback and Load Compensation Resistors

Because the resistances of components on the secondary side are generally not well known, an empirical method must be used to determine the feedback and load compensation resistor values.

$$\text{INITIALLY SET } R_{FB2} = 2k\Omega$$

$$R_{FB1} \approx R_{FB2} \frac{V_{OUT}}{V_{FB}} \frac{N_{THIRD}}{N_{SECONDARY}} - R_{FB2}$$

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Connect the resistor R_{LDCMP} between the RLDCMP pin and GND. R_{LDCMP} must be at least 10kΩ. Adjust R_{LDCMP} for minimum change of V_{OUT} over the full input and output load range. A potentiometer in series with 10kΩ may be initially used for R_{LDCMP} and adjusted. The potentiometer+10kΩ may then be removed, measured, and replaced with the equivalent fixed resistor. The resulting V_{OUT} differs from the desired V_{OUT} due to offset injected by load compensation. The change to R_{FB2} to correct this is predicted by:

$$\Delta R_{FB2} = \frac{\Delta V_{OUT}}{V_{FB}} \frac{N_{THIRD}}{N_{SECONDARY}} \frac{R_{FB2}^2}{R_{FB1}}$$

Where: ΔV_{OUT} is the desired change to V_{OUT}
ΔR_{FB2} is the required change to R_{FB2}

$N_{THIRD}/N_{SECONDARY}$ is the transformer third winding to secondary winding

OPTO-ISOLATOR FEEDBACK

For forward mode operation, the flyback voltage cannot be sensed across the transformer. Thus, opto-isolator feedback must be used. When using opto-isolator feedback, connect the FB31 pin to GND and leave the RLDCMP pin open. In this condition, the feedback amplifier sinks an average current of I_{SINK} into the ITHB pin. An example for feedback connections is shown in Figure 16. Note that since I_{SINK} is time-averaged over the switching period, the sink current varies as a function of the user-selected switching frequency.

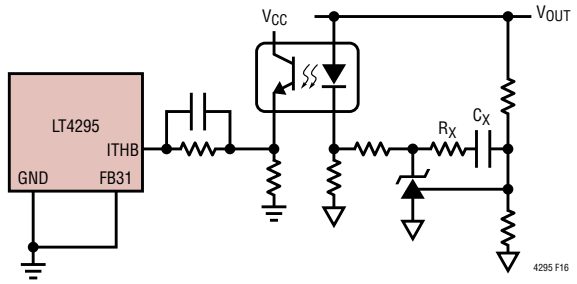

Figure 16. Opto-isolator Feedback Connections in the Forward Mode

SOFT-START

In PoE applications, a proper soft-start design is required to prevent the PD from drawing more current than the PSE can provide.

The soft-start time, t_{SFST}, is approximately the time in which the power supply output voltage, V_{OUT}, is charging its output capacitance, C_{OUT}. This results in an inrush current at the port of the PD, Iport_inrush (not to be confused with I_{INRUSH} discussed earlier in Applications Information section). Care must be taken in selecting t_{SFST} to prevent the PD from drawing more current than the PSE can provide.

In the absence of an output load current, the Iport_inrush, is approximated by the following equation:

$$Iport\_inrush \approx \frac{C_{OUT} \bullet V_{OUT}^2}{\eta \bullet t_{SFST} \bullet V_{IN}}$$

where η is the power supply efficiency,

V_{IN} is the input voltage of the PD

Iport_inrush plus the port current due to the load current must be below the current the PSE can provide. Note that the PSE current capability depends on the PSE operating standard.

The LT4295 contains a soft-start function that controls t_{SFST} by connecting an external capacitor, C_{SFST}, between the SFST pin and GND. The SFST pin is pulled up with I_{SFST} when the LT4295 begins switching. The voltage ramp on the SFST pin is proportional to the duty cycle ramp for PG.

For flyback mode, the soft-start time is:

$$t_{SFST} = \frac{600\mu A}{nF}\left(\frac{C_{SFST}}{I_{SFST}}\right)\left(t_{PGon} + t_{PGDELAY} - t_{MIN}\right)$$

where t_{PGon} is the time when PG is high as shown in Figure 8 once the power supply is in steady-state.

In forward mode, each of the back page applications schematics provides a chart with t_{SFST} vs. C_{SFST}. Select the application and choose a value of C_{SFST} that corresponds to the desired soft-start time.

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CURRENT SENSE COMPARATOR

The LT4295 uses a differential current sense comparator to reduce the effects of stray resistance and inductance on the measurement of the primary current. $ISEN^+$ and $ISEN^-$ must be Kelvin connected to the sense resistor pads.

Like most switching regulator controllers, the current sense comparator begins sensing the current t_{MIN} after PG turns on. Then, the comparator turns PG off after the voltage across $ISEN^+$ and $ISEN^-$ exceeds the current sense comparator threshold, V_{SENSE}. Note that the voltage across $ISEN^+$ and $ISEN^-$ is modified by LT4295's internal slope compensation.

SLOPE COMPENSATION

The LT4295 incorporates current slope compensation. Slope compensation is required to ensure current loop stability when the duty cycle is greater than or near 50%. The slope compensation of the LT4295 does not reduce the maximum peak current at higher duty cycles.

CONTROL LOOP COMPENSATION

In flyback mode, loop frequency compensation is performed by connecting a resistor/capacitor network from the output of the feedback amplifier (ITHB pin) to GND as shown in Figure 14. In forward mode, loop compensation is performed by varying R_X and C_X in Figure 16.

ADJUSTABLE SWITCHING FREQUENCY

The LT4295 has a default switching frequency, f_{OSC}, of 214 kHz when the ROSC pin is left open. If a higher switching frequency, f_{SW}, is desired (up to 300kHz), a resistor no smaller than 45.3kΩ may be added between the ROSC pin to GND. The resistor can be calculated below:

$$R_{OSC} = \frac{3900k\Omega \bullet kHz}{(f_{SW} - f_{OSC})}(k\Omega)$$

SHORT CIRCUIT RESPONSE

If the power supply output voltage is shorted, overloaded, or if the soft-start capacitor is too small, an overcurrent fault event occurs when the voltage across the sense pins exceeds V_{FAULT} (after the blanking period of t_{MIN}). This begins the internal fault timer t_{FAULT}. For the duration of t_{FAULT}, the LT4295 turns off PG and SG and pulls the SFST pin to GND. After t_{FAULT} expires, the LT4295 initiates soft-start.

The fault and soft-start sequence repeats as long as the short circuit or overload conditions persist. This condition is recognized by the PG waveform shown in Figure 17 repeating at an interval of t_{FAULT}.

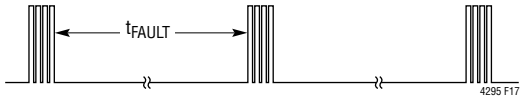

Figure 17. PG Waveforms with Output Shorted

OVERTEMPERATURE PROTECTION

The IEEE 802.3 specification requires a PD to withstand any applied voltage from 0V to 57V indefinitely. During classification, however, the power dissipation in the LT4295 may be as high as 1.5W. The LT4295 can easily tolerate this power for the maximum IEEE classification timing but overheats if this condition persists abnormally.

The LT4295 includes an overtemperature protection feature which is intended to protect the device during momentary overload conditions. If the junction temperature exceeds the overtemperature threshold, the LT4295 pulls down HSGATE pin, disables classification, and disables the switching regulator operation.

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MAXIMUM DUTY CYCLE

The maximum duty cycle of the PG pin is modified by the chosen $t_{PGDELAY}$ and f_{SW}. It is calculated below:

MAX POWER SUPPLY DUTY CYCLE
$= D_{MAX} – t_{PGDELAY} • f_{SW}$

For an appropriate margin during transient operation, the forward or flyback power supply should be designed so that its maximum steady-state duty cycle should be about 10% lower than the LT4295 Maximum Power Supply Duty Cycle calculated above.

EXTERNAL INTERFACE AND COMPONENT SELECTION

PoE Input Bridge

A PD is required to polarity-correct its input voltage. There are several different options available for bridge rectifiers; silicon diodes, Schottky diodes, and ideal diodes. When silicon or Schottky diode bridges are used, the diode forward voltage drops affect the voltage at the VPORT pin. The LT4295 is designed to tolerate these voltage drops. Note, the voltage parameters shown in the Electrical Characteristics section are specified at the LT4295 package pins.

A silicon diode bridge consumes up to 4% of the available power. In addition, silicon diode bridges exhibit poor pairset-to-pairset unbalance performance. Each branch of a silicon diode bridge shares source/return current, and thermal runaway can cause large, non-compliant current unbalances between pairsets.

While using Schottky diodes can help reduce the power loss with a lower forward voltage, the Schottky bridge may not be suitable for high temperature PD applications. Schottky diode bridges exhibit temperature induced leakage currents. The leakage current has a voltage dependency that can invalidate the measured detection signature. In addition, these leakage currents can back-feed through the unpowered branch and the unused bridge, violating IEEE 802.3 specifications.

For high efficiency applications, the LT4295 supports an LT4321-based PoE ideal diode bridge that reduces the forward voltage drop from 0.7V to 20mV per diode while maintaining IEEE 802.3 compliance. The LT4321 simplifies thermal design, eliminates costly heatsinks, and can operate in space-constrained applications.

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Auxiliary Input Diode Bridge

Some PDs are required to receive AC or DC power from an auxiliary power source. A diode bridge is typically required to handle the voltage rectification and polarity correction.

In high efficiency applications, or in low auxiliary input voltage applications, the voltage drop across the rectifier cannot be tolerated. The LT4295 can be configured with an LT4320-based ideal diode bridge to recover the diode voltage drop and ease thermal design.

For applications with auxiliary input voltages below 10V, the LT4295 must be configured with an LT4320-based ideal diode bridge to recover the voltage drop and guarantee the minimum VPORT voltage is within the VPORT AUX range as specified in the Electrical Characteristics table.

Input Capacitor

A 0.1µF capacitor is needed from V_{PORT} to GND to meet the input impedance requirement in IEEE 802.3 and to properly bypass the LT4295. When operating with the LT4321, locally bypass each with a 0.047µF capacitor, thus keeping the total port capacitance within specification.

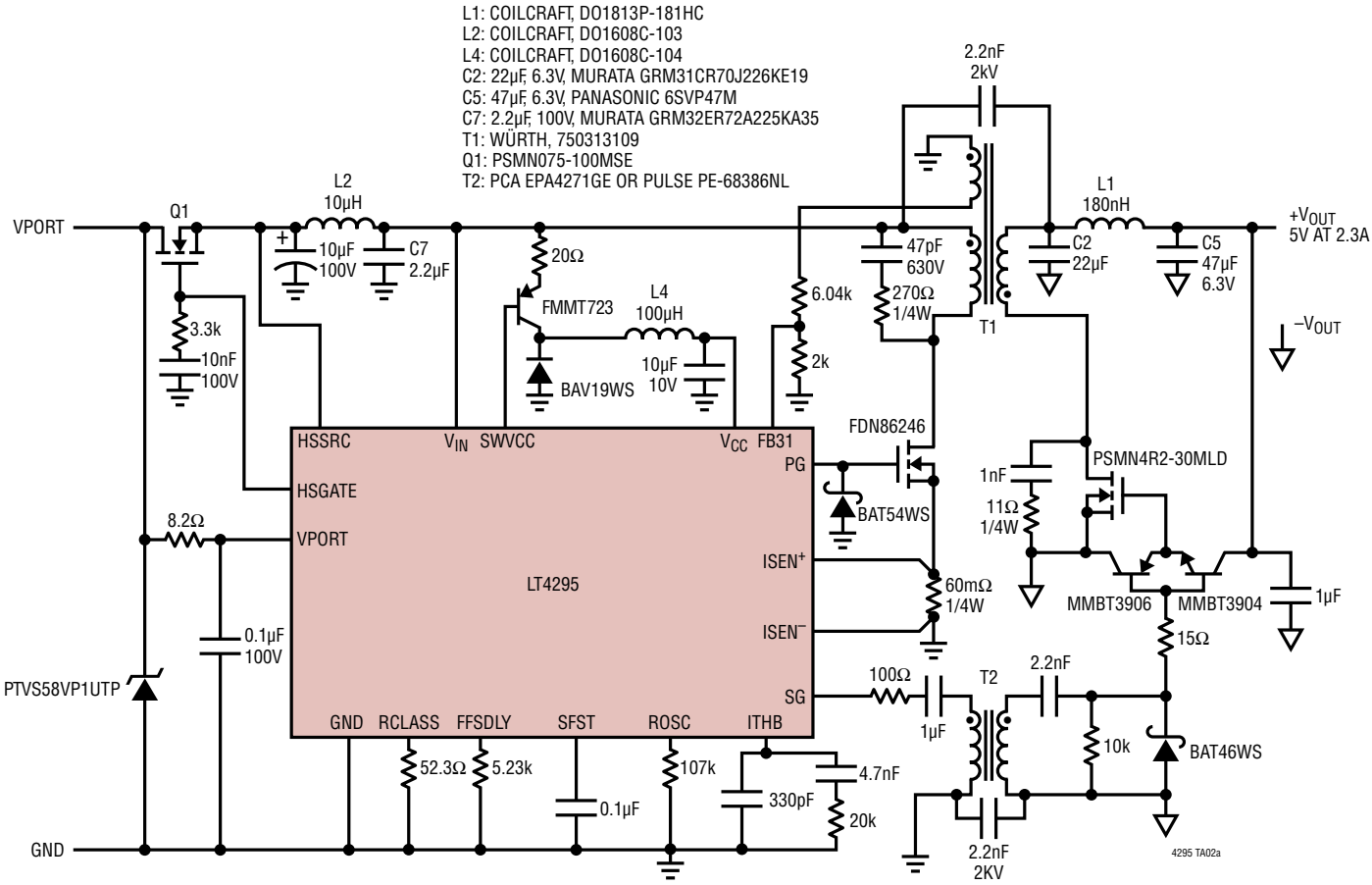
Transient Voltage Suppressor

The LT4295 specifies an absolute maximum voltage of 100V and is designed to tolerate brief overvoltage events due to Ethernet cable surges. To protect the LT4295 from an overvoltage event, install a unidirectional transient voltage suppressor (TVS) such as an SMAJ58A between the VPORT and GND pins. For PD applications that require an auxiliary power input, install a TVS between V_{IN} and GND.

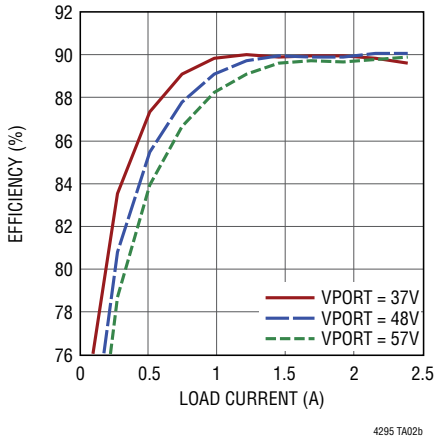
For extremely high cable discharge and surge protection, contact Analog Devices Applications.

TYPICAL APPLICATIONS

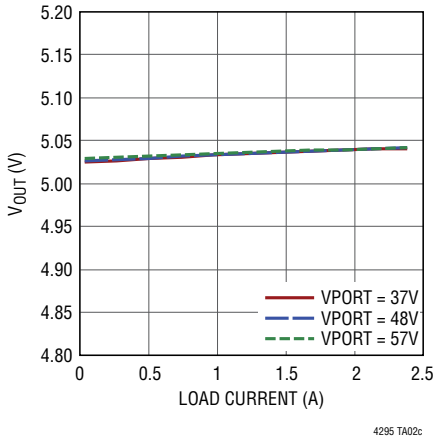
13W PoE Power Supply in Flyback Mode with 5V, 2.3A Output



Efficiency vs Load Current

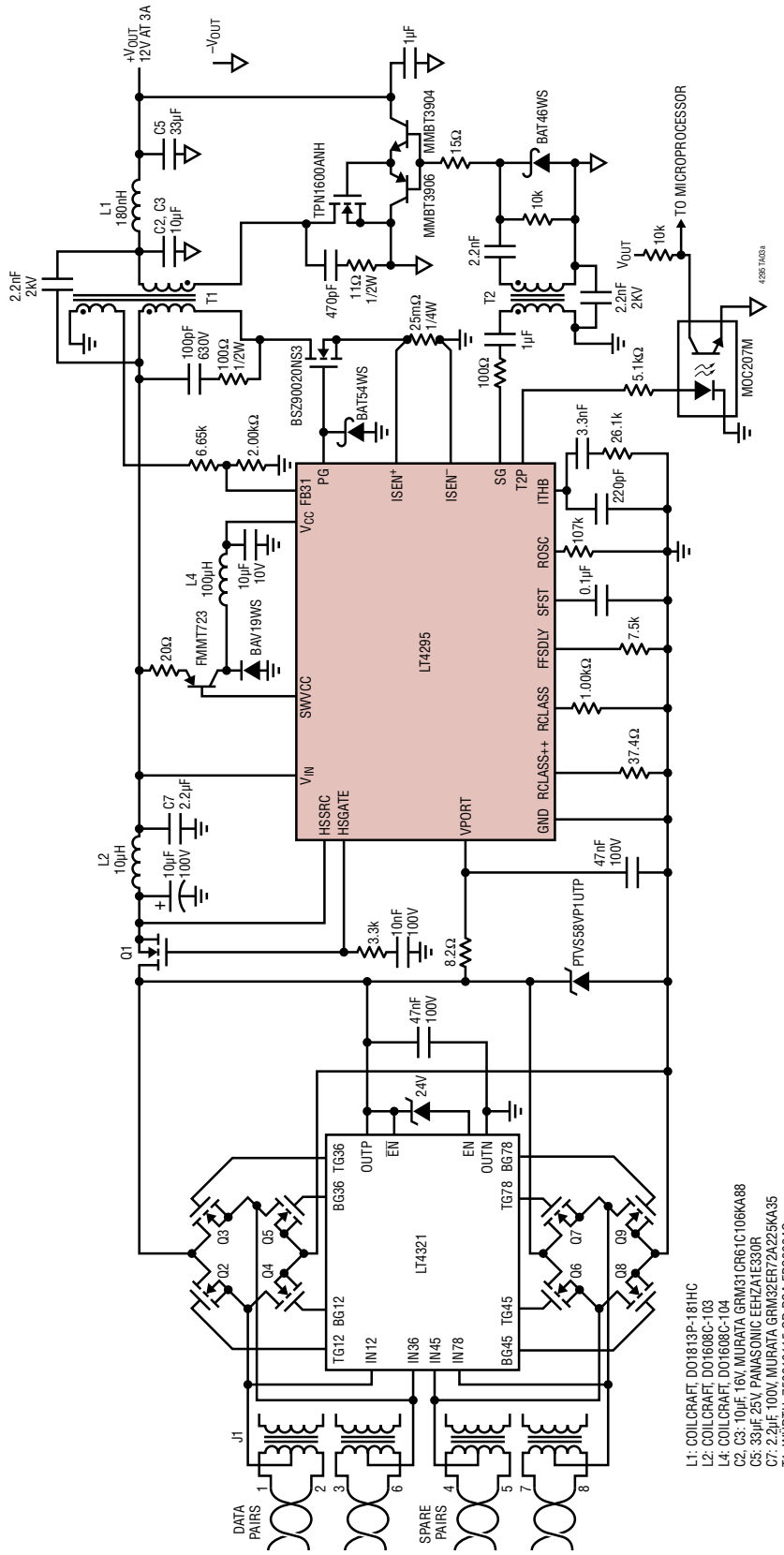


V_{OUT} vs Load Current



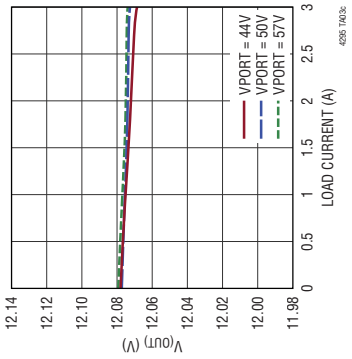
TYPICAL APPLICATIONS

40W PoE Power Supply in Flyback Mode with 12V, 3A Output

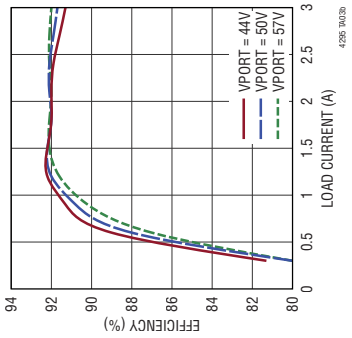


L1: COILCRAFT, DO1813P-181HC
L2: COILCRAFT, DO1608C-103
L4: COILCRAFT, DO1608C-104
C2, C3: 10µF, 16V, MURATA GRM31CR61C106KA88
C5: 33µF 25V, PANASONIC EEHZA1E330R
C7: 2.2µF 100V, MURATA GRM32ER72A225KA35
T1: WÜRTH, 750316115 OR PCA EPC3634G
Q1-Q9: PSMN075-100MSE
T2: PCA EPA4271GE OR PULSE PE-68386NL
J1: WÜRTH 7499511001A

VOUT vs Load Current

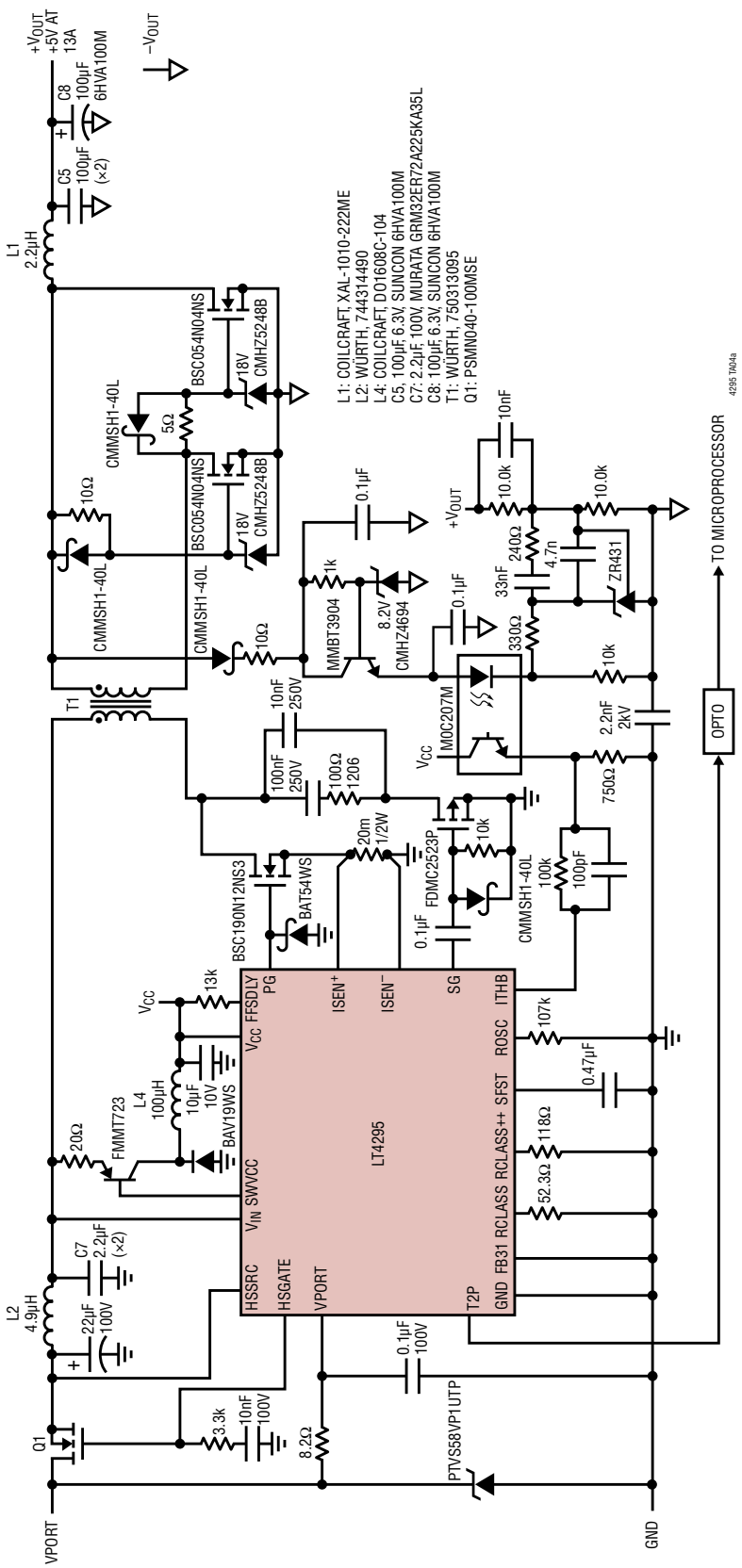


Efficiency vs Load Current

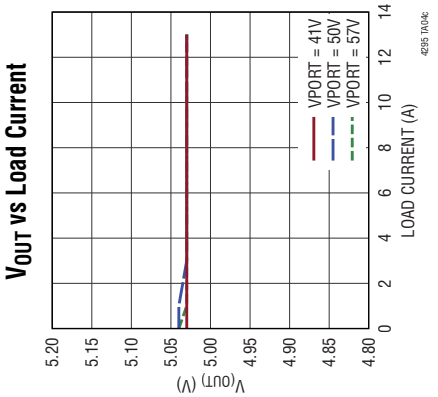


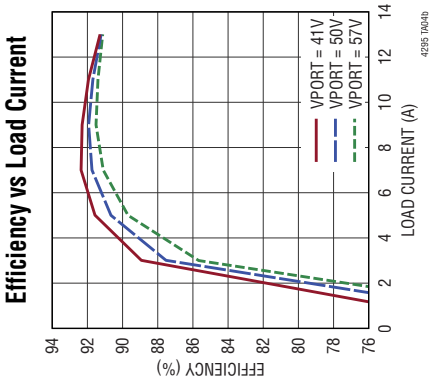
TYPICAL APPLICATIONS

71.3W PoE Power Supply in Forward Mode with 5V, 13A Output



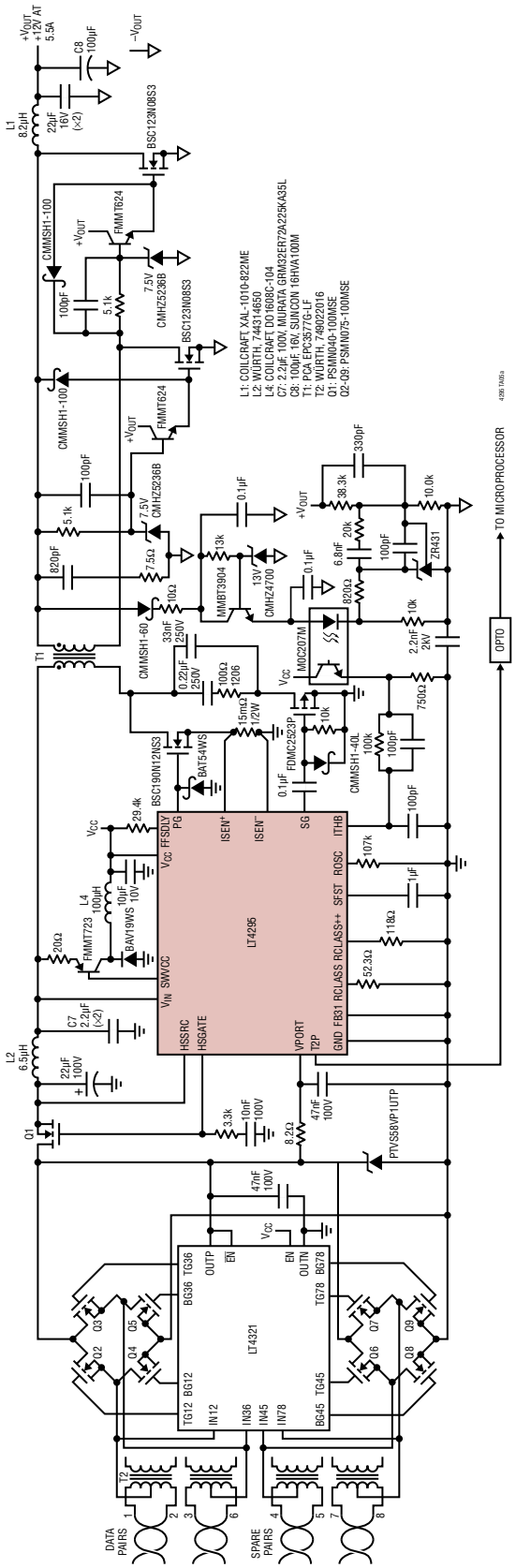
C_{SFST} (µF)	t_{SFST} (ms)
0.10	1.2
0.33	3.8
1.0	12
3.3	38





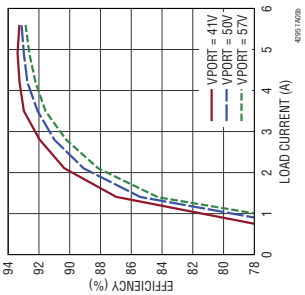
TYPICAL APPLICATIONS

71.3W PoE Power Supply in Forward Mode with 12V, 5.5A Output

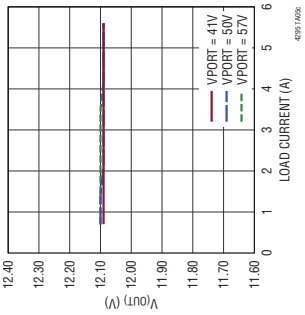


C_{SFST} (µF)	t_{SFST} (ms)
0.10	1.5
0.33	4.9
1.0	15
3.3	48

Efficiency vs Load Current

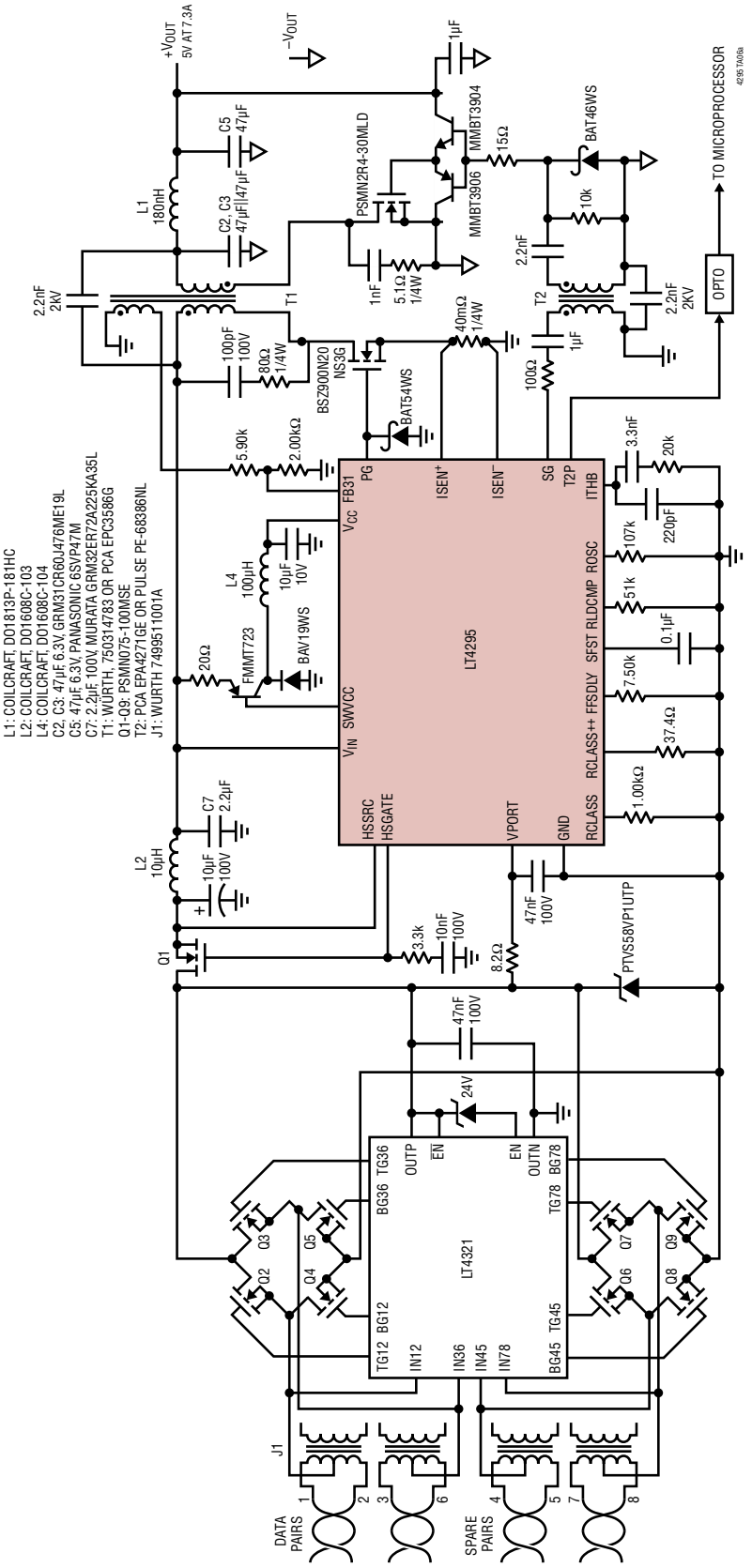


V_{OUT} vs Load Current

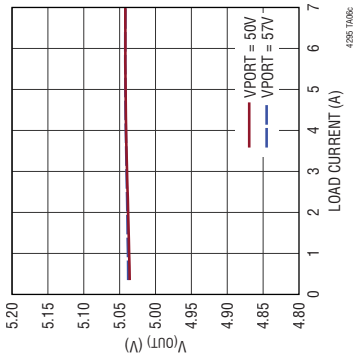


TYPICAL APPLICATIONS

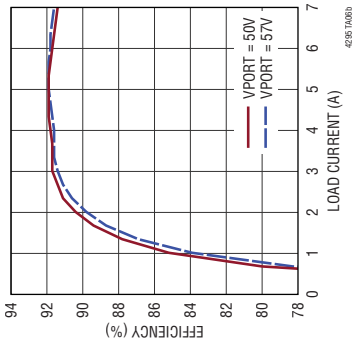
40W PoE Power Supply in Flyback Mode with 5V, 7.3A Output



VOUT vs Load Current

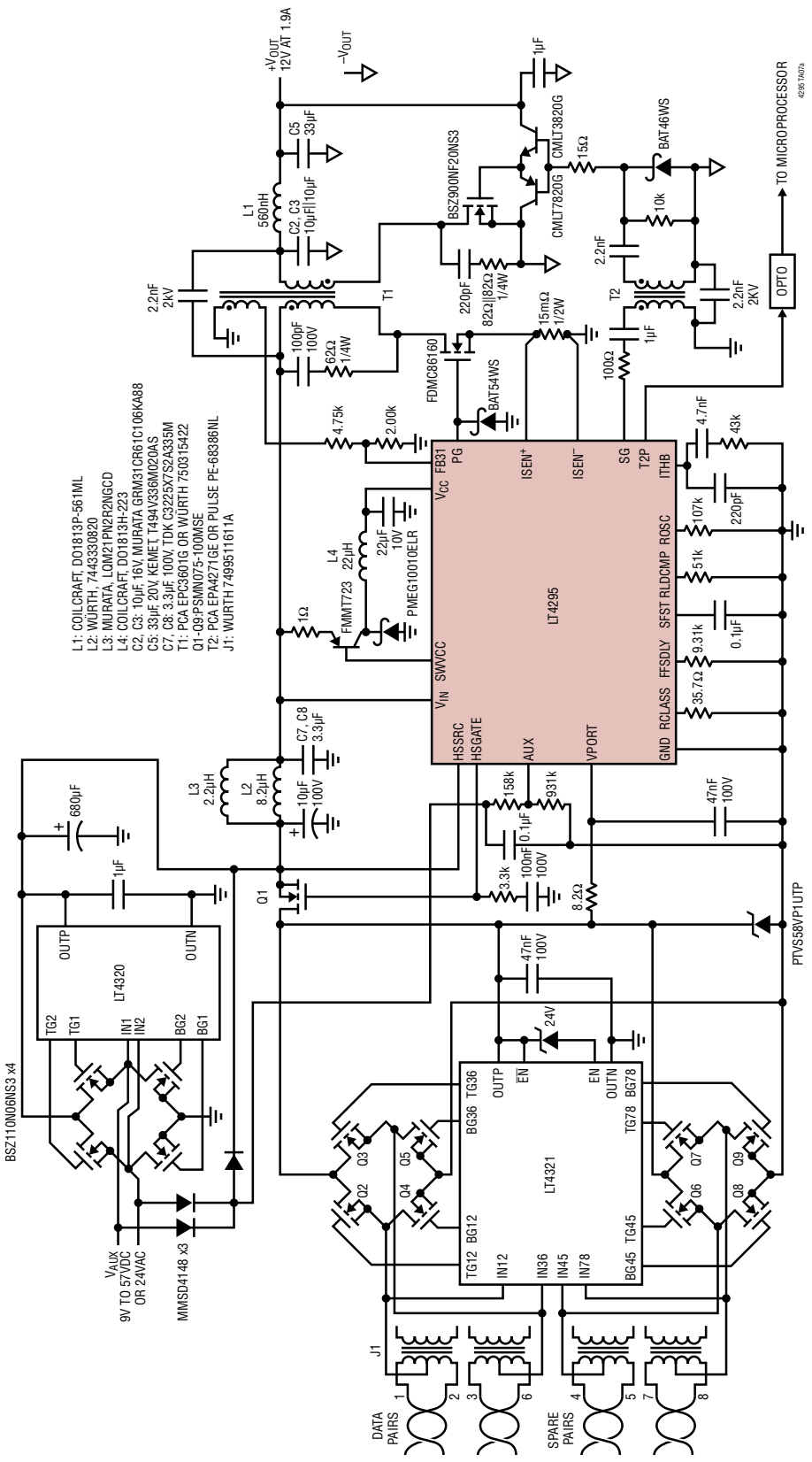


Efficiency vs Load Current

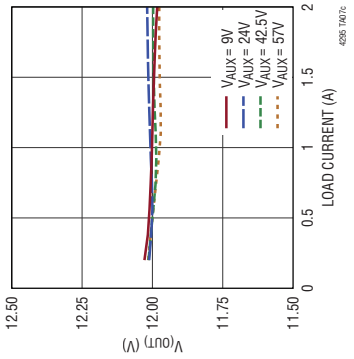


TYPICAL APPLICATIONS

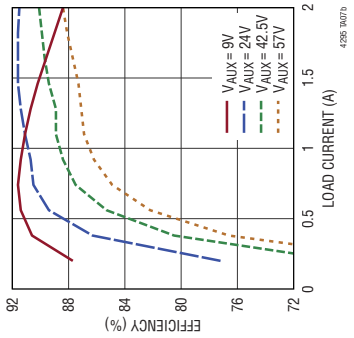
25.5W PoE and 9V to 57V Auxiliary Input Power Supply in Flyback Mode with 12V, 1.9A Output



VOUT vs Load Current

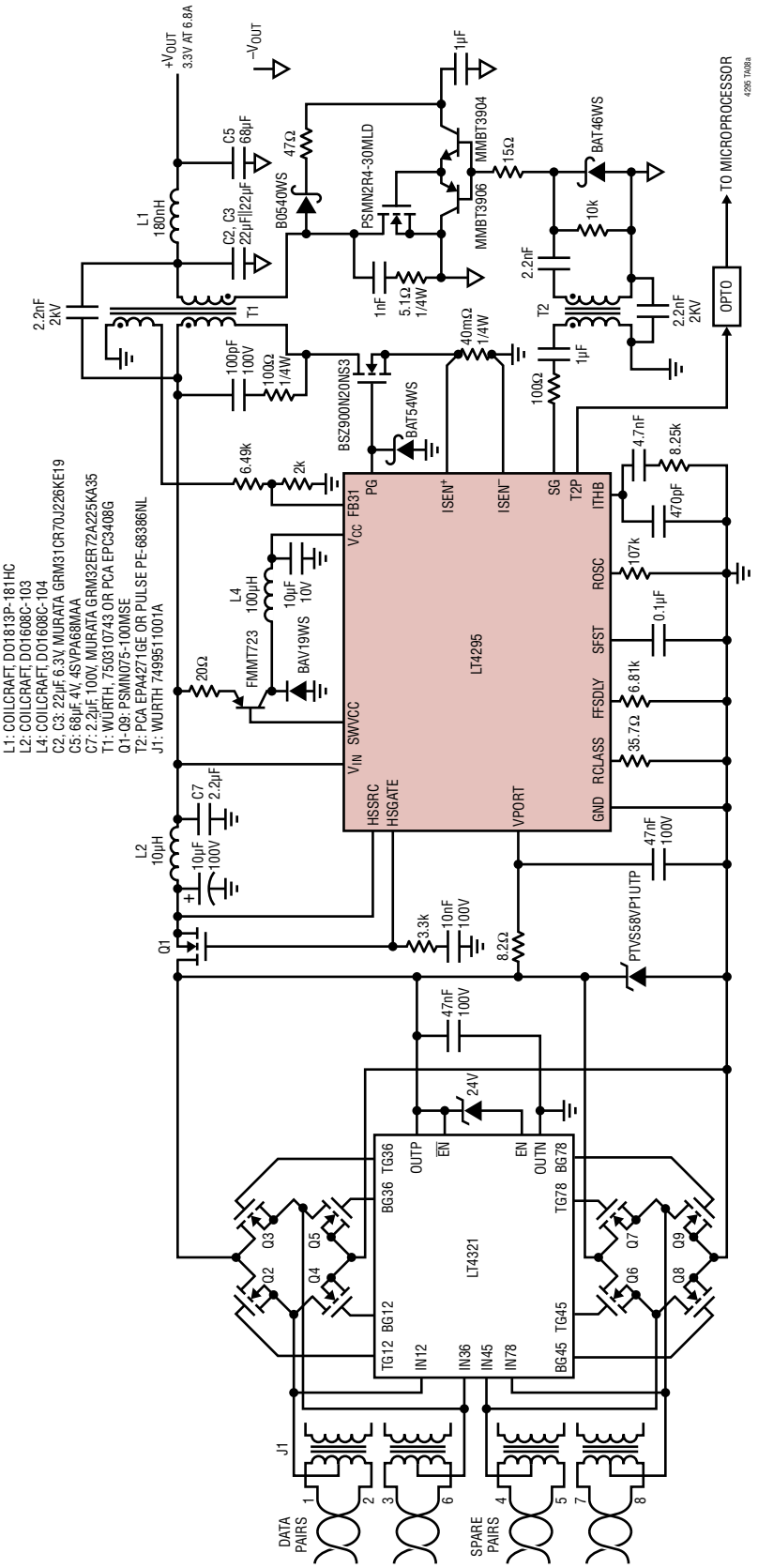


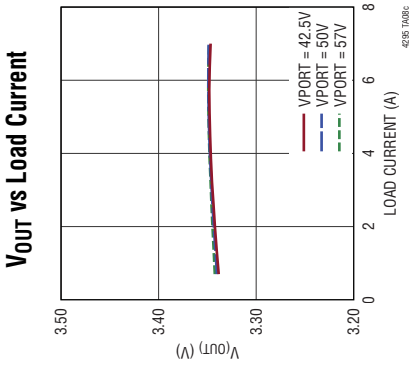
Efficiency vs Load Current

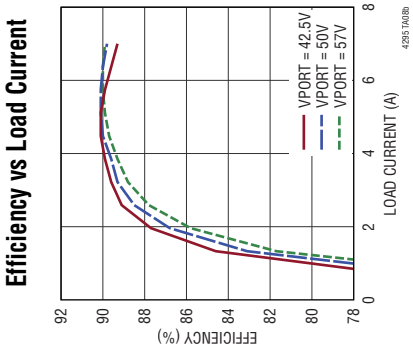


TYPICAL APPLICATIONS

25.5W PoE Power Supply in Flyback Mode with 3.3V, 6.8A Output

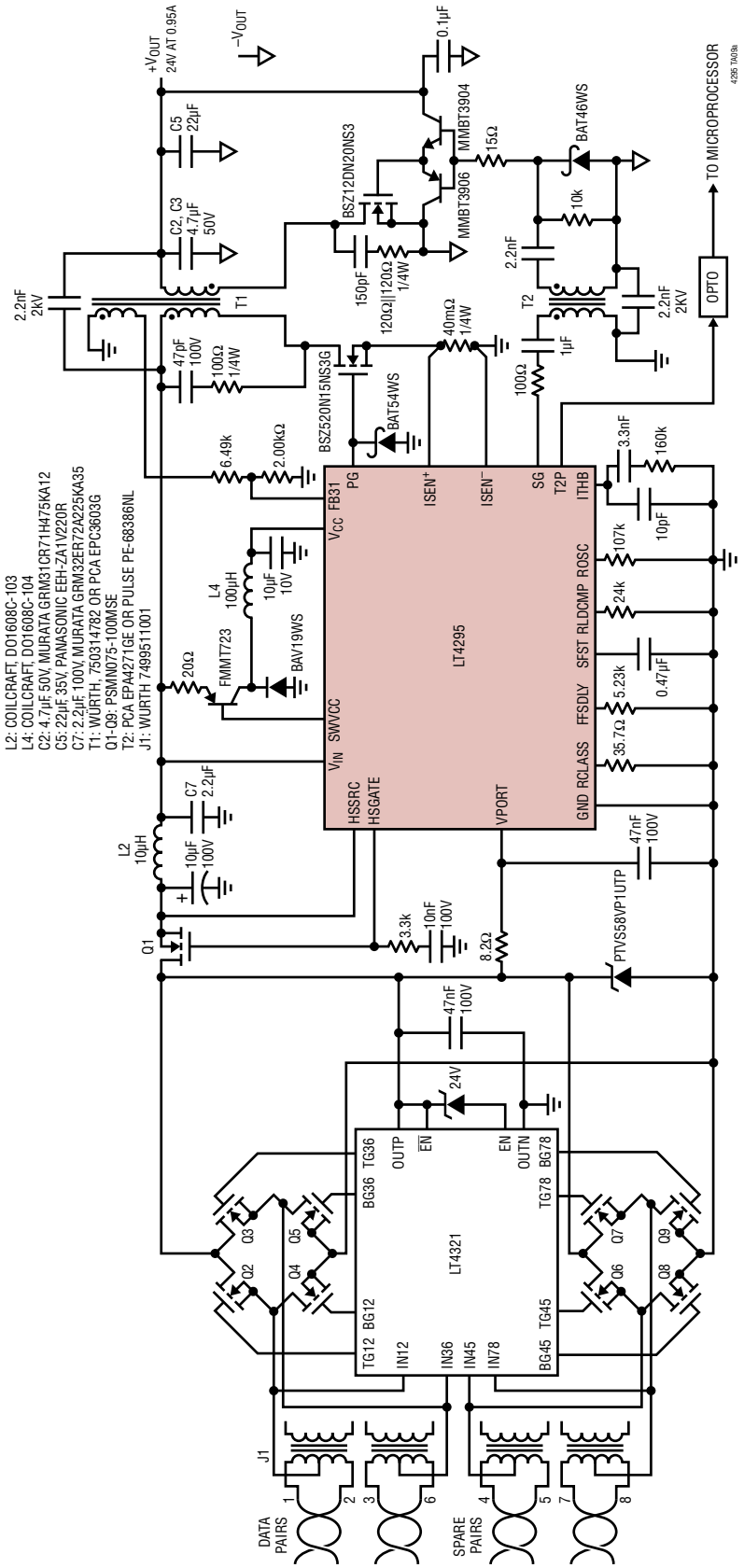




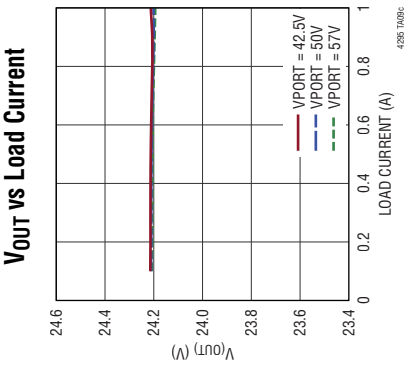


TYPICAL APPLICATIONS

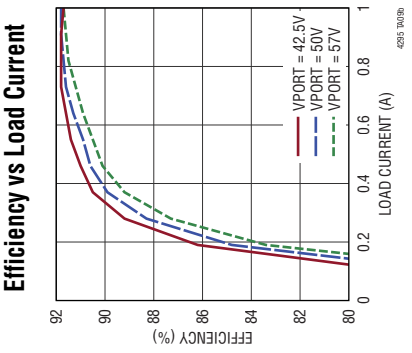
25.5W PoE Power Supply in Flyback Mode with 24V, 0.95A Output



VOUT vs Load Current

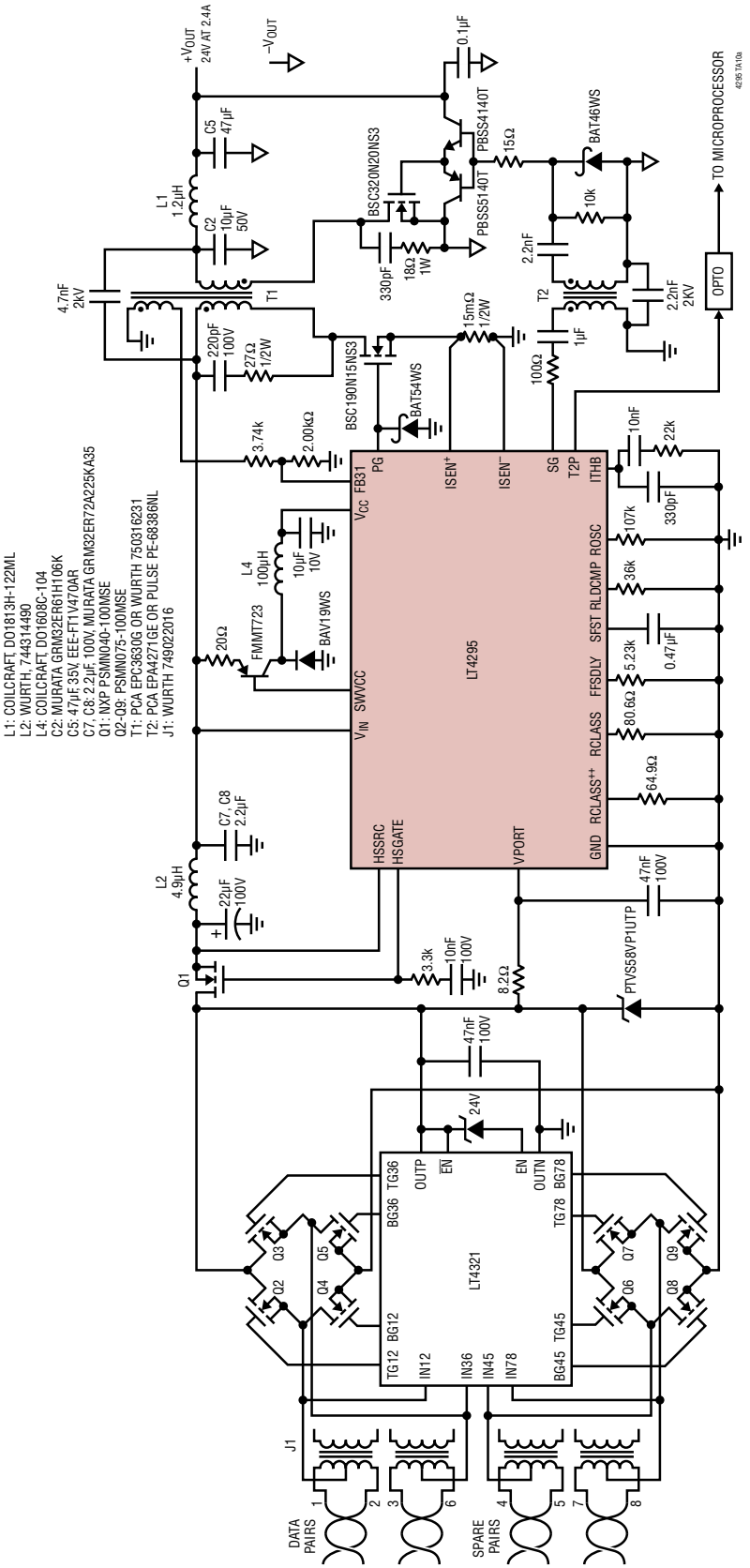


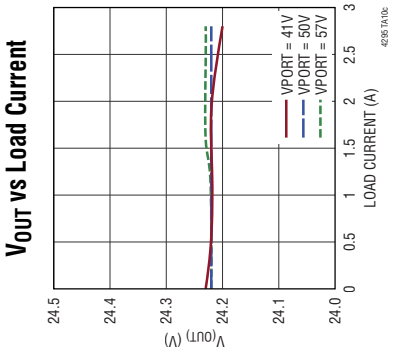
Efficiency vs Load Current

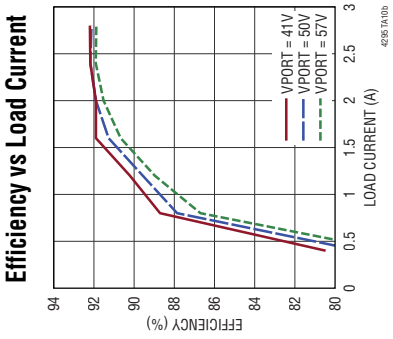


TYPICAL APPLICATIONS

62W PoE Power Supply in Flyback Mode with 24V, 2.4A Output

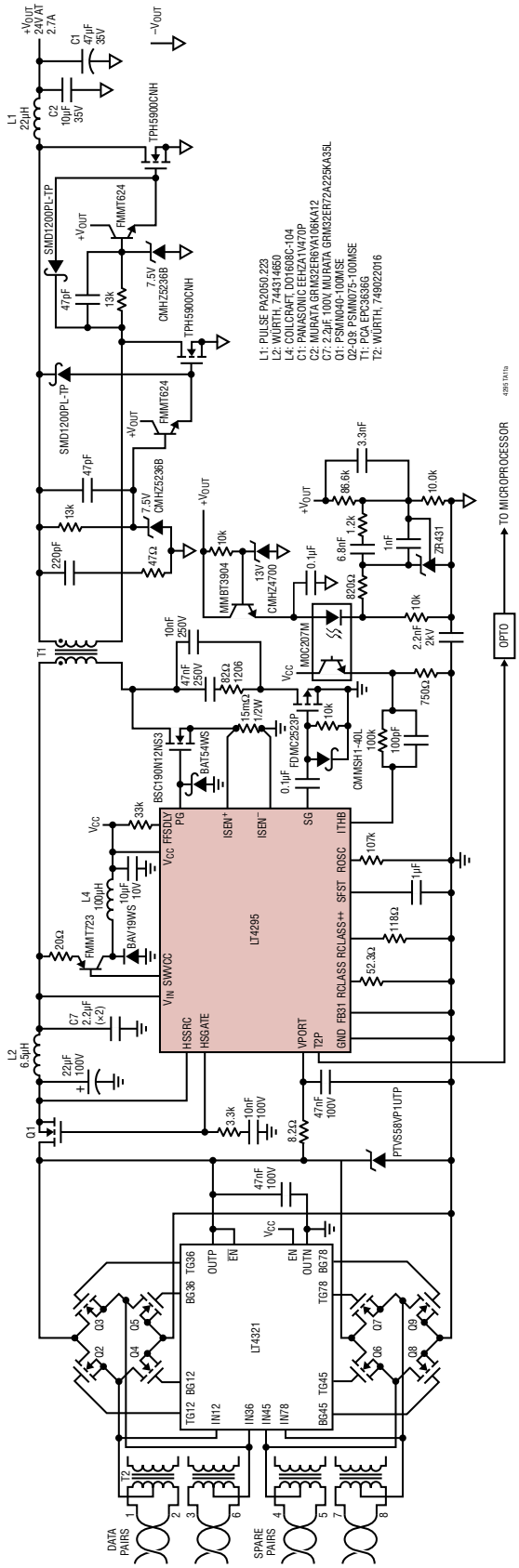






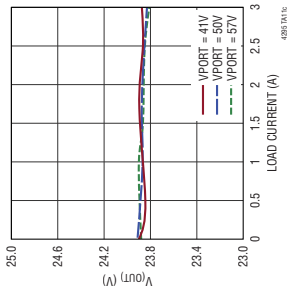
TYPICAL APPLICATIONS

71.3W PoE Power Supply in Forward Mode with 24W, 2.7A Output

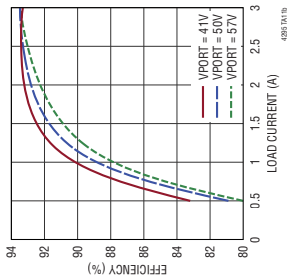


C_{SFST} (µF)	t_{SFST} (ms)
0.10	1.4
0.22	2.4
0.47	4.4
1.0	15
3.3	46

V_{OUT} vs Load Current

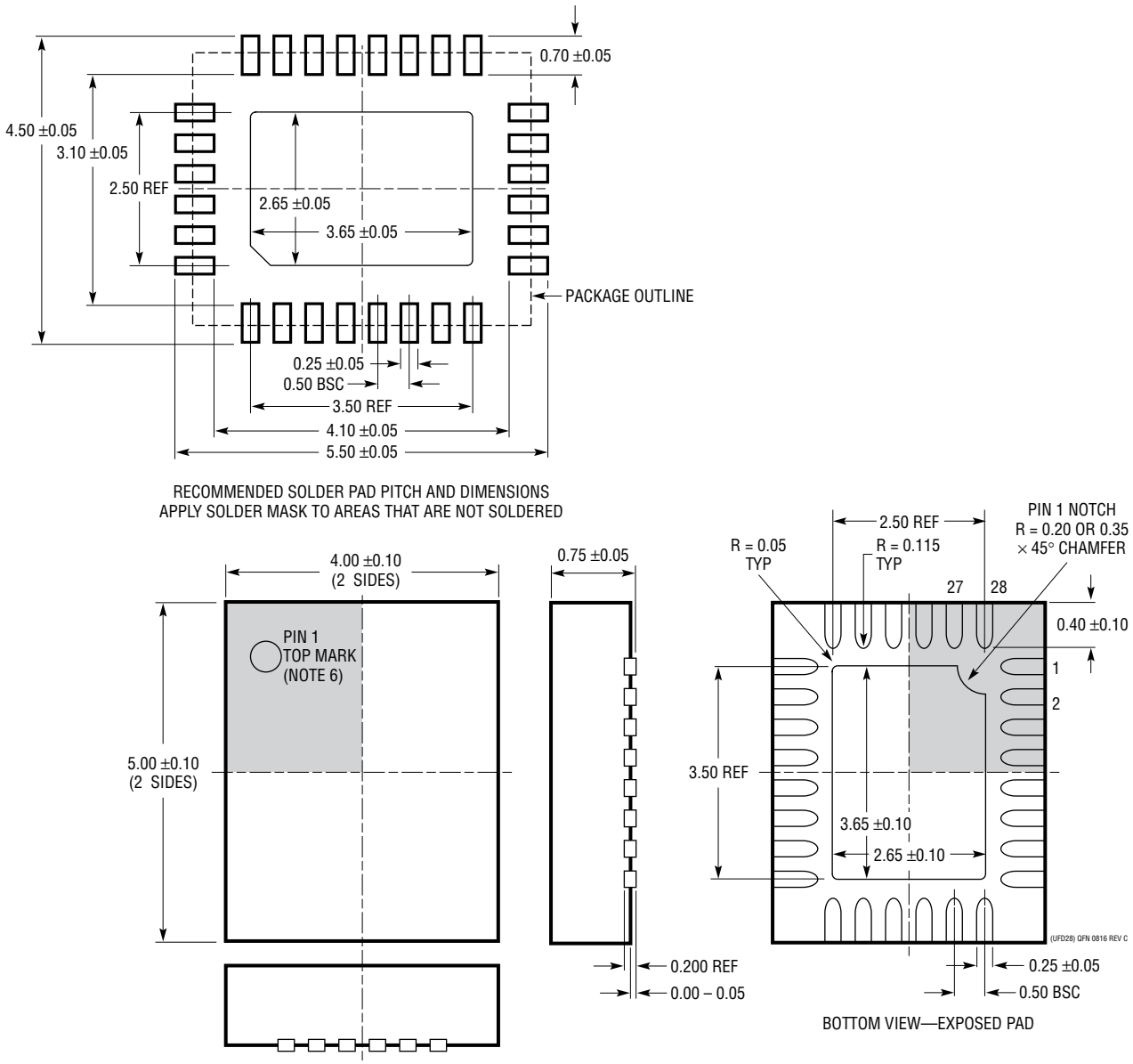


Efficiency vs Load Current



PACKAGE DESCRIPTION

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



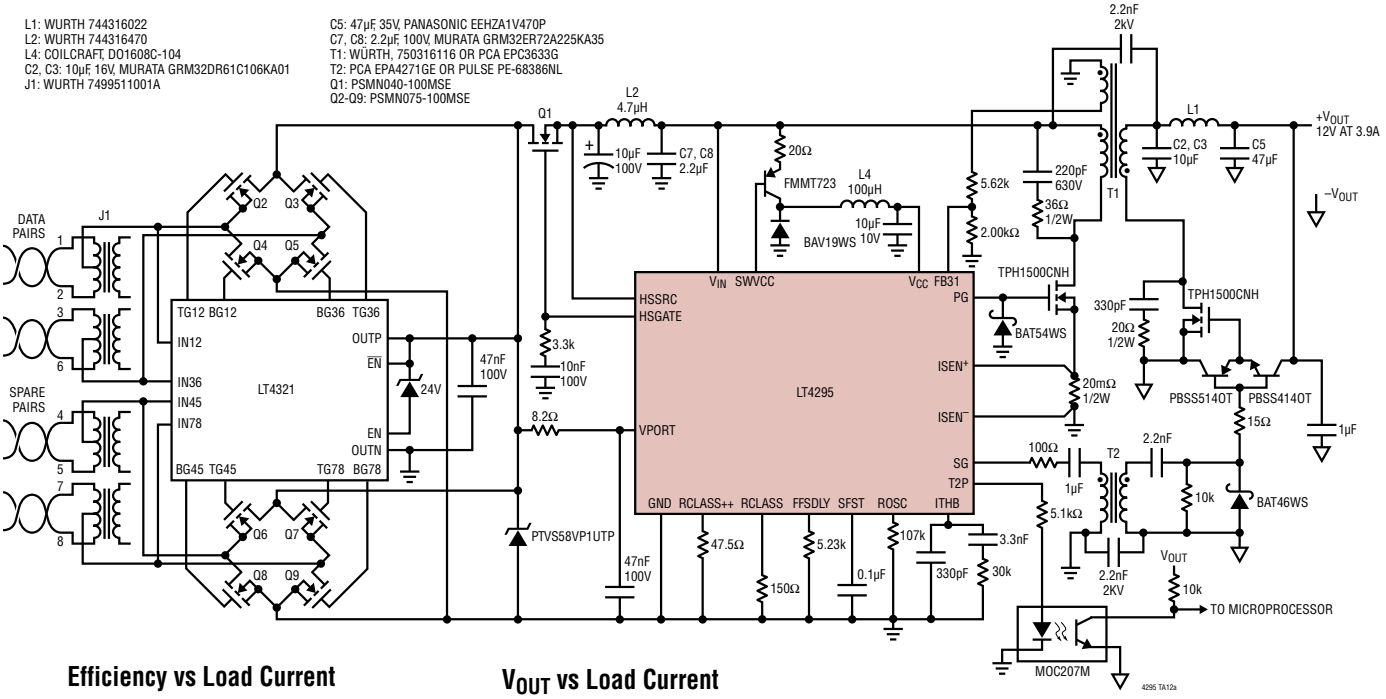
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

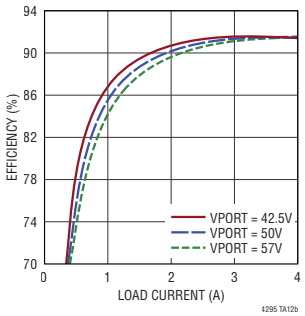
REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/18	Updated max input power to 71.3W per Draft 3.4	1-30
		Revised T2P Output, PoE Input Bridge, Input Capacitor, and Transient Voltage Supressor Applications Information	12, 17
		Changed R_{CLASS} and/or R_{CLASS}++ resistor values	20, 26
		Added J1 transformer recommendations	19, 22-26, 30
B	5/19	Removed Draft number	1-30
		Added Table 5–Interoperability	13

TYPICAL APPLICATION

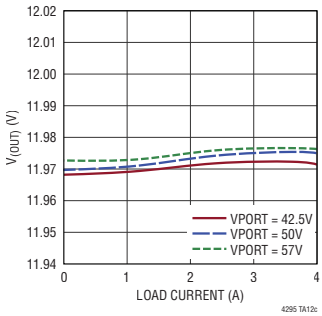
51W PoE Power Supply in Flyback Mode with 12V, 3.9A Output



Efficiency vs Load Current



V_{OUT} vs Load Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT4293	LTPoE++/IEEE 802.3bt PD Interface	Mutually identifies with LTPoE++ and IEEE 802.3bt PSEs
LT4294	IEEE 802.3bt PD Controller	External Switch, IEEE 802.3bt and AUX Support
LT4320/LT4320-1	Ideal Diode Bridge Controller	9V-72V, DC to 600Hz Input. Controls 4-NMOSFETs, Voltage Rectification without Diode Drops
LT4321	PoE Ideal Diode Bridge Controller	Controls 8-NMOSFETs for IEEE-required PD Voltage Rectification without Diode Drops
LTC4292/LTC4291-1	4-Port IEEE 802.3bt PSE Controller	Transformer Isolation, Supports IEEE 802.3bt PDs
LTC4269-1	IEEE 802.3at PD Interface with Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, Aux Support
LTC4269-2	IEEE 802.3at PD Interface with Integrated Forward Switching Regulator	2-Event Classification, Programmable Class, Synchronous Forward Controller, 100kHz to 500kHz, Aux Support
LT4275A/B/C	LTPoE++/PoE+/PoE PD Controller	External Switch, LTPoE++ Support
LT4276A/B/C	LTPoE++/PoE+/PoE PD with Forward/ Flyback Switching Regulator Controller	External Switch, LTPoE++ Support, User-Configurable Class, Forward or No-Opto Flyback Operation, Frequency, PG/SG Delays, Soft-Start, and Aux Support as Low as 9V, Incl Housekeeping Buck, Slope Compensation
LTC4278	IEEE 802.3at PD Interface with Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, 12V Aux Support