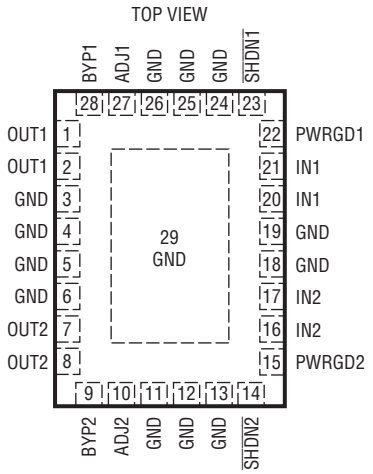
ABSOLUTE MAXIMUM RATINGS

(Note 1)

IN1, IN2 Pin Voltage ..... ±22V
OUT1, OUT2 Pin Voltage ..... ±22V
Input-to-Output Differential Voltage ..... ±22V
ADJ1, ADJ2 Pin Voltage ..... ±9V
BYP1, BYP2 Pin Voltage ..... ±0.6V
$\overline{SHDN1}$, $\overline{SHDN2}$ Pin Voltage ..... ±22V
PWRGD1, PWRGD2 Pin Voltage ..... 22V, –0.3V
Output Short-Circuit Duration ..... Indefinite

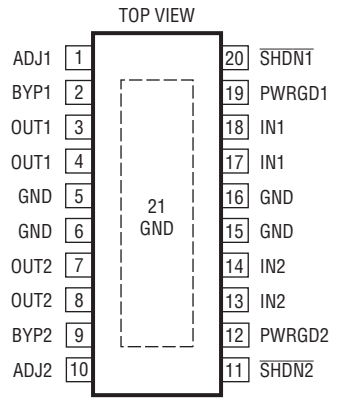
Operating Junction Temperature (Notes 2, 12)
E-/I-Grade ..... –40°C to 125°C
H-Grade ..... –40°C to 150°C
MP-Grade ..... –55°C to 150°C
Storage Temperature Range
QFN/TSSOP Package ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
(TSSOP Only) ..... 300°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 33°C/W, , θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 28°C/W, , θ_{JC} = 10°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3030EUFD#PBF	LT3030EUFD#TRPBF	3030	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3030IUFD#PBF	LT3030IUFD#TRPBF	3030	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3030HUFD#PBF	LT3030HUFD#TRPBF	3030	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C
LT3030EFE#PBF	LT3030EFE#TRPBF	LT3030FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT3030IFE#PBF	LT3030IFE#TRPBF	LT3030FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT3030HFE#PBF	LT3030HFE#TRPBF	LT3030FE	20-Lead Plastic TSSOP	–40°C to 150°C
LT3030MPFE#PBF	LT3030MPFE#TRPBF	LT3030FE	20-Lead Plastic TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 3, 11)	Output 1, I_{LOAD} = 750mA Output 2, I_{LOAD} = 250mA	● ●		1.7 1.7	2.2 2.2	V V
ADJ1, ADJ2 Pin Voltage (Notes 3, 4)	V_{IN} = 2V, I_{LOAD} = 1mA Output 1, 2.2V < V_{IN1} < 20V, 1mA < I_{LOAD} < 750mA Output 2, 2.2V < V_{IN2} < 20V, 1mA < I_{LOAD} < 250mA	 ● ●	1.208 1.196 1.196	1.220 1.220 1.220	1.232 1.244 1.244	V V V
Line Regulation (Note 3)	ΔV_{IN} = 2V to 20V, I_{LOAD} = 1mA	●		0.5	5	mV
Load Regulation (Note 3)	Output 1, V_{IN1} = 2.2V, ΔI_{LOAD} = 1mA to 750mA V_{IN1} = 2.2V, ΔI_{LOAD} = 1mA to 750mA	 ●		2	6 10	mV mV
	Output 2, V_{IN2} = 2.2V, ΔI_{LOAD} = 1mA to 250mA V_{IN2} = 2.2V, ΔI_{LOAD} = 1mA to 250mA	 ●		2	6 10	mV mV
Dropout Voltage (Output 1) V_{IN1} = $V_{OUT1(NOMINAL)}$ (Notes 5, 6, 11)	I_{LOAD} = 10mA I_{LOAD} = 10mA	 ●		0.13	0.20 0.28	V V
	I_{LOAD} = 100mA I_{LOAD} = 100mA	 ●		0.17	0.23 0.33	V V
	I_{LOAD} = 500mA I_{LOAD} = 500mA	 ●		0.27	0.32 0.43	V V
	I_{LOAD} = 750mA I_{LOAD} = 750mA	 ●		0.3	0.36 0.48	V V
Dropout Voltage (Output 2) V_{IN2} = $V_{OUT2(NOMINAL)}$ (Notes 5, 6, 11)	I_{LOAD} = 10mA I_{LOAD} = 10mA	 ●		0.14	0.20 0.28	V V
	I_{LOAD} = 50mA I_{LOAD} = 50mA	 ●		0.18	0.24 0.32	V V
	I_{LOAD} = 100mA I_{LOAD} = 100mA	 ●		0.22	0.28 0.38	V V
	I_{LOAD} = 250mA I_{LOAD} = 250mA	 ●		0.3	0.36 0.48	V V
GND Pin Current (Output 1) V_{IN1} = $V_{OUT1(NOMINAL)}$ (Notes 5, 7)	I_{LOAD} = 0mA I_{LOAD} = 10mA I_{LOAD} = 100mA I_{LOAD} = 500mA I_{LOAD} = 750mA	● ● ● ● ●		120 420 2 9 15	300 800 3.8 17 27	µA µA mA mA mA
GND Pin Current (Output 2) V_{IN2} = $V_{OUT2(NOMINAL)}$ (Notes 5, 7)	I_{LOAD} = 0mA I_{LOAD} = 10mA I_{LOAD} = 50mA I_{LOAD} = 100mA I_{LOAD} = 250mA	● ● ● ● ●		75 330 1 1.8 5	200 600 1.8 3.4 9	µA µA mA mA mA
Output Voltage Noise	C_{OUT} = 10µF, C_{BYP} = 10nF, I_{LOAD} = Full Current (Note 13) BW = 10Hz to 100kHz			20		μV_{RMS}
ADJ1/ADJ2 Pin Bias Current (Notes 3, 8)				30	100	nA
Shutdown Threshold	V_{OUT} = Off to On V_{OUT} = On to Off Hysteresis (Note 2)	● ●	1.09 0.5	1.21 0.83 0.38	1.33	V V V
$\overline{SHDN1}$/$\overline{SHDN2}$ Pin Current (Note 10)	$V_{\overline{SHDN1}}$, $V_{\overline{SHDN2}}$ = 0V $V_{\overline{SHDN1}}$, $V_{\overline{SHDN2}}$ = 20V	● ●		0 0.85	0.5 3	µA µA
Quiescent Current in Shutdown (per Channel)	V_{IN} = 20V, $V_{\overline{SHDN1}}$ = 0V, $V_{\overline{SHDN2}}$ = 0V			0.3	2	µA
PWRGD Trip Point	% of Nominal Output Voltage, Output Rising	●	86	90	94	%
PWRGD Trip Point Hysteresis (Note 2)	% of Nominal Output Voltage, Output Falling			1.6		%
PWRGD Output Low Voltage	I_{PWRGD} = 100µA	●		15	150	mV
PWRGD Leakage Current	$V_{\overline{SHDN}}$ = 0V, V_{PWRGD} = 20V	●			1	µA

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Ripple Rejection	V_{IN} = 2.72V (Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = Full Current (Note 13)		50	60		dB
	V_{IN} = $V_{OUT(NOMINAL)}$ + 1V, V_{RIPPLE} = 50mV_{RMS} f_{RIPPLE} = 1MHz, I_{LOAD} = Full Current (Note 13)			50		dB
Current Limit (Note 9)	Output 1, V_{IN1} = 6V, V_{OUT1} = 0V V_{IN1} = 2.2V, ΔV_{OUT1} = –0.1V	● ●	1.1 800	1.4	1.7	A mA
	Output 2, V_{IN2} = 6V, V_{OUT2} = 0V V_{IN2} = 2.2V, ΔV_{OUT2} = –0.1V	● ●	350 270	420	490	mA mA
Input Reverse Leakage Current	V_{IN} = –20V, V_{OUT} = 0V	●			1	mA
Reverse Output Current	V_{OUT} = 1.220V, V_{IN} = 0V			0.5	10	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3030 is tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT3030E is 100% tested at T_A = 25°C and performance is guaranteed from 0°C to 125°C. Performance of the LT3030E over the full –40°C to 125°C operating junction temperature range is assured by design, characterization and correlation with statistical process controls. The LT3030I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3030MP is 100% tested and guaranteed over the –55°C to 150°C operating junction temperature range. The LT3030H is tested at 150°C operating junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: The LT3030 is tested and specified for these conditions with the ADJ1/ADJ2 pin connected to the corresponding OUT1/OUT2 pin.

Note 4: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, limit the output current range. When operating at maximum output current, limit the input voltage range.

Note 5: To satisfy minimum input voltage requirements, the LT3030 is tested and specified for these conditions with an external resistor divider (two 243k resistors) for an output voltage of 2.447V. The external resistor divider adds 5µA of DC load on the output.

Note 6: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage equals: $V_{IN} – V_{DROPOUT}$.

Note 7: GND pin current is tested with V_{IN} = 2.447V and a current source load. This means the device is tested while operating in its dropout region or at the minimum input voltage specification. This is the worst-case GND pin current. The GND pin current decreases slightly at higher input voltages. Total GND pin current equals the sum of output 1 and output 2 GND pin currents.

Note 8: ADJ1/ADJ2 pin bias current flows into the pin.

Note 9: The LT3030 contains current limit foldback circuitry. See the Typical Performance Characteristics section for current limit as a function of the $V_{IN} – V_{OUT}$ differential voltage.

Note 10: $\overline{SHDN1}$ and $\overline{SHDN2}$ pin current flows into the pin.

Note 11: The LT3030 minimum input voltage specification limits dropout voltage under some output voltage/load conditions. See the curve of Minimum Input Voltage in the Typical Performance Characteristics section.

Note 12: The LT3030 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 13: The Full Current for I_{LOAD} is 750mA and 250mA for Output 1 and Output 2 respectively.

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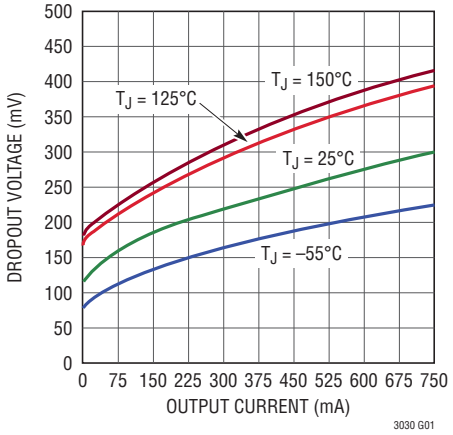
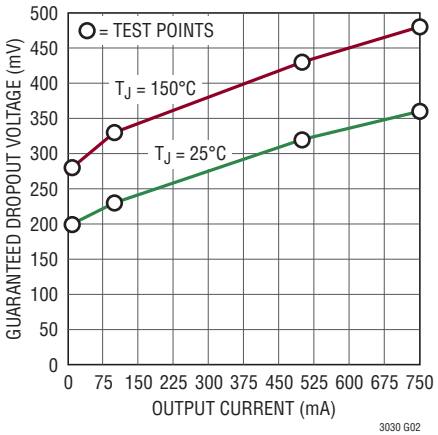
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

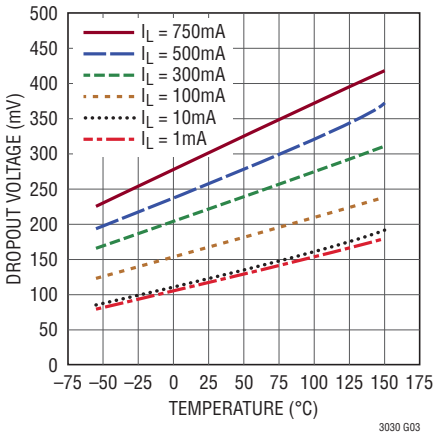
OUT1 Typical Dropout Voltage



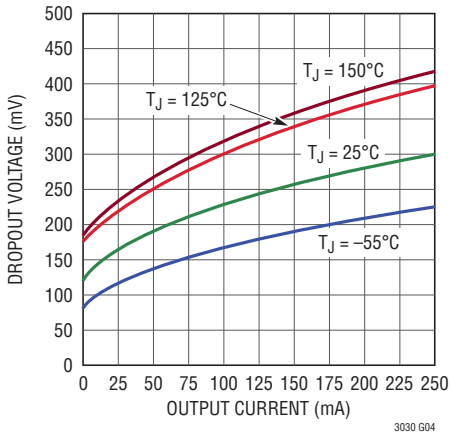
OUT1 Guaranteed Dropout Voltage



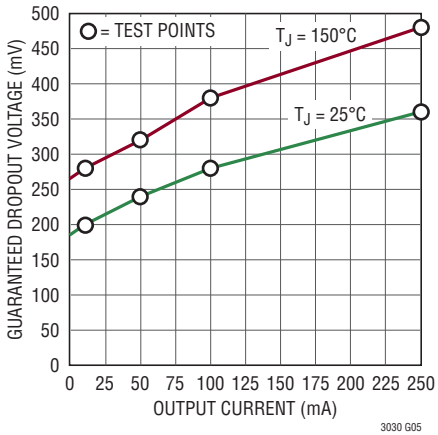
OUT1 Dropout Voltage vs Temperature



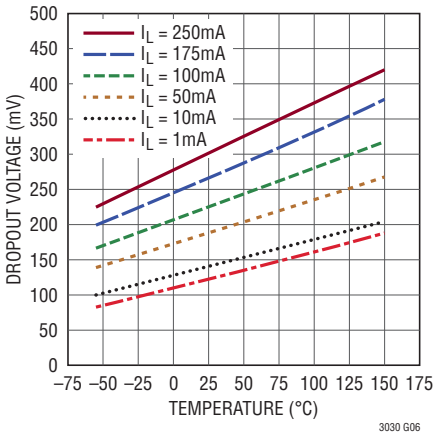
OUT2 Typical Dropout Voltage



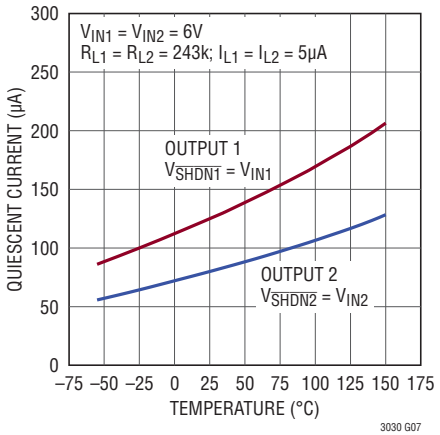
OUT2 Guaranteed Dropout Voltage



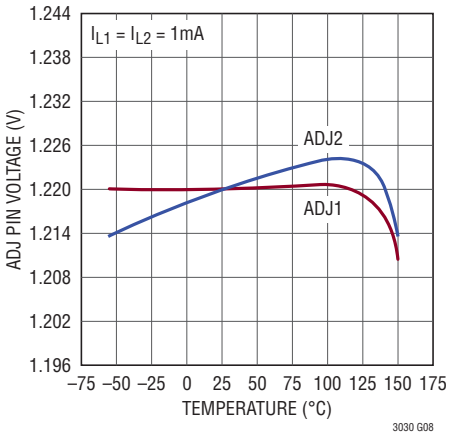
OUT2 Dropout Voltage vs Temperature



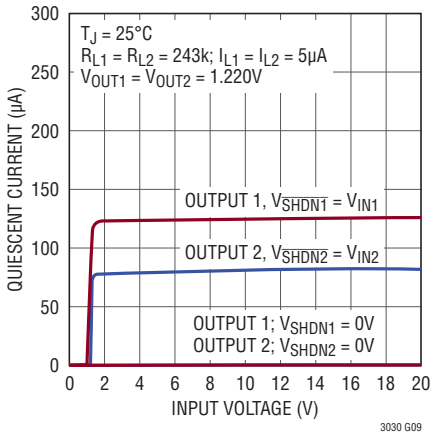
Quiescent Current



ADJ1/ADJ2 Pin Voltage



Quiescent Current



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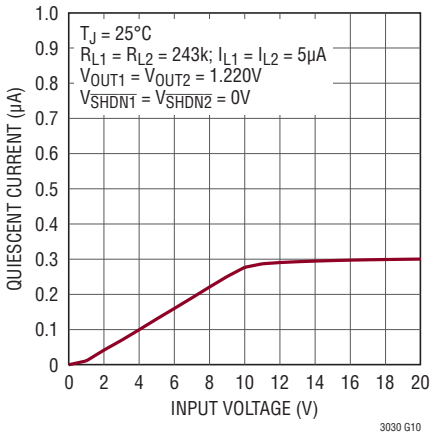
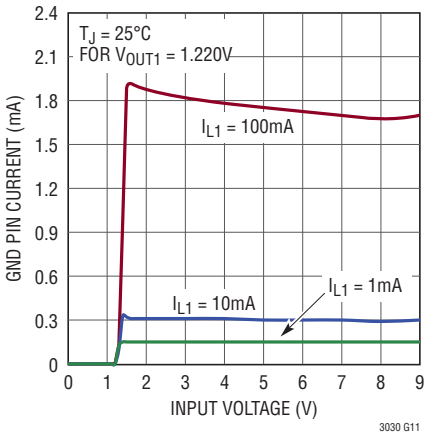
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

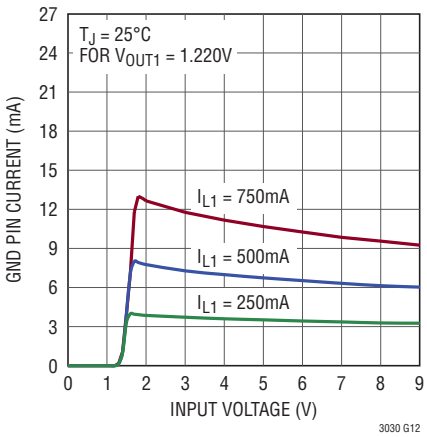
Quiescent Current in Shutdown (per Output)



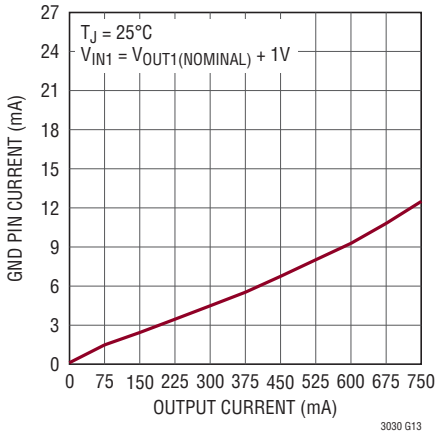
OUT1 GND Pin Current



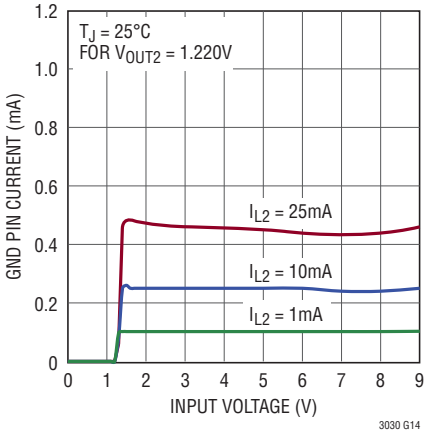
OUT1 GND Pin Current



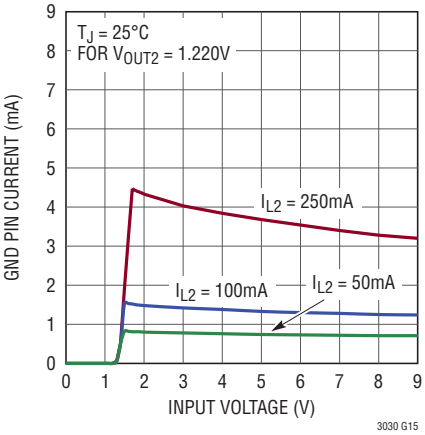
OUT1 GND Pin Current



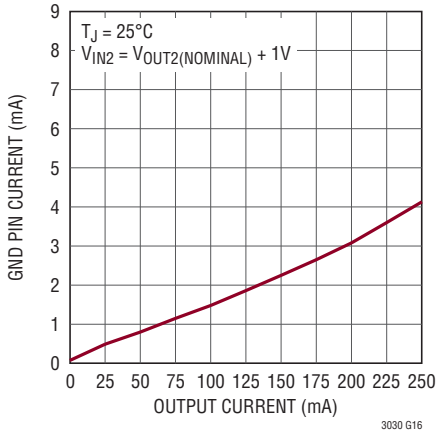
OUT2 GND Pin Current



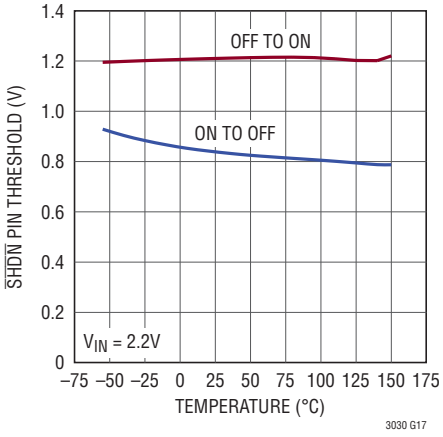
OUT2 GND Pin Current



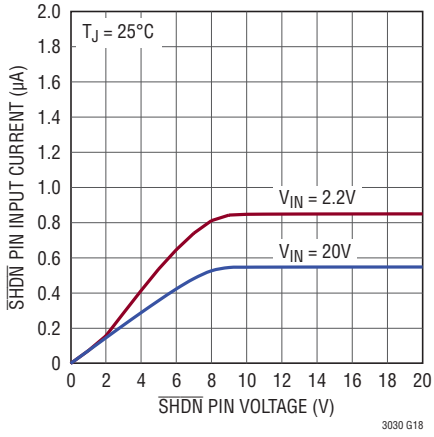
OUT2 GND Pin Current



$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Threshold



$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Input Current



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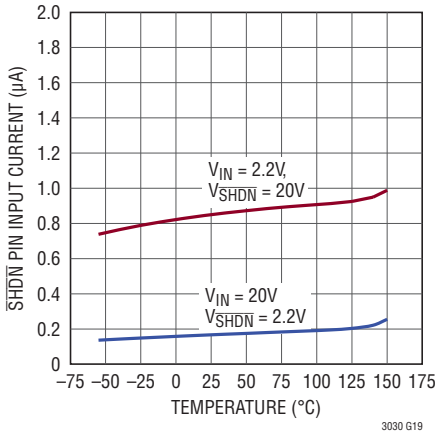
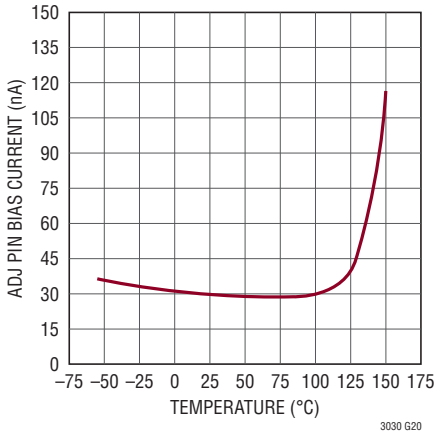
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

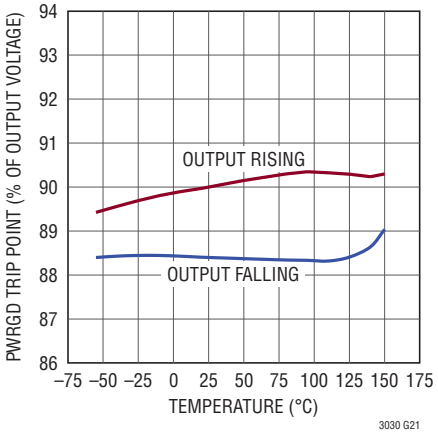
$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Input Current



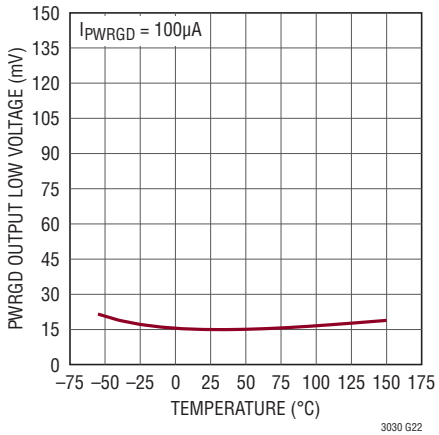
ADJ1 or ADJ2 Pin Bias Current



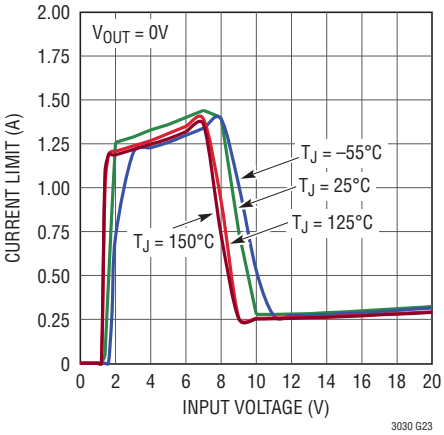
PWRGD1 or PWRGD2 Trip Point



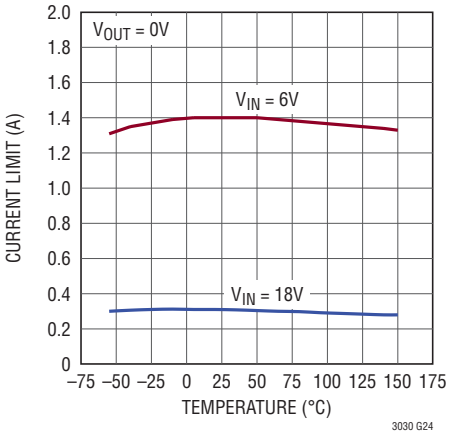
PWRGD1 or PWRGD2 Output Low Voltage



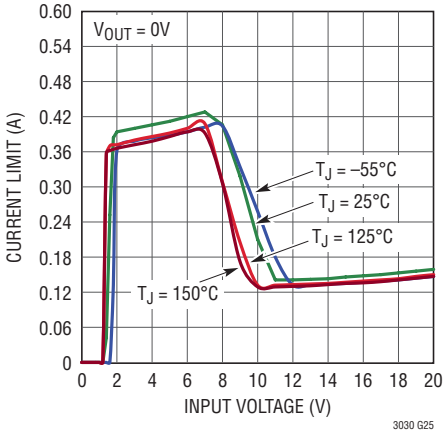
OUT1 Current Limit



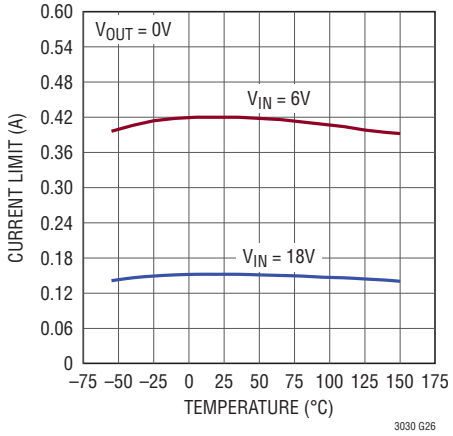
OUT1 Current Limit



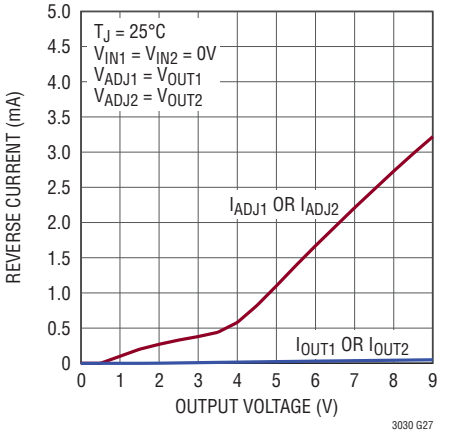
OUT2 Current Limit



OUT2 Current Limit



Reverse Current



I_{ADJ} = FLOWS INTO ADJ PIN TO GND PIN
I_{OUT} = FLOWS INTO OUT PIN TO IN PIN

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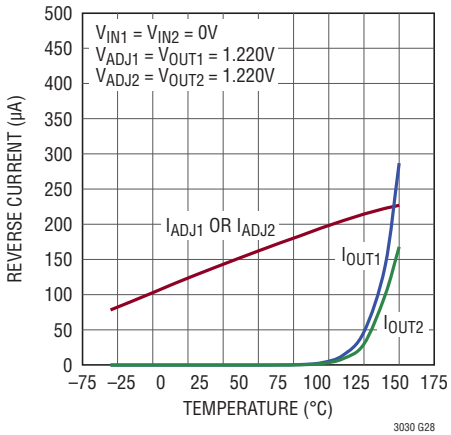
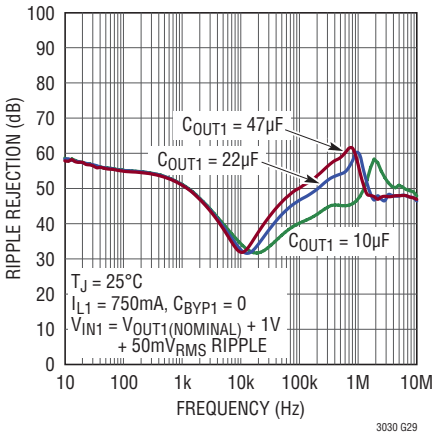
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

Reverse Current

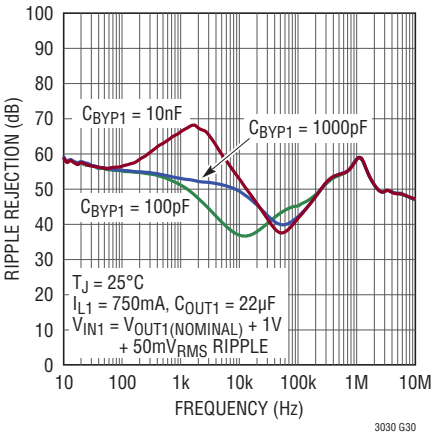


I_{ADJ} = FLOWS INTO ADJ PIN TO GND PIN
I_{OUT} = FLOWS INTO OUT PIN TO IN PIN

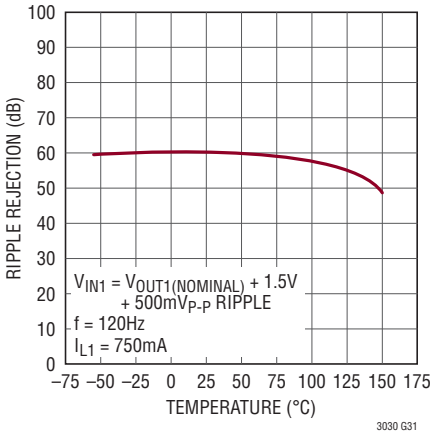
OUT1 Input Ripple Rejection



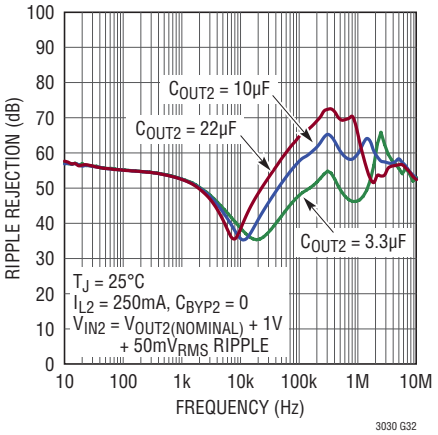
OUT1 Input Ripple Rejection



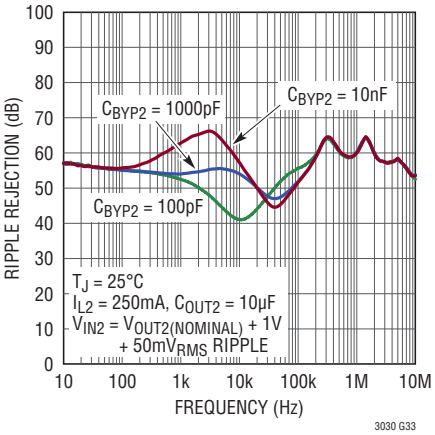
OUT1 Input Ripple Rejection



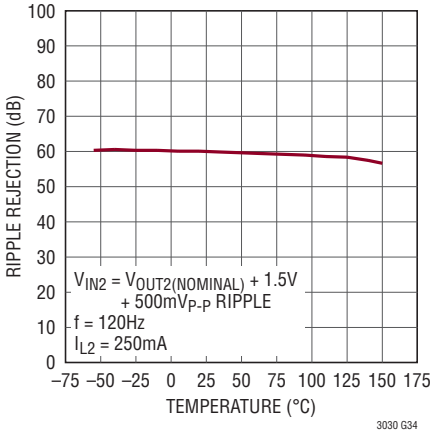
OUT2 Input Ripple Rejection



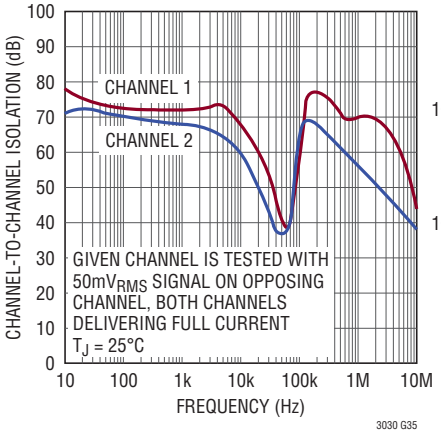
OUT2 Input Ripple Rejection



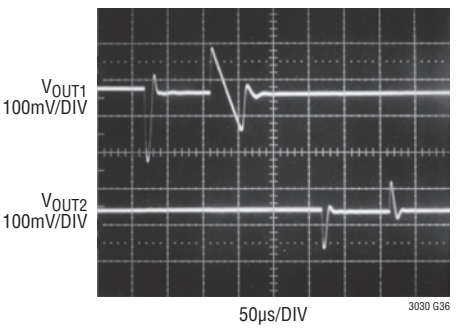
OUT2 Input Ripple Rejection



Channel-to-Channel Isolation



Channel-to-Channel Isolation



C_{OUT1} = 10µF
C_{OUT2} = 3.3µF
C_{BYP1} = C_{BYP2} = 0.01µF
ΔI_{L1} = 50mA TO 750mA
ΔI_{L2} = 50mA TO 250mA
V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 5V

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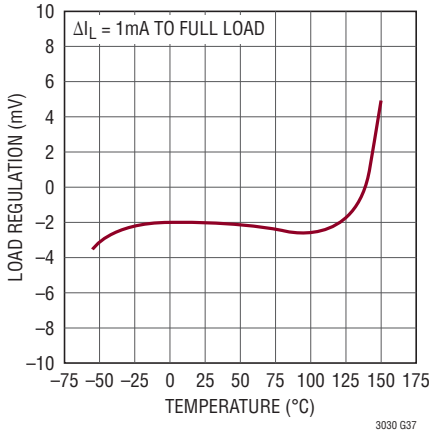
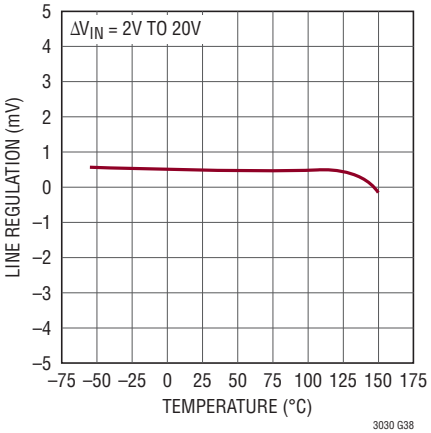
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

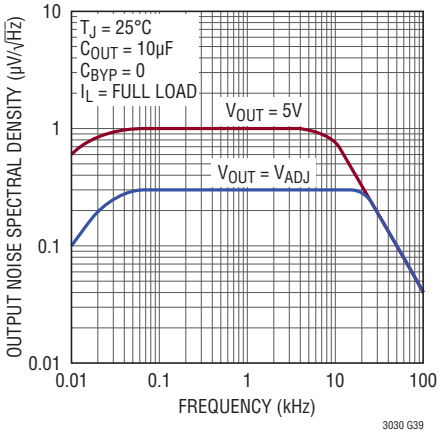
OUT1 or OUT2 Load Regulation



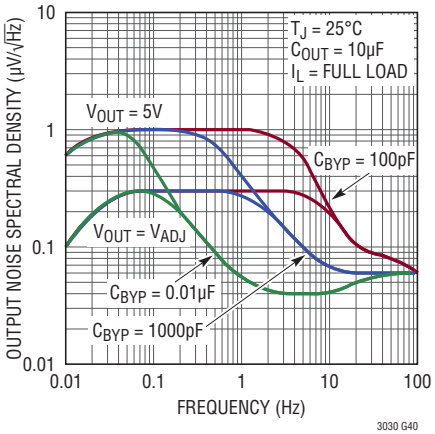
OUT1 or OUT2 Line Regulation



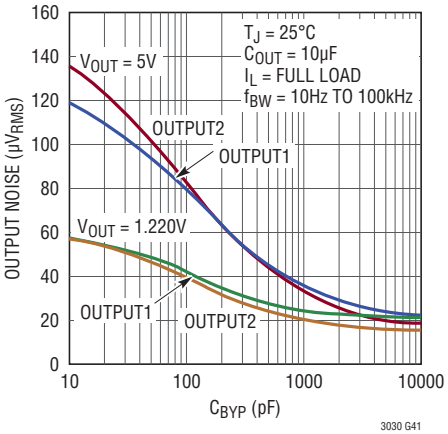
Output Noise Spectral Density



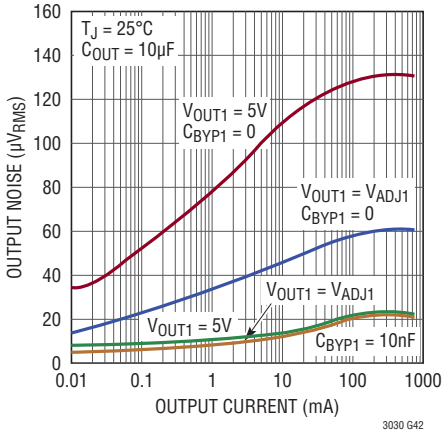
Output Noise Spectral Density



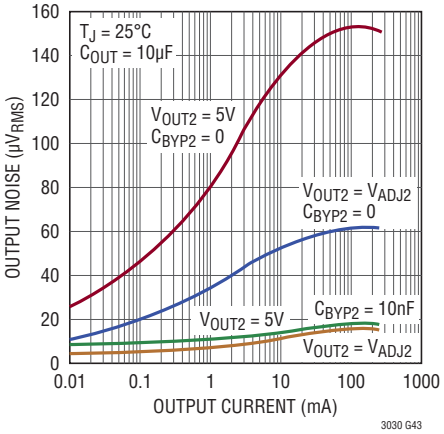
RMS Output Noise vs Bypass Capacitor



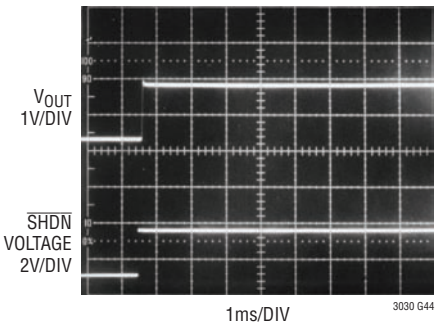
OUT1 RMS Output Noise vs Output Current (10Hz to 100kHz)



OUT2 RMS Output Noise vs Output Current (10Hz to 100kHz)

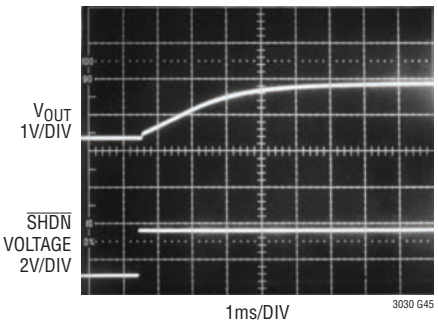


Start-Up Time from Shutdown C_{BYP} = 0pF



V_{IN} = 2.5V
C_{IN} = 10µF
C_{OUT} = 10µF
I_L = FULL LOAD
T_J = 25°C
V_{OUT} = 1.5V

Start-Up Time from Shutdown C_{BYP} = 0.01µF



V_{IN} = 2.5V
C_{IN} = 10µF
C_{OUT} = 10µF
I_L = FULL LOAD
T_J = 25°C
V_{OUT} = 1.5V

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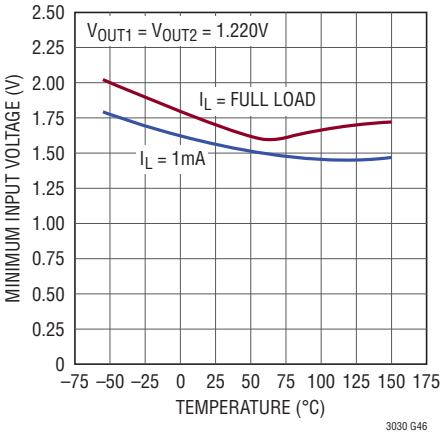
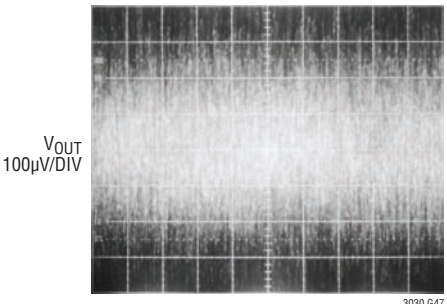
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

OUT1 or OUT2 Minimum Input Voltage

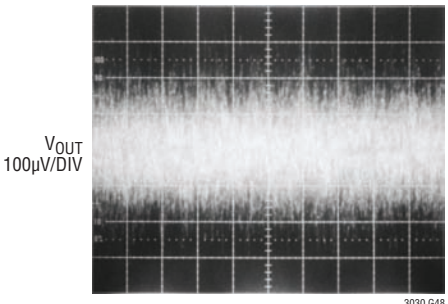


10Hz to 100kHz Output Noise, C_{BYP} = 0pF



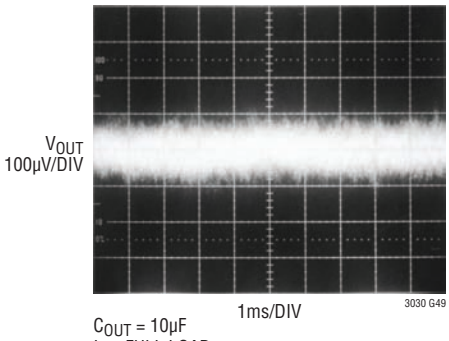
C_{OUT} = 10µF
I_L = FULL LOAD
V_{OUT} = 5V

10Hz to 100kHz Output Noise, C_{BYP} = 100pF



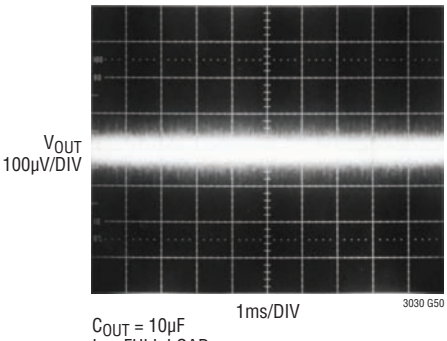
C_{OUT} = 10µF
I_L = FULL LOAD
V_{OUT} = 5V

10Hz to 100kHz Output Noise, C_{BYP} = 1000pF



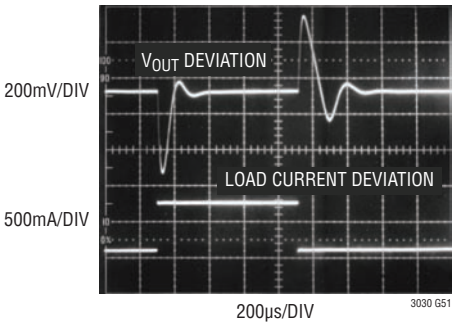
C_{OUT} = 10µF
I_L = FULL LOAD
V_{OUT} = 5V

10Hz to 100kHz Output Noise, C_{BYP} = 0.01µF



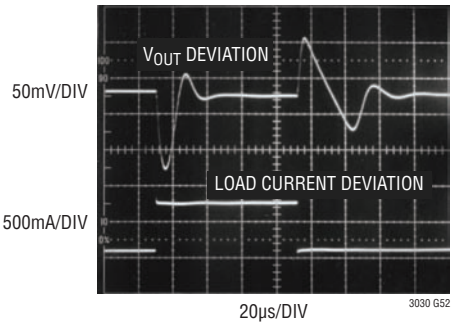
C_{OUT} = 10µF
I_L = FULL LOAD
V_{OUT} = 5V

OUT1 Transient Response C_{BYP} = 0pF



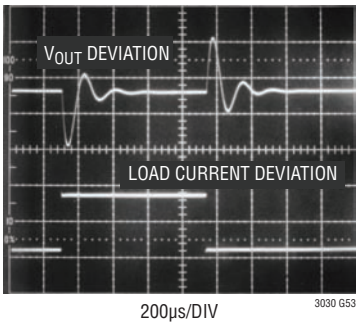
V_{IN} = 6V
C_{IN} = 22µF
C_{OUT} = 22µF
I_L = 100mA TO 750mA
T_J = 25°C
V_{OUT} = 5V

OUT1 Transient Response C_{BYP} = 0.01µF



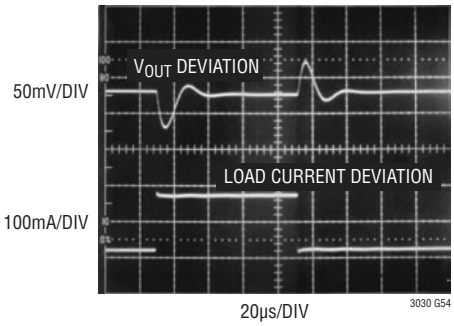
V_{IN} = 6V
C_{IN} = 22µF
C_{OUT} = 22µF
I_L = 100mA TO 750mA
T_J = 25°C
V_{OUT} = 5V

OUT2 Transient Response C_{BYP} = 0pF



V_{IN} = 6V
C_{IN} = 10µF
C_{OUT} = 10µF
I_L = 100mA TO 250mA
T_J = 25°C
V_{OUT} = 5V

OUT2 Transient Response C_{BYP} = 0.01µF



V_{IN} = 6V
C_{IN} = 10µF
C_{OUT} = 10µF
I_L = 100mA TO 250mA
T_J = 25°C
V_{OUT} = 5V

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PIN FUNCTIONS (QFN/TSSOP)

OUT1, OUT2 (Pins 1, 2, 7, 8/Pins 3, 4, 7, 8): Output. The OUT1/OUT2 pins supply power to the loads. A minimum 10µF/3.3µF output capacitor prevents oscillations on OUT1/OUT2. Applications with large output load transients require larger values of output capacitance to limit peak voltage transients. See the Applications Information section for more on output capacitance and on reverse output characteristics.

GND (Pins 3, 4, 5, 6, 11, 12, 13, 18, 19, 24, 25, 26, Exposed Pad Pin 29/Pins 5, 6, 15, 16, Exposed Pad Pin 21): Ground. The exposed pad (backside) of the QFN and TSSOP packages is an electrical connection to GND. To ensure proper electrical and thermal performance, solder the exposed pad to the PCB ground and tie directly to GND pins. Connect the bottom of the output voltage setting resistor divider directly to GND for optimum load regulation performance.

IN1, IN2 (Pins 20, 21, 16, 17/Pins 17, 18, 13, 14): Input. The IN1/IN2 pins supply power to each channel. The LT3030 requires a bypass capacitor at the IN1/IN2 pins if located more than six inches away from the main input filter capacitor. Include a bypass capacitor in battery-powered circuits, as a battery's output impedance rises with frequency. A bypass capacitor in the range of 1µF to 10µF suffices. The LT3030's design withstands reverse voltages on the IN pins with respect to ground and the OUT pins. In the case of a reversed input, which occurs if a battery is plugged in backwards, the LT3030 acts as if a diode is in series with its input. No reverse current flows into the LT3030 and no reverse voltage appears at the load. The device protects itself and the load.

PWRGD1, PWRGD2 (Pins 22, 15/Pins 19, 12): Power Good. The PWRGD flag is an open-collector flag to indicate that the output voltage has increased above 90% of the nominal output voltage. There is no internal pull-up on this pin; a pull-up resistor must be used. The PWRGD pin changes state from an open-collector pull-down to high impedance after the output increases above 90% of the nominal voltage. The maximum pull-down current of the PWRGD pin in the low state is 100µA.

$\overline{\text{SHDN1}}$, $\overline{\text{SHDN2}}$ (Pins 23, 14/Pins 20, 11): Shutdown. Pulling the $\overline{\text{SHDN1}}$ or $\overline{\text{SHDN2}}$ pin low puts its corresponding LT3030 channel into a low power state and turns its output off. The $\overline{\text{SHDN1}}$ and $\overline{\text{SHDN2}}$ pins are completely independent of each other, and each $\overline{\text{SHDN}}$ pin only affects operation on its corresponding channel. Drive the $\overline{\text{SHDN1}}$ and $\overline{\text{SHDN2}}$ pins with either logic or an open collector/drain with pull-up resistors. The resistors supply the pull-up current to the open collectors/drains and the $\overline{\text{SHDN1}}$ or $\overline{\text{SHDN2}}$ current, typically less than 1µA. If unused, connect $\overline{\text{SHDN1}}$ and $\overline{\text{SHDN2}}$ to their corresponding IN pins. Each channel will be in its low power shutdown state if its corresponding $\overline{\text{SHDN}}$ pin is not connected.

ADJ1, ADJ2 (Pins 27, 10/Pins 1, 10): Adjust Pin. These are the error amplifier inputs. These pins are internally clamped to ±9V. A typical input bias current of 30nA flows into the pins (see curve of ADJ1/ADJ2 Pin Bias Current vs Temperature in the Typical Performance Characteristics section). The ADJ1 and ADJ2 pin voltages are 1.220V referenced to ground and the output voltage range is 1.220V to 19.5V.

BYP1, BYP2 (Pins 28, 9/Pins 2, 9): Bypass. Connecting a capacitor between OUT and BYP of a respective channel bypasses the LT3030 reference to achieve low noise performance, improve transient response and soft-start the output. Internal circuitry clamps the BYP1/BYP2 pins to ±0.6V (one V_{BE}) from ground. A small capacitor from the corresponding output to this pin bypasses the reference to lower the output voltage noise. Using a maximum value of 10nF reduces the output voltage noise to a typical 20µV_{RMS} over a 10Hz to 100kHz bandwidth. If not used, this pin must be left unconnected.

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APPLICATIONS INFORMATION

The LT3030 is a dual 750mA/250mA low dropout regulator with independent inputs, micropower quiescent current and shutdown. The device supplies up to 750mA/250mA from the outputs of channel 1/channel 2 at a typical dropout voltage of 300mV. The two regulators share common GND pins and are thermally coupled. However, the two inputs and outputs of the LT3030 operate independently. **Each channel can be shut down independently, but a thermal shutdown fault on either channel shuts off the output on both channels.** The addition of a 10nF reference bypass capacitor lowers output voltage noise to 20μV_{RMS} over a 10Hz to 100kHz bandwidth. Additionally, the reference bypass capacitor improves transient response of the regulator, lowering the settling time for transient load conditions. The low operating quiescent current (120μA/75μA for channel 1/2) drops to typically less than 1μA in shutdown. In addition to the low quiescent current, the LT3030 regulator incorporates several protection features that make it ideal for use in battery powered systems. Most importantly, the device protects itself against reverse input voltages.

Adjustable Operation

Each of the LT3030's channels has an output voltage range of 1.220V to 19.5V. Figure 1 illustrates that the output voltage is set by the ratio of two external resistors. The device regulates the output to maintain the corresponding ADJ pin voltage at 1.220V referenced to ground. R1's current equals 1.220V/R1. R2's current equals R1's current plus the ADJ pin bias current. The ADJ pin bias current, 30nA at 25°C, flows through R2 into the ADJ pin. Use the formula in Figure 1 to calculate output voltage. Linear Technology recommends that the value of R1 be less than 243k to minimize errors in the output voltage due to the ADJ pin bias current. In shutdown, the output turns off and the divider current is zero. Curves of ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature appear in the Typical Performance Characteristics section.

Linear Technology tests and specifies each LT3030 channel with its ADJ pin tied to the corresponding OUT pin for a 1.220V output voltage. Specifications for output voltages greater than 1.220V are proportional to the ratio of desired output voltage to 1.220V:

$V_{OUT}/1.220V$

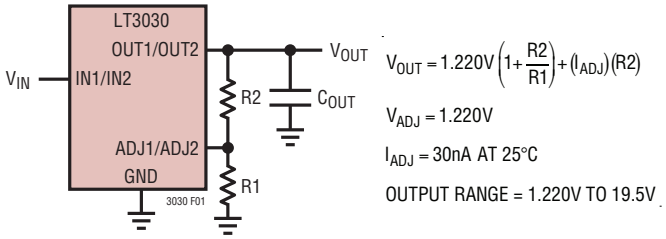

Figure 1. Adjustable Operation

For example, load regulation on OUT2 for an output current change of 1mA to full load current is typically –2mV at V_{OUT2} = 1.220V. At V_{OUT2} = 2.5V, load regulation is:

(2.5V/1.220V) • (–2mV) = –4.1mV

Table 1 shows 1% resistor divider values for some common output voltages with a resistor divider current of approximately 5μA.

Table 1. Output Voltage Resistor Divider Values

V_{OUT} (V)	R1 (k)	R2 (k)
1.5	237	54.9
1.8	237	113
2.5	243	255
3	232	340
3.3	210	357
5	200	619

Bypass Capacitance and Low Noise Performance

Using a bypass capacitor connected between a channel's BYP pin and its corresponding OUT pin significantly lowers LT3030 output voltage noise, but is not required in all applications. Linear Technology recommends a good quality low leakage capacitor. This capacitor bypasses the regulator's reference, providing a low frequency noise pole. A 10nF bypass capacitor introduces a noise pole that decreases output voltage noise to as low as 20μV_{RMS}. Using a bypass capacitor provides the added benefit of improving transient response. With no bypass capacitor and a 10μF output capacitor, a 100mA to full load step settles to within 1% of its final value in approximately 400μs. With the addition of a 10nF bypass capacitor and evaluating the same load step, output voltage excursion stays within 2% (see Transient Response in the Typical Performance Characteristics section). Using a bypass capacitor makes regulator start-up time proportional to the value of the bypass capacitor. For example, a 10nF bypass capacitor and 10μF output capacitor slow start-up time to 15ms.

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APPLICATIONS INFORMATION

Input Capacitance and Stability

Each LT3030 channel is stable with an input capacitor typically between 1µF and 10µF. Applications operating with smaller V_{IN} to V_{OUT} differential voltages and that experience large load transients may require a higher input capacitor value to prevent input voltage droop and letting the regulator enter dropout.

Very low ESR ceramic capacitors may be used. However, in cases where long wires connect the power supply to the LT3030's input and ground, use of low value input capacitors combined with an output load current of greater than 20mA may result in instability. The resonant LC tank circuit formed by the wire inductance and the input capacitor is the cause and not a result of LT3030 instability.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. However, the wire diameter has less influence on its self inductance. For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26" is about half the inductance of a 30-AWG wire with a diameter of 0.01". One foot of 30-AWG wire has 465nH of self-inductance.

Several methods exist to reduce a wire's self-inductance. One method divides the current flowing towards the LT3030 between two parallel conductors. In this case, placing the wires further apart reduces the inductance; up to a 50% reduction when placed only a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed in close proximity to each other, mutual inductance adds to the overall self inductance of the wires. The most effective technique to reducing overall inductance is to place the forward and return current conductors (the input wire and the ground wire) in close proximity. Two 30-AWG wires separated by 0.02" reduce the overall self inductance to about one-fifth of a single wire.

If a battery, mounted in close proximity, powers the LT3030, a 1µF input capacitor suffices for stability. However, if a distantly located supply powers the LT3030, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 1µF minimum) per 8 inches of wire length. The minimum input capacitance needed to stabilize the application also varies with power supply output impedance variations. Placing additional capacitance on the LT3030's output also helps. However, this requires an order of magnitude more capacitance in comparison with additional LT3030 input bypassing. Series resistance between the supply and the LT3030 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use higher ESR tantalum or electrolytic capacitors at the LT3030 input in place of ceramic capacitors.

Output Capacitance and Transient Response

The LT3030 is stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. Linear Technology recommends a minimum output capacitor of 10µF/3.3µF (channel 1 /channel 2) with an ESR of 3Ω, or less, to prevent oscillations. The LT3030 is a micropower device, and output transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes.

Ceramic capacitors require extra consideration. Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics specify the EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients, as shown in Figure 2 and Figure 3. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the applied DC bias voltage and over the operating temperature range. X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Exercise care even when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias (voltage coefficient) with X5R and X7R capacitors is better than with Y5V and Z5U capacitors, but can still be significant enough to drop

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APPLICATIONS INFORMATION

capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as case size increases. Linear Technology recommends verifying expected versus actual capacitance values at operating voltage in situ for an application.

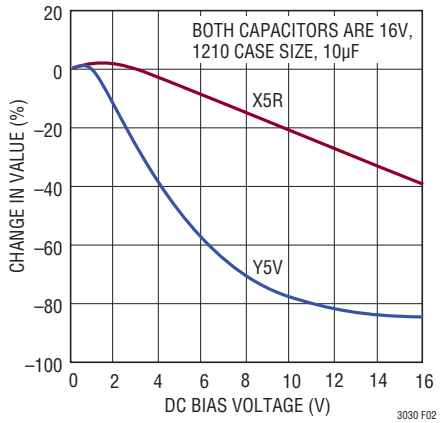

Figure 2. Ceramic Capacitor DC Bias Characteristics

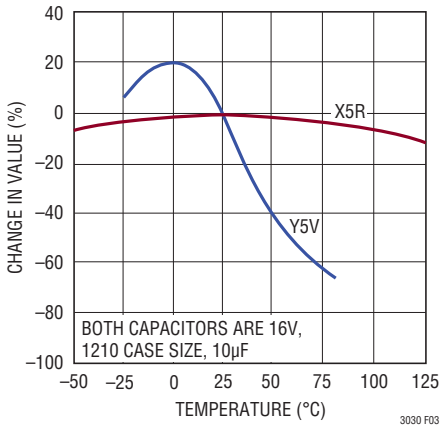

Figure 3. Ceramic Capacitor Temperature Characteristics

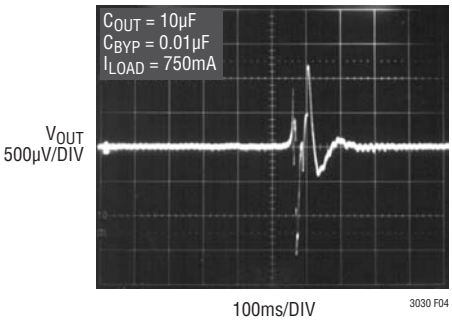

Figure 4. Noise Resulting from Tapping on a Ceramic Capacitor

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise, especially when a ceramic capacitor is used for noise bypassing. A ceramic capacitor produced the trace's response to light tapping from a pencil, as shown in Figure 4. Similar vibration induced behavior can masquerade as increased output voltage noise.

Shutdown/UVLO

The $\overline{SHDN}$ pin is used to put the LT3030 into a micropower shutdown state. The LT3030 has an accurate 1.21V threshold (during turn-on) on the $\overline{SHDN}$ pin. This threshold can be used in conjunction with a resistor divider from the system input supply to define an accurate undervoltage lockout (UVLO) threshold for the regulator. The $\overline{SHDN}$ pin current (at the threshold) needs to be considered when determining the resistor divider network.

PWRGD Flag

The PWRGD flag indicates that the ADJ pin voltage is within 10% of the regulated voltage. The PWRGD pin is an open-collector output, capable of sinking 100µA of current when the ADJ pin voltage is below 90% of the regulated voltage. There is no internal pull-up on the PWRGD pin; an external pull-up resistor must be used. As the ADJ pin voltage rises above 90% of its regulated voltage, the PWRGD pin switches to a high impedance state and the external pull-up resistor pulls the PWRGD pin voltage up. During normal operation, an internal glitch filter prevents the PWRGD pin from switching to a low voltage state if the ADJ pin voltage falls below the regulated voltage by more than 10% in a short transient (<40µs typical) event.

Thermal Considerations

The LT3030's power handling capability limits the maximum rated junction temperature (125°C, LT3030E/LT3030I or 150°C, LT3030H/LT3030MP). Two components comprise the power dissipated by each channel:

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APPLICATIONS INFORMATION

1. Output current multiplied by the input/output voltage differential: $(I_{OUT})(V_{IN} – V_{OUT})$, and
2. GND pin current multiplied by the input voltage: $(I_{GND})(V_{IN})$.

Ground pin current is found by examining the GND Pin Current curves in the Typical Performance Characteristics section.

Power dissipation for each channel equals the sum of the two components listed above. Total power dissipation for the LT3030 equals the sum of the power dissipated by each channel.

The LT3030's internal thermal shutdown circuitry protects both channels of the device if either channel experiences an overload or fault condition. Activation of the thermal shutdown circuitry turns both channels off. If the overload or fault condition is removed, both outputs are allowed to turn back on. For continuous normal conditions, do not exceed the maximum junction temperature rating of 125°C (LT3030E/LT3030I) or 150°C (LT3030H/LT3030MP).

Carefully consider all sources of thermal resistance from junction-to-ambient, including additional heat sources mounted in proximity to the LT3030. For surface mount devices, use the heat spreading capabilities of the PC board and its copper traces to accomplish heat sinking. Copper board stiffeners and plated through-holes can also spread the heat generated by power devices.

The following tables list thermal resistance as a function of copper area in a fixed board size. All measurements were taken in still air on a four-layer FR-4 board with 1oz solid internal planes, and 2oz external trace planes with a total board thickness of 1.6mm. For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD 51-7 and JESD 51-12.

Table 2. UFD Package, 28-Lead QFN

COPPER AREA			
TOPSIDE*	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	30°C/W
1000mm^2	2500mm^2	2500mm^2	32°C/W
225mm^2	2500mm^2	2500mm^2	33°C/W
100mm^2	2500mm^2	2500mm^2	35°C/W

*Device is mounted on topside.

Table 3. FE Package, 20-Lead TSSOP

COPPER AREA			
TOPSIDE*	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	25°C/W
1000mm^2	2500mm^2	2500mm^2	27°C/W
225mm^2	2500mm^2	2500mm^2	28°C/W
100mm^2	2500mm^2	2500mm^2	32°C/W

*Device is mounted on topside.

The junction-to-case thermal resistance (θ_{JC}), measured at the exposed pad on the back of the die, is 3.4°C/W for the QFN package, and 10°C/W for the TSSOP package.

Calculating Junction Temperature

Example: Channel 1's output voltage is set to 1.8V. Channel 2's output voltage is set to 1.5V. Each channel's input voltage is 2.5V. Channel 1's output current range is 0mA to 750mA. Channel 2's output current range is 0mA to 250mA. The application has a maximum ambient temperature of 50°C. What is the LT3030's maximum junction temperature?

The power dissipated by each channel equals:

$$I_{OUT(MAX)}(V_{IN} – V_{OUT}) + I_{GND}(V_{IN})$$

where for output 1:

$I_{OUT(MAX)}$ = 750mA
V_{IN} = 2.5V
I_{GND} at (I_{OUT} = 750mA, V_{IN} = 2.5V) = 13mA

For output 2:

$I_{OUT(MAX)}$ = 250mA
V_{IN} = 2.5V
I_{GND} at (I_{OUT} = 250mA, V_{IN} = 2.5V) = 4.5mA

So, for output 1:

P = 750mA (2.5V – 1.8V) + 13mA (2.5V) = 0.56W

For output 2:

P = 250mA (2.5V – 1.5V) + 4.5mA (2.5V) = 0.26W

The thermal resistance is in the range of 25°C/W to 35°C/W, depending on the copper area. So, the junction temperature rise above ambient temperature approximately equals:

(0.56W + 0.26W) 30°C/W = 24.6°C

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The maximum junction temperature then equals the maximum ambient temperature plus the maximum junction temperature rise above ambient temperature, or:

T_{JMAX} = 50°C + 24.6°C = 74.6°C

Protection Features

The LT3030 regulator incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device protects itself against reverse input voltages and reverse voltages from output to input. The two regulators have independent inputs, a common GND pin and are thermally coupled. However, the two channels of the LT3030 operate independently. Each channel's output can be shut down independently, and a fault condition on one output does not affect the other output electrically, unless the thermal shutdown circuitry is activated.

Current limit protection and thermal overload protection protect the device against current overload conditions at each output of the LT3030. For normal operation, do not allow the junction temperature to exceed 125°C (LT3030E/LT3030I) or 150°C (LT3030H/LT3030MP). The typical thermal shutdown temperature threshold is 165°C and the circuitry incorporates approximately 5°C of hysteresis.

Each channel's input withstands reverse voltages of 22V. Current flow into the device is limited to less than 1mA (typically less than 100µA) and no negative voltage appears at the respective channel's output. The device protects both itself and the load against batteries that are plugged in backwards.

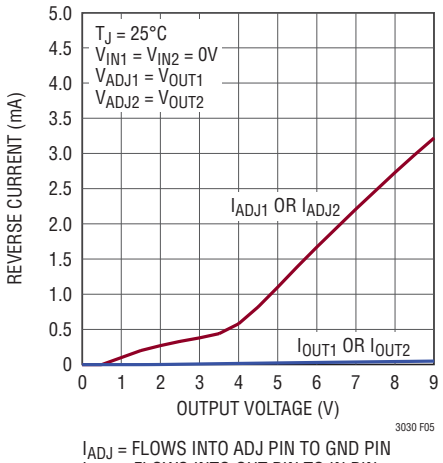
The LT3030 incurs no damage if either channel's output is pulled below ground. If the input is left open-circuit, or grounded, the output can be pulled below ground by 22V. The output acts like an open circuit, and no current flows from the output. However, current flows in (but is limited by) the external resistor divider that sets the output voltage. If the input is powered by a voltage source, the output sources current equal to its current limit capability and the LT3030 protects itself by its thermal limiting circuitry. In this case, grounding the relevant $\overline{SHDN1}$ or $\overline{SHDN2}$ pin turns off its channel's output and stops that output from sourcing current.

The LT3030 incurs no damage if either ADJ pin is pulled above or below ground by 9V. If the input is left open circuit or grounded, the ADJ pins perform like an open circuit down to –1.5V, and then like a 1.2k resistor down to –9V when pulled below ground. When pulled above ground, the ADJ pins perform like an open circuit up to 0.5V, then like a 5.7k resistor up to 3V, then like a 1.8k resistor up to 9V.

In situations where an ADJ pin connects to a resistor divider that would pull the pin above its 9V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5mA. For example, assume a resistor divider sets the regulated output voltage to 1.5V, and the output is forced to 20V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5mA when the ADJ pin is at 9V. The 11V difference between the OUT and ADJ pins divided by the 5mA maximum current into the ADJ pin yields a minimum top resistor value of 2.2k.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open-circuit. Current flow back into the output follows the curve shown in Figure 5.

If either of the LT3030's IN pins is forced below its corresponding OUT pin, or the OUT pin is pulled above its corresponding IN pin, input current for that channel typically



I_{ADJ} = FLOWS INTO ADJ PIN TO GND PIN
I_{OUT} = FLOWS INTO OUT PIN TO IN PIN

Figure 5. Reverse Output Current

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APPLICATIONS INFORMATION

drops to less than 2μA. This occurs if the IN pin is connected to a discharged (low voltage) battery, and either a backup battery or a second regulator circuit holds up the output. The state of that channel's $\overline{SHDN}$ pin has no effect on the reverse output current if the output is pulled above the input.

Overload Recovery

Like many IC power regulators, the LT3030 has safe operating area (SOA) protection. The safe area protection decreases current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protective design provides some output current at all values of input-to-output voltage up to the specified maximum operational input voltage of 20V.

When power is first applied, as input voltage rises, the output follows the input, allowing the regulator to start-up into heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, an event can occur wherein removal of an output short will not allow the output to recover. The event occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short-circuit or if the shutdown pin is pulled high after the input voltage has already been turned on. The load line intersects the output current curve at two points creating two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

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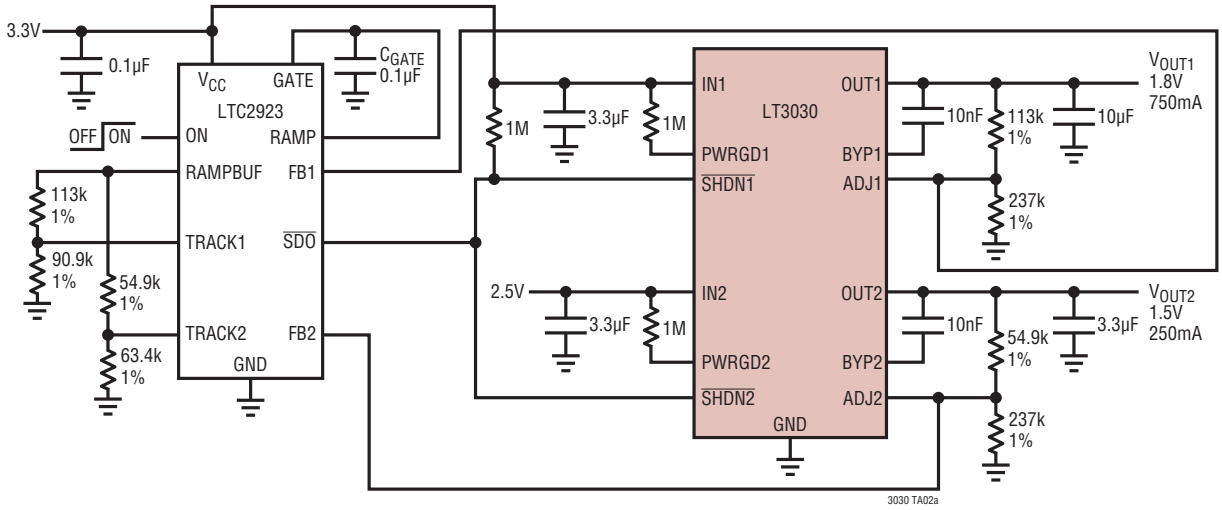
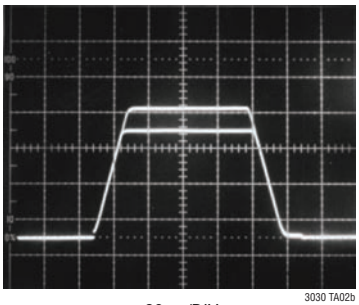
TYPICAL APPLICATIONS

Coincident Tracking Supply Application





20ms/DIV

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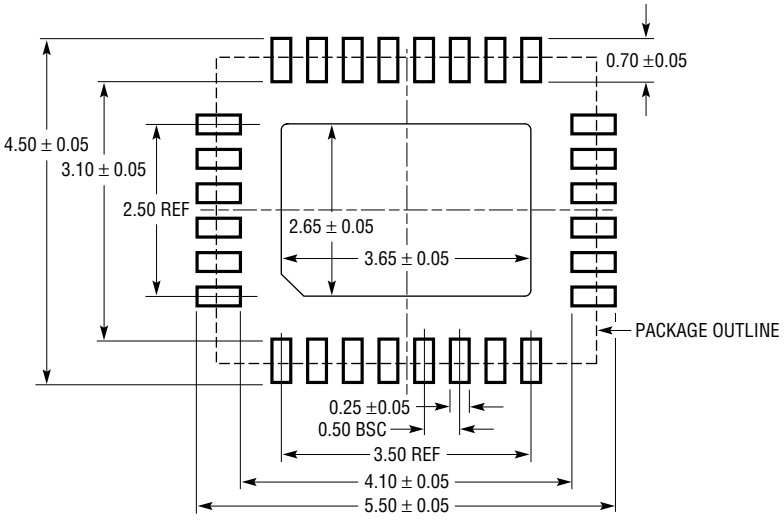
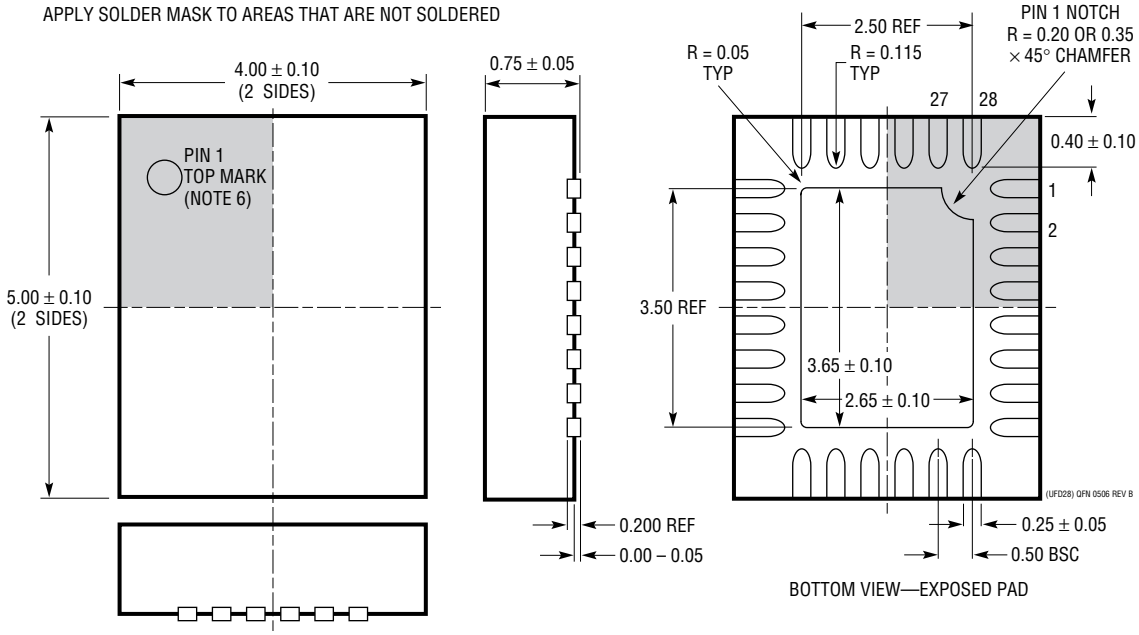
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead (4mm × 5mm) Plastic QFN
(Reference LTC DWG # 05-08-1712 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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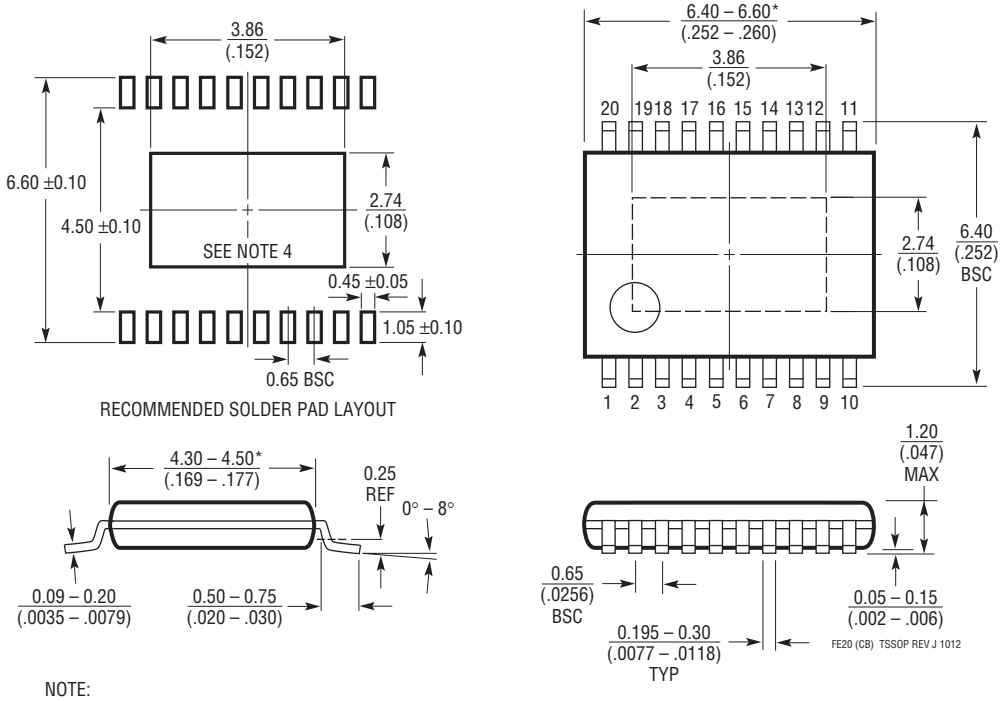
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev J)

Exposed Pad Variation CB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/13	Lowered V_{IN} minimum to 1.7V	1
		Added H-grade in QFN package	2
		Modified OUT2 GND curve pin current graph labels	6

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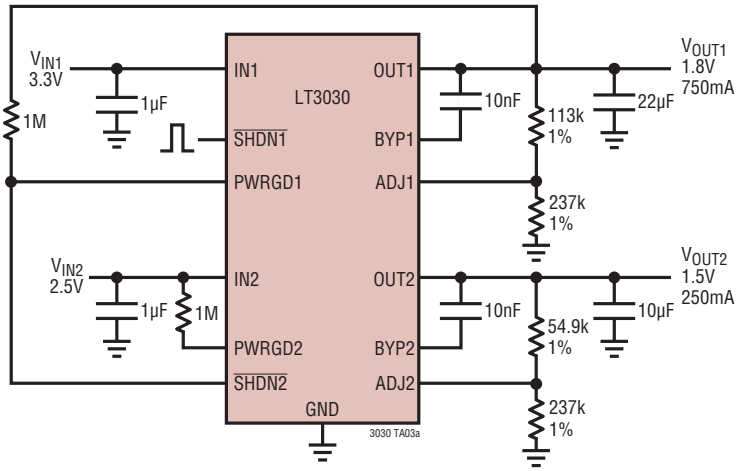
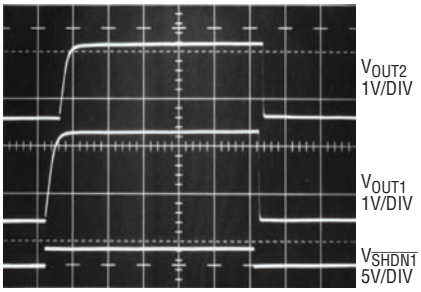
TYPICAL APPLICATION

Sequencing Supply Application





RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise Micropower LDO	V_{IN}: 1.8V to 20V, V_{OUT} = 1.22V, V_{DO} = 0.3V, I_Q = 20µA, I_{SD} <1µA, Low Noise < 20µV_{RMS}, Stable with 1µF Ceramic Capacitors, ThinSOT™ Package
LT1763	500mA, Low Noise Micropower LDO	V_{IN}: 1.8V to 20V, V_{OUT} = 1.22V, V_{DO} = 0.3V, I_Q = 30µA, I_{SD} <1µA, Low Noise < 20µV_{RMS}, S8 Package
LT1963/ LT1963A	1.5A, Low Noise, Fast Transient Response LDOs	V_{IN}: 2.1V to 20V, $V_{OUT(MIN)}$ = 1.21V, V_{DO} = 0.34V, I_Q = 1mA, I_{SD} < 1µA, Low Noise: < 40µV_{RMS}, "A" Version Stable with Ceramic Capacitors, DD, TO220-5, SOT223, S8 Packages
LT1964	200mA, Low Noise Micropower, Negative LDO	V_{IN}: –2.2V to –20V, $V_{OUT(MIN)}$ = 1.21V, V_{DO} = 0.34V, I_Q = 30µA, I_{SD} = 3µA, Low Noise: <30µV_{RMS}, Stable with Ceramic Capacitors, ThinSOT Package
LT1965	1.1A, Low Noise, Fast Transient Response LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.20V, V_{DO} = 0.3V, I_Q = 0.5mA, I_{SD} < 1µA, Low Noise: < 40µV_{RMS}, Stable with Ceramic Capacitors, 3mm × 3mm DFN, MS8E, DD-Pak, TO-220 Packages
LT3023	Dual 100mA, Low Noise, Micropower LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 40µA, I_{SD} <1µA, DFN, MS10 Packages
LT3024	Dual 100mA/500mA, Low Noise, Micropower LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 60µA, I_{SD} <1µA, DFN, TSSOP-16E Packages
LT3027	Dual 100mA, Low Noise, Micropower LDO with Independent Inputs	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 40µA, I_{SD} <1µA, DFN, MS10E Packages
LT3028	Dual 100mA/500mA, Low Noise, Micropower LDO with Independent Inputs	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.30V, I_Q = 60µA, I_{SD} <1µA, DFN, TSSOP-16E Packages
LT3029	Dual 500mA/500mA, Low Noise, Micropower LDO with Independent Inputs	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.215V, V_{DO} = 0.30V, I_Q = 55µA, I_{SD} <1µA, DFN, MSOP-16E Packages
LT3032	Dual 150mA Positive/Negative Low Noise, Low Dropout Linear Regulator	V_{IN}: ±2.3V to ±20V, $V_{OUT(MIN)}$ = ±1.22V, V_{DO} = 0.30V, I_Q = 30µA, I_{SD} <1µA, 14-Lead DFN Package
LT3080/ LT3080-1	1.1A, Parallelable, Low Noise LDO	300mV Dropout Voltage (2-Supply Operation), Low Noise 40µV_{RMS}, V_{IN} = 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors, TO-220, SOT-223, MSOP and 3mm × 3mm DFN

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LT3030
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