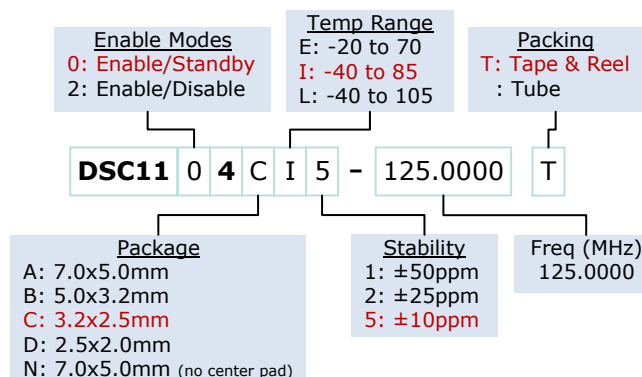


Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	$V_{DD}+0.3$	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
HBM		4000		
MM		400		
CDM		1500		

Ordering Code



Note: 1000+ years of data retention on internal memory

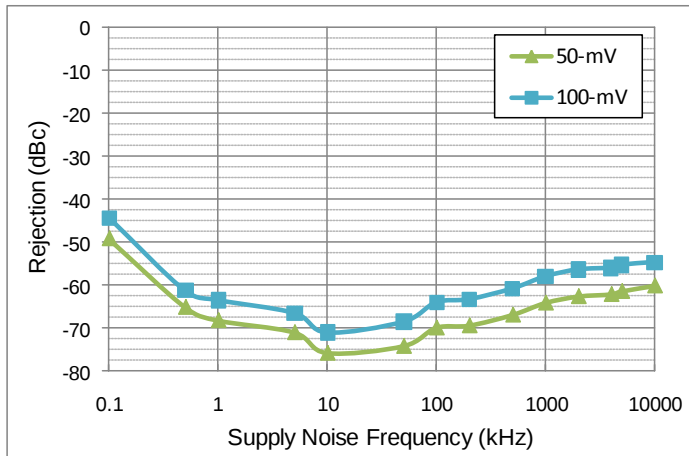
Specifications

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage ¹	V_{DD}		2.25		3.6	V
Supply Current	I_{DD}	EN pin low – outputs are disabled DSC1104 DSC1124		20	0.095 22	mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±10 ±25 ±50	ppm
Aging	Δf	1 year @25°C			±5	ppm
Startup Time ²	t_{SU}	T=25°C			5	ms
Input Logic Levels						
Input logic high	V_{IH}		0.75x V_{DD}		-	V
Input logic low	V_{IL}		-		0.25x V_{DD}	
Output Disable Time ³	t_{DA}				5	ns
Output Enable Time	t_{EN}	DSC1104 DSC1124			5 20	ms ns
Enable Pull-Up Resistor ⁴		Pull-up resistor exist		40		kΩ
HCSL Outputs						
Supply Current	I_{DD}	Output Enabled, $R_L=50\Omega$		40	42	mA
Output Logic Levels						
Output logic high	V_{OH}	$R_L=50\Omega$	0.725		-	V
Output logic low	V_{OL}		-		0.1	
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition time ³						
Rise Time	t_R	20% to 80% $R_L=50\Omega$, $C_L=2pF$	200		400	ps
Fall Time	t_F					
Frequency	f_0	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter	J_{PER}			2.5		ps _{RMS}
Integrated Phase Noise	J_{PH}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.37 1.7	2	ps _{RMS}

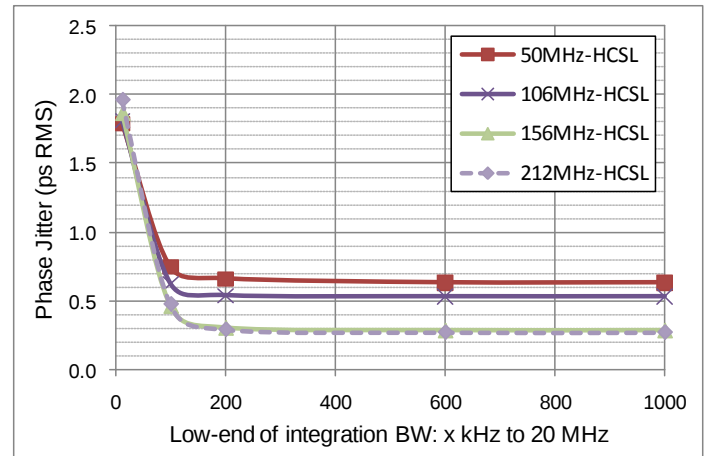
Notes:

- Pin 6 V_{DD} should be filtered with 0.1uF capacitor.
- t_{SU} is time to 100ppm of output frequency after V_{DD} is applied and outputs are enabled.
- Output Waveform and Test Circuit figures below define the parameters.
- Output is enabled if pad is floated or not connected.

Nominal Performance Parameters (Unless specified otherwise: $T=25^{\circ}\text{C}$, $V_{DD}=3.3\text{V}$)

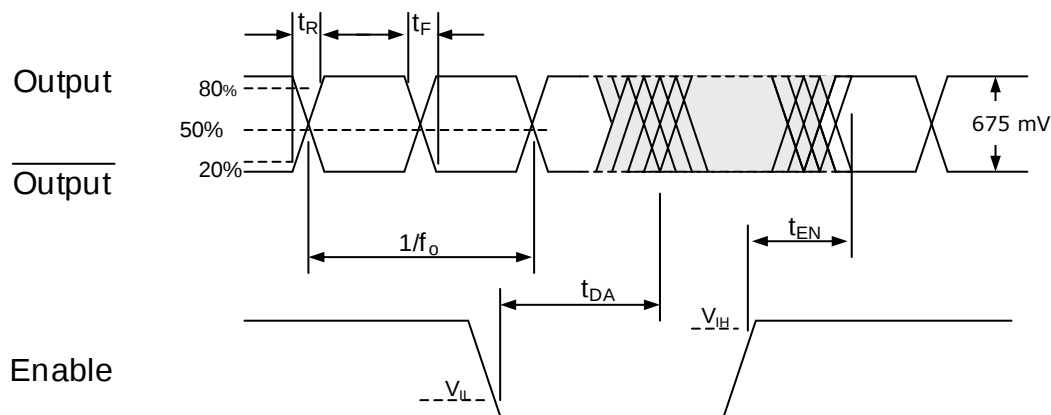


Power supply rejection ratio

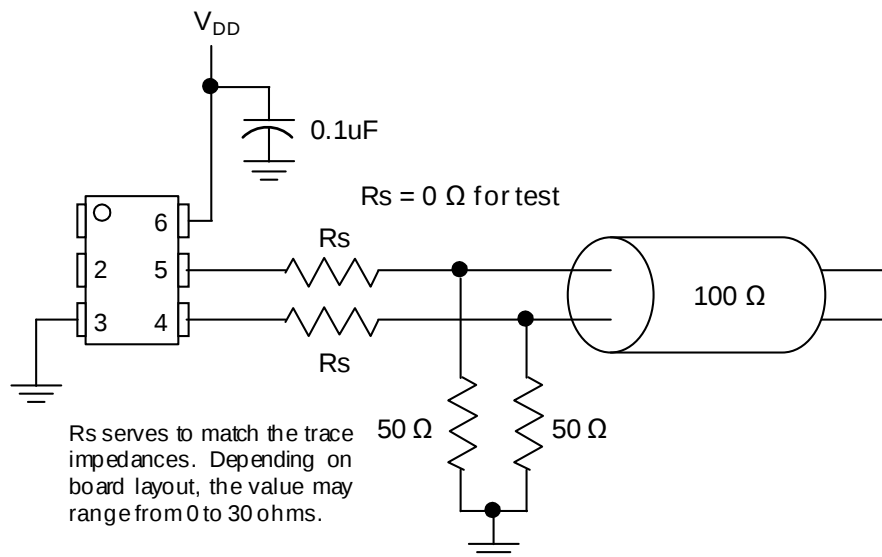


Phase jitter (integrated phase noise)

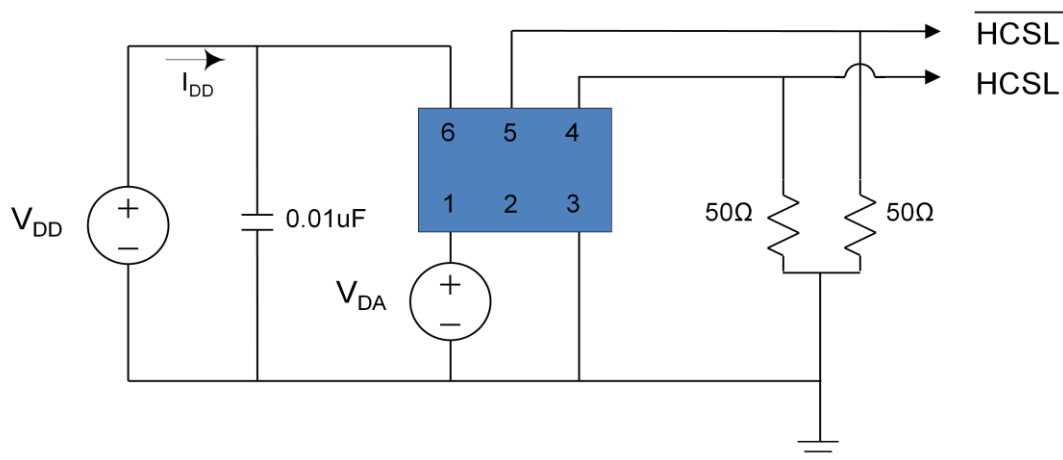
Output Waveform



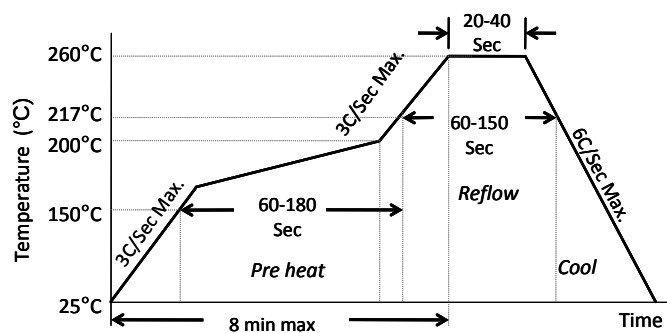
Typical Termination Scheme



Test Circuit



Solder Reflow Profile



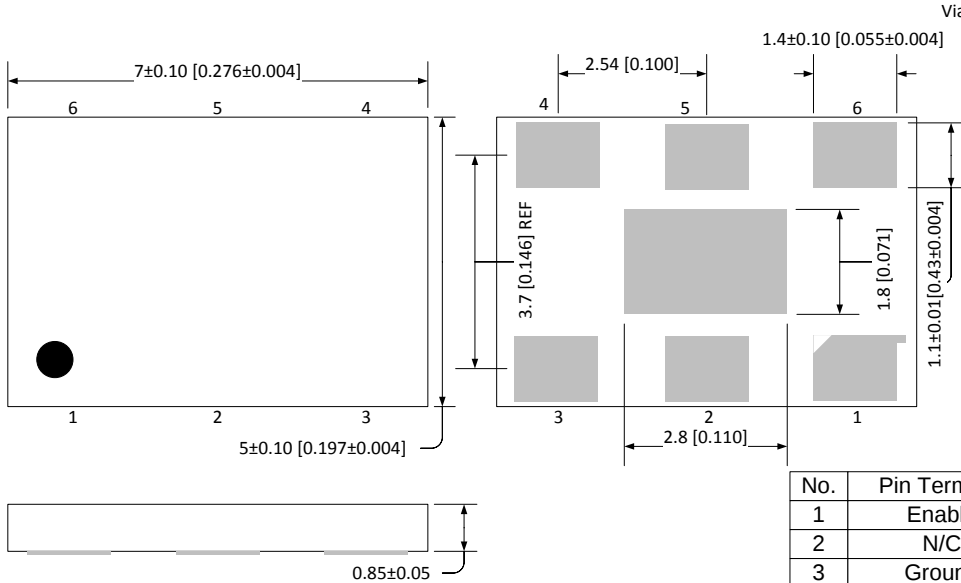
MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

Package Dimensions

7.0 x 5.0 mm Plastic Package

EXTERNAL DIMENSIONS

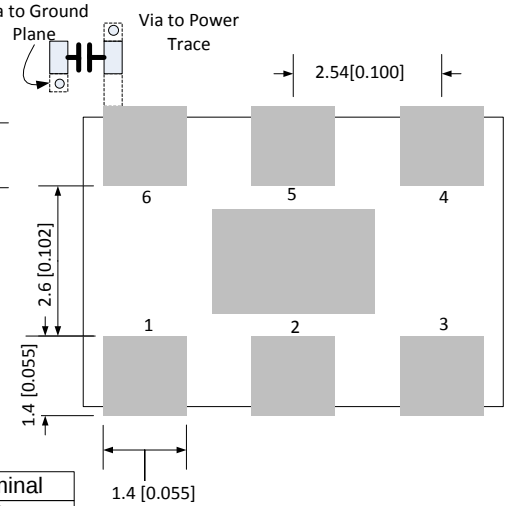
Units: mm [inches]



No.	Pin Terminal
1	Enable
2	N/C
3	Ground
4	OUT
5	OUT-
6	VDD
PAD	TIE TO GND

RECOMMENDED SOLDER PAD LAYOUT

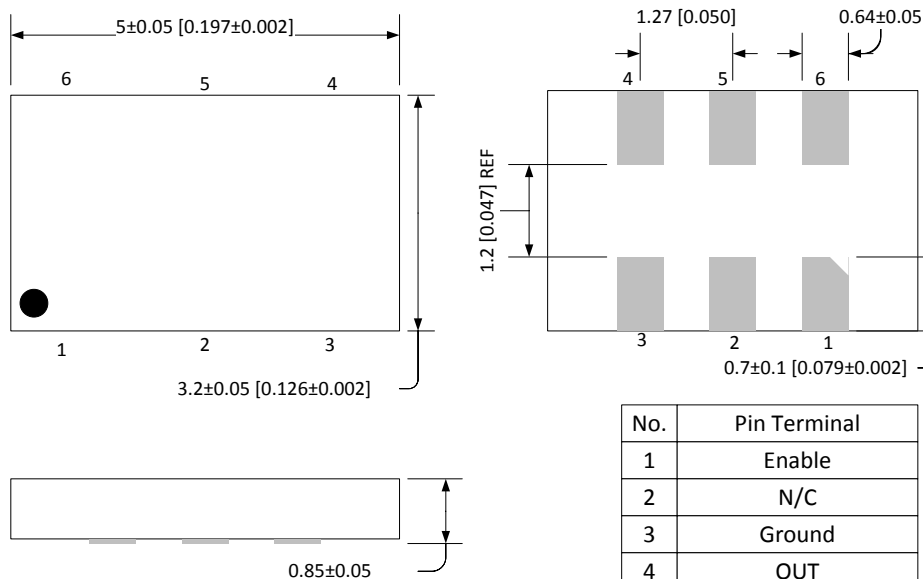
Units: mm [inches]



5.0 x 3.2 mm Plastic Package

EXTERNAL DIMENSIONS

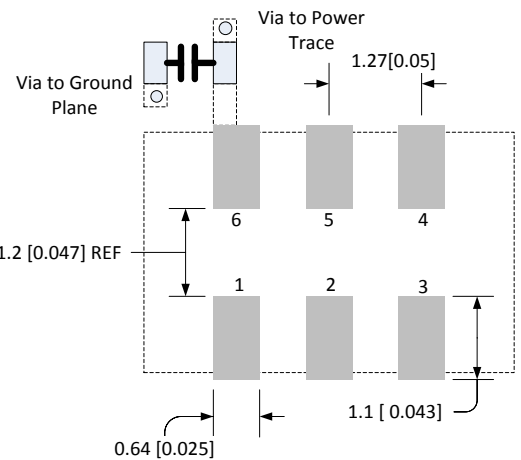
Units: mm [inches]



No.	Pin Terminal
1	Enable
2	N/C
3	Ground
4	OUT
5	OUT-
6	VDD

RECOMMENDED SOLDER PAD LAYOUT

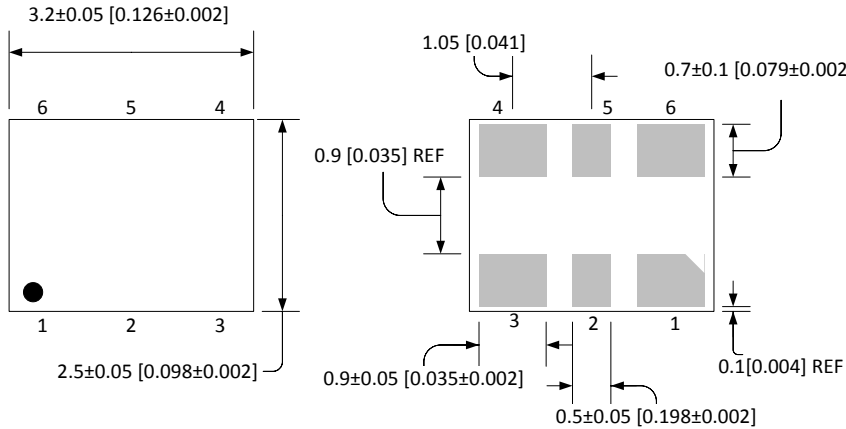
Units: mm [inches]



3.2 x 2.5 mm Plastic Package

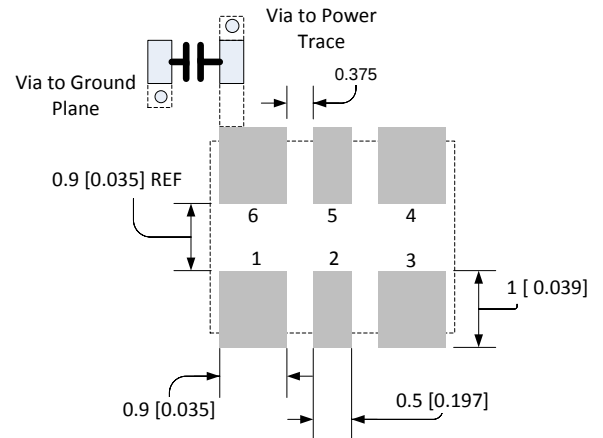
EXTERNAL DIMENSIONS

Units: mm [inches]



RECOMMENDED SOLDER PAD LAYOUT

Units: mm [inches]

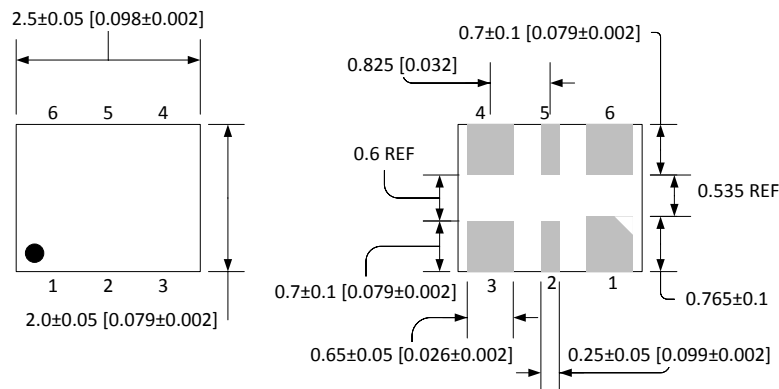


No.	Pin Terminal
1	Enable
2	N/C
3	Ground
4	OUT
5	OUT-
6	VDD

2.5 x 2.0 mm Plastic Package

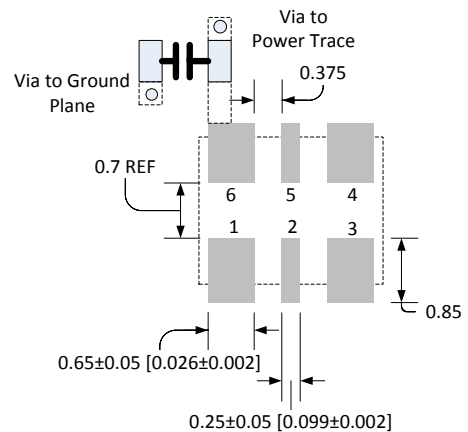
EXTERNAL DIMENSIONS

Units: mm [inches]



RECOMMENDED SOLDER PAD LAYOUT

Units: mm [inches]

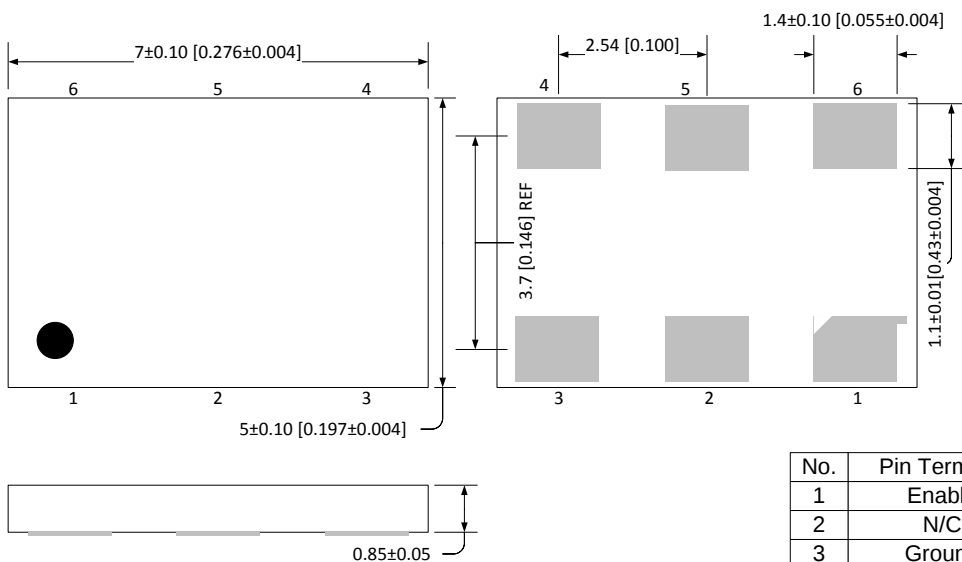


No.	Pin Terminal
1	Enable
2	N/C
3	Ground
4	OUT
5	OUT-
6	VDD

7.0 x 5.0 mm Plastic Package

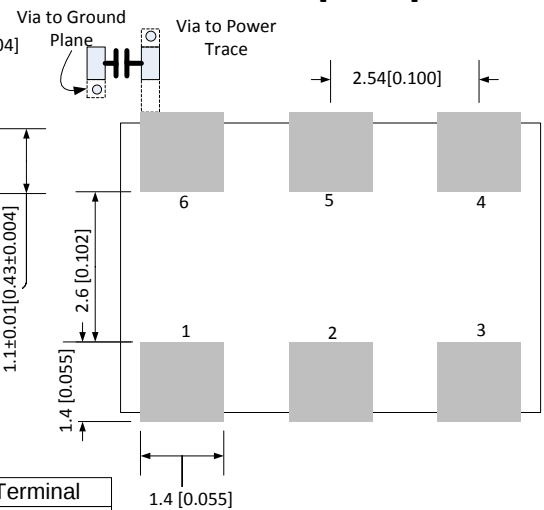
EXTERNAL DIMENSIONS

Units: mm [inches]



RECOMMENDED SOLDER PAD LAYOUT

Units: mm [inches]



No.	Pin Terminal
1	Enable
2	N/C
3	Ground
4	OUT
5	OUT-
6	VDD

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