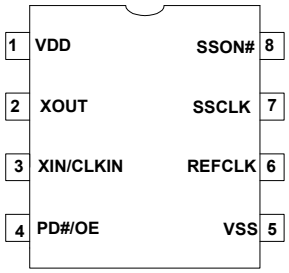
Contents

Pinouts

Figure 1. 8-pin SOIC/TSSOP pinout

CY25100



Pin Description

Pin	Name	Type	Description
1	VDD	Power	3.3 V power supply.
2	XOUT	Output	Crystal output. Leave this pin floating if external clock is connected to pin 3.
3	XIN/CLKIN	Input	Crystal input or reference clock input.
4	PD#/OE	Input	User has the option of choosing either PD# or OE function. Power Down pin: Active LOW. If PD# = 0, PLL and crystal oscillator circuit are powered down, and outputs are weakly pulled low. Output Enable pin: Active HIGH. If OE = 1, SSCLK and REFCLK are enabled.
5	VSS	Power	Power supply ground.
6	REFCLK	Output	Buffered reference output.
7	SSCLK	Output	Spread spectrum clock output.
8	SSON#	Input	Spread spectrum control: Active LOW. 0 = spread on. 1 = spread off.

User Specified Variables

Pin Function	Input Frequency	Total Crystal Load Capacitance	Output Frequency	Spread Percent (0.5% – 5%, 0.25% granularity)	Reference Output	Power Down or Output Enable
Pin Name	XIN and XOUT	XIN and XOUT	SSCLK	SSCLK	REFOUT	PD#/OE
Pin#	3 and 2	3 and 2	7	7	6	4
Unit	MHz	pF	MHz	% and Center- or Down-spread	On or Off	Select PD# or OE
	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED	USER SPECIFIED

Programming Description

Field Programmable CY25100

The CY25100 is programmed at the package level, and must be programmed prior to installation on a circuit board. Field programmable devices are denoted by an “F” in the ordering code, and are blank when shipped. The CY25100 is Flash technology based, which allows it to be reprogrammed up to 100 times. This allows fast and easy design changes and product updates, and eliminates issues with old and out of date inventory.

Samples and small prototype quantities can be programmed on the CY3672 programmer with the CY3690 (TSSOP package) or CY3691 (SOIC package) socket adapter.

CY3672 Programmer and CY3690/CY3691 Socket Adapters

The Cypress CY3672 programmer and the CY3690 or CY3691 socket adapter may be used to program field programmable versions of the CY25100. The CY3690 enables users to program the CY25100ZXCF and CY25100ZXIF (TSSOP). CY3691 provides the ability to program the CY25100SXCF and CY25100SXIF (SOIC). The CY3690 and CY3691 are separate orderable items, so the existing users of the CY3672 programmer need to order only the specific socket adapter to program the CY25100.

Factory Programmable CY25100

Factory programming by Cypress is available for high volume orders. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.

Product Functions

Input Frequency (XIN, Pin 3 and XOUT, Pin 2)

The input to the CY25100 can be a crystal or a clock. The input frequency range for crystals is 8 to 30 MHz, and for clock signals is 8 to 166 MHz.

C_{XIN} and C_{XOUT} (Pin 3 and Pin 2)

The CY25100 has internal load capacitors at Pin 3 (C_{XIN}) and Pin 2 (C_{XOUT}) C_{XIN} always equals C_{XOUT}, and they are programmable from 12 pF to 60 pF, in 0.5 pF increments.This feature eliminates the need for external crystal load capacitors.

The following formula is used to calculate the value of C_{XIN} and C_{XOUT} for matching the crystal load (C_L):

$C_{XIN} = C_{XOUT} = 2C_L – C_P$

where C_L is the crystal load capacitor as specified by the crystal manufacturer and C_P is the parasitic PCB capacitance on each node of the crystal.

For example, if a crystal with C_L of 16 pF is used, and C_P is 2 pF, C_{XIN} and C_{XOUT} are calculated as:

$C_{XIN} = C_{XOUT} = (2 \times 16) – 2 = 30$ pF

If using a driven reference, set C_{XIN} and C_{XOUT} to the minimum value 12 pF, connect the reference to XIN/CLKIN, and leave XOUT unconnected.

Output Frequency (SSCLK, Pin 7)

The modulated frequency at the SSCLK output is produced by synthesizing the input reference clock. The modulation can be stopped by SSON# digital control input (SSON# = HIGH, no modulation). If modulation is stopped, the clock frequency is the nominal value of the synthesized frequency without modulation (spread percentage = 0). The range of synthesized clock is from 3 to 200 MHz.

Spread Percentage (SSCLK, Pin 7)

The SSCLK spread can be programmed at any percentage value from ±0.25% to ±2.5% for center spread and from –0.5% to –5.0% for down spread.

Reference Output (REFOUT, Pin 6)

The reference clock output has the same frequency and the same phase as the input clock. This output can be programmed to be enabled (clock on) or disabled (High Z, clock off). If this output is not required, it is recommended that the disabled (High Z, Clock Off) option be selected.

Modulation Frequency

The modulation frequency is 31.5 kHz for all SSCLK frequencies from 3 to 200 MHz.

Power Down or Output Enable (PD# or OE, Pin 4)

The part can be programmed to include either PD# or OE function. PD# function powers down the oscillator and PLL. The OE function disables the outputs.

Absolute Maximum Ratings

Supply Voltage (V_{DD}) ..... –0.5 to +7.0 V

DC Input Voltage ..... –0.5 V to V_{DD} + 0.5 V

Storage Temperature (Non condensing) ..... –55 °C to +125 °C

Junction Temperature ..... –40 °C to +125 °C

Data Retention at Tj = 125 °C .....> 10 years

Package Power Dissipation ..... 350 mW

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... ≥ 2000V

Recommended Crystal Specifications

Parameter	Description	Comments	Min	Typ	Max	Unit
f_{NOM}	Nominal Crystal Frequency	Parallel resonance, fundamental mode, AT cut	8	–	30	MHz
C_{LNOM}	Nominal Load Capacitance	Internal load caps	6	–	30	pF
R_1	Equivalent Series Resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of Third Overtone Mode ESR to Fundamental Mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	–
DL	Crystal Drive Level	No external series resistor assumed	–	0.5	2	mW

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	3.13	3.30	3.45	V
T_A	Ambient Commercial Temperature	0	–	70	°C
	Ambient Industrial Temperature	–40	–	85	°C
C_{LOAD}	Maximum Load Capacitance at Pin 6 and Pin 7	–	–	15	pF
f_{REF}	External Reference Crystal (Fundamental tuned crystals only)	8	–	30	MHz
	External Reference Clock	8	–	166	MHz
f_{SSCLK}	SSCLK Output Frequency, C_{LOAD} = 15 pF	3	–	200	MHz
f_{REFCLK}	REFCLK Output Frequency, C_{LOAD} = 15 pF	8	–	166	MHz
f_{MOD}	Spread Spectrum Modulation Frequency	30.0	31.5	33.0	kHz
t_{PU}	Power Up Time for all V_{DD}'s to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$ V, $V_{DD} = 3.3$ V (source)	10	12	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$ V, $V_{DD} = 3.3$ V (sink)	10	12	–	mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7 × V_{DD}	–	V_{DD}	V
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	–	–	0.3 × V_{DD}	V
I_{IH}	Input High Current, PD#/OE and SSON# Pins	$V_{in} = V_{DD}$	–10	–	10	µA
I_{IL}	Input Low Current, PD#/OE and SSON# Pins	$V_{in} = V_{SS}$	–10	–	10	µA
I_{OZ}	Output Leakage Current	Three-state output, PD#/OE = 0, output pulldown resistor disabled	–10	–	10	µA
C_{XIN} or C_{XOUT}[1]	Programmable Capacitance at Pin 2 and Pin 3	Capacitance at minimum setting	–	12	–	pF
		Capacitance at maximum setting	–	60	–	pF
C_{IN}[1]	Input Capacitance at Pin 4 and Pin 8	Input pins excluding XIN and XOUT	–	5	7	pF
I_{VDD}	Supply Current	$V_{DD} = 3.45$ V, Fin = 30 MHz, REFCLK = 30 MHz, SSCLK = 66 MHz, $C_{LOAD} = 15$ pF, PD#/OE = SSON# = V_{DD}	–	25	35	mA
I_{DDS}	Standby Current	$V_{DD} = 3.45$ V, Device powered down with PD# = 0 V (driven reference pulled down)	–	15	30	µA

Thermal Resistance

Parameter [2]	Description	Test Conditions	8-pin SOIC	8-pin TSSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	134	161	°C/W
θ_{JC}	Thermal resistance (junction to case)		49	31	°C/W

Notes
1. Guaranteed by characterization, not 100% tested.
2. These parameters are guaranteed by design and are not tested.

AC Electrical Characteristics

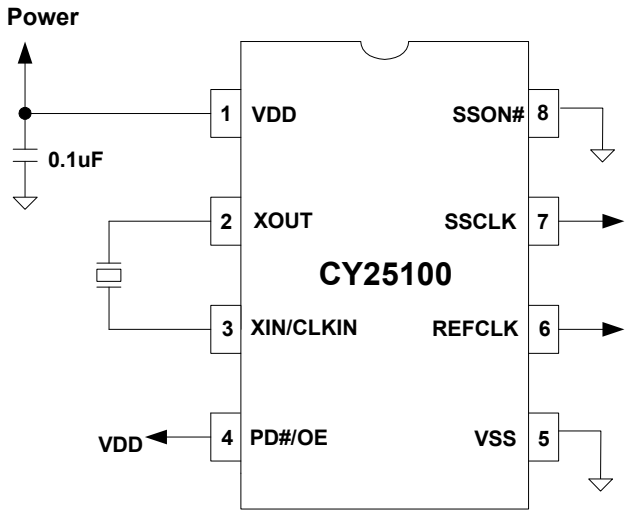
The AC Electrical Characteristics for part CY25100 is as follows. [3]

Parameter	Description	Condition	Min	Typ	Max	Unit
DC	Output Duty Cycle	SSCLK, Measured at $V_{DD}/2$	45	50	55	%
	Output Duty Cycle	REFCLK, Measured at $V_{DD}/2$, Duty Cycle of CLKIN = 50% at input bias	40	50	60	%
SR1	Rising Edge Slew Rate	SSCLK from 3 to 100 MHz; REFCLK from 3 to 100 MHz; 20%–80% of V_{DD}	0.7	1.1	3.6	V/ns
SR2	Falling Edge Slew Rate	SSCLK from 3 to 100 MHz; REFCLK from 3 to 100 MHz; 80%–20% of V_{DD}	0.7	1.1	3.6	V/ns
SR3	Rising Edge Slew Rate	SSCLK from 100 to 200 MHz; REFCLK from 100 to 166 MHz; 20%–80% of V_{DD}	1.0	1.6	4.0	V/ns
SR4	Falling Edge Slew Rate	SSCLK from 100 to 200 MHz; REFCLK from 100 to 166 MHz; 80%–20% of V_{DD}	1.2	1.6	4.0	V/ns
t_{CCJ1}[4]	Cycle-to-Cycle Jitter, SSCLK (Pin 7)	CLKIN = SSCLK = 166 MHz, 2% spread, REFCLK off	–	90	120	ps
		CLKIN = SSCLK = 66 MHz, 2% spread, REFCLK off	–	100	130	ps
		CLKIN = SSCLK = 33 MHz, 2% spread, REFCLK off	–	130	170	ps
t_{CCJ2}[4]	Cycle-to-Cycle Jitter, SSCLK (Pin 7)	CLKIN = SSCLK = 166 MHz, 2% spread, REFCLK on	–	100	130	ps
		CLKIN = SSCLK = 66 MHz, 2% spread, REFCLK on	–	105	140	ps
		CLKIN = SSCLK = 33 MHz, 2% spread, REFCLK on	–	200	260	ps
t_{CCJ3}[4]	Cycle-to-Cycle Jitter, REFCLK (Pin 6)	CLKIN = SSCLK = 166 MHz, 2% spread, REFCLK on	–	80	100	ps
		CLKIN = SSCLK = 66 MHz, 2% spread, REFCLK on	–	100	130	ps
		CLKIN = SSCLK = 33 MHz, 2% spread, REFCLK on	–	135	180	ps
t_{STP}	Power down Time (pin 4 = PD#)	Time from falling edge on PD# to stopped outputs (Asynchronous)	–	150	350	ns
t_{OE1}	Output Disable Time (pin 4 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)	–	150	350	ns
t_{OE2}	Output Enable Time (pin 4 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	150	350	ns
t_{PU1}	Power Up Time, Crystal is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)	–	3.5	5	ms
t_{PU2}	Power Up Time, Reference clock is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous), reference clock at correct frequency	–	2	3	ms

Notes
3. Guaranteed by characterization, not 100% tested.
4. Jitter is configuration dependent. Actual jitter is dependent on XIN jitter and edge rate, number of active outputs, output frequencies, spread percentage, temperature, and output load.

Application Circuit

Figure 2. Application Circuit Diagram [5, 6, 7]



Notes

5. Because the load capacitors (C_{XIN} and C_{XOUT}) are provided by the CY25100, no external capacitors are needed on the X_{IN} and X_{OUT} pins to match the crystal load capacitor (C_L). Only a single 0.1-µF bypass capacitor is required on the V_{DD} pin.
6. If an external clock is used, apply the clock to X_{IN} (pin 3) and leave X_{OUT} (pin 2) floating (unconnected).
7. If SSON# (pin 8) is LOW (V_{SS}), the frequency modulation is on at SSCLK (pin 7).

Switching Waveforms

Figure 3. Duty Cycle Timing (DC = t_{1A}/t_{1B})

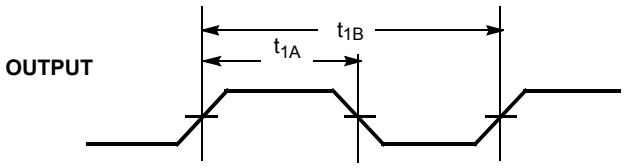
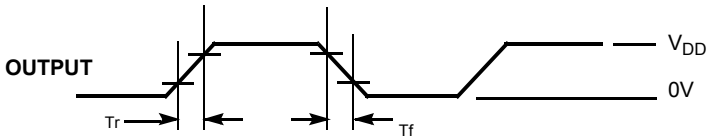


Figure 4. Output Rise/Fall Time (SSCLK and REFCLK)



Output Rise time (Tr) = (0.6 x V_{DD})/SR1 (or SR3)
Output Fall time (Tf) = (0.6 x V_{DD})/SR2 (or SR4)

Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

Figure 5. Power Down and Power Up Timing

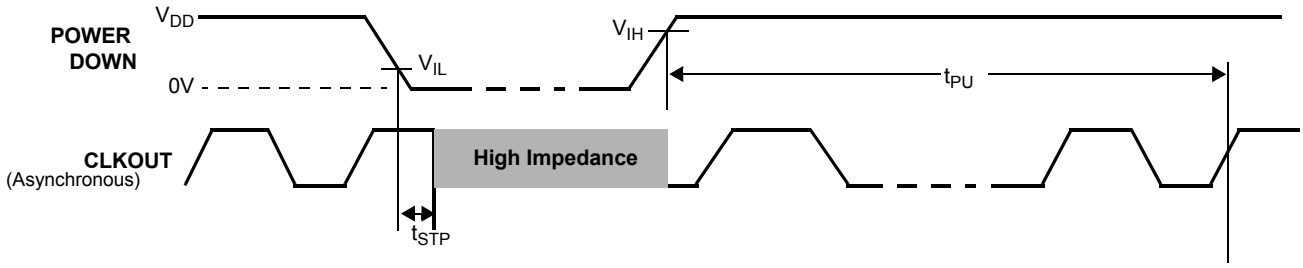
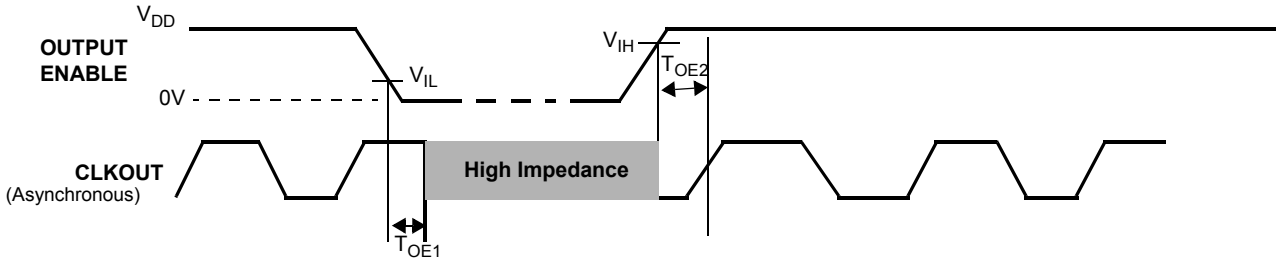
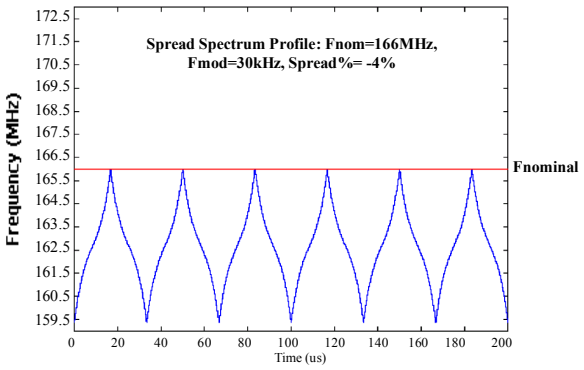


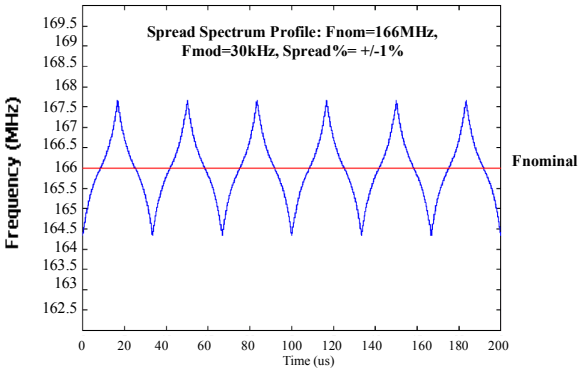
Figure 6. Output Enable/Disable Timing

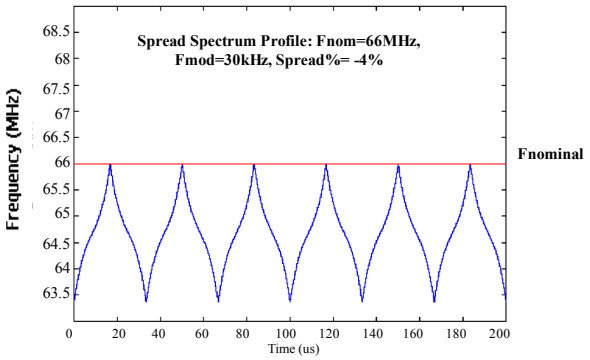


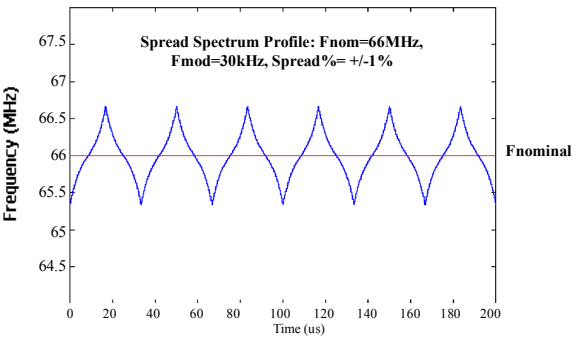
Informational Graphs

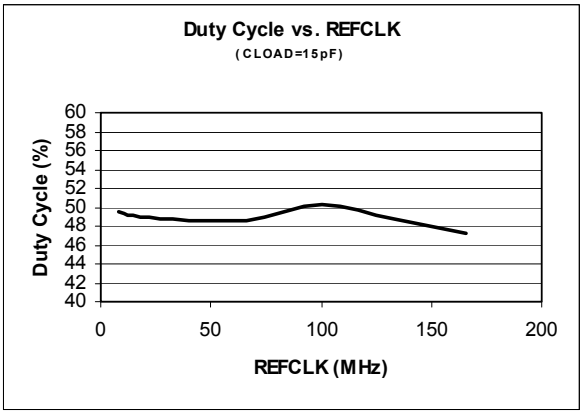
The Informational Graphs are as follows. [8]

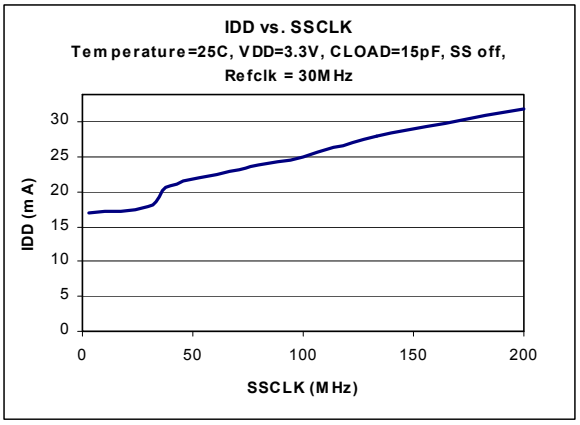










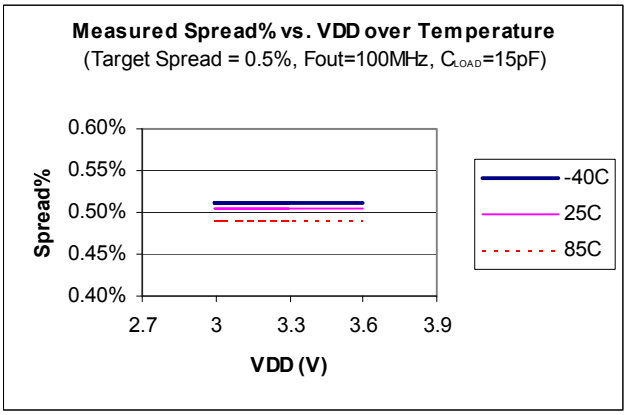


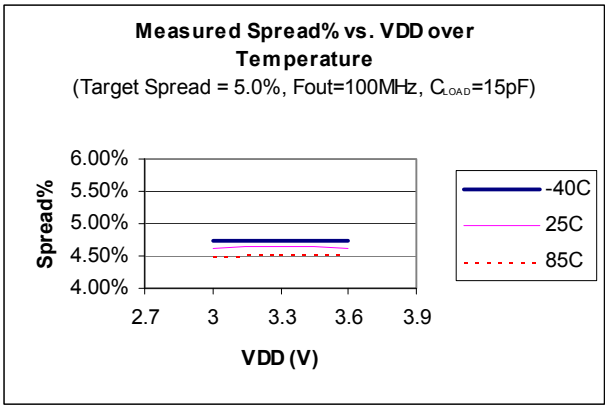
Note

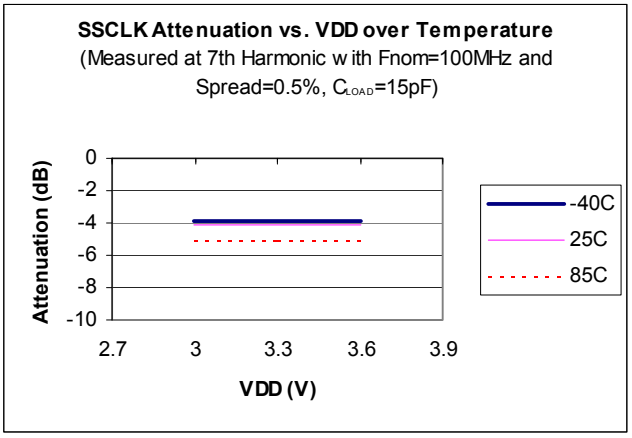
8. The Informational Graphs are meant to convey the typical performance levels. No performance specifications is implied or guaranteed. Refer to DC Electrical Characteristics on page 6 and AC Electrical Characteristics on page 7 for device specifications.

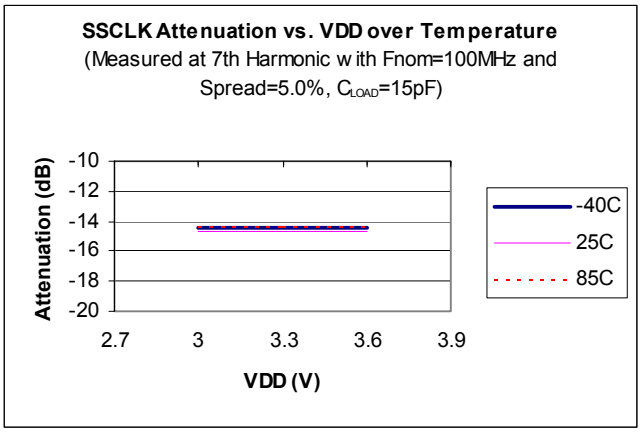
Informational Graphs (continued)

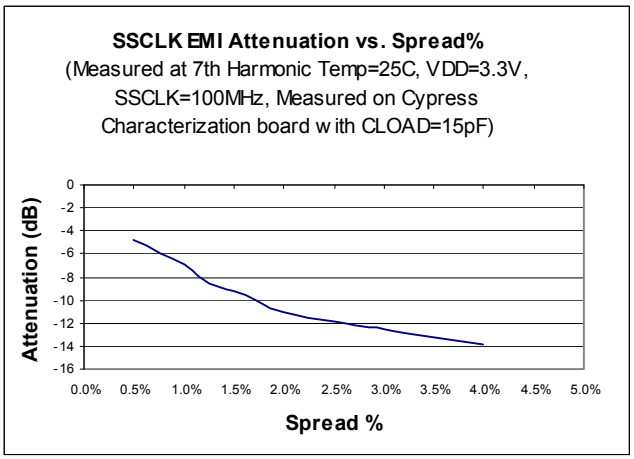
The Informational Graphs are as follows. [8]

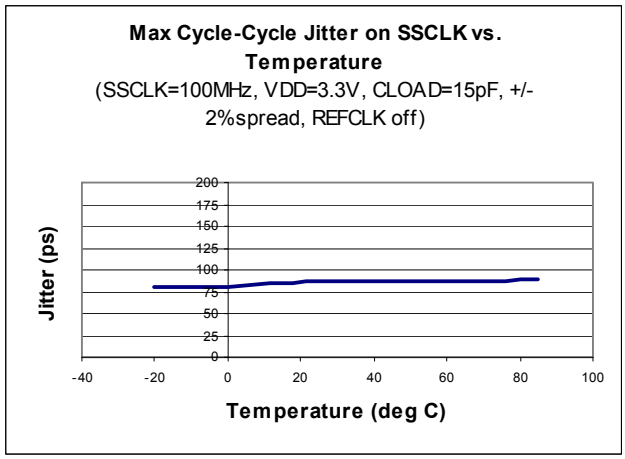












Ordering Information

Ordering Code	Package Description	Product Flow
Pb-free		
CY25100SXCF	8-pin SOIC	Commercial, 0 °C to 70 °C
CY25100SXCFT	8-pin SOIC – Tape and Reel	Commercial, 0 °C to 70 °C
CY25100SXIF	8-pin SOIC	Industrial, –40 °C to 85 °C
CY25100SXIFT	8-pin SOIC – Tape and Reel	Industrial, –40 °C to 85 °C
CY25100ZXCF	8-pin TSSOP	Commercial, 0 °C to 70 °C
CY25100ZXCFT	8-pin TSSOP – Tape and Reel	Commercial, 0 °C to 70 °C
CY25100ZXIF	8-pin TSSOP	Industrial, –40 °C to 85 °C
CY25100ZXIFT	8-pin TSSOP – Tape and Reel	Industrial, –40 °C to 85 °C
Programmer		
CY3672-USB	Programmer, for devices with ordering codes ending in “F” and “FT”	
CY3690	CY25100ZXCF/IF Adapter (TSSOP) for CY3672-USB Programmer	
CY3691	CY25100SXCF/IF Adapter (SOIC) for CY3672-USB Programmer	

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

Possible Configurations

Ordering Code	Package Description	Product Flow
CY25100ZIxxx[9, 10]	8-pin TSSOP	Industrial, –40 °C to 85 °C
CY25100ZIxxxT[9, 10]	8-pin TSSOP – Tape and Reel	Industrial, –40 °C to 85 °C
Pb-free		
CY25100SXCxxx[9]	8-pin SOIC	Commercial, 0 °C to 70 °C
CY25100SXCxxxT[9]	8-pin SOIC – Tape and Reel	Commercial, 0 °C to 70 °C
CY25100SXIxxx[9]	8-pin SOIC	Industrial, –40 °C to 85 °C
CY25100SXIxxxT[9]	8-pin SOIC – Tape and Reel	Industrial, –40 °C to 85 °C
CY25100ZXCxx[9]	8-pin TSSOP	Commercial, 0 °C to 70 °C
CY25100ZXCxxT[9]	8-pin TSSOP – Tape and Reel	Commercial, 0 °C to 70 °C
CY25100ZXIxx[9]	8-pin TSSOP	Industrial, –40 °C to 85 °C
CY25100ZXIxxT[9]	8-pin TSSOP – Tape and Reel	Industrial, –40 °C to 85 °C

Note
9. Ordering codes with “xxx” or “xx” are factory-programmed configurations. “xxx” or “xx” denotes the specific device configuration. “w” denotes the revision. Factory programming is available for high-volume orders. For more details, contact your local Cypress field application engineer or Cypress Sales Representative.
10. Not recommended for new designs. New designs should use Pb-free devices.

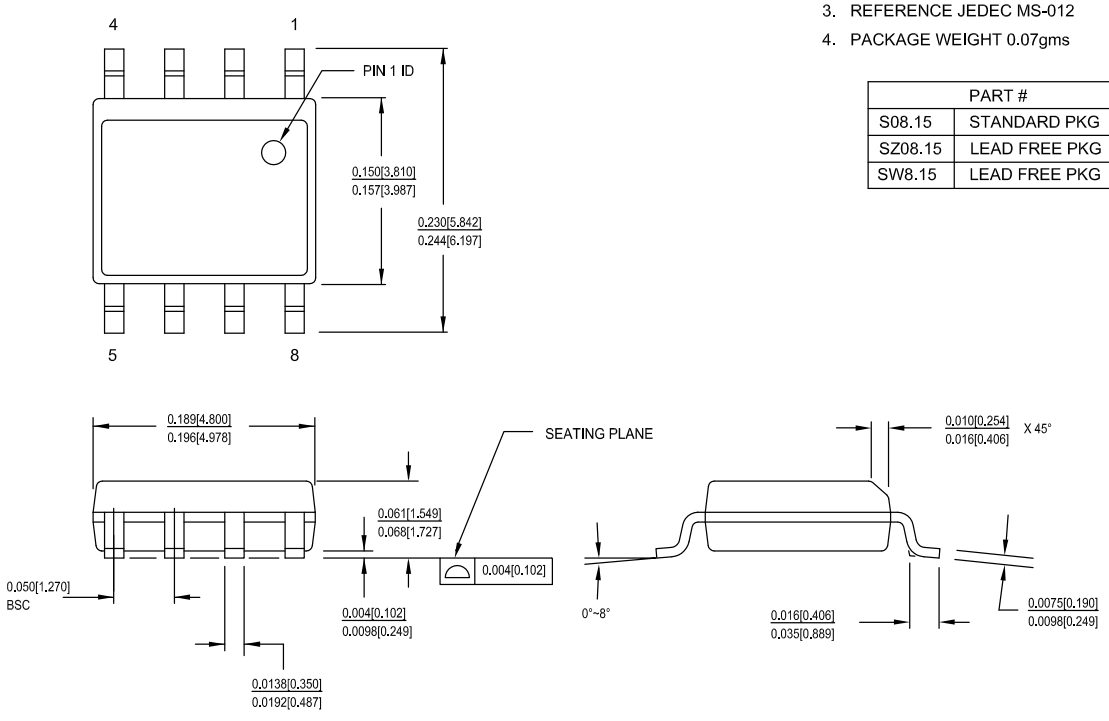
Ordering Code Definitions

CY 25100 X X X F (xx, xxx) T

- T = Tape and Reel; blank = Tube
- Custom configuration code (Factory Programmed Device only)
- Programming: F = Field Programmable; blank = Factory Programmed
- Temperature Range: X = C or I
  C = Commercial; I = Industrial
- X = Pb-free package
- Package Type: X = S or Z
  S = 8-pin SOIC; Z = 8-pin TSSOP
- Base Part Number
- Company ID: CY = Cypress

Package Diagrams

Figure 7. 8-pin SOIC (150 Mils) S08.15/SZ08.15/SW815 Package Outline, 51-85066



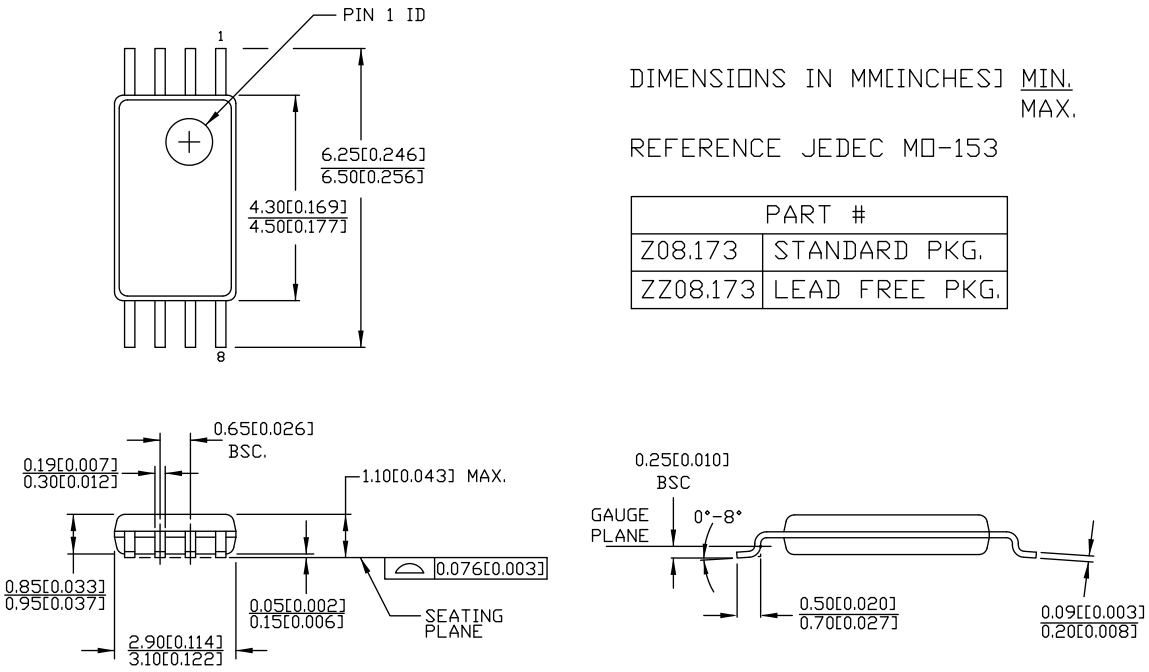
1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG

51-85066 *H

Package Diagrams (continued)

Figure 7. 8-pin TSSOP (4.40 mm Body) Z08.173/ZZ08.173 Package Outline, 51-85093



Acronyms

Acronym	Description
DC	Direct Current
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FAE	Field Application Engineer
JEDEC	Joint Electron Devices Engineering Council
OE	Output Enable
PCB	Printed Circuit Board
PD	Power Down
PLL	Phase Locked Loop
SOIC	Small Outline Integrated Circuit
SSC	Spread Spectrum Clock
SSCG	Spread Spectrum Clock Generator
TSSOP	Thin Shrunk Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
MHz	megahertz
µA	microampere
µF	microfarad
mA	milliampere
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY25100, Field and Factory Programmable Spread Spectrum Clock Generator for EMI Reduction Document Number: 38-07499				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	126578	CKN	06/27/03	New data sheet.
*A	128753	IJATMP	08/29/03	Changes to reflect field programmability
*B	130342	RGL	12/02/03	Changes to Application Circuit diagram and correction to the package description listed under the Ordering Information table for CY3690 and CY3691.
*C	204121	RGL	See ECN	Add Industrial Temperature Range Corrected the Ordering Information to match the DevMaster
*D	215392	RGL	See ECN	Added Lead Free devices
*E	2513909	AESA	06/10/08	Updated template. Added Note “Not recommended for new designs.” Added part number CY25100KSXCF, CY25100KSXIF, CY25100KSXI-xxx, CY25100KZXC-xxx, CY25100KZXI-xxx, CY25100KSXI-xxxT, CY25100KZXC-xxxT, CY25100KZXI-xxxT, and CY25100KZXIF in ordering information table. Added Pb-Free header in the ordering information table. Removed Pb-Free from Package description in the ordering information table. Changed CY3672-PRG with CY3672-USB in the ordering information table. Removed CY25100SCF, CY25100SIF, CY25100ZCF, CY25100ZIF, and CY3672 in the ordering information table. Changed Lead free to Pb-Free.
*F	2601881	KVM / PYRS	11/06/08	Rising edge slew rate (SR3) minimum limit changed from 1.2 V/ns to 1.0 V/ns. Removed part numbers added in rev *E.
*G	2742910	KVM	07/23/09	General text cleanup Moved General Description to p. 1 to replace the Benefits section Removed “FTG” from references to CY3672 Added “Type” column to Pin Description table Revised software description section Revised Modulation Frequency section to remove mention of optional modulation frequencies Added minimum values to I_{IH} and I_{IL} Added to I_{OZ} conditions: applies only for output pulldown disabled Standardized timing parameter names to upper case Corrected some part numbers to remove dashes and revision code Added part numbers to the Ordering Information table: CY25100ZI-xxx, CY25100ZI-xxxT, CY25100SXCFT, CY25100SXIFT, CY25100ZXCFT and CY25100ZXIFT Revised Ordering Information table footnotes
*H	2897317	KVM	03/22/10	Removed obsolete parts from Ordering Information table and moved ‘xxx’ parts to Possible Configurations table Updated Package Diagrams.
*I	3366141	PURU	09/12/2011	Updated Logic Block Diagram. Added Ordering Code Definitions. Updated Package Diagrams. Added Acronyms and Units of Measure. Updated to new template.
*J	4108421	CINM	08/30/2013	Updated Package Diagrams: spec 51-85066 – Changed revision from *E to *F. spec 51-85093 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.

Document History Page (continued)

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*K	4581659	TAVA	11/28/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagrams: spec 51-85093 – Changed revision from *D to *E.
*L	5516747	PSR / PAWK	11/10/2016	Updated Programming Description: Removed “CyberClocks™ Online Software”. Added Thermal Resistance. Updated Package Diagrams: spec 51-85066 – Changed revision from *F to *H. Updated to new template. Completing Sunset Review.

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