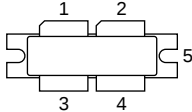
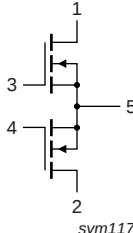
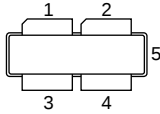
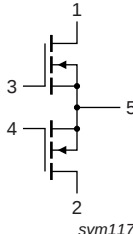


2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF178XR (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		
BLF178XRS (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF178XR	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF178XRS	-	earless flanged balanced LDMOST ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

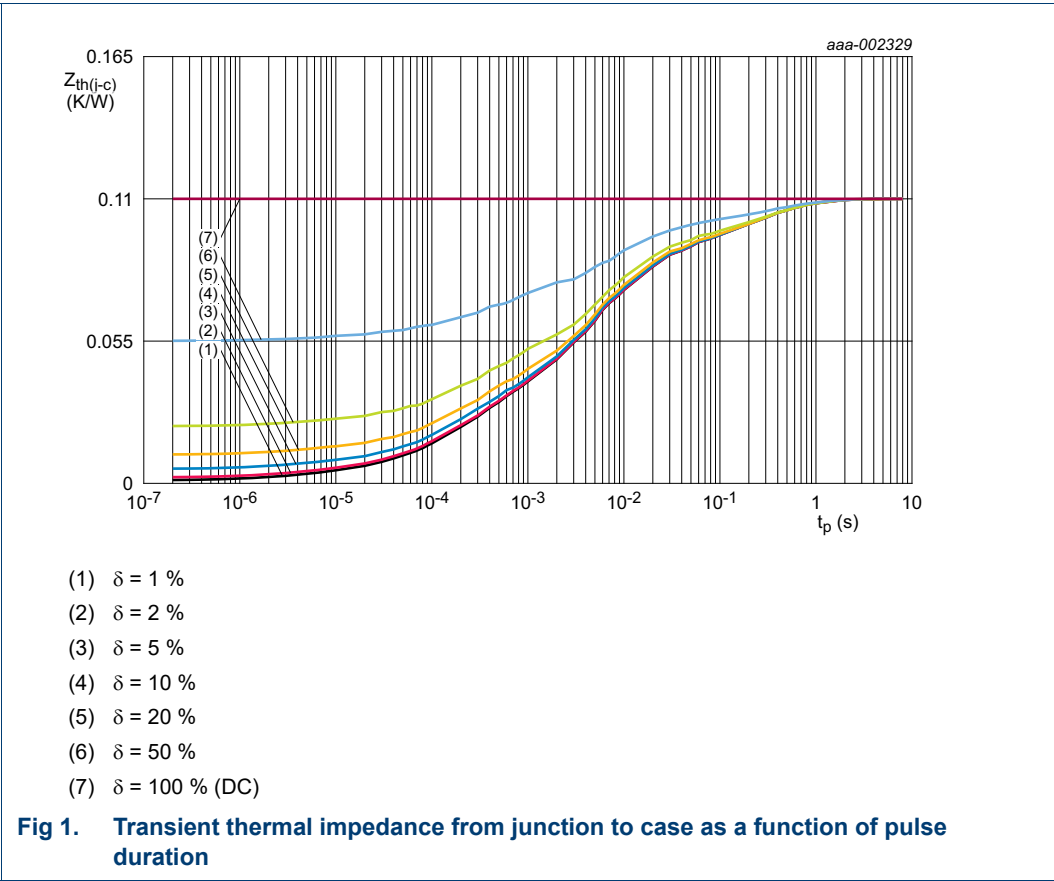
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_j = 150\text{ }^{\circ}\text{C}$	[1][2] 0.11	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_j = 150\text{ }^{\circ}\text{C}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$	[3] 0.033	K/W

- [1] T_j is the junction temperature.
[2] $R_{th(j-c)}$ is measured under RF conditions.
[3] See [Figure 1](#).



6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^{\circ}\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 5.5\text{ mA}$	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 550\text{ mA}$	1.25	1.7	2.25	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 50\text{ V}$; $I_D = 20\text{ mA}$	0.8	1.3	1.8	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$	-	-	2.8	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	77	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 19.25\text{ A}$	-	0.07	-	Ω

Table 7. AC characteristics

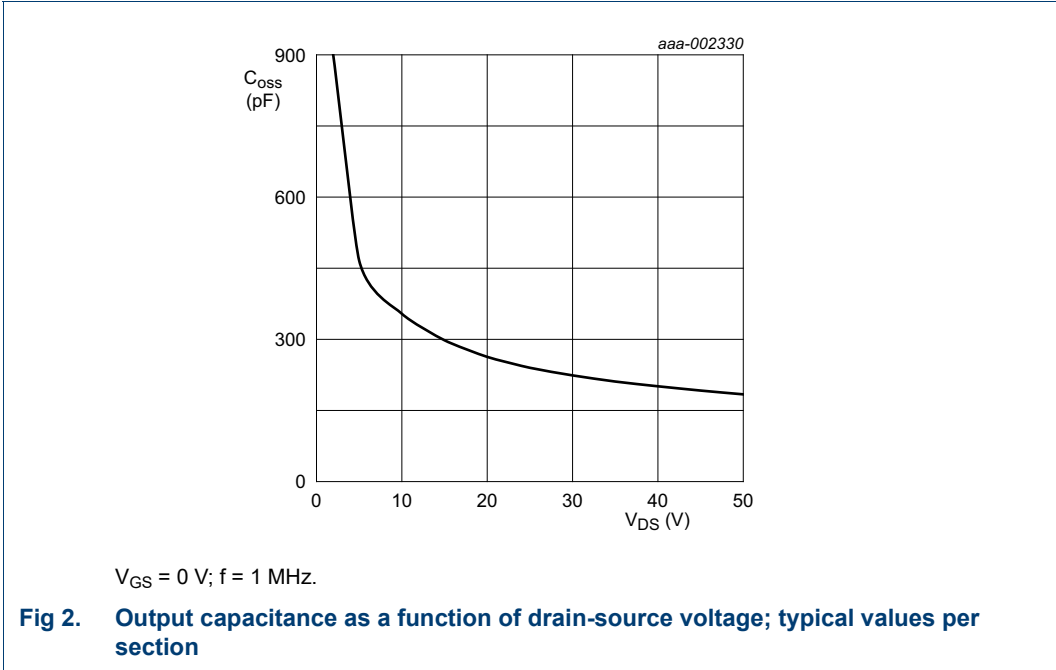
$T_j = 25\text{ }^{\circ}\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	5.5	-	pF
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	414	-	pF
C_{oss}	output capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $f = 1\text{ MHz}$	-	184	-	pF

Table 8. RF characteristics

Test signal: pulsed RF; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\%$; $f = 108\text{ MHz}$; RF performance at $V_{DS} = 50\text{ V}$; $I_{DQ} = 40\text{ mA}$; $T_{case} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_L = 1400\text{ W}$	27	28	-	dB
RL_{in}	input return loss	$P_L = 1400\text{ W}$	-	-15	-11	dB
η_D	drain efficiency	$P_L = 1400\text{ W}$	68	72	-	%



7. Test information

7.1 Ruggedness in class-AB operation

The BLF178XR and BLF178XRS are capable of withstanding a load mismatch corresponding to $VSWR > 65 : 1$ through all phases under the following conditions: $V_{DS} = 50\text{ V}; I_{Dq} = 40\text{ mA}; P_L = 1400\text{ W}$ pulsed; $f = 108\text{ MHz}.$

7.2 Impedance information

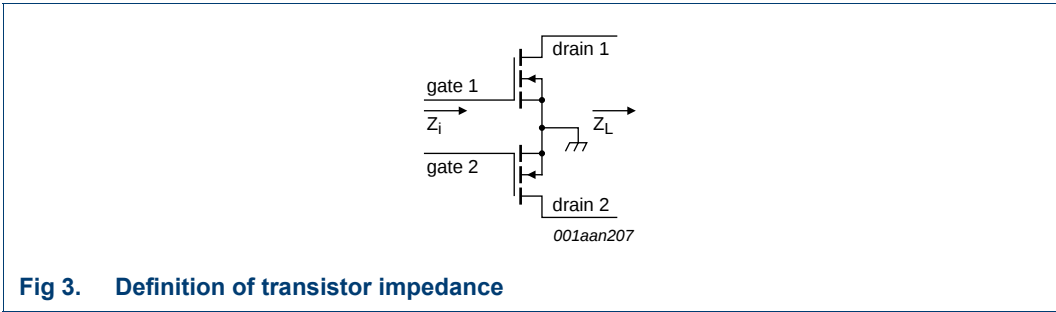


Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at $V_{DS} = 50\text{ V}$ and $P_L = 1400\text{ W}.$

f (MHz)	Z_i (Ω)	Z_L (Ω)
108	$2.35 - j6.06$	$2.78 + j0.48$

7.3 Test circuit

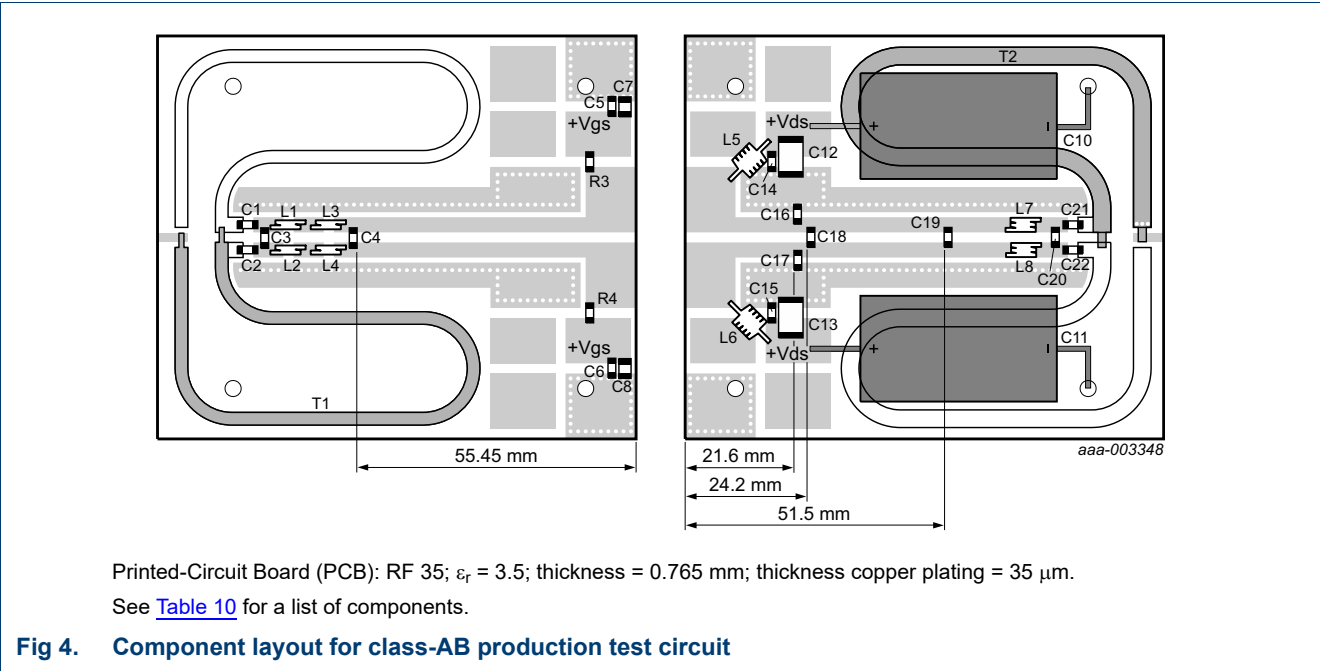


Table 10. List of components

For test circuit see [Figure 4](#).

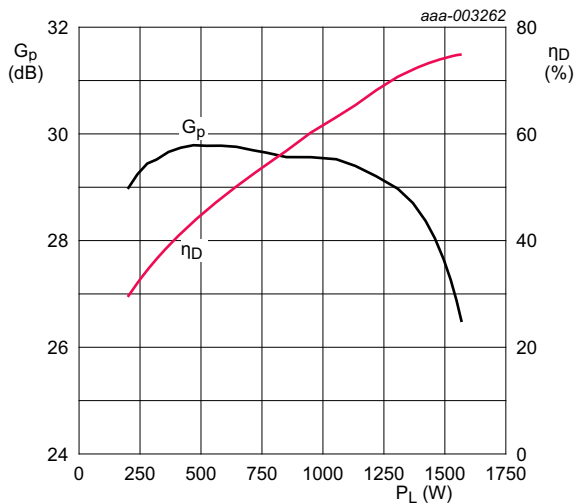
Component	Description	Value	Remarks
C1, C2, C5, C6, C14, C15, C21, C22	multilayer ceramic chip capacitor	1 nF	[1]
C3	multilayer ceramic chip capacitor	82 pF	[1]
C4	multilayer ceramic chip capacitor	240 pF	[1]
C7, C8	multilayer ceramic chip capacitor	4.7 μF ; 50 V	
C10, C11	electrolytic capacitor	2200 μF ; 63 V	
C12, C13	multilayer ceramic chip capacitor	4.7 μF ; 100 V	
C16, C17	multilayer ceramic chip capacitor	120 pF	[1]
C18	multilayer ceramic chip capacitor	82 pF	[1]
C19	multilayer ceramic chip capacitor	110 pF	[1]
C20	multilayer ceramic chip capacitor	56 pF	[1]
L1, L2, L3, L4	1.5 turn 0.8 mm copper wire	D = 3 mm; length = 2 mm	
L5, L6	5 turn 0.8 mm copper wire	D = 3 mm; length = 4.5 mm	
L7, L8	2.5 turn 0.8 mm copper wire	D = 3 mm; length = 3 mm	
R3, R4	SMD resistor	9.1 Ω	1206
T1	semi rigid coax	25 Ω ; 160 mm	UT-090C-25
T2	semi rigid coax	25 Ω ; 160 mm	UT-141C-25

[1] American Technical Ceramics type 800B or capacitor of same quality.

7.4 Graphical data

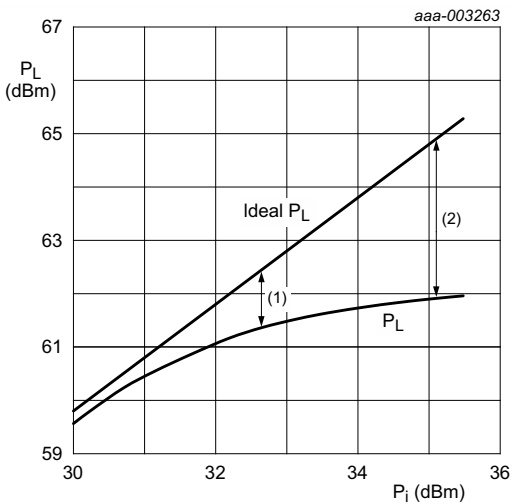
The following figures are measured in a class-AB production test circuit.

7.4.1 1-Tone CW pulsed



$V_{DS} = 50\text{ V}$; $I_{Dq} = 40\text{ mA}$; $f = 108\text{ MHz}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

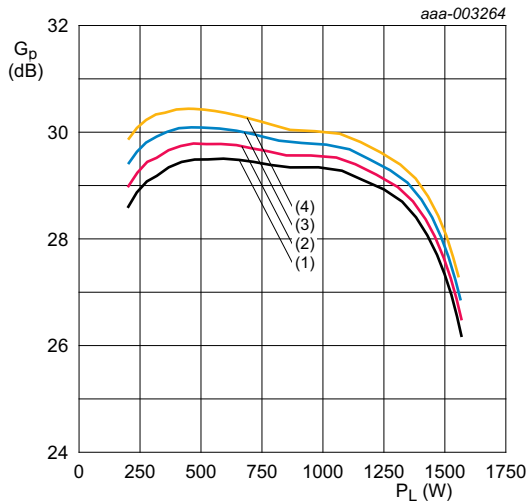
Fig 5. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 50\text{ V}$; $I_{Dq} = 40\text{ mA}$; $f = 108\text{ MHz}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\text{ }\%$.

- (1) $P_{L(1dB)} = 61.3\text{ dBm}$ (1350 W)
- (2) $P_{L(3dB)} = 61.9\text{ dBm}$ (1550 W)

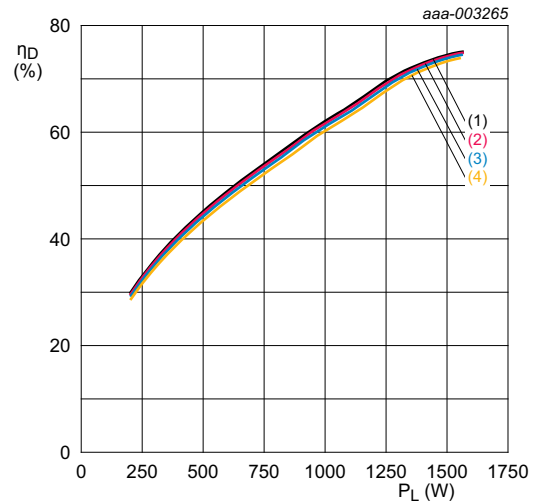
Fig 6. Output power as a function of input power; typical values



$V_{DS} = 50 \text{ V}$; $f = 108 \text{ MHz}$; $t_p = 100 \text{ } \mu\text{s}$; $\delta = 20 \text{ } \%$.

- (1) $I_{Dq} = 20 \text{ mA}$
- (2) $I_{Dq} = 40 \text{ mA}$
- (3) $I_{Dq} = 80 \text{ mA}$
- (4) $I_{Dq} = 160 \text{ mA}$

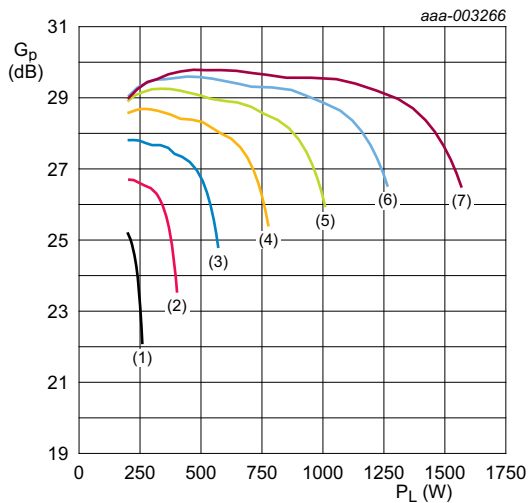
Fig 7. Power gain as a function of output power; typical values



$V_{DS} = 50 \text{ V}$; $f = 108 \text{ MHz}$; $t_p = 100 \text{ } \mu\text{s}$; $\delta = 20 \text{ } \%$.

- (1) $I_{Dq} = 20 \text{ mA}$
- (2) $I_{Dq} = 40 \text{ mA}$
- (3) $I_{Dq} = 80 \text{ mA}$
- (4) $I_{Dq} = 160 \text{ mA}$

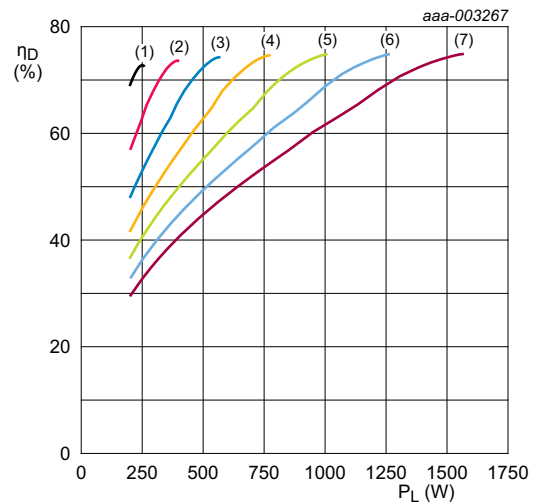
Fig 8. Drain efficiency as a function of output power; typical values



$I_{Dq} = 40 \text{ mA}$; $f = 108 \text{ MHz}$; $t_p = 100 \text{ } \mu\text{s}$; $\delta = 20 \text{ } \%$.

- (1) $V_{DS} = 20 \text{ V}$
- (2) $V_{DS} = 25 \text{ V}$
- (3) $V_{DS} = 30 \text{ V}$
- (4) $V_{DS} = 35 \text{ V}$
- (5) $V_{DS} = 40 \text{ V}$
- (6) $V_{DS} = 45 \text{ V}$
- (7) $V_{DS} = 50 \text{ V}$

Fig 9. Power gain as a function of output power; typical values



$I_{Dq} = 40 \text{ mA}$; $f = 108 \text{ MHz}$; $t_p = 100 \text{ } \mu\text{s}$; $\delta = 20 \text{ } \%$.

- (1) $V_{DS} = 20 \text{ V}$
- (2) $V_{DS} = 25 \text{ V}$
- (3) $V_{DS} = 30 \text{ V}$
- (4) $V_{DS} = 35 \text{ V}$
- (5) $V_{DS} = 40 \text{ V}$
- (6) $V_{DS} = 45 \text{ V}$
- (7) $V_{DS} = 50 \text{ V}$

Fig 10. Drain efficiency as a function of output power; typical values

8. Package outline

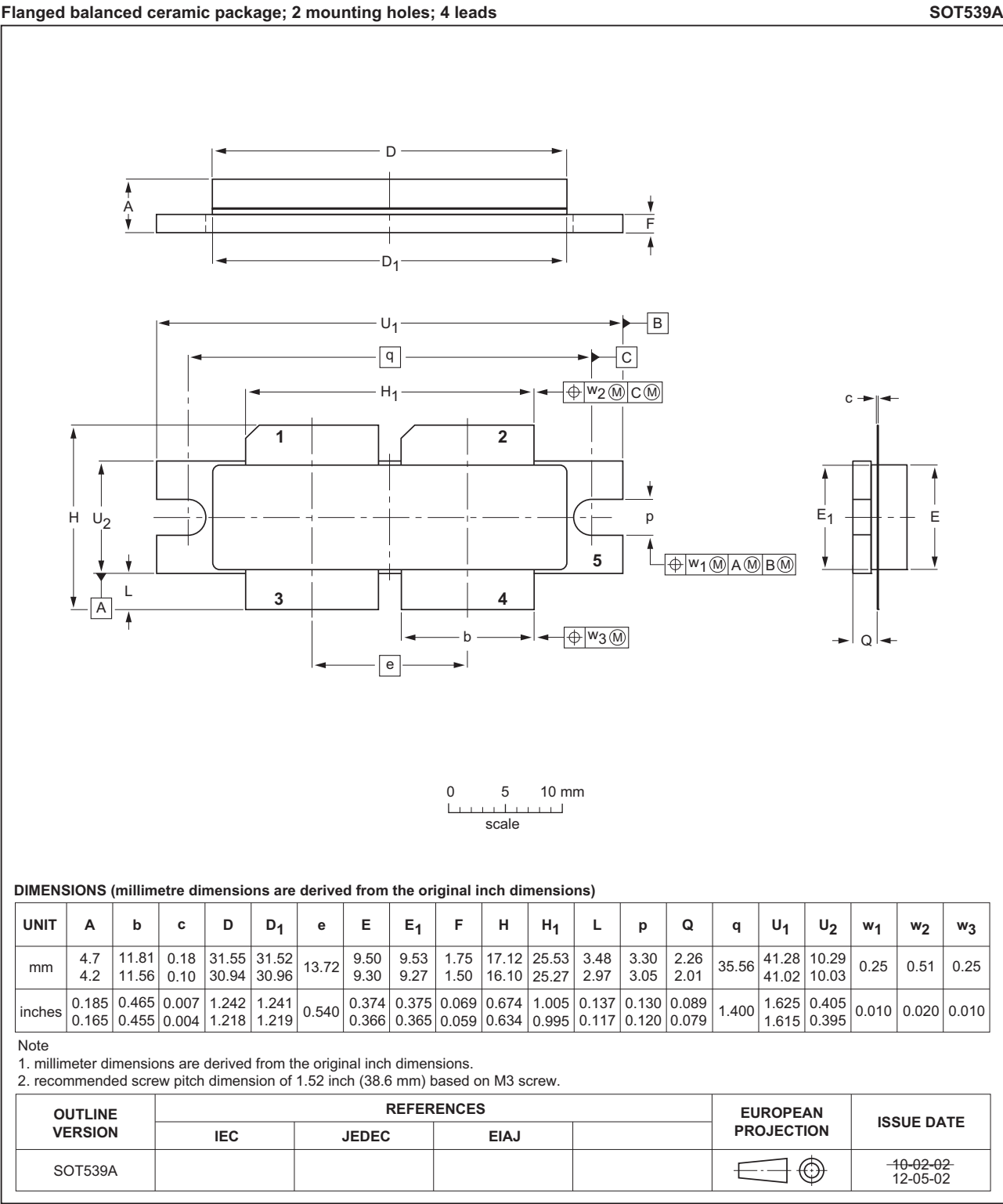


Fig 11. Package outline SOT539A

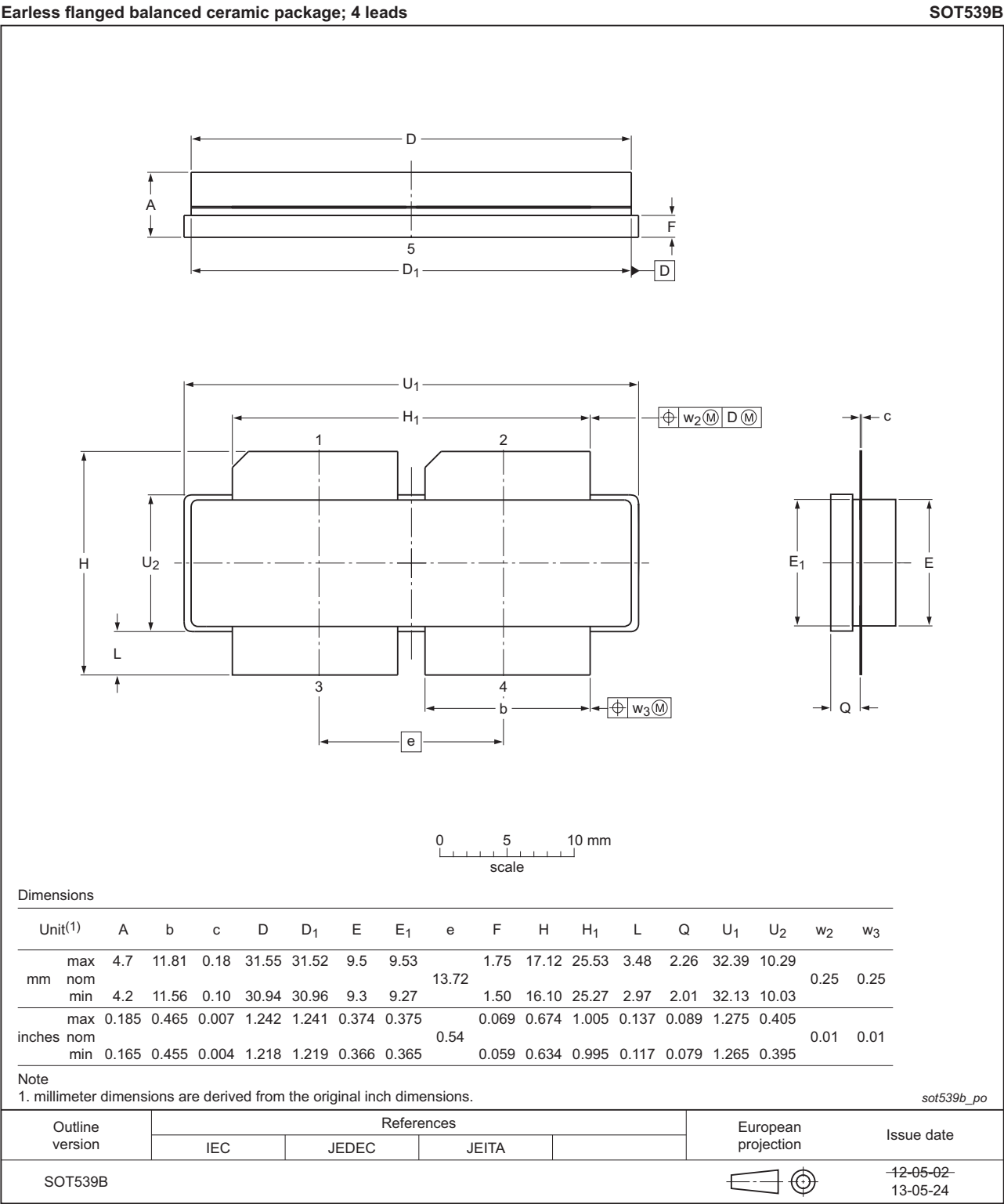


Fig 12. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF178XR_BLF178XRS#5	20150901	Product data sheet	-	BLF178XR_BLF178XRS v.4
Modifications:	- The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. - Legal texts have been adapted to the new company name where appropriate.			
BLF178XR_BLF178XRS v.4	<td>	Product data sheet	-	BLF178XR_BLF178XRS v.3
BLF178XR_BLF178XRS v.3	20120625	Product data sheet	-	BLF178XR_BLF178XRS v.2
BLF178XR_BLF178XRS v.2	20120515	Preliminary data sheet	-	BLF178XR_BLF178XRS v.1
BLF178XR_BLF178XRS v.1	20120130	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

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