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REVISION HISTORY

3/2017—Rev. A to Rev. B

Changed CP-16-3 to CP-16-27 ... Throughout
Changes to Figure 2 ... 4
Changes to Figure 20 ... 11
Changes to Ordering Guide ... 13
Updated Outline Dimensions ... 13

7/2005—Rev. 0 to Rev. A

Changes to Table 1 ... 3
Changes to Ordering Guide ... 13

3/2005—Revision 0: Initial Version

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SPECIFICATIONS

Test Conditions: VCC = 2.9 V to 3.6 V, VEE = 0 V, T_A = −40°C to +95°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
QUANTIZER DC CHARACTERISTICS					
Input Voltage Range	1.8		2.8	V p-p	At PIN or NIN, dc-coupled
Input Common Mode	2.1		2.7	V	DC-coupled
Differential Input Range			2.0	V p-p	AC-coupled
Differential Input Sensitivity	5.2	3.5		mV p-p	3.2 Gbps, PRBS $2^{23} - 1$, BER ≤ 10^{-10}
Input Offset Voltage		100		µV	
Input RMS Noise		235		µV rms	
Input Resistance		50		Ω	Single-ended
Input Capacitance		0.65		pF	
QUANTIZER AC CHARACTERISTICS					
Input Data Rate	155		3200	Mb/s	
Small Signal Gain		50		dB	Differential
S11		−10		dB	Differential, f < 3.2 GHz
S22		−10		dB	Differential, f < 3.2 GHz
Random Jitter		4.0	6.4	ps rms	Input ≥ 10 mV p-p, OC-48, PRBS $2^{23} - 1$
Deterministic Jitter		9.0	34	ps p-p	Input ≥ 10 mV p-p, OC-48, PRBS $2^{23} - 1$
Low Frequency Cutoff		30		kHz	CAZ = Open
		1.0		kHz	CAZ = 0.0 1 µF
Power Supply Rejection Ratio		45		dB	f < 10 MHz
LOSS OF SIGNAL DETECTOR (LOS)					
LOS Assert Level	1.9	3.5	5.6	mV p-p	R_{THRADJ} = 100 kΩ
	19	35	53	mV p-p	R_{THRADJ} = 1 kΩ
Electrical Hysteresis	2.4	5.0		dB	OC-3, PRBS $2^{23} - 1$
	2.75	5.0		dB	OC-48, PRBS $2^{23} - 1$
LOS Assert Time		950		ns	DC-coupled
LOS De-Assert Time		62		ns	DC-coupled
RSSI					
Input Current Range	5		1000	µA	
RSSI Output Linearity		2		%	5 µA < I_{IN} ≤ 1000 µA
Gain		1.0		mA/mA	I_{RSSI}/I_{PD}
Offset		145		nA	Difference between measured RSSI output and PD_CATHODE (input) current of 5 µA
Compliance Voltage	VCC − 0.9		VCC − 0.4	V	Measured at PD_CATHODE, with I = 5 µA or I = 1 mA
POWER SUPPLIES					
VCC	2.9	3.3	3.6	V	
I_{CC}		45	49	mA	
OPERATING TEMPERATURE RANGE	−40	+25	+95	°C	T_{MIN} to T_{MAX}
CML OUTPUT CHARACTERISTICS					
Output Impedance		50		Ω	Single-ended
Output Voltage Swing	600	660	850	mV p-p	Differential
Output Rise and Fall Time		80	130	ps	20% to 80%

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS (SQUELCH)					
V_{IH}, Input High Voltage	2.0			V	
V_{IL}, Input Low Voltage			0.8	V	
Input Current			40	µA	I_{INH}, V_{IN} = 2.4 V, 100 kΩ pull-down resistor on-chip
			6	µA	I_{INL}, V_{IN} = 0.4 V, 100 kΩ pull-down resistor on-chip
LOGIC OUTPUTS (LOS)					
V_{OH}, Output High Voltage	2.4			V	Open drain output, 4.7 kΩ to 10 kΩ pull-up resistor to VCC
V_{OL}, Output Low Voltage			0.4	V	Open drain output, 4.7 kΩ to 10 kΩ pull-up resistor to VCC

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ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Power Supply Voltage	4.2 V
Minimum Voltage (All Inputs and Outputs)	VEE − 0.4 V
Maximum Voltage (All Inputs and Outputs)	VCC + 0.4 V
Storage Temperature	−65°C to +150°C
Operating Temperature Range	−40°C to +95°C
Production Soldering Temperature	J-STD-20
Junction Temperature	125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for 4-layer PCB with exposed paddle soldered to GND.

Table 3.

Package Type	θ_{JA}	Unit
3 mm × 3 mm, 16-lead LFCSP	28	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

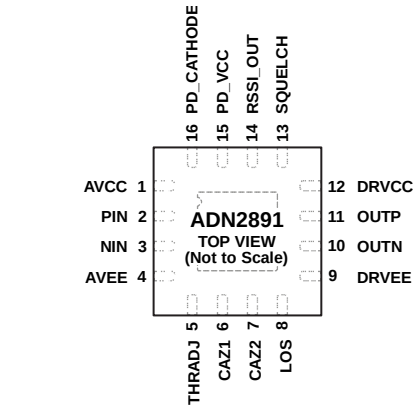

Figure 2. Pin Configuration

Note that the LFCSP has an exposed pad on the bottom. To improve heat dissipation, the exposed pad must be soldered to the GND plane with filled vias.

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	I/O Type[1]	Descriptions
1	AVCC	P	Analog Power Supply.
2	PIN	AI	Differential Data Input, Positive Port, 50 Ω On-Chip Termination.
3	NIN	AI	Differential Data Input, Negative Port, 50 Ω On-Chip Termination.
4	AVEE	P	Analog Ground.
5	THRADJ	AO	LOS Threshold Adjust Resistor.
6	CAZ1	AI	If needed, one capacitor can connect between the CAZ1 and CAZ2 pin for input offset correction.
7	CAZ2	AI	If needed, one capacitor can connect between the CAZ1 and CAZ2 pin for input offset correction.
8	LOS	DO	LOS Detector Output, Open Collector.
9	DRVEE	P	Output Buffer Ground.
10	OUTN	DO	Differential Data Output, CML, Negative Port, 50 Ω On-Chip Termination.
11	OUTP	DO	Differential Data Output, CML, Positive Port, 50 Ω On-Chip Termination.
12	DRVCC	P	Output Buffer Power Supply.
13	SQUELCH	DI	Disable Outputs, 100 kΩ On-Chip Pull-Down Resistor.
14	RSSI_OUT	AO	Average Current Output.
15	PD_VCC	P	Power Input for RSSI Measurement.
16	PD_CATHODE	AO	Photodiode Bias Voltage.
Exposed Pad	Pad	P	Connect to Ground.

[1] P = power; DI = digital input; DO = digital output; AI = analog input; and AO = analog output.

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TYPICAL PERFORMANCE CHARACTERISTICS

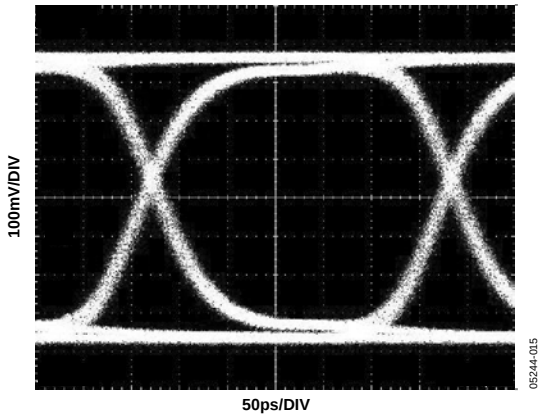

Figure 3. Eye of ADN2891 @ 25°C, 3.2 Gbps, and 10 mV Input

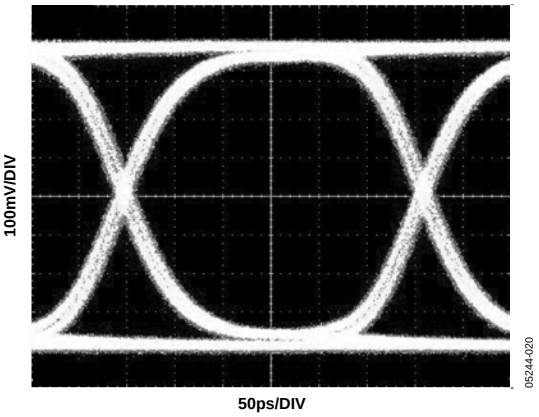

Figure 6. Eye of ADN2891 @ 95°C, 3.2 Gbps, and 500 mV Input

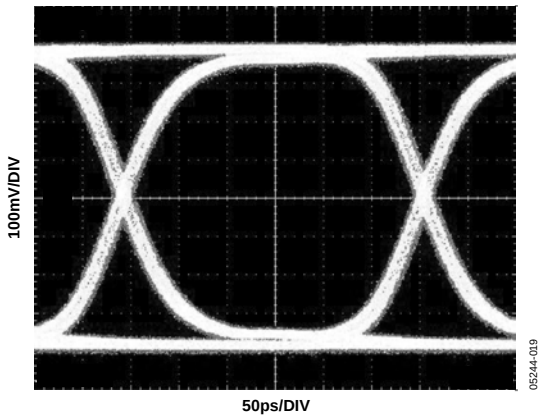

Figure 4. Eye of ADN2891 @ 25°C, 3.2 Gbps, and 500 mV Input

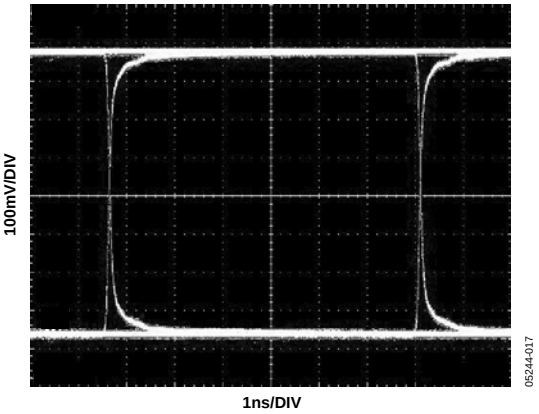

Figure 7. Eye of ADN2891 @ 25°C, 155 Mbps, and 10 mV Input

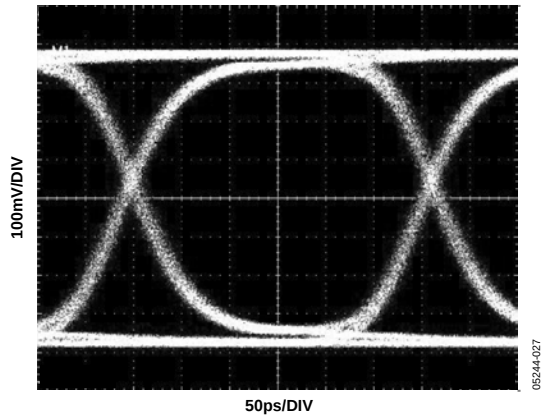

Figure 5. Eye of ADN2891 @ 95°C, 3.2 Gbps, and 10 mV Input

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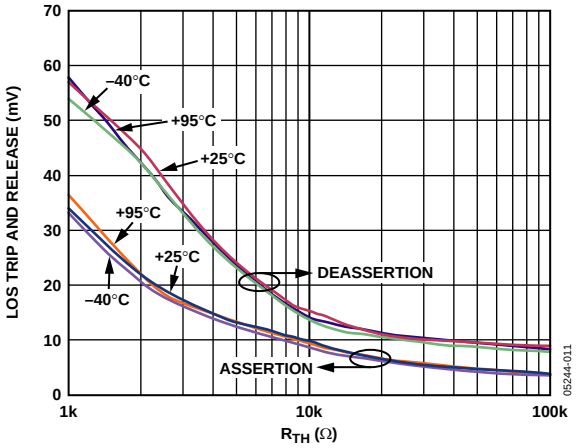

Figure 8. LOS Trip and Release vs. R_{TH} at OC48

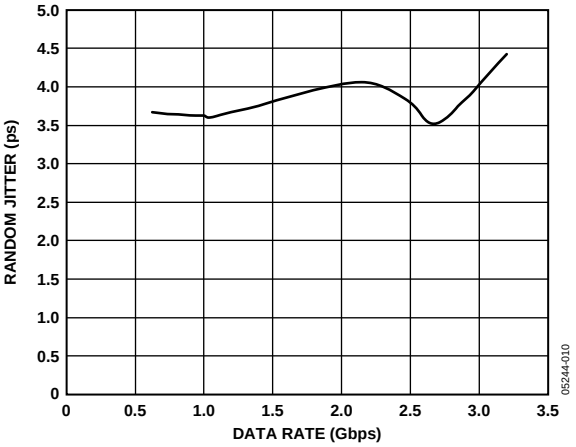

Figure 11. Random Jitter vs. Data Rate

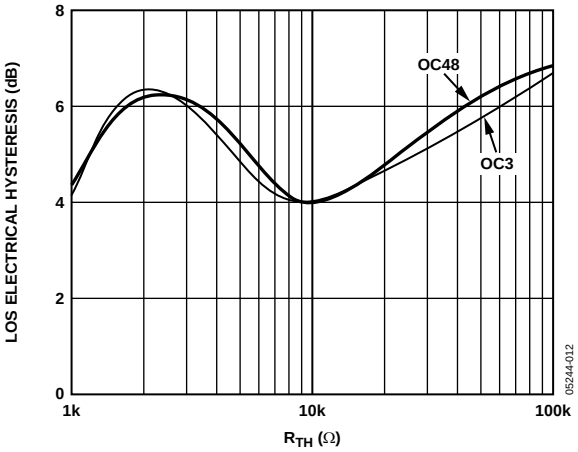

Figure 9. LOS Electrical Hysteresis vs. R_{TH} at 25°C

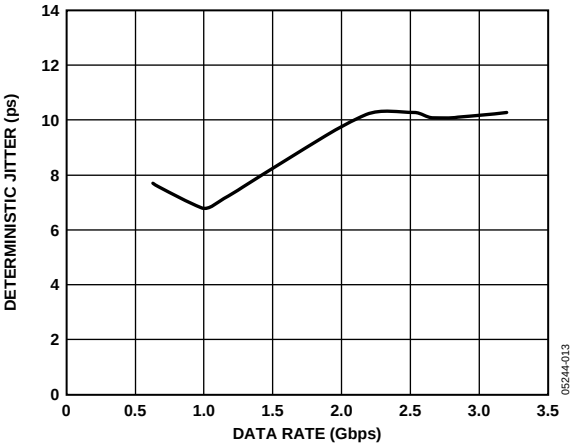

Figure 12. Deterministic Jitter vs. Data Rate

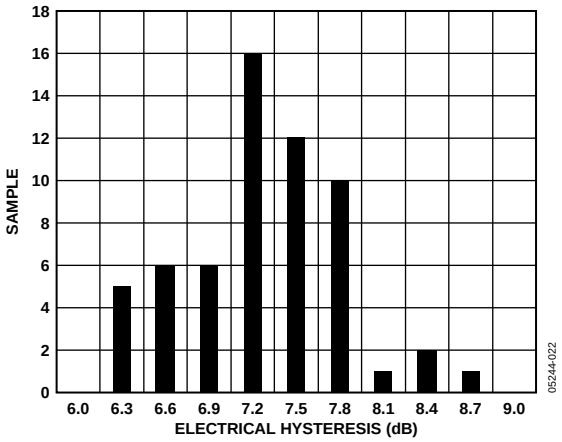

Figure 10. Sample Lot Distribution—Worst-Case Condition: Conditions = 155 Mbps, 100 kΩ @ 95°C, 3.6 V

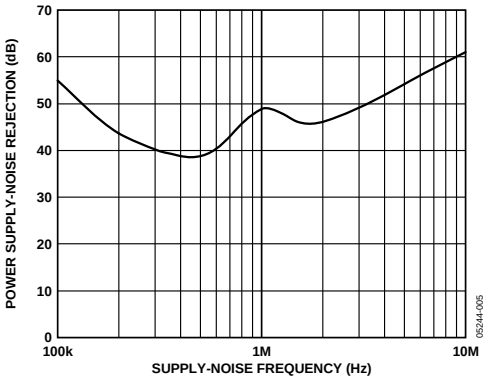

Figure 13. PSRR vs. Supply-Noise Frequency

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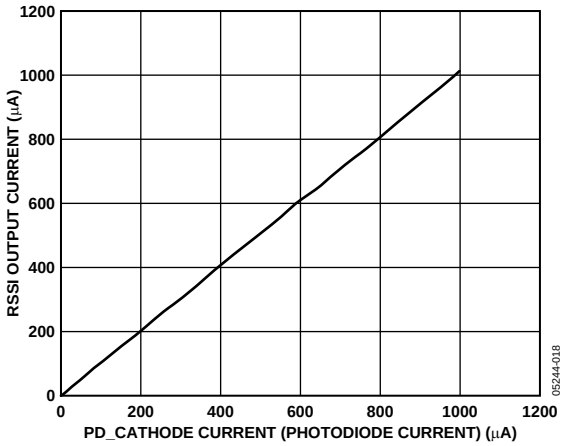

Figure 14. RSSI Output vs. Average Photodiode Current

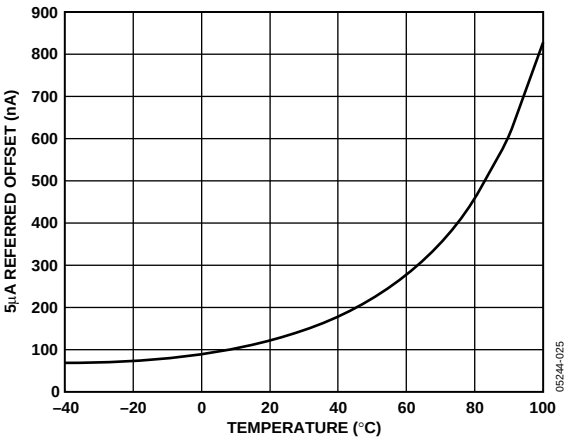

Figure 17. RSSI Offset is the Difference Between Measured RSSI Output and PD_CATHODE (Input) Current of 5 µA

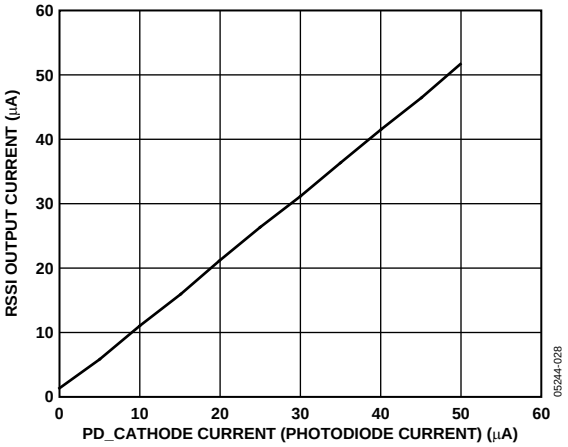

Figure 15. RSSI Output vs. Average Photodiode Current (Zoomed)

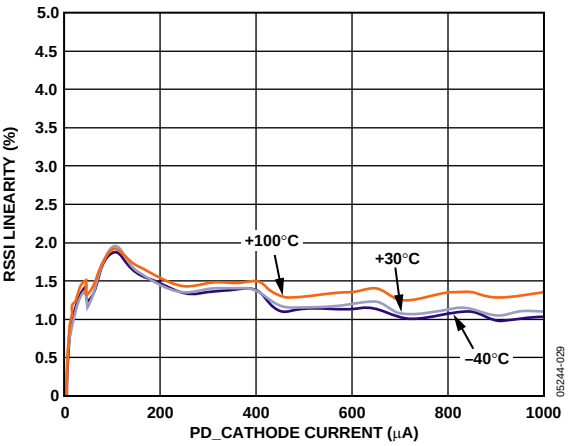

Figure 18. RSSI Linearity % vs. PD_CATHODE Current

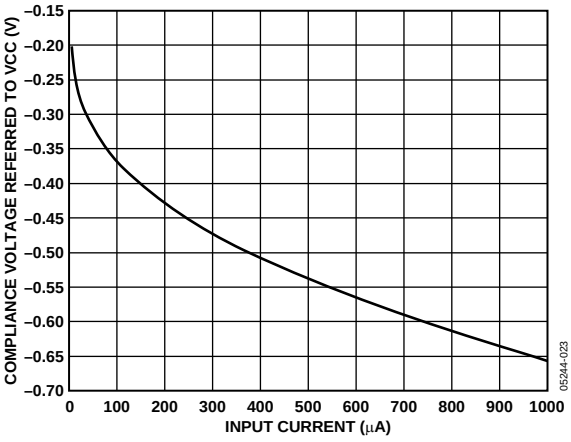

Figure 16. PD_CATHODE Compliance Voltage vs. Input Current RSSI (Refer to VCC)

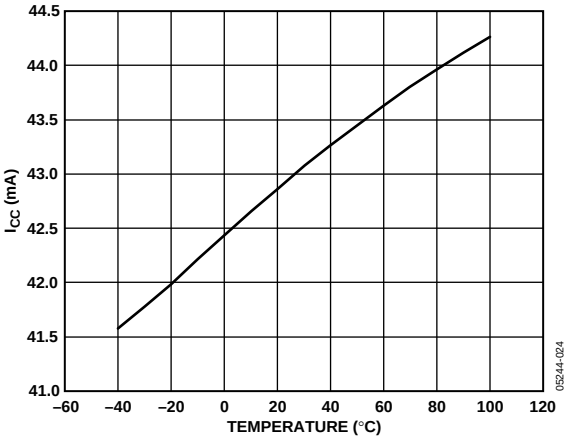

Figure 19. ADN2891 I_{CC} Current vs. Temperature

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THEORY OF OPERATION

LIMITING AMPLIFIER

Input Buffer

The ADN2891 limiting amplifier provides differential inputs (PIN/NIN), each having single-ended, on-chip, 50 Ω termination. The amplifier can accept either dc-coupled or ac-coupled signals; however, an ac-coupled signal is recommended. Using a dc-coupled signal, the amplifier needs a correct input common-mode voltage and enough headroom to handle the dynamic input signal strength. Additionally, TIA output offset drifts may degrade receiver performance.

The ADN2891 limiting amplifier is a high gain device. It is susceptible to dc offsets in the signal path. The pulse width distortion presented in the NRZ data or a distortion generated by the TIA may appear as dc offset or a corrupted signal to the ADN2891 inputs. An internal offset correction loop can compensate for certain levels of offset. To compensate for more offset, an external capacitor connected between the CAZ1 and CAZ2 pins maybe necessary. For GbE and FC applications, no external capacitor is necessary; however, for SONET applications, a 0.01 µF capacitor helps the input signal offset compensation and provides a 3 dB cutoff frequency at 1 kHz.

CML Output Buffer

The ADN2891 provides differential CML outputs, OUTP and OUTN. Each output has an internal 50 Ω termination to VCC.

LOSS OF SIGNAL (LOS) DETECTOR

The on-chip LOS circuit drives LOS to logic high when the input signal level falls below a user-programmable threshold. The threshold level can be set to anywhere from 3.5 mV p-p to 35 mV p-p, typical, and is set by a resistor connected between the THRADJ pin and VEE. See Figure 8 and Figure 9 for the LOS threshold vs. THRADJ. The ADN2891 LOS circuit has an electrical hysteresis greater than 2.5 dB to prevent chatter at the LOS signal. The LOS output is an open-collector output that must be pulled up externally with a 4.7 kΩ to 10 kΩ resistor.

RECEIVED SIGNAL STRENGTH INDICATOR (RSSI)

The ADN2891 has an on-chip, RSSI circuit. By monitoring the current supplied to the photodiode, the RSSI circuit provides an accurate, average power measurement. The output of the RSSI is a current that is directly proportional to the average amount of PIN photodiode current. Placing a resistor between the RSSI_OUT pin and GND converts the current to a GND referenced voltage. This function eliminates the need for external RSSI circuitry for SFF-8472-compliant optical receivers. For more information, see Figure 14 to Figure 18.

SQUELCH MODE

Driving the SQUELCH input to logic high disables the limiting amplifier outputs. Using LOS output to drive the SQUELCH input, the limiting amplifier outputs stop toggling anytime a signal input level to the limiting amplifier drops below the programmed LOS threshold.

The SQUELCH pin has a 100 kΩ, internal, pull-down resistor.

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APPLICATIONS

PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used to ensure optimal performance.

Output Buffer Power Supply and Ground Planes

Pin 9 (DRVEE) and Pin 12 (DRVCC) are the power supply and ground pins that provide current to the differential output buffer. To reduce possible series inductance, Pin 9, which is the ground return of the output buffer, should connect to ground directly. If the ground plane is an internal plane and connections to the ground plane are vias, multiple vias in parallel to ground can reduce series inductance.

Similarly, to reduce the possible series inductance, Pin 12, which supplies power to the high speed differential OUTP/OUTN output buffer, should connect to the power plane directly. If the power plane is an internal plane and connections to the power plane are vias, multiple vias in parallel can reduce the series inductance, especially on Pin 12. See Figure 20 for the recommended connections.

The exposed pad should connect to the GND plane using filled vias so that solder does not leak through the vias during reflow. Using filled vias in parallel under the package greatly reduces the thermal resistance and enhances the reliability of the connectivity of the exposed pad to the GND plane during reflow.

To reduce power noise, a 10 µF electrolytic decoupling capacitor between power and ground should be close to where the 3.3 V supply enters the PCB. The other 0.1 µF and 1 nF ceramic chip decoupling capacitors should be close to the VCC and VEE pins to provide better decouple filtering and a shorter current return loop.

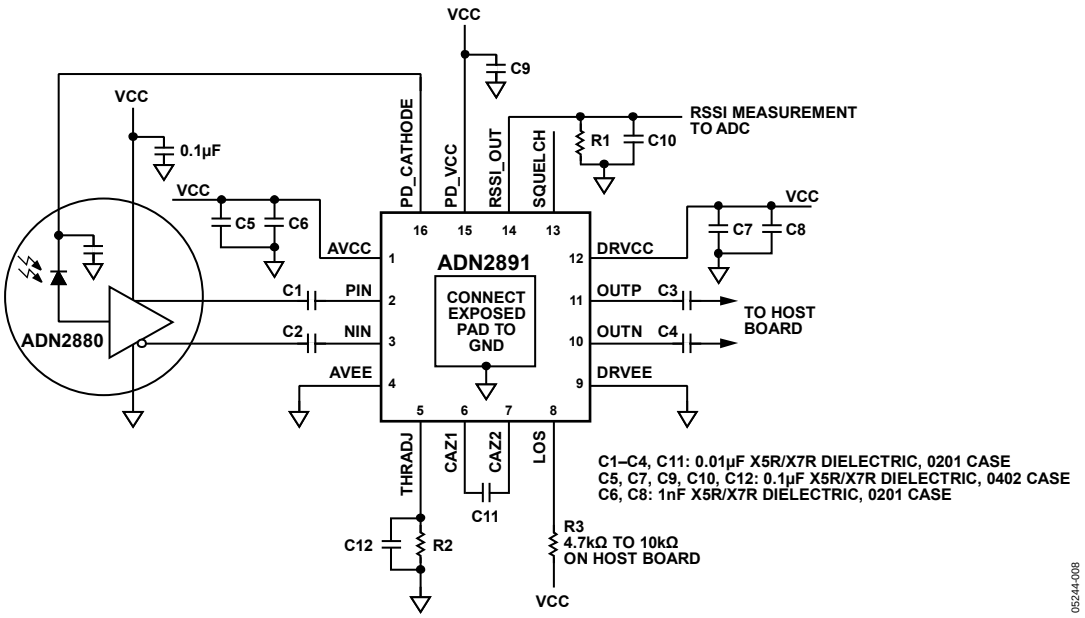

Figure 20. Typical Applications Circuit (Example of Using PIN PD and On-Chip RSSI Detector)

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PCB Layout

Figure 21 shows the recommended PCB layout. The 50 Ω transmission lines are the traces that bring the high frequency input and output signals (PIN, NIN, OUTP, and OUTN) to the SMA connectors with minimum reflection. To avoid a signal skew between the differential traces, each differential PIN/NIN and OUTP/OUTN pair should have matched trace lengths from the signal pins to the corresponding SMA connectors. C1, C2, C3, and C4 are ac coupling capacitors in series with the high speed, signal input/output paths. To minimize the possible mismatch, the ac coupling capacitor pads should be the same width as the 50 Ω transmission line trace width. To reduce supply noise, a 1 nF decoupling capacitor should be placed on the same layer as close as possible to the VCC pins. A 0.1 µF decoupling capacitor can be placed on the bottom of the PCB directly underneath the 1 nF capacitor. All high speed, CML outputs have internal 50 Ω resistor termination between the output pin and VCC. The high speed inputs, PIN and NIN, also have the internal 50 Ω termination to an internal reference voltage.

As with any high speed, mixed-signal design, keep all high speed digital traces away from sensitive analog nodes.

Soldering Guidelines for the LFCSP

The lands on the 16-lead LFCSP are rectangular. The PCB pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the LFCSP has a central exposed pad. The pad on the printed circuit board should be at least as large as the exposed pad. Users must connect the exposed pad to VEE using filled vias so that solder does not leak through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

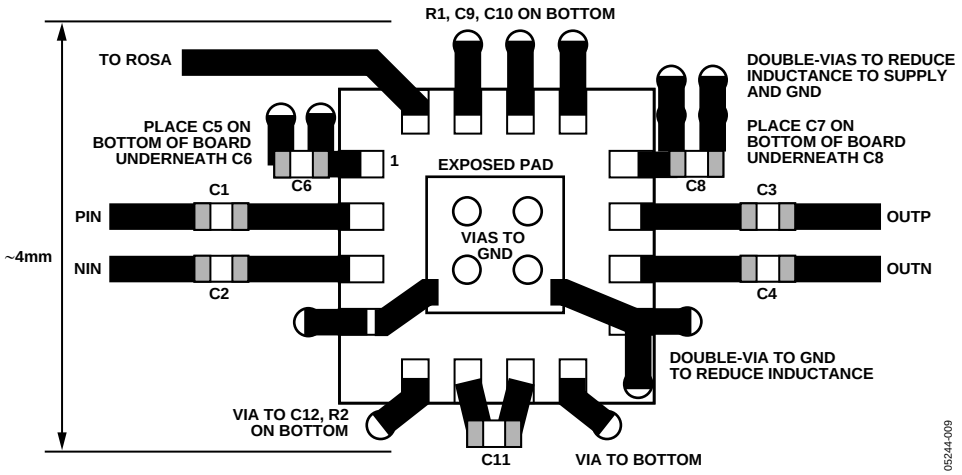

Figure 21. Recommended PCB Layout (Top View)

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OUTLINE DIMENSIONS

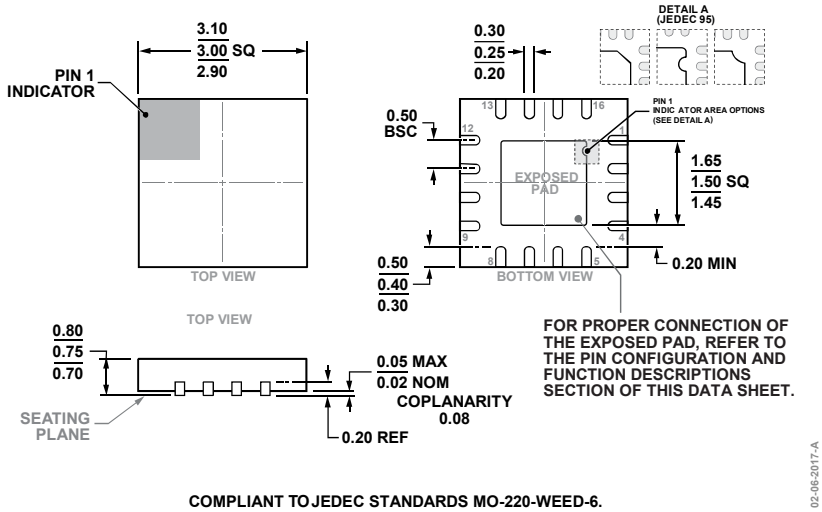

Figure 22. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-27)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADN2891ACPZ-500RL7	–40°C to +95°C	16-Lead LFCSP, 500 pieces	CP-16-27	F04
ADN2891ACPZ-RL7	–40°C to +95°C	16-Lead LFCSP, 1,500 pieces	CP-16-27	F04
ADN2891ACPZ-RL	–40°C to +95°C	16-Lead LFCSP, 5,000 pieces	CP-16-27	F04
EVAL-ADN2891EBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

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