AD8036/AD8037–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5$ V; $R_{LOAD} = 100\ \Omega$; $A_V = +1$ (AD8036); $A_V = +2$ (AD8037), V_H, V_L open, unless otherwise noted)

Parameter	Conditions	AD8036A Min	AD8036A Typ	AD8036A Max	AD8037A Min	AD8037A Typ	AD8037A Max	Unit
DYNAMIC PERFORMANCE								
Bandwidth (–3 dB)								
Small Signal	$V_{OUT} \le 0.4$ V p-p	150	240		200	270		MHz
Large Signal[1]	8036, V_{OUT} = 2.5 V p-p; 8037, V_{OUT} = 3.5 V p-p	160	195		160	190		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT} \le 0.4$ V p-p							
	8036, $R_F = 140\ \Omega$; 8037, $R_F = 274\ \Omega$		130			130		MHz
Slew Rate, Average +/–	V_{OUT} = 4 V Step, 10–90%	900	1200		1100	1500		V/µs
Rise/Fall Time	V_{OUT} = 0.5 V Step, 10–90%		1.4			1.2		ns
	V_{OUT} = 4 V Step, 10–90%		2.6			2.2		ns
Settling Time								
To 0.1%	V_{OUT} = 2 V Step		10			10		ns
To 0.01%	V_{OUT} = 2 V Step		16			16		ns
HARMONIC/NOISE PERFORMANCE								
2nd Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–59	–52		–52	–45	dBc
	$R_L = 500\ \Omega$		–66	–59		–72	–65	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–68	–61		–70	–63	dBc
	$R_L = 500\ \Omega$		–72	–65		–80	–73	dBc
3rd Order Intercept	25 MHz		46			41		dBm
Noise Figure	$R_S = 50\ \Omega$		18			14		dB
Input Voltage Noise	1 MHz to 200 MHz		6.7			4.5		$nV\sqrt{Hz}$
Input Current Noise	1 MHz to 200 MHz		2.2			2.1		$pA\sqrt{Hz}$
Average Equivalent Integrated								
Input Noise Voltage	0.1 MHz to 200 MHz		95			60		µV rms
Differential Gain Error (3.58 MHz)	$R_L = 150\ \Omega$		0.05	0.09		0.02	0.04	%
Differential Phase Error (3.58 MHz)	$R_L = 150\ \Omega$		0.02	0.04		0.02	0.04	Degree
Phase Nonlinearity	DC to 100 MHz		1.1			1.1		Degree
CLAMP PERFORMANCE								
Clamp Voltage Range[2]	V_{CH} or V_{CL}	±3.3	±3.9		±3.3	±3.9		V
Clamp Accuracy	2× Overdrive, V_{CH} = +2 V, V_{CL} = –2 V		±3	±10		±3	±10	mV
	T_{MIN}–T_{MAX}			±20			±20	mV
Clamp Nonlinearity Range[3]			100			100		mV
Clamp Input Bias Current (V_H or V_L)	8036, $V_{H,L} = \pm 1$ V; 8037, $V_{H,L} = \pm 0.5$ V		±40	±60		±50	±70	µA
	T_{MIN}–T_{MAX}			±80			±90	µA
Clamp Input Bandwidth (–3 dB)	V_{CH} or V_{CL} = 2 V p-p	150	240		180	270		MHz
Clamp Overshoot	2× Overdrive, V_{CH} or V_{CL} = 2 V p-p		1	5		1	5	%
Overdrive Recovery	2× Overdrive		1.5			1.3		ns
DC PERFORMANCE[4], $R_L = 150\ \Omega$								
Input Offset Voltage[5]			2	7		2	7	mV
	T_{MIN}–T_{MAX}			11			10	mV
Offset Voltage Drift			±10			±10		µV/°C
Input Bias Current			4	10		3	9	µA
	T_{MIN}–T_{MAX}			15			15	µA
Input Offset Current			0.3	3		0.1	3	µA
	T_{MIN}–T_{MAX}			5			5	µA
Common-Mode Rejection Ratio	$V_{CM} = \pm 2$ V	66	90		70	90		dB
Open-Loop Gain	$V_{OUT} = \pm 2.5$ V	48	55		54	60		dB
	T_{MIN}–T_{MAX}	40			46			dB
INPUT CHARACTERISTICS								
Input Resistance			500			500		kΩ
Input Capacitance			1.2			1.2		pF
Input Common-Mode Voltage Range			±2.5			±2.5		V
OUTPUT CHARACTERISTICS								
Output Voltage Range, $R_L = 150\ \Omega$		±3.2	±3.9		±3.2	±3.9		V
Output Current			70			70		mA
Output Resistance			0.3			0.3		Ω
Short Circuit Current			240			240		mA
POWER SUPPLY								
Operating Range		±3.0	±5.0	±6.0	±3.0	±5.0	±6.0	V
Quiescent Current			20.5	21.5		18.5	19.5	mA
	T_{MIN}–T_{MAX}			25			24	mA
Power Supply Rejection Ratio	T_{MIN}–T_{MAX}	50	60		56	66		dB

NOTES
[1]See Max Ratings and Theory of Operation sections of data sheet.
[2]See Max Ratings.
[3]Nonlinearity is defined as the voltage delta between the set input clamp voltage (V_H or V_L) and the voltage at which V_{OUT} starts deviating from V_{IN} (see Figure 73).
[4]Measured at $A_V = 50$.
[5]Measured with respect to the inverting input.

Specifications subject to change without notice.

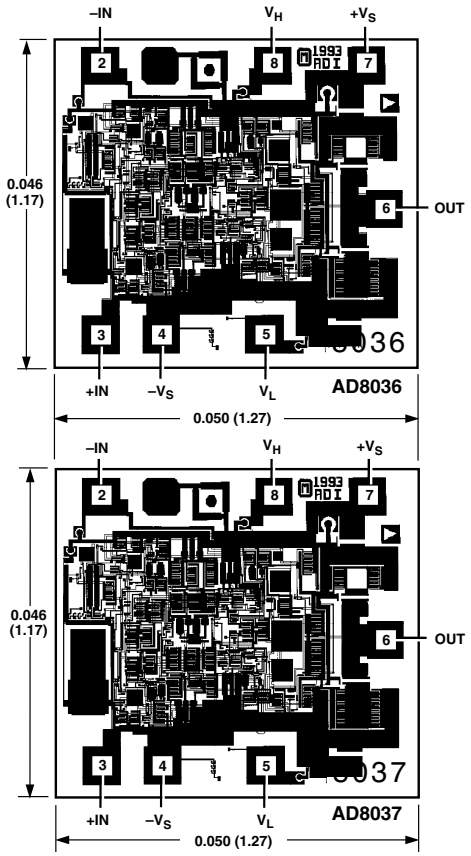
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Voltage Swing × Bandwidth Product . . . . . 350 V-MHz
$|V_H–V_{IN}|$ . . . . . ≤ 6.3 V
$|V_L–V_{IN}|$ . . . . . ≤ 6.3 V
Internal Power Dissipation[2]
Plastic DIP Package (N) . . . . . 1.3 Watts
Small Outline Package (SO) . . . . . 0.9 Watts
Input Voltage (Common Mode) . . . . . $±V_S$
Differential Input Voltage . . . . . ±1.2 V
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range N, R . . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Lead Plastic DIP: θ_{JA} = 90°C/W
8-Lead SOIC: θ_{JA} = 155°C/W
8-Lead Cerdip: θ_{JA} = 110°C/W.

METALIZATION PHOTO

Dimensions shown in inches and (mm).
Connect Substrate to $–V_S$.



MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by these devices is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8036 and AD8037 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

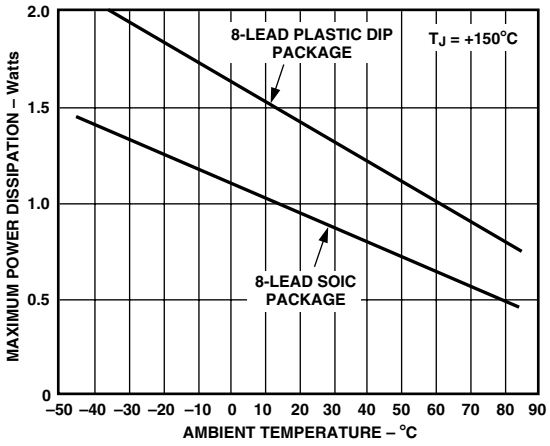


Figure 2. Plot of Maximum Power Dissipation vs. Temperature

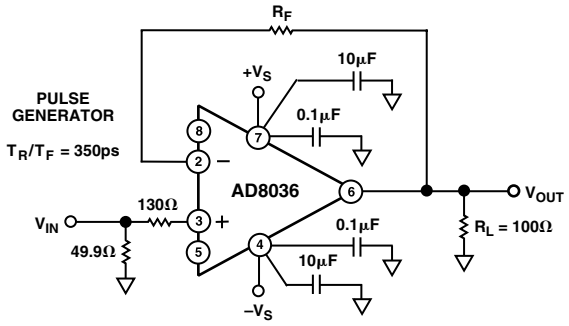
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8036AN	–40°C to +85°C	Plastic DIP	N-8
AD8036AR	–40°C to +85°C	SOIC	SO-8
AD8036AR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8
AD8036AR-REEL7	–40°C to +85°C	7" Tape and Reel	SO-8
AD8036ACHIPS	–40°C to +85°C	Die	
AD8036-EB		Evaluation Board	
5962-9559701MPA	–55°C to +125°C	Cerdip	Q-8
AD8037AN	–40°C to +85°C	Plastic DIP	N-8
AD8037AR	–40°C to +85°C	SOIC	SO-8
AD8037AR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8
AD8037AR-REEL7	–40°C to +85°C	7" Tape and Reel	SO-8
AD8037ACHIPS	–40°C to +85°C	Die	
AD8037-EB		Evaluation Board	

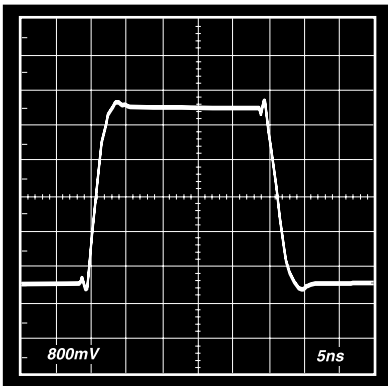
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8036/AD8037 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

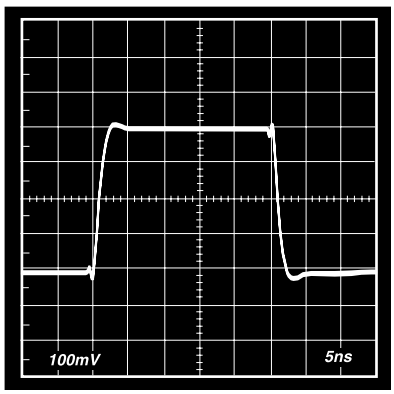
AD8036–Typical Characteristics



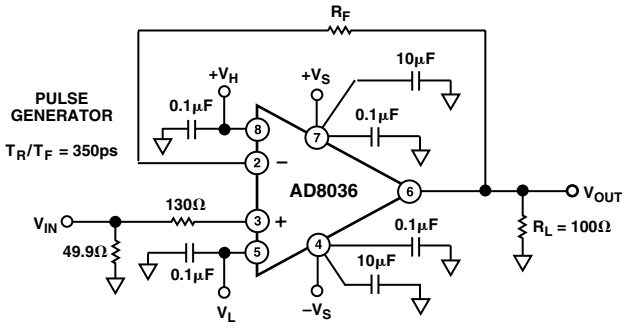
TPC 1. Noninverting Configuration, G = +1



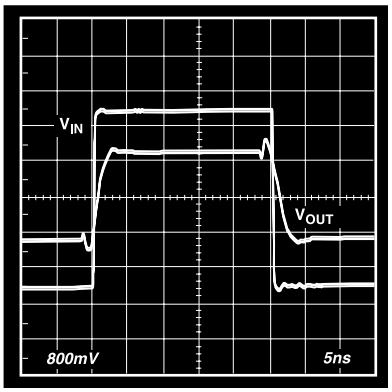
TPC 2. Large Signal Transient Response; V_O = 4 V p-p, G = +1, R_F = 140 Ω



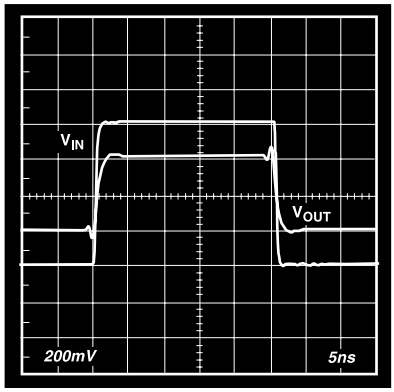
TPC 3. Small Signal Transient Response; V_O = 400 mV p-p, G = +1, R_F = 140 Ω



TPC 4. Noninverting Clamp Configuration, G = +1

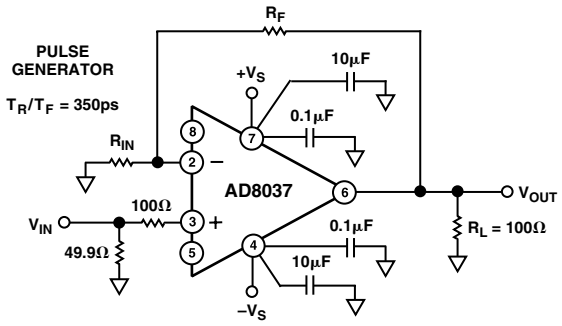


TPC 5. Clamped Large Signal Transient Response (2× Overdrive); V_O = 2 V p-p, G = +1, R_F = 140 Ω, V_H = +1 V, V_L = –1 V

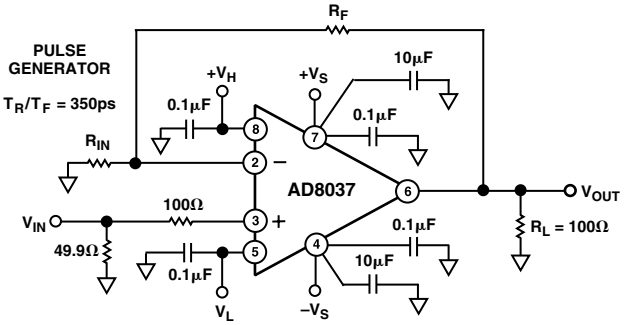


TPC 6. Clamped Small Signal Transient Response (2× Overdrive); V_O = 400 mV p-p, G = +1, R_F = 140 Ω, V_H = +0.2 V, V_L = –0.2 V

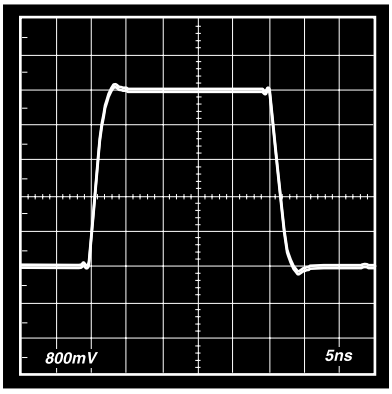
AD8037–Typical Characteristics



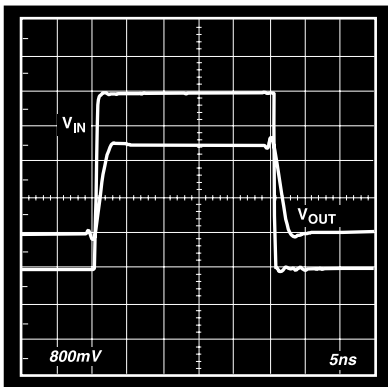
TPC 7. Noninverting Configuration, G = +2



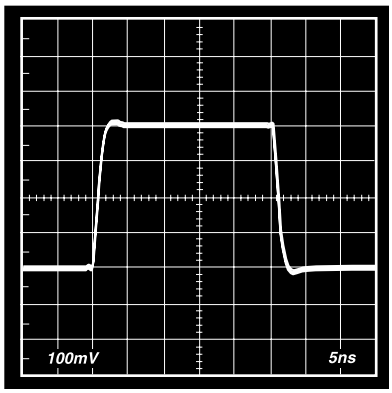
TPC 10. Noninverting Clamp Configuration, G = +2



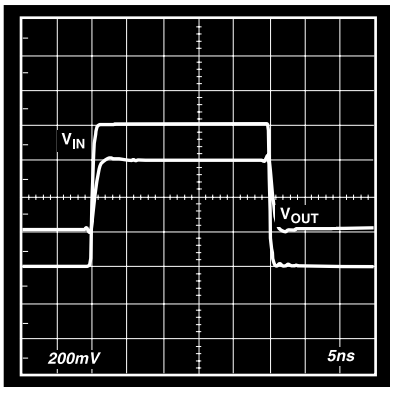
TPC 8. Large Signal Transient Response; V_O = 4 V p-p, G = +2, $R_F = R_{IN}$ = 274 Ω



TPC 11. Clamped Large Signal Transient Response (2× Overdrive); V_O = 2 V p-p, G = +2, $R_F = R_{IN}$ = 274 Ω, V_H = +0.5 V, V_L = –0.5 V

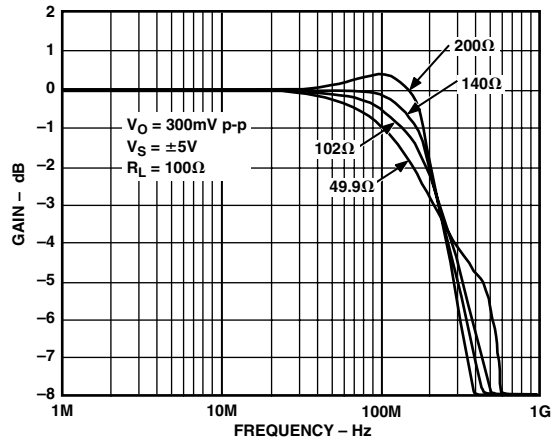


TPC 9. Small Signal Transient Response; V_O = 400 mV p-p, G = +2, $R_F = R_{IN}$ = 274 Ω

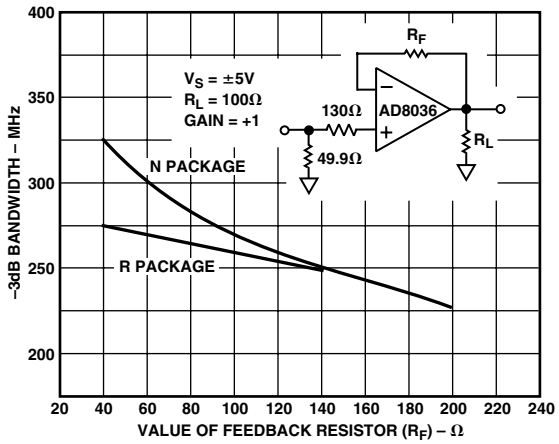


TPC 12. Clamped Small Signal Transient Response (2× Overdrive); V_O = 400 mV p-p, G = +2, $R_F = R_{IN}$ = 274 Ω, V_H = +0.1 V, V_L = –0.1 V

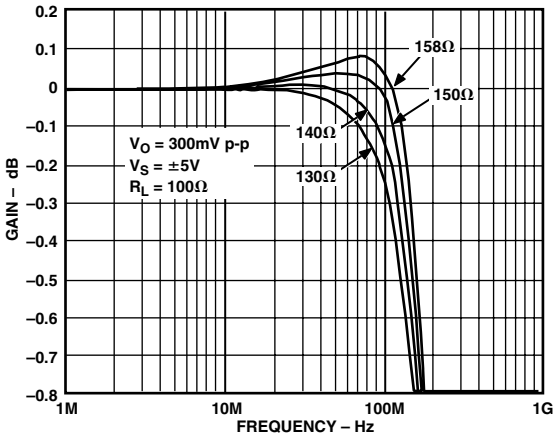
AD8036–Typical Characteristics



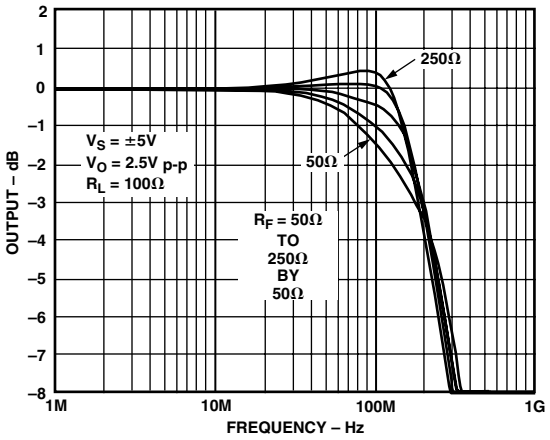
TPC 13. AD8036 Small Signal Frequency Response, G = +1



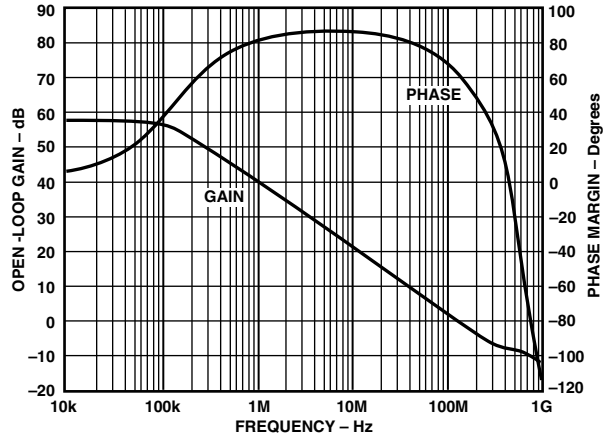
TPC 16. AD8036 Small Signal –3 dB Bandwidth vs. R_F



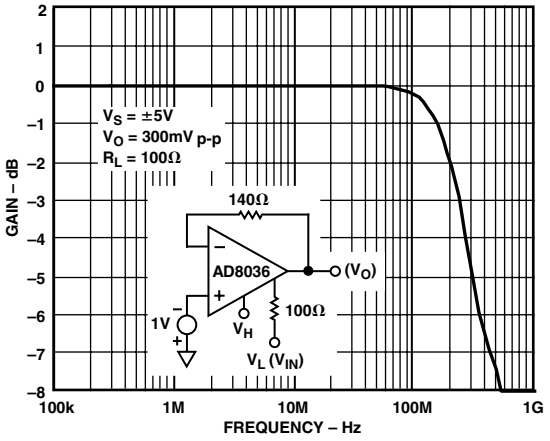
TPC 14. AD8036 0.1 dB Flatness, N Package (for R Package Add 20 Ω to R_F)



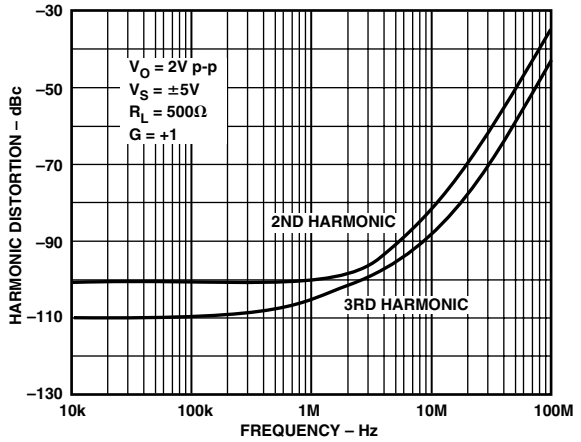
TPC 17. AD8036 Large Signal Frequency Response, G = +1



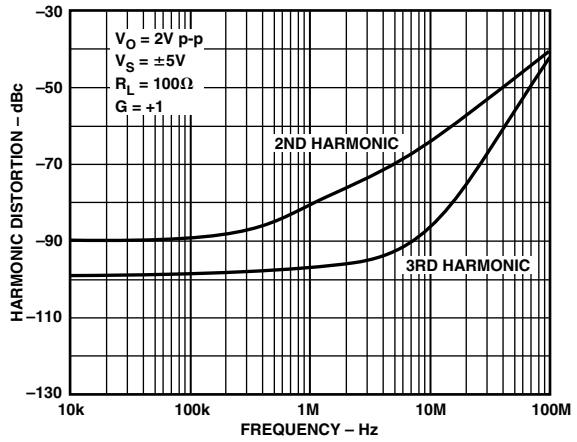
TPC 15. AD8036 Open-Loop Gain and Phase Margin vs. Frequency, R_L = 100 Ω



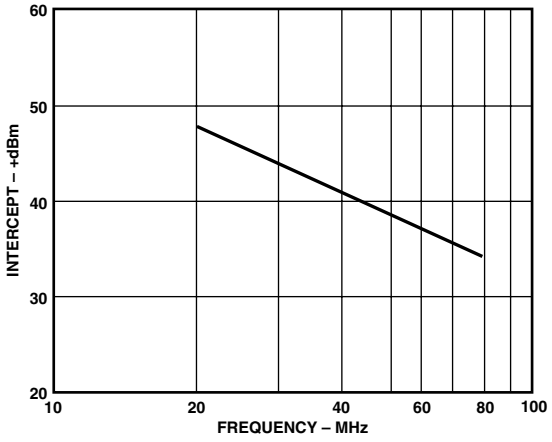
TPC 18. AD8036 Clamp Input Bandwidth, V_H, V_L



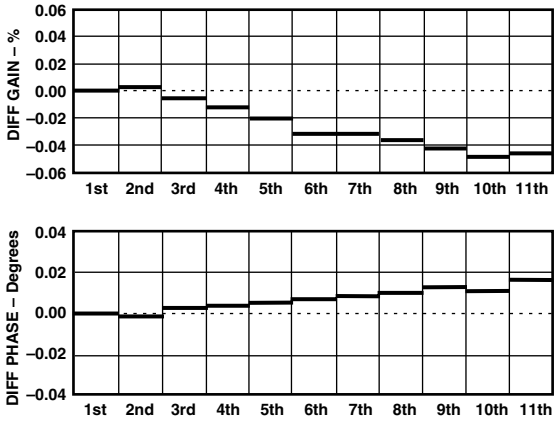
TPC 19. AD8036 Harmonic Distortion vs. Frequency, R_L = 500 Ω



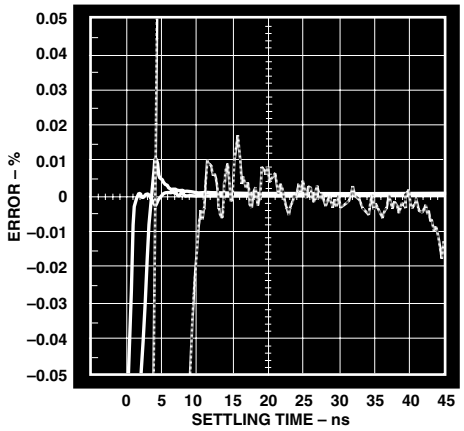
TPC 20. AD8036 Harmonic Distortion vs. Frequency, R_L = 100 Ω



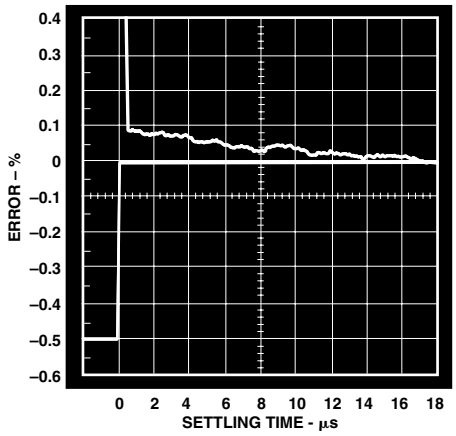
TPC 21. AD8036 Third Order Intercept vs. Frequency



TPC 22. AD8036 Differential Gain and Phase Error, G = +1, R_L = 150 Ω, F = 3.58 MHz

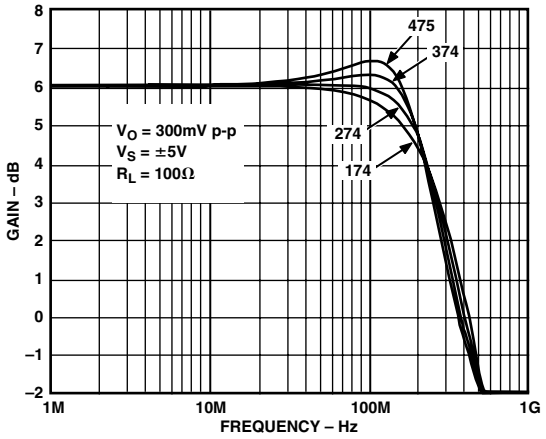


TPC 23. AD8036 Short-Term Settling Time to 0.01%, 2 V Step, G = +1, R_L = 100 Ω

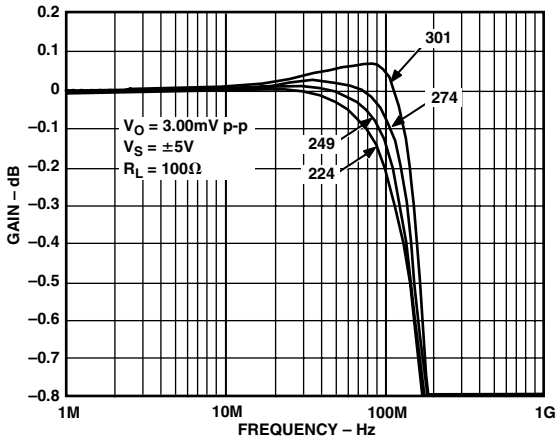


TPC 24. AD8036 Long-Term Settling Time, 2 V Step, G = +1, R_L = 100 Ω

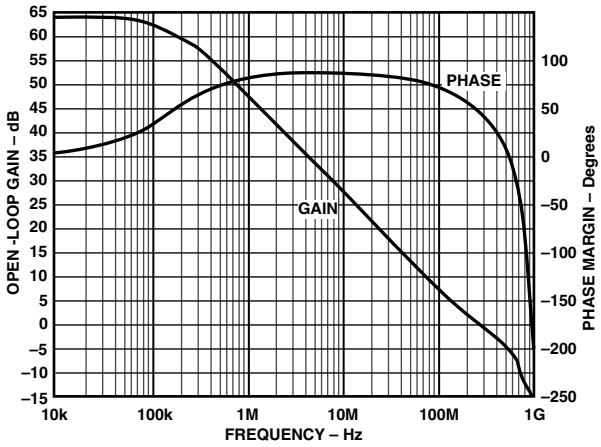
AD8037–Typical Characteristics



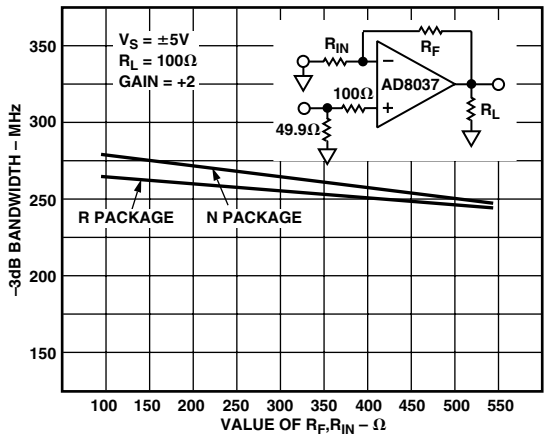
TPC 25. AD8037 Small Signal Frequency Response, G = +2



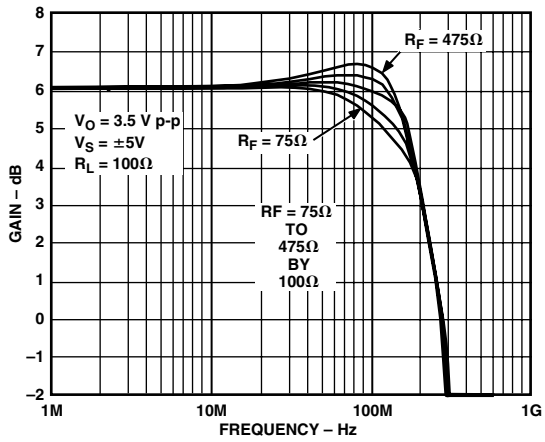
TPC 26. AD8037 0.1 dB Flatness, N Package (for R Package Add 20 Ω to R_F)



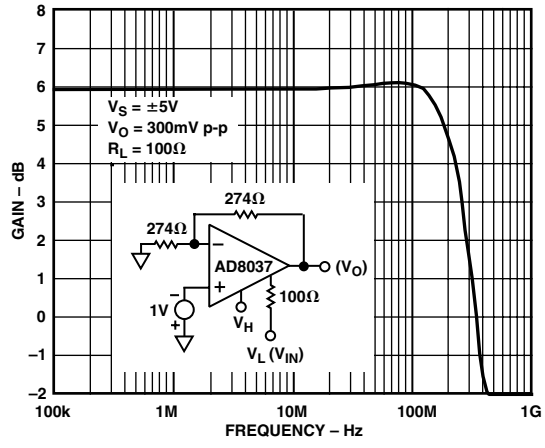
TPC 27. AD8037 Open-Loop Gain and Phase Margin vs. Frequency, R_L = 100 Ω



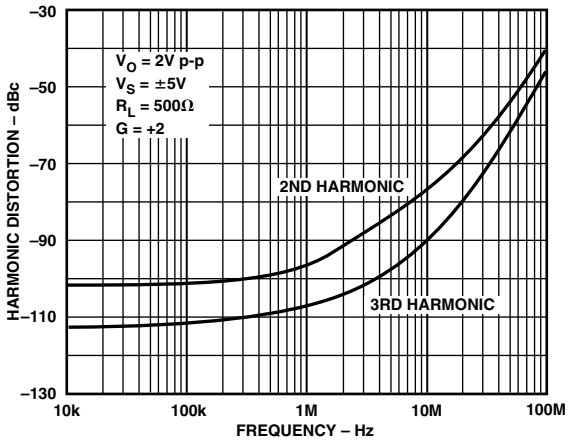
TPC 28. AD8037 Small Signal –3 dB Bandwidth vs. R_F, R_{IN}



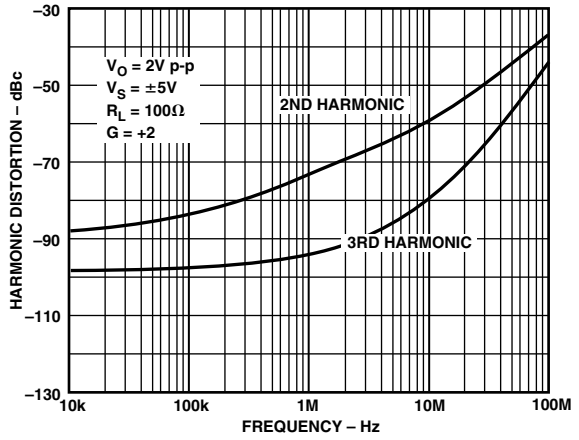
TPC 29. AD8037 Large Signal Frequency Response, G = +2



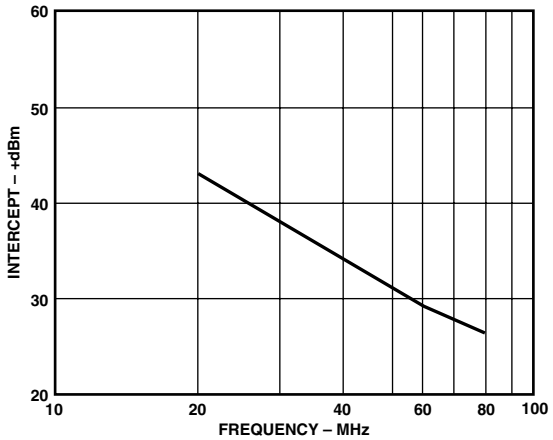
TPC 30. AD8037 Clamp Input Bandwidth, V_H, V_L



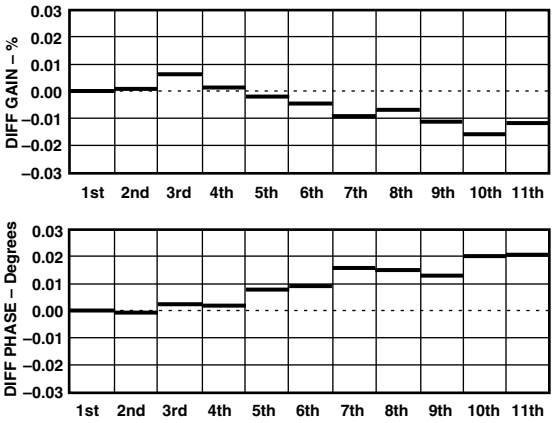
TPC 31. AD8037 Harmonic Distortion vs. Frequency, R_L = 500 Ω



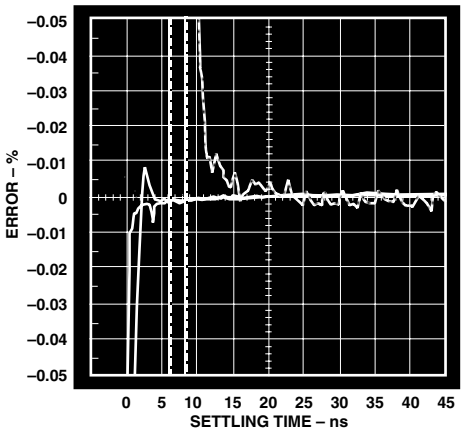
TPC 32. AD8037 Harmonic Distortion vs. Frequency, R_L = 100 Ω



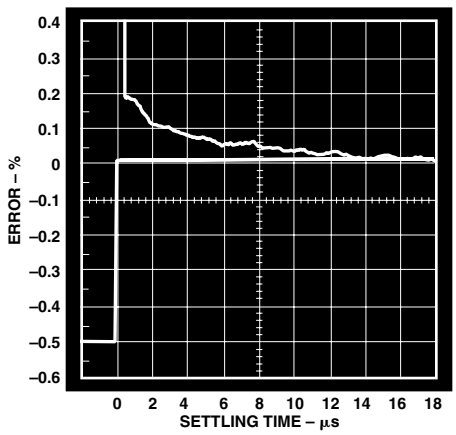
TPC 33. AD8037 Third Order Intercept vs. Frequency



TPC 34. AD8037 Differential Gain and Phase Error G = +2, R_L = 150 Ω, F = 3.58 MHz

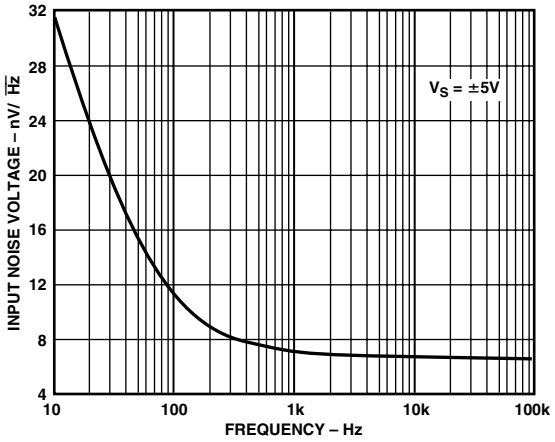


TPC 35. AD8037 Short-Term Settling Time to 0.01%, 2 V Step, G = +2, R_L = 100 Ω

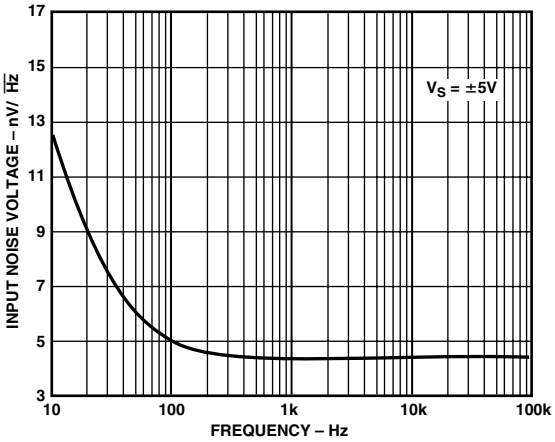


TPC 36. AD8037 Long-Term Settling Time 2 V Step, R_L = 100 Ω

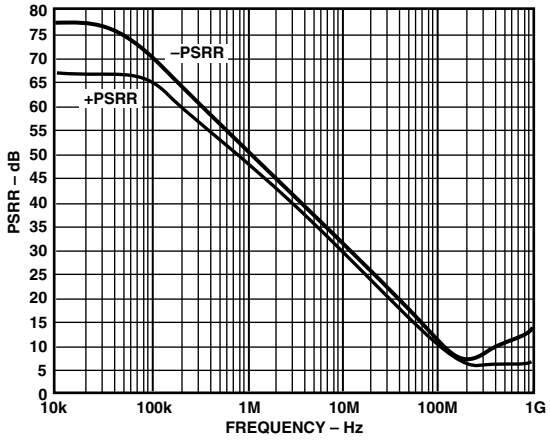
AD8036/AD8037–Typical Characteristics



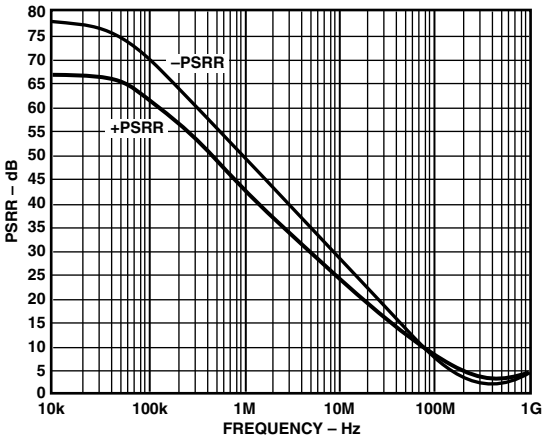
TPC 37. AD8036 Noise vs. Frequency



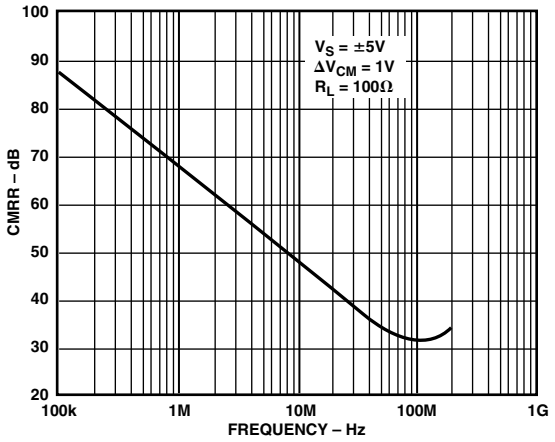
TPC 40. AD8037 Noise vs. Frequency



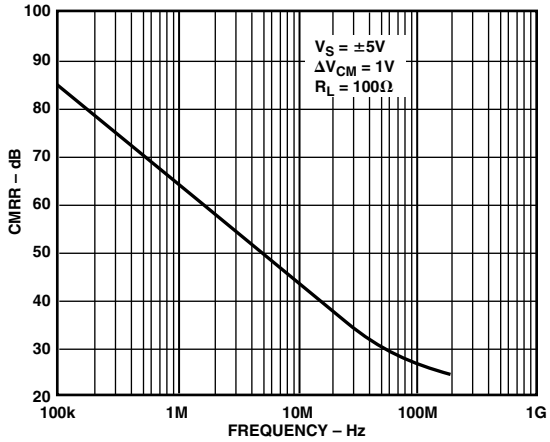
TPC 38. AD8036 PSRR vs. Frequency



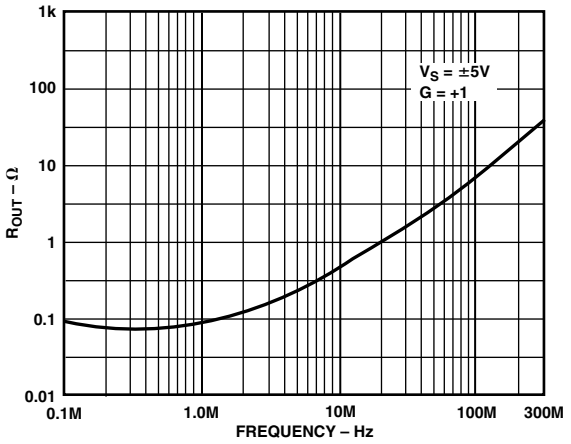
TPC 41. AD8037 PSRR vs. Frequency



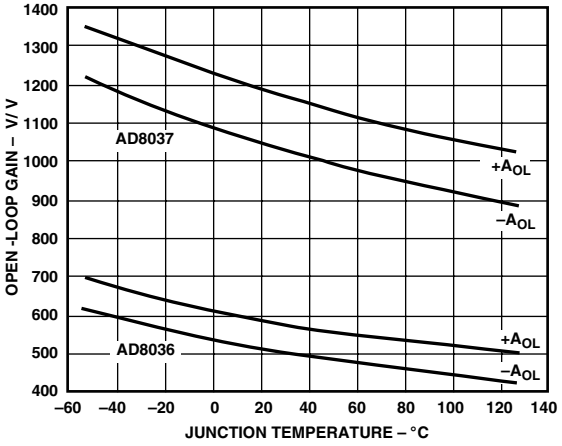
TPC 39. AD8036 CMRR vs. Frequency



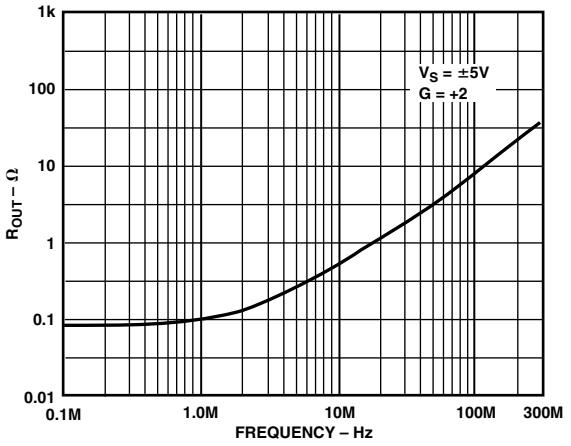
TPC 42. AD8037 CMRR vs. Frequency



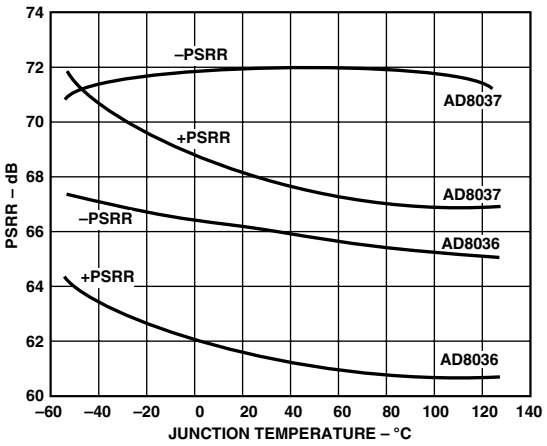
TPC 43. AD8036 Output Resistance vs. Frequency



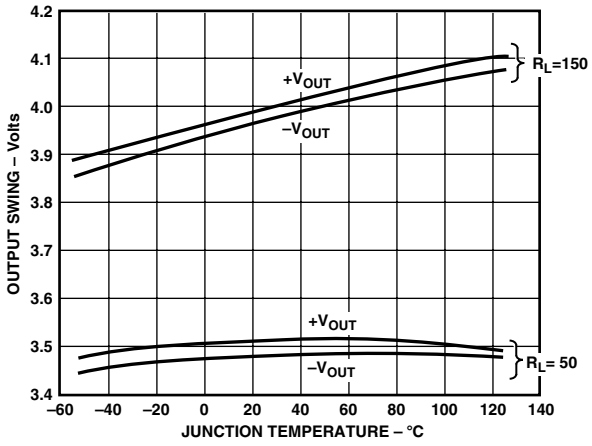
TPC 46. Open-Loop Gain vs. Temperature



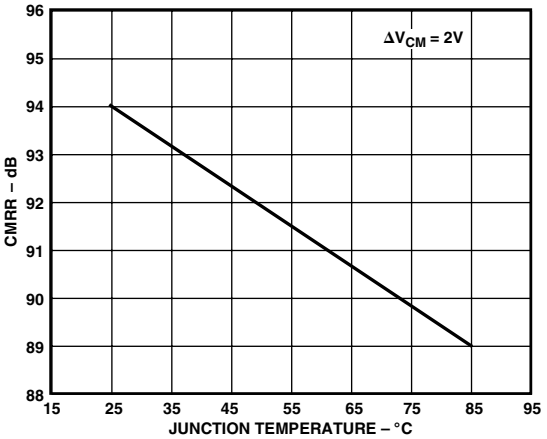
TPC 44. AD8037 Output Resistance vs. Frequency



TPC 47. PSRR vs. Temperature

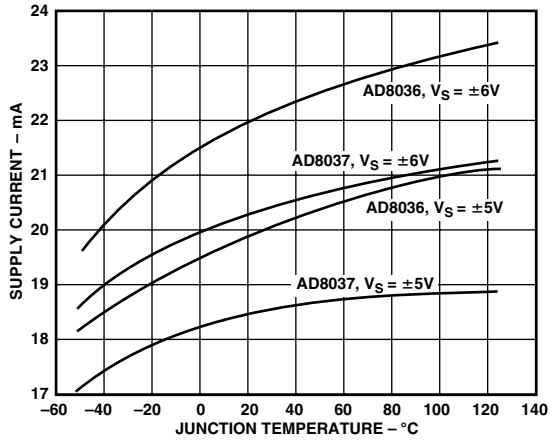


TPC 45. AD8036/AD8037 Output Swing vs. Temperature

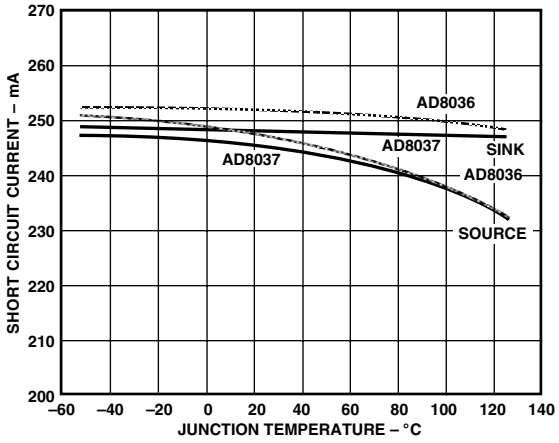


TPC 48. AD8036/AD8037 CMRR vs. Temperature

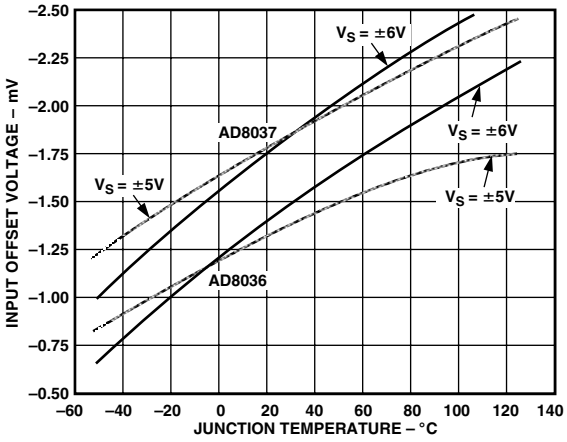
AD8036/AD8037–Typical Characteristics



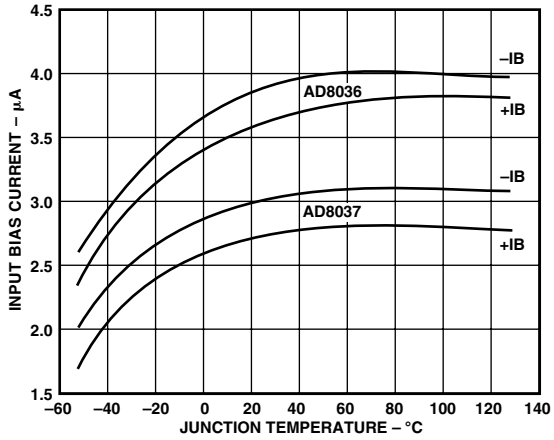
TPC 49. Supply Current vs. Temperature



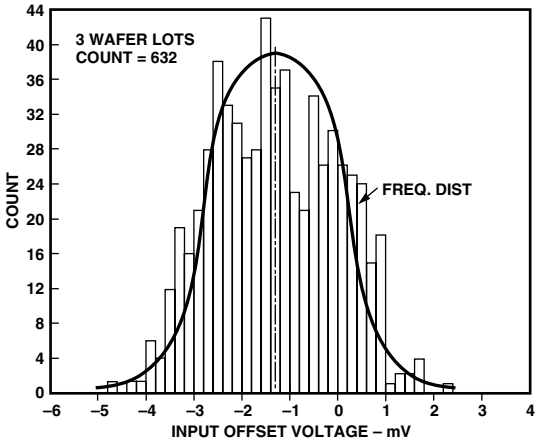
TPC 52. Short Circuit Current vs. Temperature



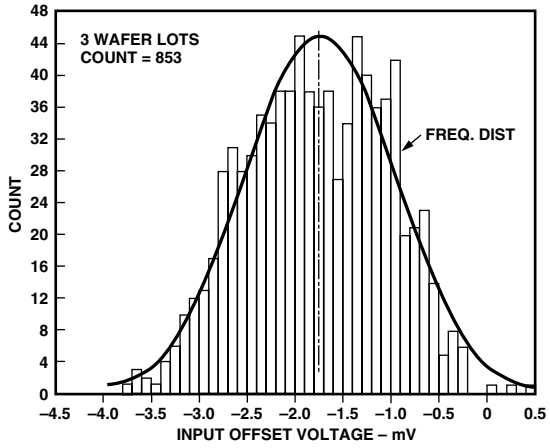
TPC 50. Input Offset Voltage vs. Temperature



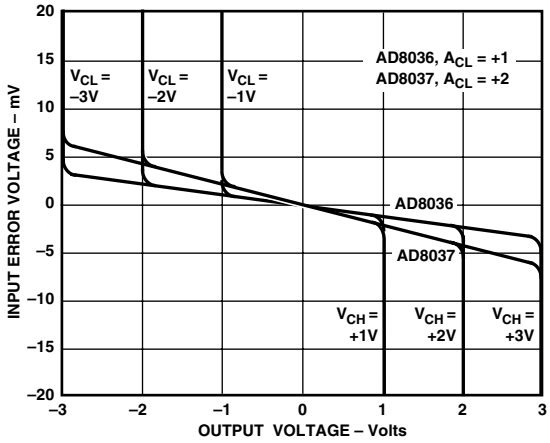
TPC 53. Input Bias Current vs. Temperature



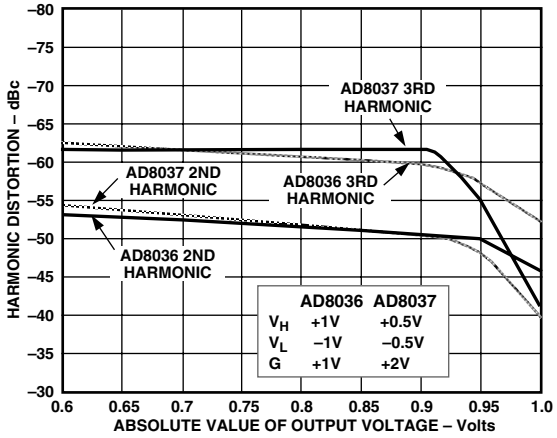
TPC 51. AD8036 Input Offset Voltage Distribution



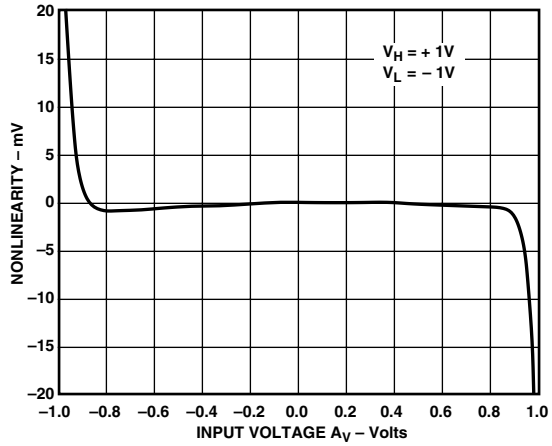
TPC 54. AD8037 Input Offset Voltage Distribution



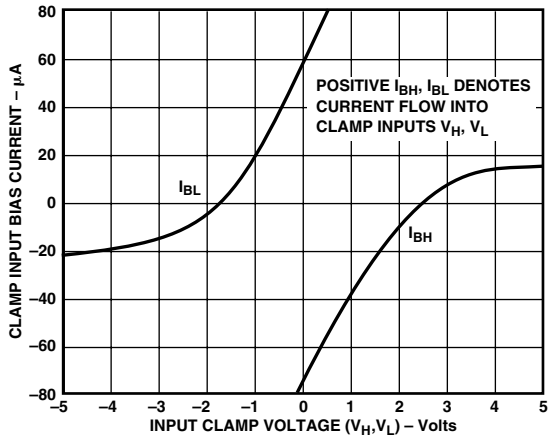
TPC 55. Input Error Voltage vs. Clamped Output Voltage



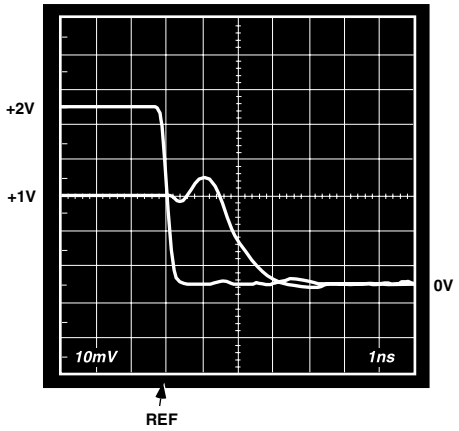
TPC 58. Harmonic Distortion as Output Approaches Clamp Voltage; V_O = 2 V p-p, R_L = 100 Ω, f = 20 MHz



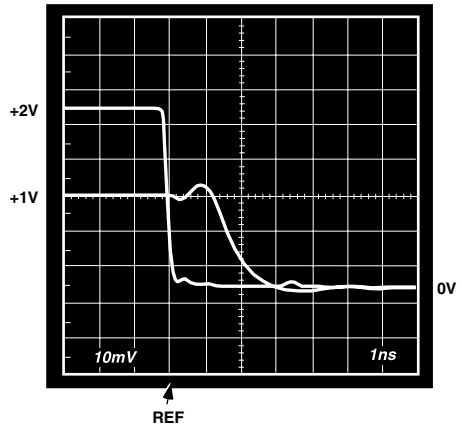
TPC 56. AD8036/AD8037 Nonlinearity Near Clamp Voltage



TPC 59. AD8036/AD8037 Clamp Input Bias Current vs. Input Clamp Voltage

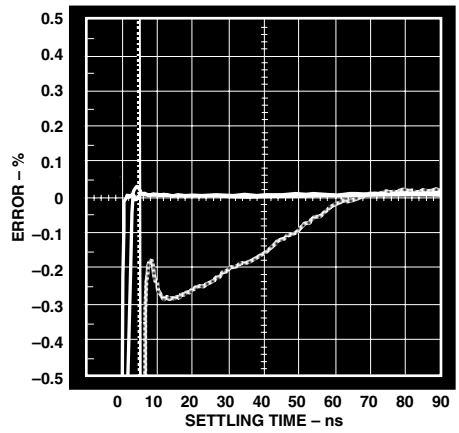


TPC 57. AD8036 Clamp Overdrive (2×) Recovery

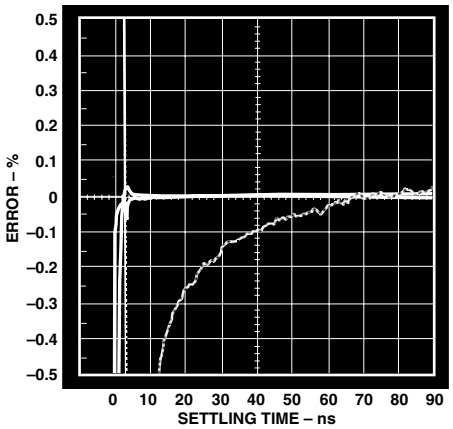


TPC 60. AD8037 Clamp Overdrive (2×) Recovery

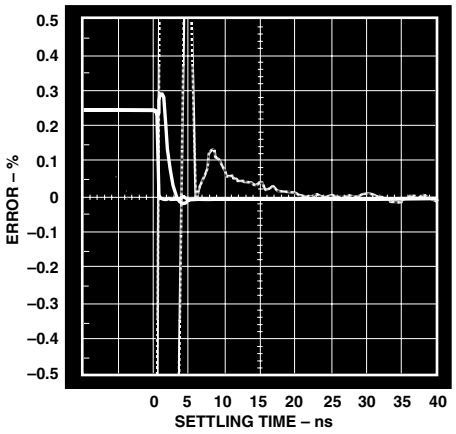
AD8036/AD8037–Clamp Characteristics



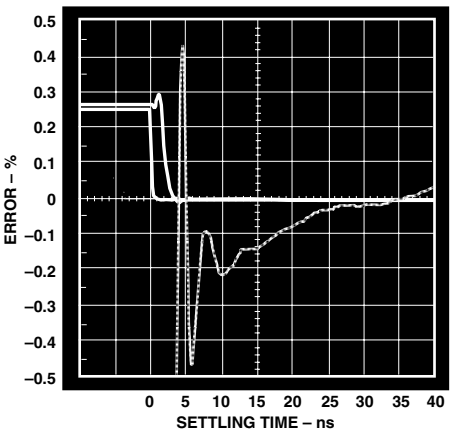
TPC 61. AD8036 Clamp Settling (0.1%), V_H = +1 V, V_L = –1 V, 2× Overdrive



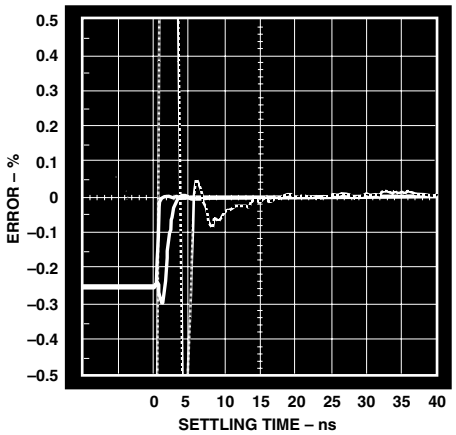
TPC 64. AD8037 Clamp Settling (0.1%), V_H = +0.5 V, V_L = –0.5 V, 2× Overdrive



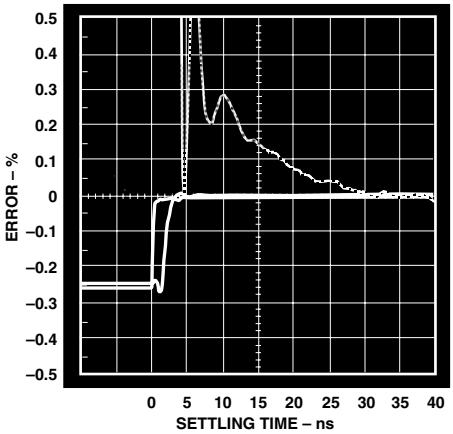
TPC 62. AD8036 Clamp Recovery Settling Time (High), from +2× Overdrive to 0 V



TPC 65. AD8037 Clamp Recovery Settling Time (High), from +2× Overdrive to 0 V



TPC 63. AD8036 Clamp Recovery Settling Time (Low), from –2× Overdrive to 0 V



TPC 66. AD8037 Clamp Recovery Settling Time (Low), from –2× Overdrive to 0 V

THEORY OF OPERATION

General

The AD8036 and AD8037 are wide bandwidth, voltage feedback clamp amplifiers. Since their open-loop frequency response follows the conventional 6 dB/octave roll-off, their gain bandwidth product is basically constant. Increasing their closed-loop gain results in a corresponding decrease in small signal bandwidth. This can be observed by noting the bandwidth specification, between the AD8036 (gain of 1) and AD8037 (gain of 2). The AD8036/AD8037 typically maintain 65 degrees of phase margin. This high margin minimizes the effects of signal and noise peaking.

While the AD8036 and AD8037 can be used in either an inverting or noninverting configuration, the clamp function will only work in the noninverting mode. As such, this section shows connections only in the noninverting configuration. Applications that require an inverting configuration will be discussed in the Applications section. In applications that do not require clamping, Pins 5 and 8 (respectively V_L and V_H) may be left floating. See Input Clamp Amp Operation and Applications sections otherwise.

Feedback Resistor Choice

The value of the feedback resistor is critical for optimum performance on the AD8036 (gain +1) and less critical as the gain increases. Therefore, this section is specifically targeted at the AD8036.

At minimum stable gain (+1), the AD8036 provides optimum dynamic performance with R_F = 140 Ω. This resistor acts only as a parasitic suppressor against damped RF oscillations that can occur due to lead (input, feedback) inductance and parasitic capacitance. This value of R_F provides the best combination of wide bandwidth, low parasitic peaking, and fast settling time.

In fact, for the same reasons, a 100–130 Ω resistor should be placed in series with the positive input for other AD8036 noninverting configurations. The correct connection is shown in Figure 3.

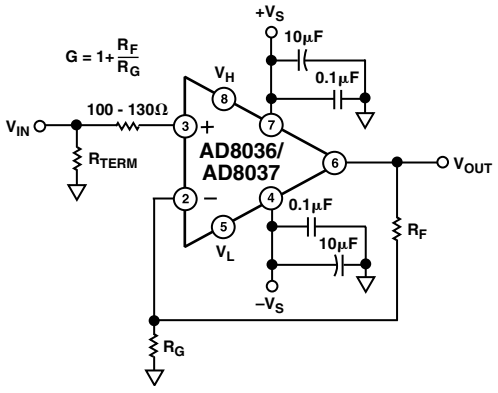


Figure 3. Noninverting Operation

For general voltage gain applications, the amplifier bandwidth can be closely estimated as:

$$f_{3\,dB} \cong \frac{\omega_O}{2\pi\left[1+\left(\frac{R_F}{R_G}\right)\right]}$$

This estimation loses accuracy for gains of +2/–1 or lower due to the amplifier's damping factor. For these "low gain" cases, the bandwidth will actually extend beyond the calculated value (see Closed-Loop BW plots, TPCs 13 and 25).

Pulse Response

Unlike a traditional voltage feedback amplifier, where the slew speed is dictated by its front end dc quiescent current and gain bandwidth product, the AD8036 and AD8037 provide "on demand" current that increases proportionally to the input "step" signal amplitude. This results in slew rates (1200 V/µs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (2.1 pA/$\sqrt{\text{Hz}}$), gives the AD8036 and AD8037 the best attributes of both voltage and current feedback amplifiers.

Large Signal Performance

The outstanding large signal operation of the AD8036 and AD8037 is due to a unique, proprietary design architecture. In order to maintain this level of performance, the maximum 350 V-MHz product must be observed, (e.g., @ 100 MHz, $V_O \le 3.5$ V p-p).

Power Supply and Input Clamp Bypassing

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 µF) will be required to provide the best settling time and lowest distortion. A parallel combination of at least 4.7 µF, and between 0.1 µF and 0.01 µF, is recommended. Some brands of electrolytic capacitors will require a small series damping resistor ≈4.7 Ω for optimum results.

When the AD8036 and AD8037 are used in clamping mode, and a dc voltage is connected to clamp inputs V_H and V_L, a 0.1 µF bypassing capacitor is required between each input pin and ground in order to maintain stability.

Driving Capacitive Loads

The AD8036 and AD8037 were designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, the best frequency response is obtained by the addition of a small series resistance as shown in Figure 4. The accompanying graph shows the optimum value for R_{SERIES} vs. capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L. For capacitive loads of 6 pF or less, no R_{SERIES} is necessary.

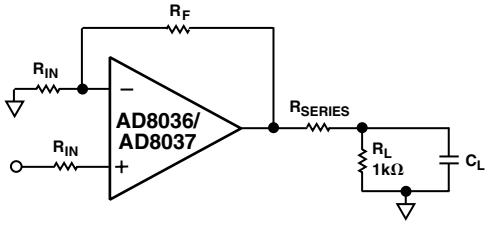


Figure 4. Driving Capacitive Loads

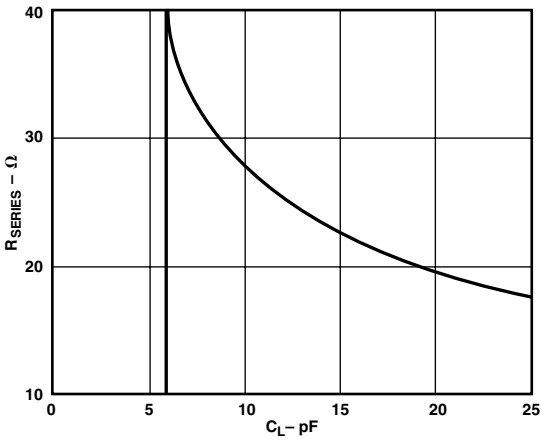


Figure 5. Recommended R_{SERIES} vs. Capacitive Load

INPUT CLAMPING AMPLIFIER OPERATION

The key to the AD8036 and AD8037's fast, accurate clamp and amplifier performance is their unique patent pending CLAMPIN input clamp architecture. This new design reduces clamp errors by more than 10× over previous output clamp based circuits, as well as substantially increasing the bandwidth, precision and versatility of the clamp inputs.

Figure 6 is an idealized block diagram of the AD8036 connected as a unity gain voltage follower. The primary signal path comprises A1 (a 1200 V/µs, 240 MHz high voltage gain, differential to single-ended amplifier) and A2 (a G = +1 high current gain output buffer). The AD8037 differs from the AD8036 only in that A1 is optimized for closed-loop gains of two or greater.

The CLAMPIN section is comprised of comparators C_H and C_L, which drive switch S1 through a decoder. The unity-gain buffers in series with $+V_{IN}$, V_H, and V_L inputs isolate the input pins from the comparators and S1 without reducing bandwidth or precision.

The two comparators have about the same bandwidth as A1 (240 MHz), so they can keep up with signals within the useful bandwidth of the AD8036. To illustrate the operation of the CLAMPIN circuit, consider the case where V_H is referenced to 1 V, V_L is open, and the AD8036 is set for a gain of +1, by connecting its output back to its inverting input through the recommended 140 Ω feedback resistor. Note that the main signal path always operates closed loop, since the CLAMPIN circuit only affects A1's noninverting input.

If a 0 V to 2 V voltage ramp is applied to the AD8036's $+V_{IN}$ for the connection just described, V_{OUT} should track $+V_{IN}$ perfectly up to 1 V, then should limit at exactly 1 V as $+V_{IN}$ continues to 2 V.

In practice, the AD8036 comes close to this ideal behavior. As the $+V_{IN}$ input voltage ramps from zero to 1 V, the output of the high limit comparator C_H starts in the off state, as does the output of C_L. When $+V_{IN}$ just exceeds V_{IN} (ideally, by say 1 µV, practically by about 18 mV), C_H changes state, switching S1 from "A" to "B" reference level. Since the + input of A1 is now connected to V_H, further increases in $+V_{IN}$ have no effect on the AD8036's output voltage. In short, the AD8036 is now operating as a unity-gain buffer for the V_H input, as any variation in V_H, for V_H > 1 V, will be faithfully reproduced at V_{OUT}.

Operation of the AD8036 for negative input voltages and negative clamp levels on V_L is similar, with comparator C_L controlling S1. Since the comparators see the voltage on the $+V_{IN}$ pin as their common reference level, then the voltage V_H and V_L are defined as "High" or "Low" with respect to $+V_{IN}$. For example, if V_{IN} is set to zero volts, V_H is open, and V_L is +1 V, comparator C_L will switch S1 to "C," so the AD8036 will buffer the voltage on V_L and ignore $+V_{IN}$.

The performance of the AD8036 and AD8037 closely matches the ideal just described. The comparator's threshold extends from 60 mV inside the clamp window defined by the voltages on V_L and V_H to 60 mV beyond the window's edge. Switch S1 is implemented with current steering, so that A1's +input makes a continuous transition from say, V_{IN} to V_H as the input voltage traverses the comparator's input threshold from 0.9 V to 1.0 V for V_H = 1.0 V.

The practical effect of these nonidealities is to soften the transition from amplification to clamping modes, without compromising the absolute clamp limit set by the CLAMPIN circuit. Figure 7 is a graph of V_{OUT} vs. V_{IN} for the AD8036 and a typical output clamp amplifier. Both amplifiers are set for G = +1 and V_H = 1 V.

The worst case error between V_{OUT} (ideally clamped) and V_{OUT} (actual) is typically 18 mV times the amplifier closed-loop gain. This occurs when V_{IN} equals V_H (or V_L). As V_{IN} goes above and/or below this limit, V_{OUT} will settle to within 5 mV of the ideal value.

In contrast, the output clamp amplifier's transfer curve typically will show some compression starting at an input of 0.8 V, and can have an output voltage as far as 200 mV over the clamp limit. In addition, since the output clamp in effect causes the amplifier to operate open loop in clamp mode, the amplifier's output impedance will increase, potentially causing additional errors.

The AD8036's and AD8037's CLAMPIN input clamp architecture works only for noninverting or follower applications and, since it operates on the input, the clamp voltage levels V_H and V_L, and input error limits will be multiplied by the amplifier's

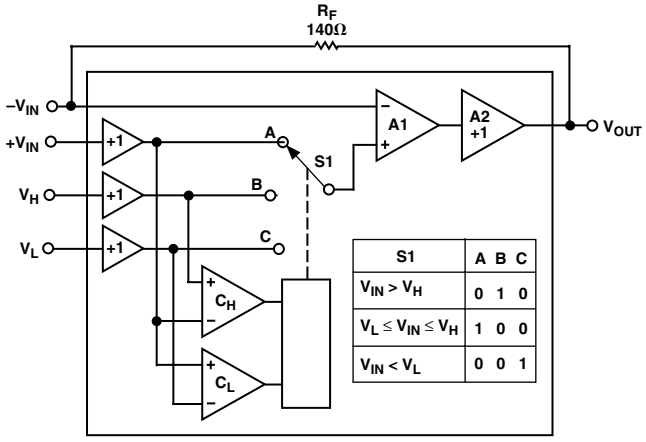


Figure 6. AD8036/AD8037 Clamp Amp System

closed-loop gain at the output. For instance, to set an output limit of ±1 V for an AD8037 operating at a gain of 3.0, V_H and V_L would need to be set to +0.333 V and –0.333 V, respectively.

The only restriction on using the AD8036's and AD8037's $+V_{IN}$, V_L, V_H pins as inputs is that the maximum voltage difference between $+V_{IN}$ and V_H or V_L should not exceed 6.3 V, and all three voltages be within the supply voltage range. For example, if V_L is set at –3 V, then V_{IN} should not exceed +3.3 V.

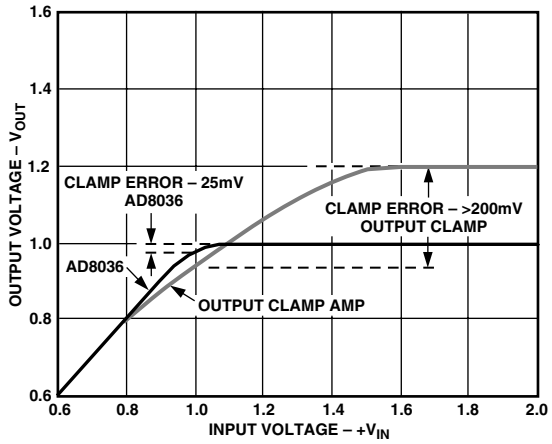


Figure 7. Output Clamp Error vs. Input Clamp Error

AD8036/AD8037 APPLICATIONS

The AD8036 and AD8037 use a unique input clamping circuit to perform the clamping function. As a result, they provide the clamping function better than traditional output clamping devices and provide additional flexibility to perform other unique applications.

There are, however, some restrictions on circuit configurations; and some calculations need to be performed in order to figure the clamping level, as a result of clamping being performed at the input stage.

The major restriction on the clamping feature of the AD8036/AD8037 is that clamping occurs only when using the amplifiers in the noninverting mode. To clamp in an inverting circuit, an additional inverting gain stage is required. Another restriction is that V_H be greater than V_L, and that each be within the output voltage range of the amplifier (±3.9 V). V_H can go below ground and V_L can go above ground as long as V_H is kept higher than V_L.

Unity Gain Clamping

The simplest circuit for calculating the clamp levels is a unity gain follower as shown in Figure 8. In this case, the AD8036 should be used since it is compensated for noninverting unity gain.

This circuit will clamp at an upper voltage set by V_H (the voltage applied to Pin 8) and a lower voltage set by V_L (the voltage applied to Pin 5).

Clamping with Gain

Figure 9 shows an AD8037 configured for a noninverting gain of two. The AD8037 is used in this circuit since it is compensated for gains of two or greater and provides greater bandwidth. In this case, the high clamping level at the output will occur at

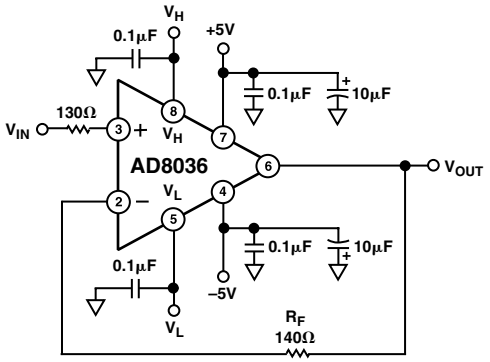


Figure 8. Unity Gain Noninverting Clamp

$2 \times V_H$ and the low clamping level at the output will be $2 \times V_L$. The equations governing the output clamp levels in circuits configured for noninverting gain are:

$$V_{CH} = G \times V_H$$

$$V_{CL} = G \times V_L$$

where: V_{CH} is the high *output* clamping level
V_{CL} is the low *output* clamping level
G is the gain of the amplifier configuration
V_H is the high input clamping level (Pin 8)
V_L is the low input clamping level (Pin 5)

*Amplifier offset is assumed to be zero.

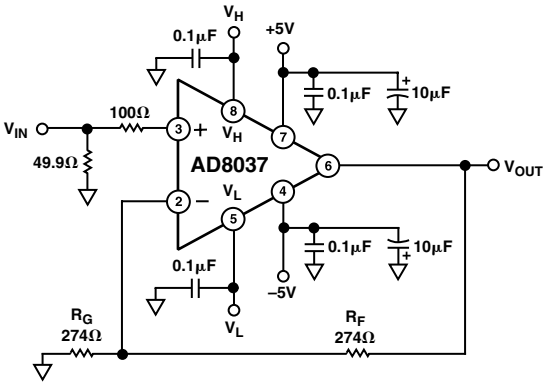


Figure 9. Gain of Two Noninverting Clamp

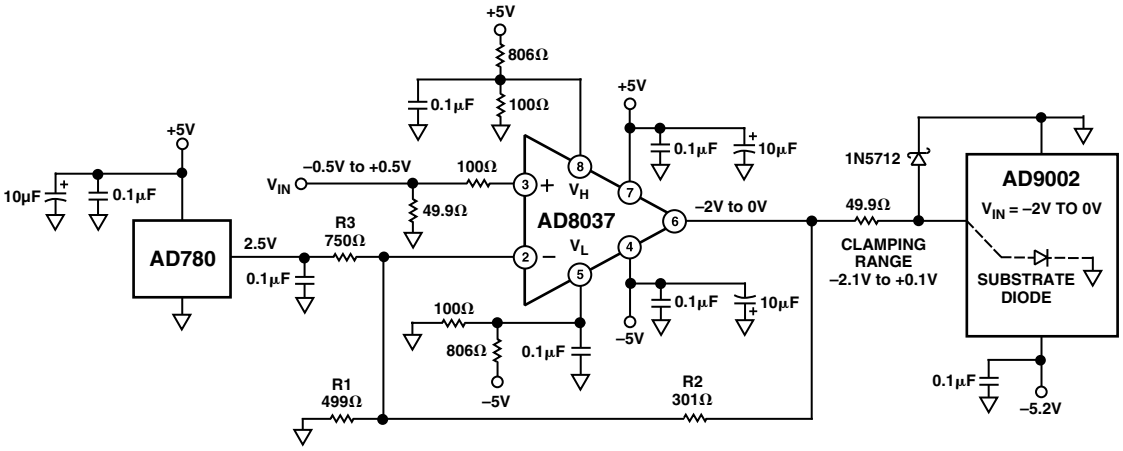


Figure 10. Gain of Two, Noninverting with Offset AD8037 Driving an AD9002—8-Bit, 125 MSPS A/D Converter

Clamping with an Offset

Some op amp circuits are required to operate with an offset voltage. These are generally configured in the inverting mode where the offset voltage can be summed in as one of the inputs. Since AD8036/AD8037 clamping does not function in the inverting mode, it is not possible to clamp with this configuration.

Figure 10 shows a noninverting configuration of an AD8037 that provides clamping and also has an offset. The circuit shows the AD8037 as a driver for an AD9002, an 8-bit, 125 MSPS A/D converter and illustrates some of the considerations for using an AD8037 with offset and clamping.

The analog input range of the AD9002 is from ground to –2 V. The input should not go more than 0.5 V outside this range in order to prevent disruptions to the internal workings of the A/D and to avoid drawing excess current. These requirements make the AD8037 a prime candidate for signal conditioning.

When an offset is added to a noninverting op amp circuit, it is fed in through a resistor to the inverting input. The result is that the op amp must now operate at a closed-loop gain greater than unity. For this circuit a gain of two was chosen which allows the use of the AD8037. The feedback resistor, R2, is set at 301 Ω for optimum performance of the AD8037 at a gain of two.

There is an interaction between the offset and the gain, so some calculations must be performed to arrive at the proper values for R1 and R3. For a gain of two the parallel combination of resistors R1 and R3 must be equal to the feedback resistor R2. Thus

$$R1 \times R3/R1 + R3 = R2 = 301\ \Omega$$

The reference used to provide the offset is the AD780 whose output is 2.5 V. This must be divided down to provide the 1 V offset desired. Thus

$$2.5\ V \times R1/(R1 + R3) = 1\ V$$

When the two equations are solved simultaneously we get R1 = 499 Ω and R3 = 750 Ω (using closest 1% resistor values in all cases). This positive 1 V offset at the input translates to a –1 V offset at the output.

The usable input signal swing of the AD9002 is 2 V p-p. This is centered about the –1 V offset making the usable signal range from 0 V to –2 V. It is desirable to clamp the input signal so that it goes no more than 100 mV outside of this range in either direction. Thus, the high clamping level should be set at +0.1 V and the low clamping level should be set at –2.1 V as seen at the input of the AD9002 (output of AD8037).

Because the clamping is done at the input stage of the AD8037, the clamping level as seen at the output is affected by not only the gain of the circuit as previously described, but also by the offset. Thus, in order to obtain the desired clamp levels, V_H must be biased at +0.55 V while V_L must be biased at –0.55 V.

The clamping levels as seen at the output can be calculated by the following:

$$V_{CH} = V_{OFF} + G \times V_H$$

$$V_{CL} = V_{OFF} + G \times V_L$$

Where V_{OFF} is the offset voltage that appears at the output.

The resistors used to generate the voltages for V_H and V_L should be kept to a minimum in order to reduce errors due to clamp bias current. This current is dependent on V_H and V_L (see TPC 59) and will create a voltage drop across whatever resistance is in series with each clamp input. This extra error voltage is multiplied by the closed-loop gain of the amplifier and can be substantial, especially in high closed-loop gain configurations. A 0.1 μF bypass capacitor should be placed between input clamp pins V_H and V_L and ground to ensure stable operation.

The 1N5712 Schottky diode is used for protection from forward biasing the substrate diode in the AD9002 during power-up transients.

Programmable Pulse Generator

The AD8036/AD8037's clamp output can be set accurately and has a well controlled flat level. This along with wide bandwidth and high slew rate make them very well suited for programmable level pulse generators.

Figure 11 is a schematic for a pulse generator that can directly accept TTL generated timing signals for its input and generate pulses at the output up to 24 V p-p with 2500 V/μs slew rate. The output levels can be programmed to anywhere in the range –12 V to +12 V.

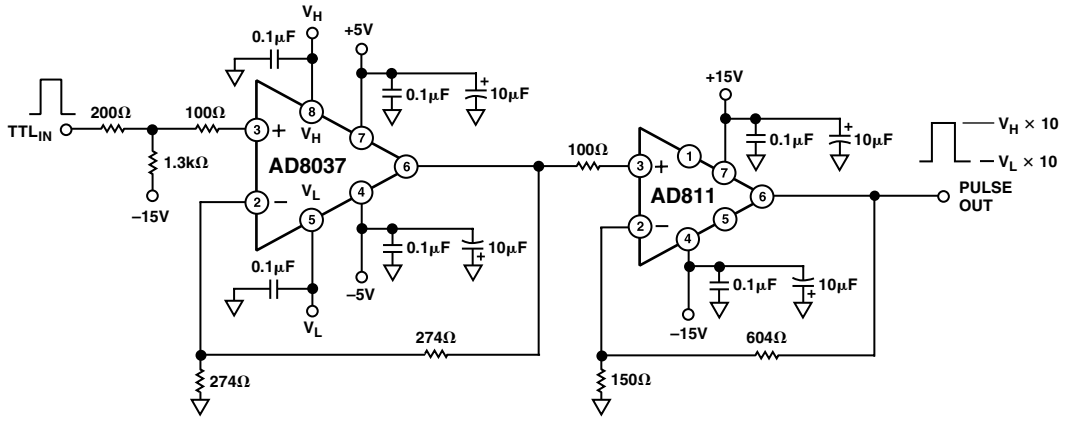


Figure 11. Programmable Pulse Generator

The circuit uses an AD8037 operating at a gain of two with an AD811 to boost the output to the ±12 V range. The AD811 was chosen for its ability to operate with ±15 V supplies and its high slew rate.

R1 and R2 act as a level shifter to make the TTL signal levels be approximately symmetrical above and below ground. This ensures that both the high and low logic levels will be clamped by the AD8037. For well controlled signal levels in the output pulse, the high and low output levels should result from the clamping action of the AD8037 and not be controlled by either the high or low logic levels passing through a linear amplifier. For good rise and fall times at the output pulse, a logic family with high speed edges should be used.

The high logic levels are clamped at two times the voltage at V_H, while the low logic levels are clamped at two times the voltage at V_L. The output of the AD8037 is amplified by the AD811 operating at a gain of 5. The overall gain of 10 will cause the high output level to be 10 times the voltage at V_H, and the low output level to be 10 times the voltage at V_L.

High Speed, Full-Wave Rectifier

The clamping inputs are additional inputs to the input stage of the op amp. As such they have an input bandwidth comparable to the amplifier inputs and lend themselves to some unique functions when they are driven dynamically.

Figure 12 is a schematic for a full-wave rectifier, sometimes called an absolute value generator. It works well up to 20 MHz and can operate at significantly higher frequencies with some degradation in performance. The distortion performance is significantly better than diode based full-wave rectifiers, especially at high frequencies.

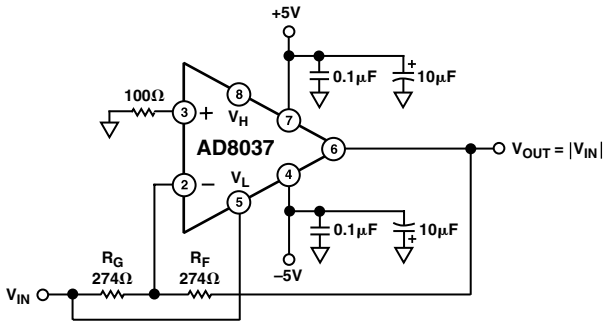


Figure 12. Full-Wave Rectifier

The circuit is configured as an inverting amplifier with a gain of one. The input drives the inverting amplifier and also directly drives V_L, the lower level clamping input. The high level clamping input, V_H, is left floating and plays no role in this circuit.

When the input is negative, the amplifier acts as a regular unity-gain inverting amplifier and outputs a positive signal at the same amplitude as the input with opposite polarity. V_L is driven negative by the input, so it performs no clamping action, because the positive output signal is always higher than the negative level driving V_L.

When the input is positive, the output result is the sum of two separate effects. First, the inverting amplifier multiplies the input by –1 because of its unity-gain inverting configuration. This effectively produces an offset as explained above, but with a dynamic level that is equal to –1 times the input.

Second, although the positive input is grounded (through 100 Ω), the output is clamped at two times the voltage applied to V_L (a positive, dynamic voltage in this case). The factor of two is because the noise gain of the amplifier is two.

The sum of these two actions results in an output that is equal to unity times the input signal for positive input signals, see Figure 13. For a input/output scope photo with an input signal of 20 MHz and amplitude ±1 V, see Figure 14.

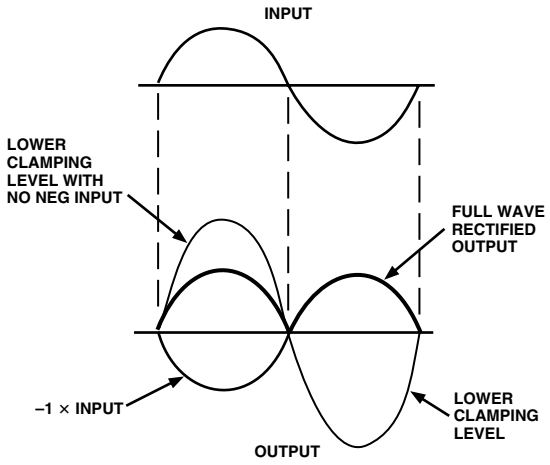


Figure 13.

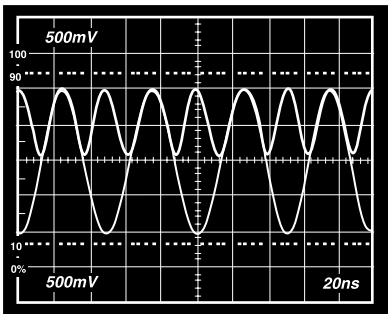


Figure 14. Full-Wave Rectifier Scope

Thus for either positive or negative input signals, the output is unity times the absolute value of the input signal. The circuit can be easily configured to produce the negative absolute value of the input by applying the input to V_H instead of V_L.

The circuit can get to within about 40 mV of ground during the time when the input crosses zero. This voltage is fixed over a wide frequency range and is a result of the switching between the conventional op amp input and the clamp input. But because there are no diodes to rapidly switch from forward to reverse bias, the performance far exceeds that of diode based full wave rectifiers.

The 40 mV offset mentioned can be removed by adding an offset to the circuit. A 27.4 kΩ input resistor to the inverting input will have a gain of 0.01, while changing the gain of the circuit by only 1%. A plus or minus 4 V dc level (depending on the polarity of the rectifier) into this resistor will compensate for the offset.

Full wave rectifiers are useful in many applications including AM signal detection, high frequency ac voltmeters and various arithmetic operations.

Amplitude Modulator

In addition to being able to be configured as an amplitude demodulator (AM detector), the AD8037 can also be configured as an amplitude modulator as shown in Figure 15.

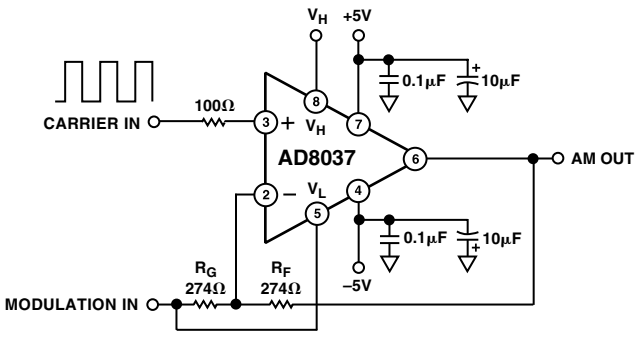


Figure 15. Amplitude Modulator

The positive input of the AD8037 is driven with a square wave of sufficient amplitude to produce clamping action at both the high and low levels. This is the higher frequency carrier signal.

The modulation signal is applied to both the input of a unity gain inverting amplifier and to V_L, the lower clamping input. V_H is biased at 0.5 V dc.

To understand the circuit operation, it is helpful to first consider a simpler circuit. If both V_L and V_H were dc biased at –0.5 V and the carrier and modulation inputs driven as above, the output would be a 2 V p-p square wave at the carrier frequency riding on a waveform at the modulating frequency. The inverting input (modulation signal) is creating a varying offset to the 2 V p-p square wave at the output. Both the high and low levels clamp at twice the input levels on the clamps because the noise gain of the circuit is two.

When V_L is driven by the modulation signal instead of being held at a dc level, a more complicated situation results. The resulting waveform is composed of an upper envelope and a lower envelope with the carrier square wave in between. The upper and lower envelope waveforms are 180° out of phase as in a typical AM waveform.

The upper envelope is produced by the upper clamp level being offset by the waveform applied to the inverting input. This offset is the opposite polarity of the input waveform because of the inverting configuration.

The lower envelope is produced by the sum of two effects. First, it is offset by the waveform applied to the inverting input as in the case of the simplified circuit above. The polarity of this offset is in the same direction as the upper envelope. Second, the output is driven in the opposite direction of the offset at twice the offset voltage by the modulation signal being applied to V_L. This results from the noise gain being equal to two, and since there is no inversion in this connection, it is opposite polarity from the offset.

The result at the output for the lower envelope is the sum of these two effects, which produces the lower envelope of an amplitude modulated waveform. See Figure 16.

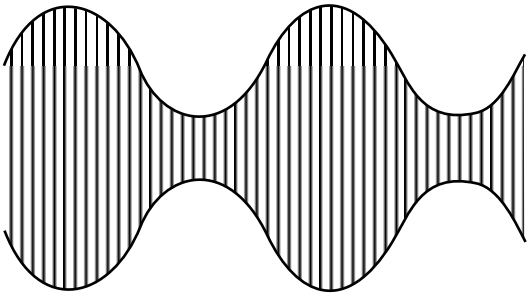


Figure 16. AM Waveform

The depth of modulation can be modified in this circuit by changing the amplitude of the modulation signal. This changes the amplitude of the upper and lower envelope waveforms.

The modulation depth can also be changed by changing the dc bias applied to V_H. In this case the amplitudes of the upper and lower envelope waveforms stay constant, but the spacing between them changes. This alters the ratio of the envelope amplitude to the amplitude of the overall waveform.

Layout Considerations

The specified high speed performance of the AD8036 and AD8037 requires careful attention to board layout and component selection. Proper RF design techniques and low pass parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Chip capacitors should be used for supply and input clamp bypassing (see Figure 17). One end should be connected to the ground plane and the other within 1/8 inch of each power and clamp pin. An additional large (0.47 µF–10 µF) tantalum electrolytic capacitor should be connected in parallel, though not necessarily so close, to supply current for fast, large signal changes at the output.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

Evaluation Board

An evaluation board for both the AD8036 and AD8037 is available that has been carefully laid out and tested to demonstrate that the specified high speed performance of the device can be realized. For ordering information, please refer to the Ordering Guide.

The layout of the evaluation board can be used as shown or serve as a guide for a board layout.

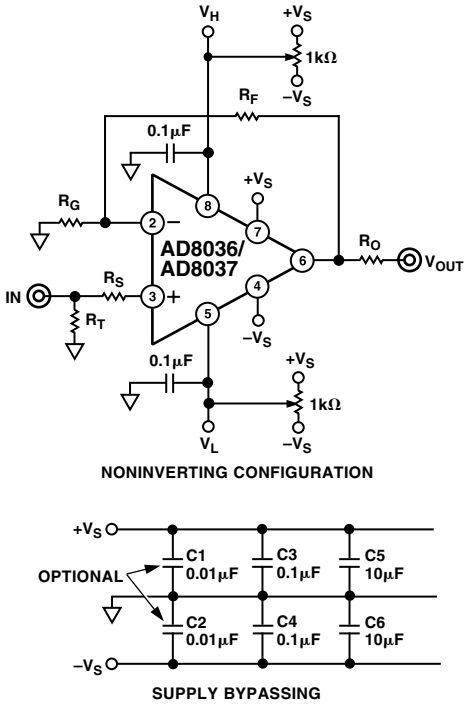


Figure 17. Noninverting Configurations for Evaluation Boards

Table I.

	AD8036A Gain				AD8037A Gain		
Component	**+1**	**+2**	**+10**	**+100**	**+2**	**+10**	**+100**
R_F	140 Ω	274 Ω	2 kΩ	2 kΩ	274 Ω	2 kΩ	2 kΩ
R_G		274 Ω	221 Ω	20.5 Ω	274 Ω	221 Ω	20.5 Ω
R_O (Nominal)	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω
R_S	130 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω
R_T (Nominal)	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω	49.9 Ω
Small Signal BW (MHz)	240	90	10	1.3	275	21	3

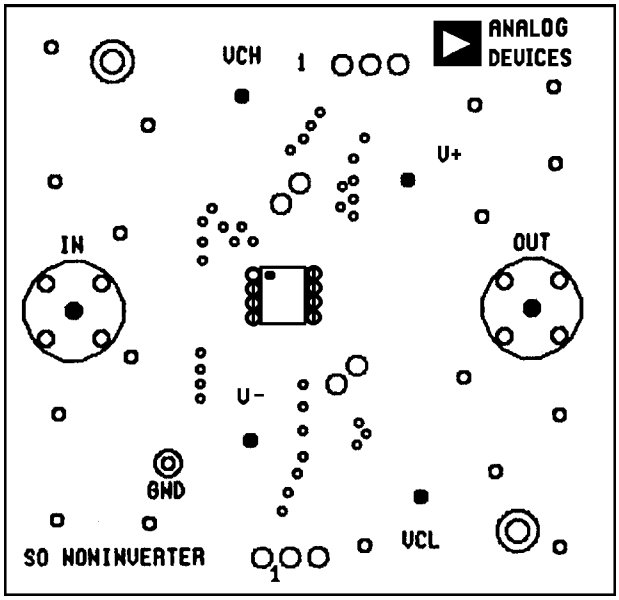


Figure 18. Evaluation Board Silkscreen (Top)

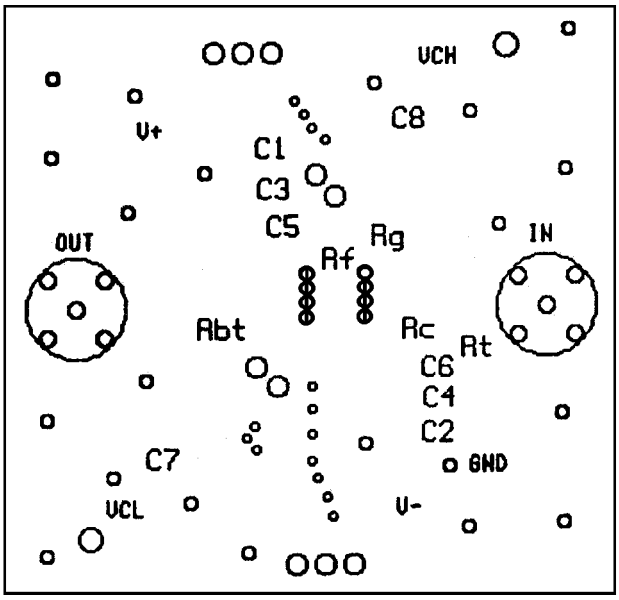


Figure 19. Evaluation Board Silkscreen (Bottom)

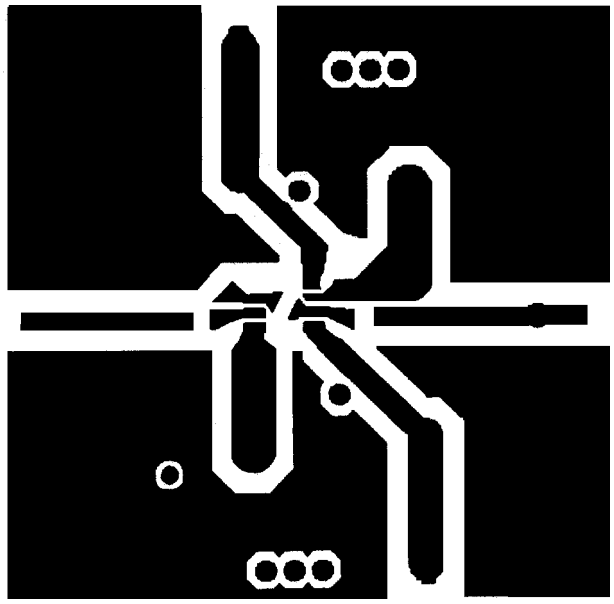


Figure 20. Board Layout (Solder Side)

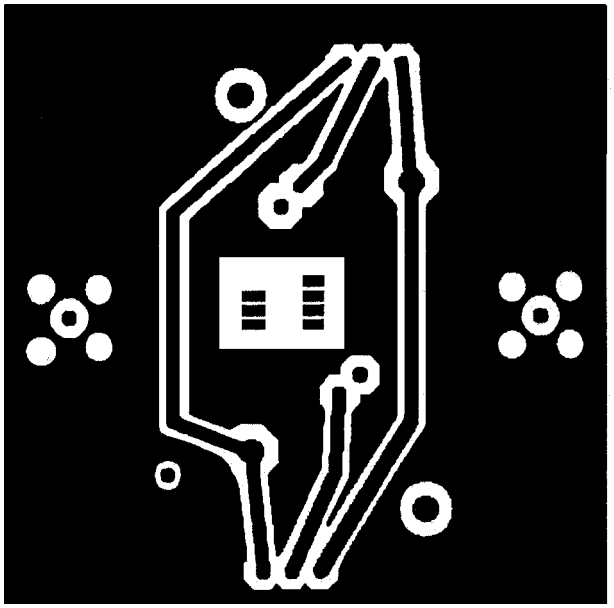
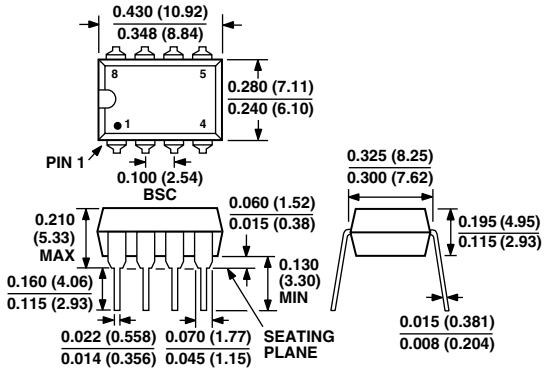


Figure 21. Board Layout (Component Side)

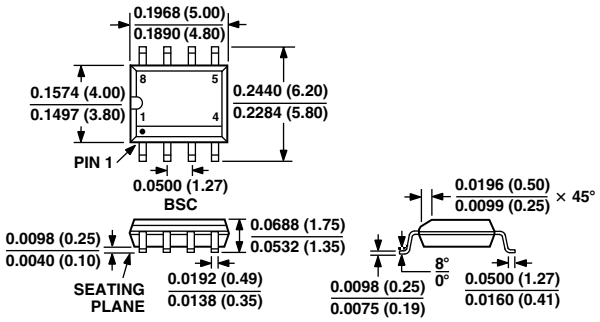
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

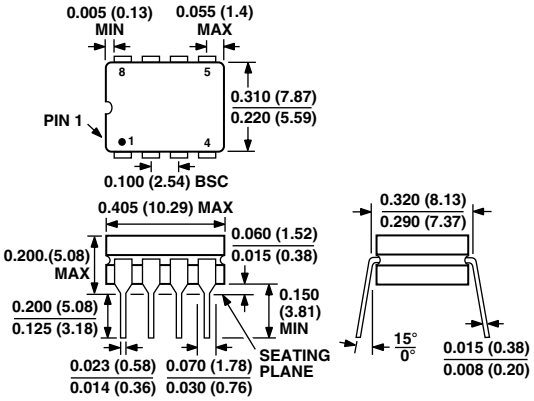
8-Lead Plastic DIP
(N Package)



8-Lead Plastic SOIC
(SO Package)



8-Lead Cerdip
(Q Package)



C01057–0–12/00 (rev. B)

PRINTED IN U.S.A.