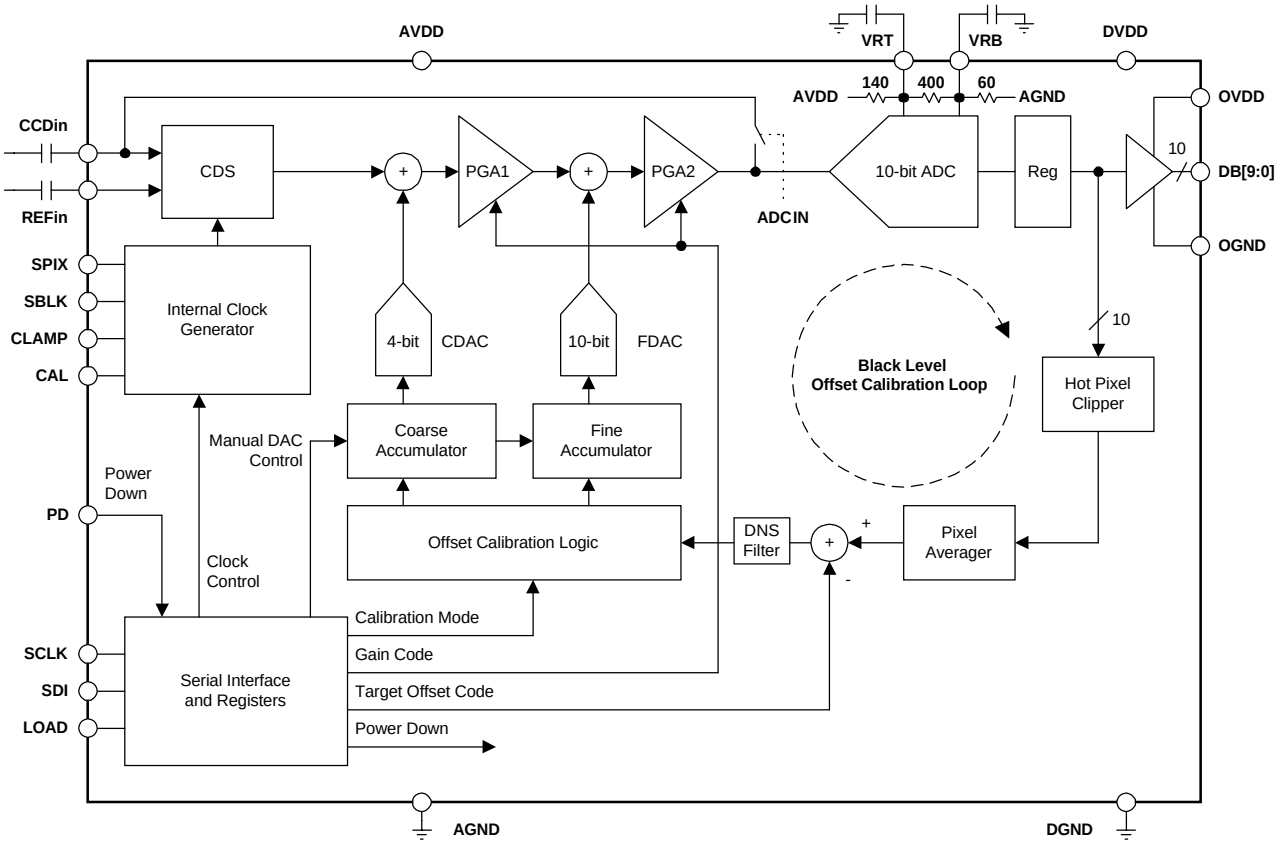
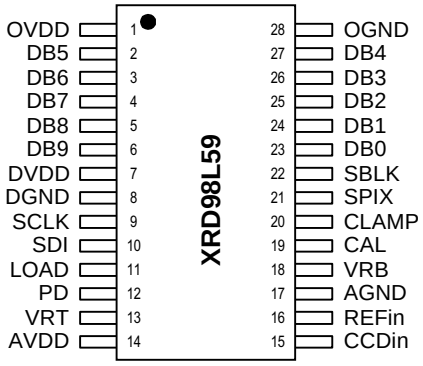


Figure 1. XRD98L59 Block Diagram

PIN CONFIGURATION



28-Lead TSSOP

PIN DESCRIPTION

Pin #	Symbol	Description
1	OV_{DD}	Digital Output Power Supply ($\leq AV_{DD}$)
2	DB5	ADC Output
3	DB6	ADC Output
4	DB7	ADC Output
5	DB8	ADC Output
6	DB9	ADC Output, MSB
7	DV_{DD}	Digital Power Supply (Must = AV_{DD})
8	DGND	Digital Ground. Connect to AGND
9	SCLK	Shift Clock. Latches SDI data on Serial Port
10	SDI	Serial Data Input. Serial Port
11	LOAD	Data Load. Serial Port
12	PD	Power Down, Active High
13	VRT	Top ADC Reference. Sets full scale of ADC
14	AV_{DD}	Analog V_{DD}
15	CCD_{IN}	CDS inverting input. Connect through capacitor to CCD signal
16	REF_{IN}	Reference input (CDS non inverting input). Connect through capacitor to CCD Ground
17	AGND	Analog Ground
18	VRB	Bottom ADC Reference. Sets zero for ADC.
19	CAL	Optical Black (OB) Clamp
20	CLAMP	CDS DC Restore Clamp
21	SPIX	Sample Video Pixel (CDS Clock)
22	SBLK	Sample Black Reference (CDS Clock)
23	DB0	ADC Output, LSB
24	DB1	ADC Output
25	DB2	ADC Output
26	DB3	ADC Output
27	DB4	ADC Output
28	OGND	Digital Output GND. Connect to AGND

DC ELECTRICAL CHARACTERISTICS – XRD98L59
Unless otherwise specified: $OV_{DD} = DV_{DD} = AV_{DD} = 3.0V$, Pixel Rate = 20MSPS, $T_A = 25°C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CDS Performance						
$CDSV_{IN}$	Input Range			800	mV_{PP}	Pixel (V_{Black} - V_{Video}), (See Figure 2)
V_{DARK}	Maximum Dark Voltage Offset		150		mV	At any gain. (See Figure 2)
r_{ON}	CLAMP On Resistance		120		Ω	
PGA Parameters						
AV_{MIN}	Minimum Gain	3.5	5	6.5	dB	
AV_{MAX}	Maximum Gain		36		dB	
PGA n	Resolution		8		bits	Transfer function is linear steps in dB (1LSB = 0.125dB)
ADC Parameters (Measured in ADCIN Test Mode), SDI = 0100 0000 0101 b						
ADC n	Resolution	10			bits	
f_s	Max Sample Rate	20			MSPS	
DNL	Differential Non-Linearity	-1	±0.75	1.5	LSB	
EZS	Zero Scale Error		±25		mV	Measured relative to V_{RB}
EFS	Full Scale Error		1.5		% FS	
V_{IN}	DC Input Range	GND		AV_{DD}	V	AV_{IN} of the ADC can swing from AGND to AV_{DD}. Input range is limited by the output swing of the PGA.
ΔV_{REF}	ADC Reference Voltage		2		V	
V_{RB}	Self Bias V_{RB} $\left(V_{RB} = \frac{AV_{DD}}{10}\right)$	0.2	0.3	0.4	V	
V_{RT}	Self Bias V_{RT} $\left(V_{RB} = \frac{AV_{DD}}{1.30}\right)$	2.0	2.3	2.6	V	

DC ELECTRICAL CHARACTERISTICS - XRD98L59 (CONT'D)
Unless otherwise specified: OV_{DD} = DV_{DD} = AV_{DD} = 3.0V, Pixel Rate = 20MSPS, T_A = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
System Specifications						
DNL_S	System DNL	-1	±0.75	1.5	LSB	No missing codes, monotonic
INL_{SMIN}	System INL @ Minimum Gain		2		LSB	INL error is dominated by CDS/PGA linearity
INL_{SMAX}	System INL @ Maximum Gain		2		LSB	INL error is dominated by CDS/PGA linearity
$e_{n\ MAXAV}$	Input Referred Noise @ Max Gain		0.2		mV_{rms}	Gain Code = FFh
$e_{n\ MINAV}$	Input Referred Noise @ Min Gain		0.7		mV_{rms}	Gain Code = 00h
Latency	Pipeline Delay			4	cycles	
Digital Inputs						
V_{IH}	Digital Input High Voltage	2.1			V	
V_{IL}	Digital Input Low Voltage			0.5	V	
I_L	DC Leakage Current		5		µA	V_{IN} = GND or V_{DD}
C_{IN}	Input Capacitance		5		pF	
Digital Outputs						
V_{OH}	Digital Output High Voltage	OV_{DD}-0.5			V	While sourcing 2mA
V_{OL}	Digital Output Low Voltage			0.5	V	While sinking 2mA
I_{OZ}	High–Z Leakage	-10		10	µA	OE = 0 or PD = 1 Output = OGND or ODV_{DD}

DC ELECTRICAL CHARACTERISTICS - XRD98L59 (CONT'D)
Unless otherwise specified: OV_{DD} = DV_{DD} = AV_{DD} = 3.0V, Pixel Rate = 20MSPS, T_A = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Digital I/O Timing						
t_{DL}	Data Valid Delay		28	35	ns	
t_{PW1}	Pulse Width of SPIX	10			ns	
t_{PW2}	Pulse Width of SBLK	10			ns	
t_{PIX}	Pixel Period	50			ns	
t_{BK}	Sample Black (SBLK), Aperture Delay		3.5		ns	SBLK Delay = 000
t_{VD}	Sample Video (SPIX), Aperture Delay		2.7		ns	SPIX Delay = 000
t_{SCLK}	Shift Clock Period		100		ns	
t_{SET}	Shift Register Setup Time	10			ns	
t_{HOLD}	Shift Register Hold Time			0	ns	
t_{L1}	Load Set-up Time	10			ns	
t_{L2}	Load Hold Time	10			ns	
Power Supplies						
AV_{DD}	Analog Supply Voltage	2.7	3.0	3.6	V	
DV_{DD}	Digital Supply Voltage	2.7	3.0	3.6	V	Set DV_{DD} = AV_{DD}
OV_{DD}	Digital Output Supply Voltage	2.7	3.0	3.6	V	$OV_{DD} \leq AV_{DD}$
I_{DD}	Supply Current		40	55	mA	OV_{DD} = AV_{DD} = DV_{DD} =3.0V, Includes Reference Current
I_{DDPD}	Power Down Supply Current		5	25	µA	PD = 1, Clocked

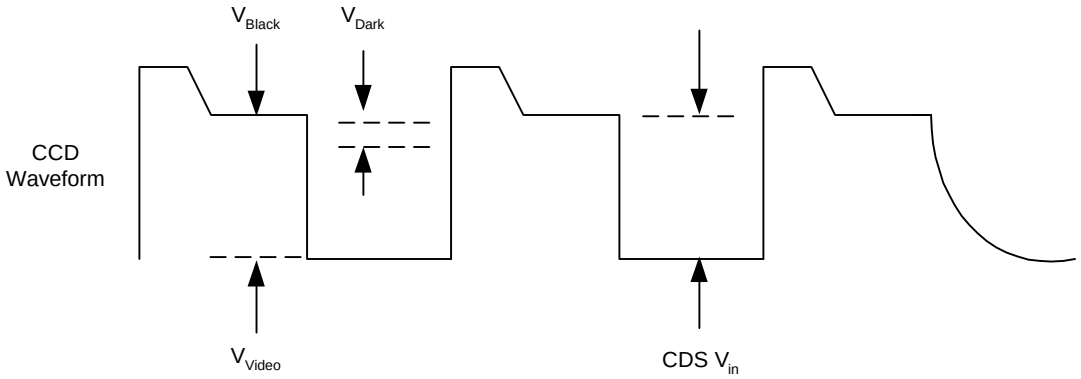


Figure 2. Definition of terms for V_{Out} of the CCD waveform: $CDSV_{IN} = (V_{Black} - V_{Video})$

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +7.0V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND -0.5V
V_{IN} ..... V_{DD} +0.5 to GND -0.5V
All Inputs ..... V_{DD} +0.5 to GND -0.5V
All Outputs ..... V_{DD} +0.5 to GND -0.5V
Storage Temperature ..... -65°C to 150°C

Lead Temperature (Soldering 10 seconds) ..... 300°C
Maximum Junction Temperature ..... 150°C
Package Power Dissipation Ratings (T_A= +70°C)
TSSOP ..... θ_{JA} = 90°C/W
ESD 2000V

Notes:

1 *Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

3 *V_{DD} refers to AV_{DD}, OV_{DD} and DV_{DD}. GND refers to AGND, OGND and DGND.*

SERIAL INTERFACE

The XRD98L59 uses a three wire serial interface (LOAD, SDI & SCLK) to access the programmable features and controls of the chip. The serial interface uses a 12-bit shift register. The first 4 bits shifted in are the address bits, the next 8 bits are the data bits. The address bits select which of the internal registers will receive the 8 data bits. There is no checking or read back of the address bits to ensure a valid register is written to. If the address bits select an undefined register, the data will be discarded.

SERIAL PORT PROCEDURES

1) Set LOAD pin low to enable shift register.
2) Shift in 4 address bits (msb first), followed by 8 data bits (msb first).
3) Set LOAD pin high to transfer data from the shift register to the serial interface register array.

For optimum image quality, do not run the serial port during active video. Serial port clocking can couple into the signal path and degrade accuracy. Also, do not continuously run SCLK.

Reseting the XRD98L59 is recommended after initial power-up. It is generally good practice to reset the XRD98L59 because the serial data may be forced to an unknown state during power supply cycling by the digital ASIC.

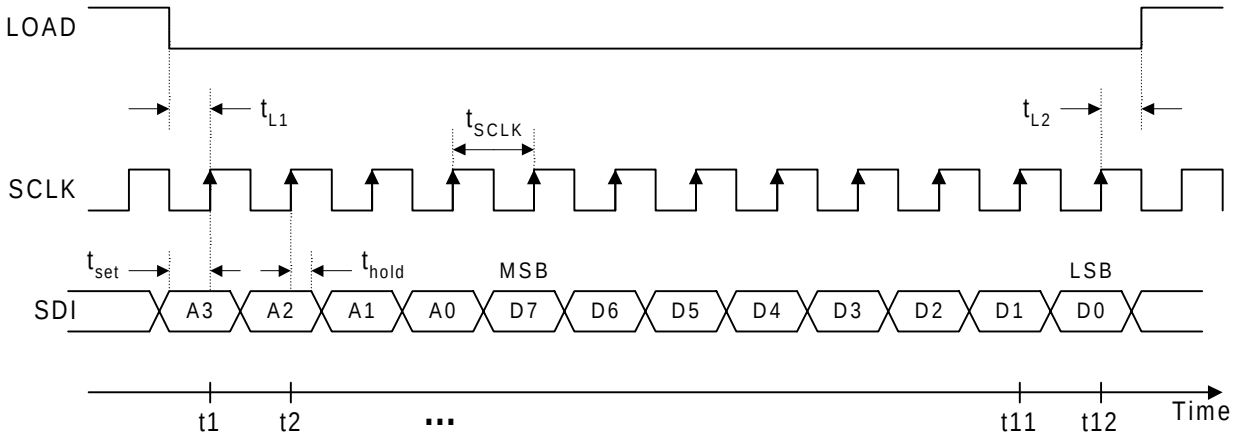


Figure 3. Serial Interface Timing Diagram

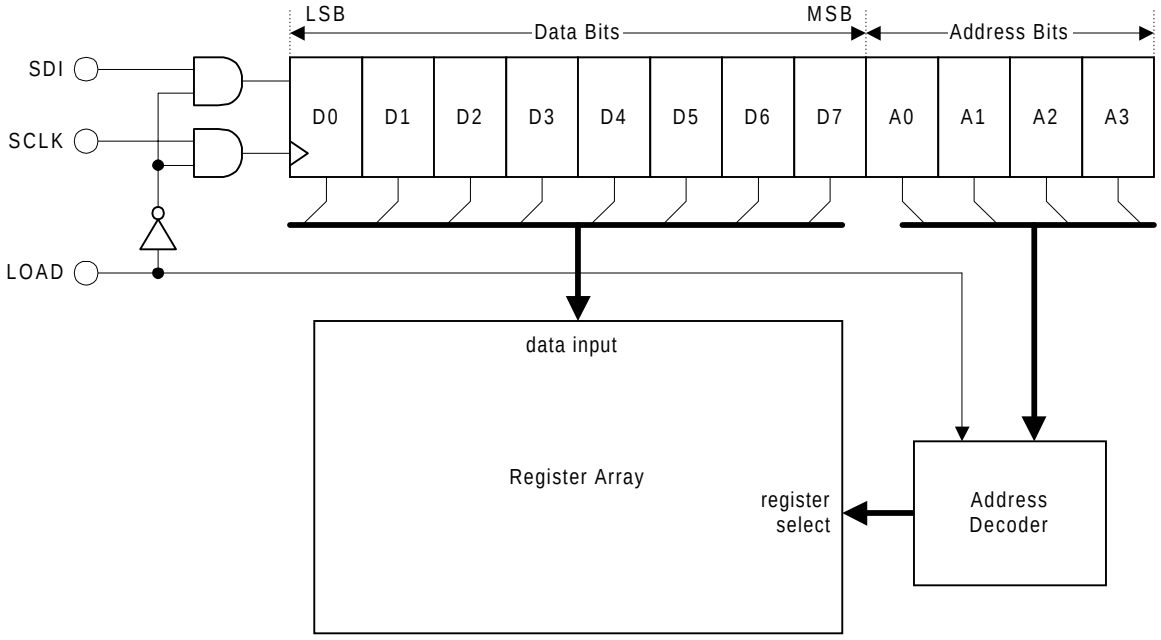


Figure 4. Serial Interface Timing Diagram

	Address bits				Data bits							
Reg. Name	**A3**	**A2**	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Gain	0	0	0	0	Gain [7:0]							
Target Offset	0	0	0	1		Offset [5:0]						
Delay	0	0	1	0	SBLK delay [2:0]			SPIX delay[2:0]			Exar test	
Clock	0	0	1	1		RST rej	Exar test	Clamp opt	SBLK pol	SPIXpol	Clamp pol	CAL pol
Control	0	1	0	0					Delay test	ADCIN	PD	OE
Calibration	0	1	0	1				Cal Hold	Speed Up	DNS 1	DNS 0	Man DAC
FDAC (msb)	0	1	1	0	FDAC [9:2]							
FDAC (lsb)	0	1	1	1							FDAC	[1:0]
CDAC	1	0	0	0					CDAC		[3:0]	
• • •					Not Used							
Reset	1	1	1	1								Reset

Table 1. Serial Interface Register Address Map

D7	D6	D5	D4	D3	D2	D1	D0
Gain[7:0]							
0 0 0 0 0 0 0 0 minimum gain (6 dB) *							
1 1 1 1 1 1 1 1 maximum gain (38 dB)							

Table 2. Gain Register bit assignment (Address 0000)

D7	D6	D5	D4	D3	D2	D1	D0
not used	not used	Offset[5:0]					
		0 0 0 0 0 0 Do not use (00h)					
		0 0 0 0 0 1 Do not use (01h)					
		0 0 0 0 1 0 minimum offset (02h)					
		1 0 0 0 0 0 default offset (20h) *					
		1 1 1 1 1 1 maximum offset (3Fh)					

Table 3. Target Offset Register bit assignment (Address 0001) for PGA

D7	D6	D5	D4	D3	D2	D1	D0
SBLK delay[2:0]			SPIX delay[2:0]			Exar test	
0 0 0 min delay *			0 0 0 min delay *			0 0 default	
1 1 1 max delay			1 1 1 max delay			01, 10, 11 do not use	

Table 4. Delay Register bit assignment (Address 0010)

D7	D6	D5	D4	D3	D2	D1	D0
not used	RST rej	Exar test	CLAMP opt	SBLK pol	SPIX pol	CLAMP pol	CAL pol
	0 switch ON*	0 default	0 Cal only	0 active low*	0 active low*	0 active low*	0 active low*
	1 clocked	1 do not use	1 Clamp+Cal*	1 active high	1 active high	1 active high	1 active high

Table 5. Clock Register bit assignment (Address 0011) for SPIX or SBLK

D7	D6	D5	D4	D3	D2	D1	D0
not used	not used	not used	not used	Delay test	ADCIN	PD	OE
				0 test off *	0 test off *	0 convert *	0 outputs off
				1 test on	1 test on	1 power down	1 outputs on *

Table 6. Control Register bit assignment (Address 0100)

D7	D6	D5	D4	D3	D2	D1	D0
not used	not used	not used	Cal Hold	Speed Up	DNS1	DNS0	Man DAC
			0 cal active*	0 Speed Up off	0 DNS off	0 = Wide*	0 automatic*
			1 hold value	1 Speed Up on*	1 DNS on*	1 = Narrow	1 manual

Table 7. Calibration Register bit assignment (Address 0101)

Note: ** Shading indicates default values after power up or reset. The XRD98L59 does not reset the registers to default value after PD.*

D7	D6	D5	D4	D3	D2	D1	D0
FDAC[9:2]							
1 1 1 1 1 1 1 1 max pos offset							
1 0 0 0 0 0 0 0 zero offset							
0 0 0 0 0 0 0 0 max neg offset *							

Table 8. FDAC (MSB) Register bit assignment (Address 0110)

D7	D6	D5	D4	D3	D2	D1	D0
not used	not used	not used	not used	not used	not used	FDAC[1:0]	
						1 1	max pos offset
						0 0	max neg offset *

Table 9. FDAC (LSB) Register bit assignment (Address 0111)

D7	D6	D5	D4	D3	D2	D1	D0
not used	not used	not used	not used	CDAC[3:0]			
				1 1 1 1	max pos offset	+50 mV	
				1 0 1 1	zero offset		
				0 0 0 0	max neg offset *	-137.5 mV	

Table 10. CDAC Register bit assignment (Address 1000)

D7	D6	D5	D4	D3	D2	D1	D0
not used	not used	not used	not used	not used	not used	not used	Reset
							0 normal *
							1 reset chip

Table 11. Reset Register bit assignment (Address 1111)

Note: ** Shading indicates default values after power up or reset. The XRD98L59 does **not** reset the registers to default value after PD.*

CORRELATED DOUBLE SAMPLE/HOLD (CDS)

The function of the CDS block is to sense the voltage difference between the black level and video level for each pixel. The PGA then amplifies this difference to the desired level for the ADC. The CDS and PGA are fully differential. The PGA output is converted to a single ended signal and fed to the ADC. The CCDin pin (CDS inverting input) should be connected, via a capacitor, to the CCD output signal. The REFin pin (CDS non-inverting input) should be connected, via a capacitor, to the CCD "Common" voltage. This is typically the CCD Reference output or ground.

At the beginning (or end) of every video line, the DC restore switch forces one side of the external capacitors to an internal Vbias1 level (approximately 0.8V). The DC restore switch is controlled by the combination of the CLAMP signal ANDed with the ϕ2 clock. (See Figure 5).

During the black reference phase of each CCD pixel the ϕ1 (Sample Black Reference) switches are turned on, shorting the PGA1 inputs to a second bias level. The Coarse Offset DAC adds an adjustment to the Vbias2 level to cancel offset in the CCD signal. When the ϕ1 switches turn off, the pixel black reference(V_{BLACK}) is sampled on the internal reference sample capacitors, and the PGA is ready to gain up the CCD video signal.

During the video phase of each CCD pixel the difference between the pixel black reference level and video level is transmitted through the internal reference sample capacitors and converted to a fully differential signal by the PGA1 amplifier. At this time the ϕ2 (Sample Pixel value) switches turn on, and the internal video sample capacitors track the amplified difference.

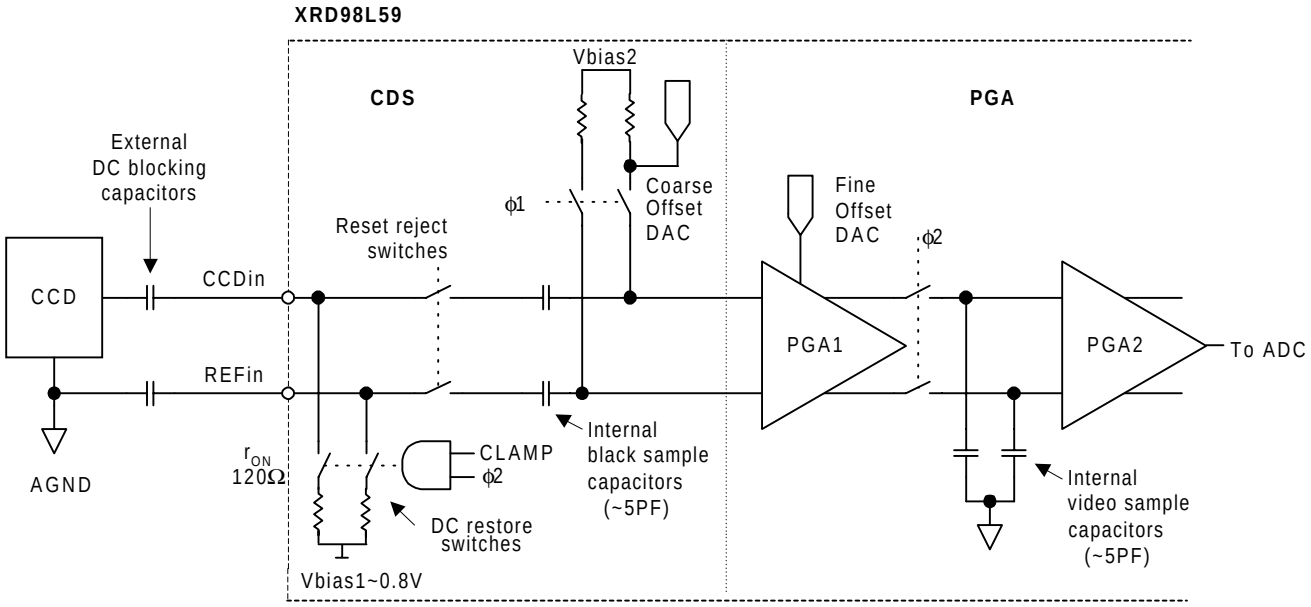


Figure 5. Block Diagram of CDS and PGAs

PIXEL TIMING SBLK & SPIX

The timing required by the XRD98L59 to sample individual pixel data from a CCD output is shown below in Figure 6. The diagram shows the general relationship of timing signals SBLK and SPIX to the CCD waveform. The XRD98L59 was designed to sample any analog CCD waveform. In order to do this the timing signals need to be referenced to the waveform itself, not to the CCD's timing generator.

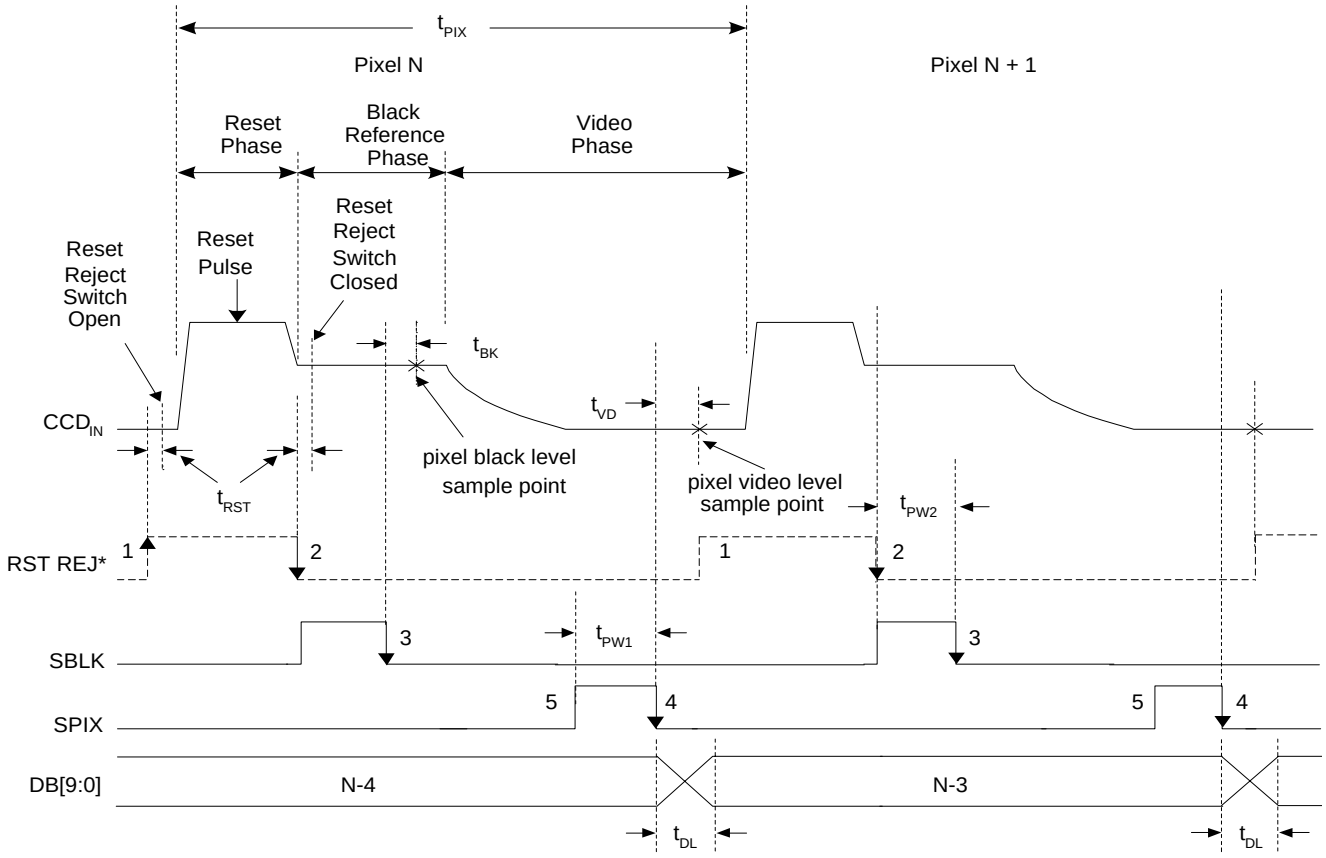


Figure 6. CDS Timing Diagram - Proper Placement of Timing is Critical to Image Quality, SDI=0011 0100 1100
RST REJ is an internally generated signal.

Event		Action
1	↑ RSTREJ	Disconnects CDS Inputs from Reset Noise
2	↓ RSTREJ	Connects CDS Inputs
3	SBLK High	Sample Black Level
4	SPIX High	Sample Video Level
5	SBLK/SPIX Low	Hold Video and Black Level

Table 12. Event Table for CDS Timing (SDI=0011 0100 1100)

RSTREJ reduces CCD reset noise by disconnecting the input of the XRD98L59 from the CCD during the CCD reset pulse. RSTREJ is an internally generated signal. RSTREJ disconnects the input after the SPIX and before the SBLK sampling events to reject CCD reset noise. The RSTREJ switch is always closed (the input is always connected) if D6=0 in the clock register (address 0011) of the serial port.

For the timing example shown in Figure 6, SBLK high samples the pixel black level. The actual hold point of the pixel black level occurs after a delay of t_{BK}. t_{BK} is the aperture delay of the SBLK timing signal.

The polarities of the SBLK and SPIX signals are independently programmable via the serial port.

For the timing example shown in Figure 6, SPIX high samples the pixel video level. The actual hold point of the pixel video level occurs after a delay of t_{VD}. t_{VD} is the aperture delay of the SPIX timing signal. The polarity of the SPIX signal is serial port programmable.

The function of the CDS block, shown in Figure 7, is to sense the voltage difference between the black level and video level for each pixel. The CDS and PGA are fully differential to reject common mode noise. The PGA output is converted to a single ended signal, and then fed to the ADC.

REF_{IN} (CDS non-inverting input) should be connected, via a capacitor, to the CCD "Common" voltage. This is typically CCD ground. CCD_{IN} (CDS inverting input) should be connected, via a capacitor, to the CCD output signal. The external coupling capacitors on CCD_{IN} and REF_{IN} should be of equal values to minimize gain errors (typically 0.01µf +/-10%).

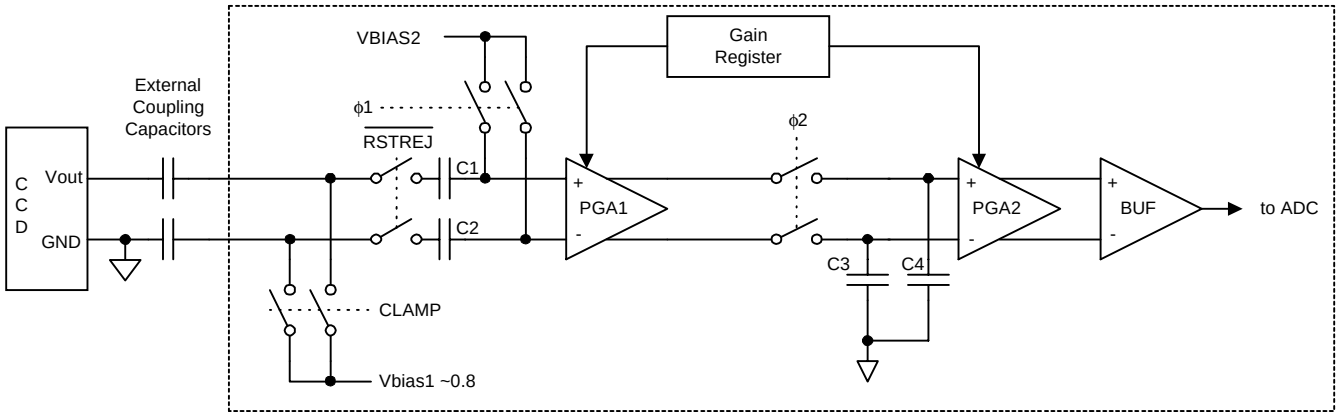


Figure 7. Block Diagram of the CDS, Reset Phase: RSTREJ Switch is Open

During the reset phase of each pixel the RSTREJ switches are turned off, see Figure 7, opening the XRD98L59 CDS input. This is done to limit reset pulse transients seen by the front end of the XRD98L59.

During the black reference phase of each pixel the RSTREJ switches are closed, allowing the difference between the black reference level voltage and VBIAS2 to develop across capacitors C1 and C2 (see Figure 8). ϕ1 is closed when SBLK is active.

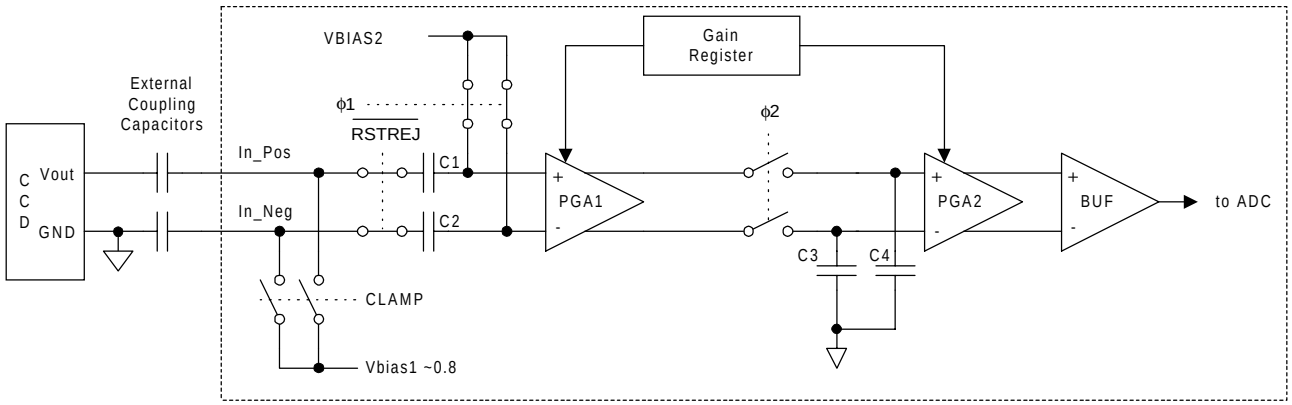


Figure 8. CDS - Black Reference Phase: RSTREJ and ϕ1 Switch Closed

During the video phase of each pixel the ϕ2 switches are closed when SPIX is active. The difference between the pixel black reference level and video level is transmitted through capacitors C1 & C2. Differential amplifier PGA1 amplifies both CDS inputs from CCD_{IN} and REF_{IN}. The inactive phase of SPIX turns off the ϕ2 switches, storing the differential pixel value on capacitors C3 & C4 (see Figure 9).

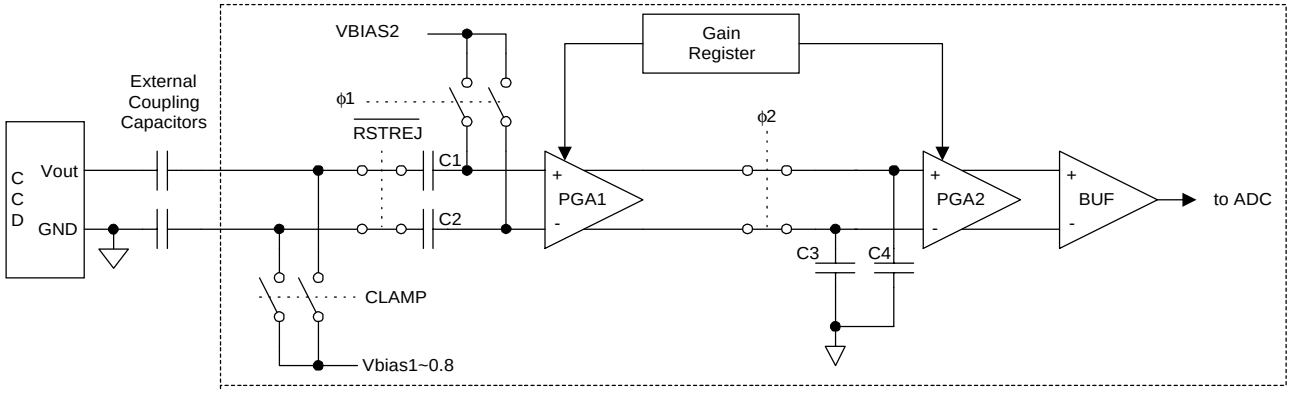


Figure 9. CDS - Video Phase: ϕ1 Switches Open, ϕ2 and RSTREJ Switches Closed

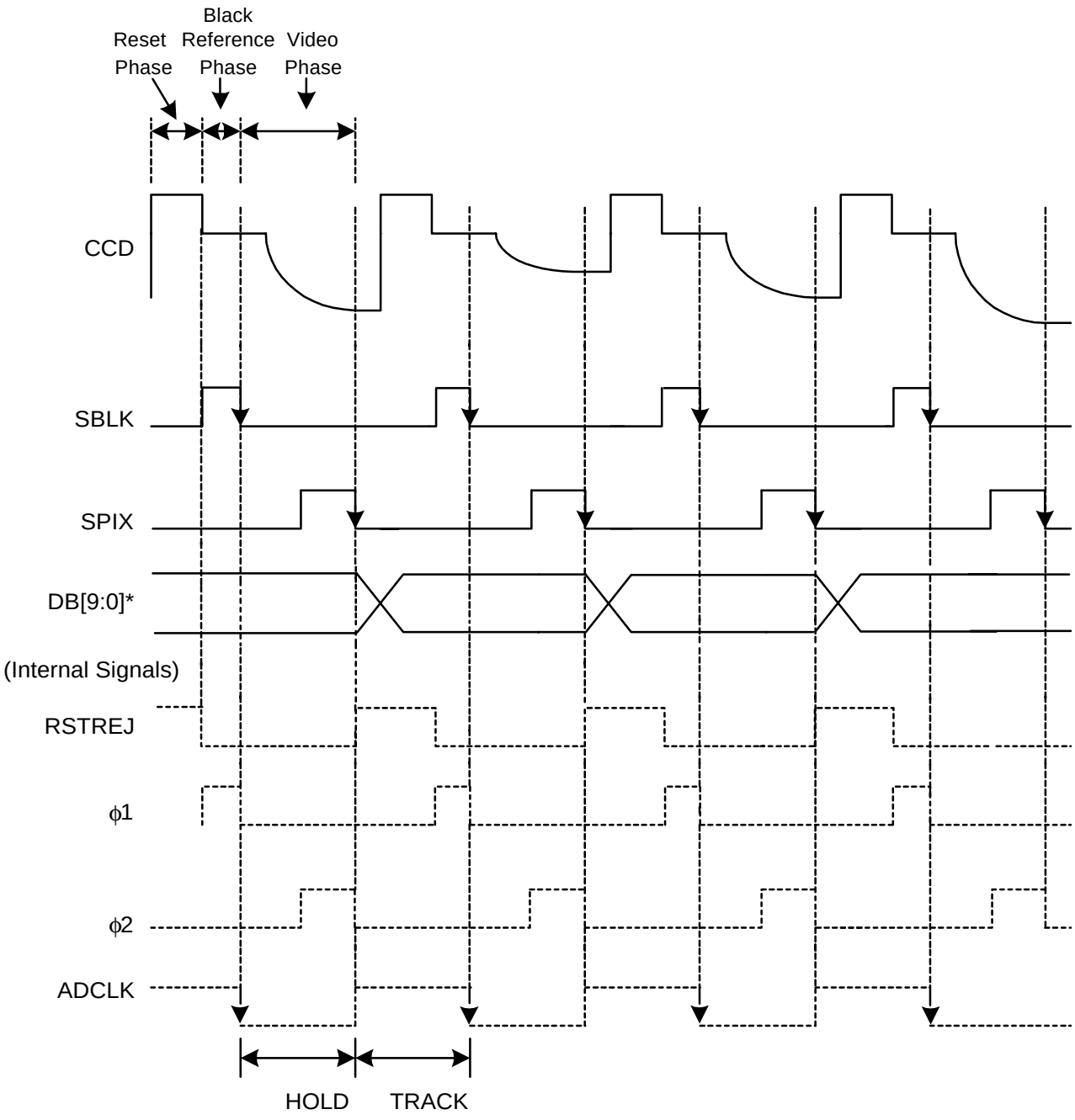


Figure 10. Timing Diagram of the CDS Clocks and Internal Signals (RSTREJ, ϕ1, ϕ2, ADCCLK)
SDI = 0011 0100 1100
*** Digital Output Data is Updated on the Falling Edge of ϕ2.**
This Update Position is Affected by the Aperture Delay of ϕ2.

Note: Aperture Delay is not Shown

SBLK and SPIX Programmable Aperture Delay (SDI Address = 0010)

The positioning of ϕ1 and ϕ2 from Figure 10, are optimized by using a programmable aperture delay function. ϕ1 and ϕ2 are delayed internally by the amount specified in the serial port. SBLK delay (D7:D5) delays the ϕ1 clock and SPIX delay (D4:D2) delays the ϕ2 clock. The delay is 2ns per lsb. The aperture delays t_{BK} and t_{VD} are added to the programmable aperture delay to determine final positioning. The tables below include the t_{BK} and t_{VD} aperture delays.

D7	D6	D5	ϕ1 Aperture Delay
0	0	0	3.5ns (default)
0	0	1	5.5ns
0	1	0	7.5ns
0	1	1	9.5ns
1	0	0	11.5ns
1	0	1	13.5ns
1	1	0	15.5ns
1	1	1	17.5ns

Table 13. Programmable ϕ1 Delays

D4	D3	D2	ϕ2 Aperture Delay
0	0	0	2.7ns (default)
0	0	1	4.7ns
0	1	0	6.7ns
0	1	1	8.7ns
1	0	0	10.7ns
1	0	1	12.7ns
1	1	0	14.7ns
1	1	1	16.7ns

Table 14. Programmable ϕ2 Delays

The aperture delay of ϕ2 also delays the output data bus DB[9:0]. Digital output data is updated on the falling edge of ϕ2 as shown in Figure 10. Data is valid after t_{DL} plus the change in ϕ2 aperture delay. For example, if D[4:2] equals 001b, then data is valid at t_{DL} + 2ns. (t_{DL} is shown in Figure 6).

LINE CALIBRATION MODE

Line calibration mode calibrates during the OB pixel output from the CCD at the end of every line. Figure 11, shows the outline of a typical CCD area array. The active (white) pixels are shown with the OB (shaded) pixels around the edges. The OB pixels used in line calibration are identified below in Figure 11 as the dark shaded OB pixels on the right hand side of the array.

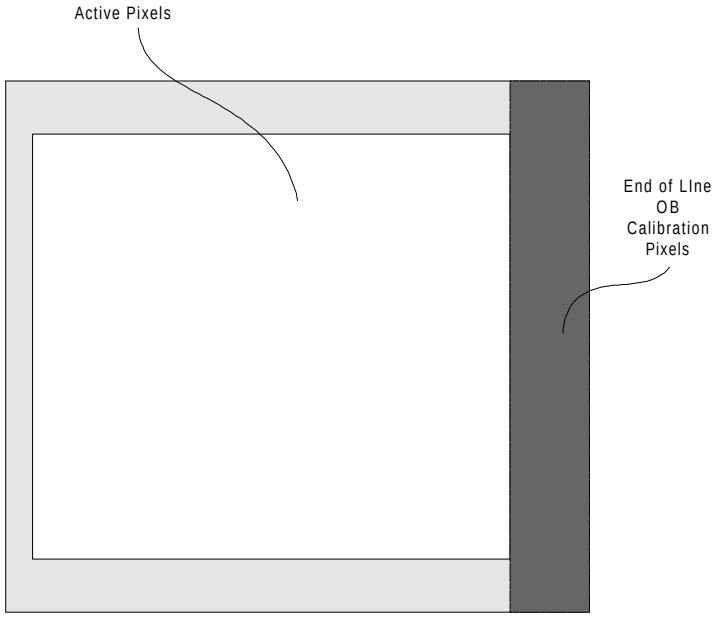


Figure 11. End of Line OB Pixels Used for Line Calibration Mode on a Typical CCD Array

Most timing generators (TG's) have signals that define the start of line and end of line OB pixels on the CCD array. CAL should always be active on start or the end of line that defines the greatest number of OB pixels possible. The more OB pixels that the XRD98L59 can use for its auto-calibration, the faster it can achieve and maintain calibration. CAL and CLAMP must never be active at the same time. CLAMP is used to set the input DC bias voltage. (See Figure 5).

Line Timing: CLAMP and CAL

CLAMP & CAL Line Timing
(SDI address = 0011, D4 = 1)

The timing needed for Line Calibration Mode is shown in Figure 12. The timing signal CAL gates the XRD98L59's auto-calibration logic. CAL is active during the end of line OB pixels.

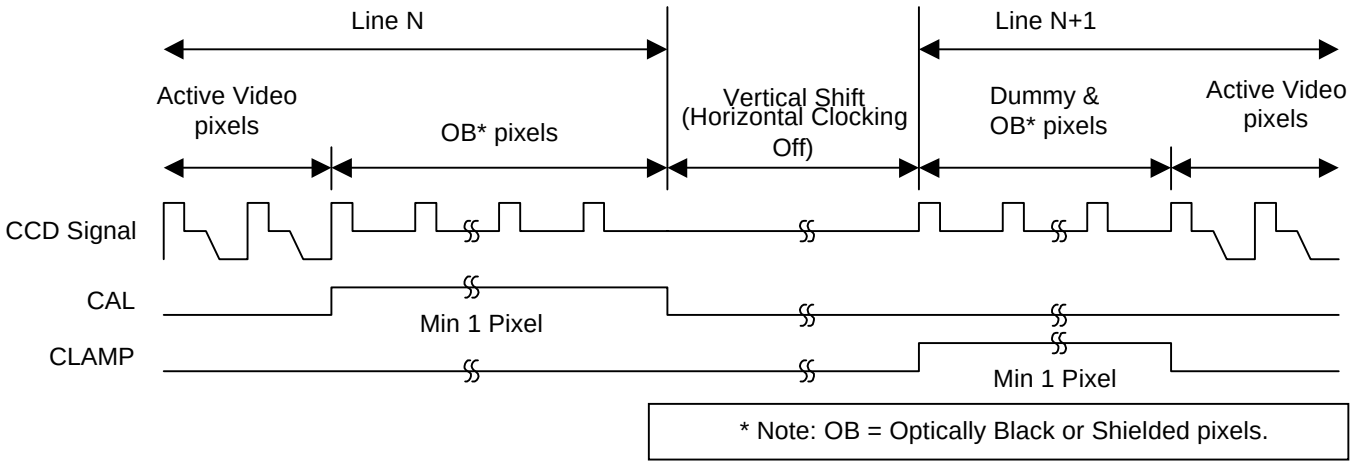


Figure 12. Example of CLAMP & CAL Line Calibration Mode Timing (CAL and CLAMP Polarity are Serial Port Programmable) SDI = 0011 0001 0011

Line Timing: CAL Only

CAL Only Line Timing
(SDI address = 0011, D4 = 0)

The timing needed for "CAL Only" Line Calibration Mode is shown in Figure 13. In "CAL Only" Line Calibration the timing signal CAL has two functions, DC Clamping of the CCDIN and REFin inputs and gating the auto-calibration logic. Using "CAL Only" Line Timing enables the designer to eliminate the requirement of providing a CLAMP Timing signal to the XRD98L59.

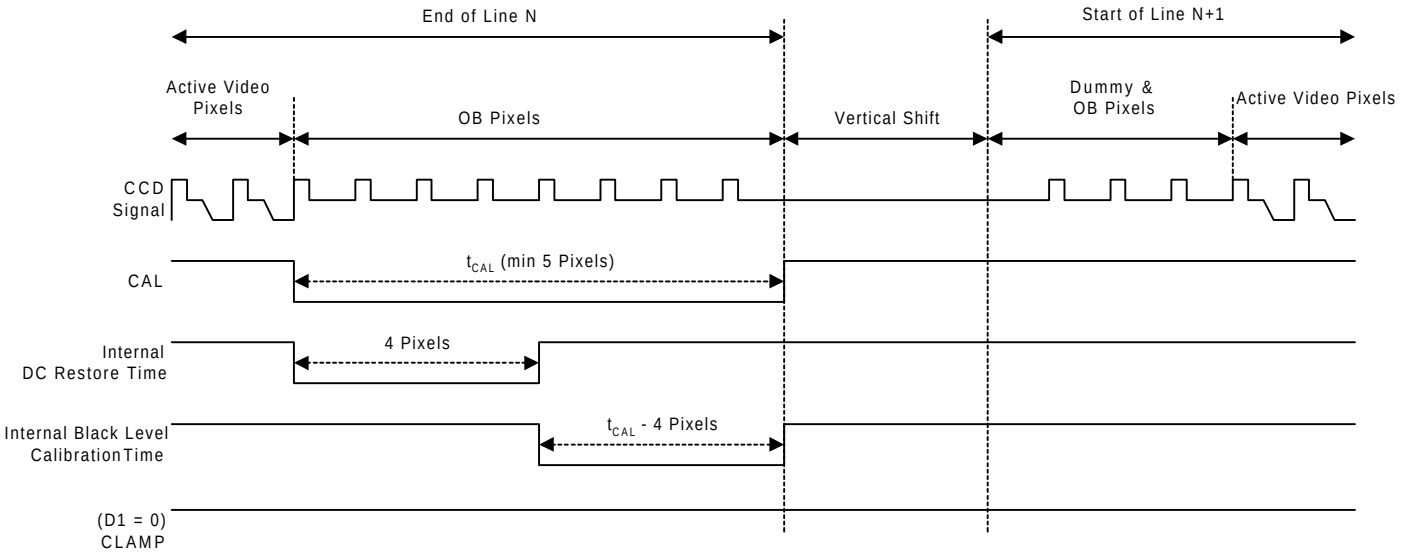


Figure 13. Example of Minimum Timing Requirements for CAL Only Line Calibration Mode (CAL and CLAMP Polarity are Serial Port Programmable) SDI = 0011 0000 0000

Most timing generators (TG's) define the start of line and end of line OB pixels on the CCD array. The CAL timing signal should always be active for the greatest number of OB pixels possible, either during start or end of line. The more OB pixels that the XRD98L59 can use for its auto-calibration, the faster it can achieve and maintain calibration.

While in "CAL ONLY" Line Calibration Timing Mode, CLAMP needs to be held inactive during the output of active video and OB pixels from the CCD. Figure 13 shows the minimum timing requirements for the "CAL ONLY" Line Calibration Timing Mode. The inactive state for CLAMP depends on the CLAMP-Polarity setting (Clock Reg bit D1).

Vertical Shift Reject

The CLAMP input can be used to implement a Vertical Shift Reject function while in "CAL ONLY" Line Calibration Timing Mode. The Vertical Shift Rejection, also called preblanking, can be used to reject and any large transients present in the CCD output during the vertical clocking.

To implement the Vertical Shift Reject (Preblanking) function on the XRD98L59 the CLAMP opt bit must be low (Clock Reg D4=0) and the CLAMP input driven with the preblanking timing signal. The preblanking timing signal, commonly called PBLK, is generated by the system timing generator and defines the vertical shift of the CCD (see Figure 13a). The preblanking pulse opens the Reset Reject Switches internal to the XRD98L59, see Figure 5, thereby rejecting any transients in the CCD output while the vertical shifting is being done.

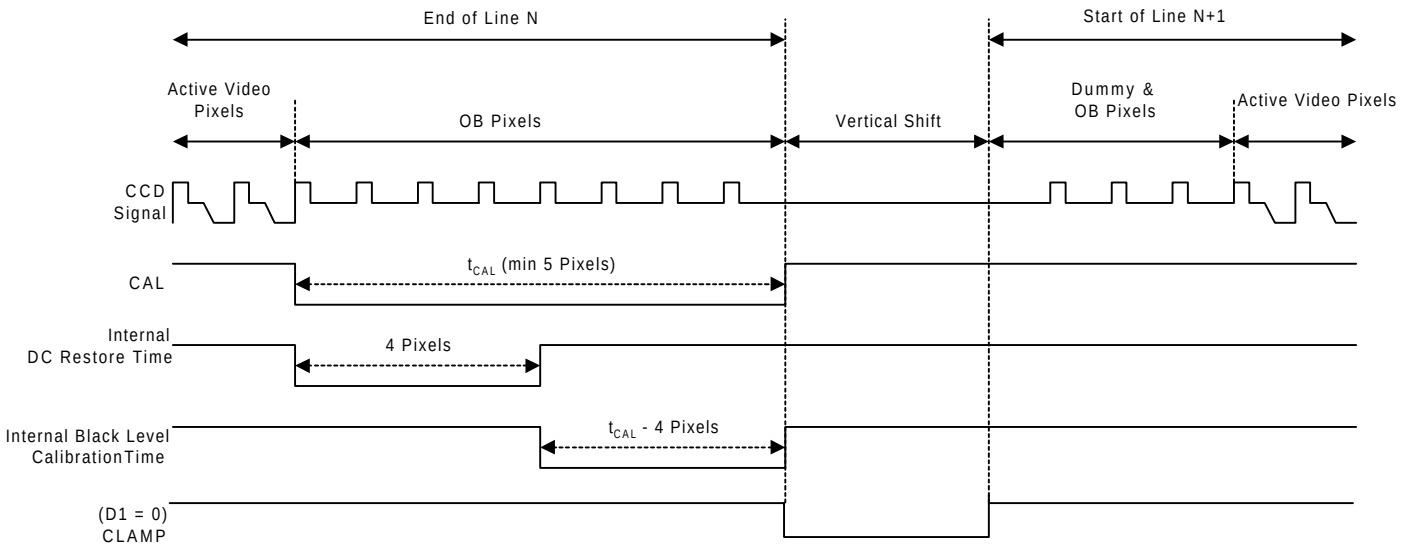


Figure 13a. Example of Vertical Shift Reject Timing using the CLAMP input while in "CAL ONLY" Line Calibration Mode. (CAL and CLAMP Polarity are Serial Port Programmable) SDI = 0011 000 0000

PROGRAMMABLE GAIN AMPLIFIER (PGA)

PGA1 provides gains of 0dB, 8dB & 16dB (1x, 2.5x, and 6.25x). The gain transitions occur at PGA gain codes 64d and 128d (40h & 80h). PGA2 provides gain from 6dB to 22dB (2x to 12.5x) with 0.125dB steps. The combined PGA blocks provide a programmable gain range of 32dB. The minimum gain (code 00h) is 6dB. The maximum gain (code FFh) is 38dB. The following equation can be used to compute PGA gain from the gain code:

$$Gain[dB] = 6 + \left(\frac{Code}{256} \times 32\right)$$

where *Code* is the 8 bit value (0 to 255) programmed in the serial interface Gain register. Due to device mismatch the gain steps at codes 63 - 64 and 127 - 128 may not be monotonic.

ANALOG TO DIGITAL CONVERTER (ADC)

The analog-to-digital converter is based upon a two-step sub-ranging flash converter architecture with a built in track and hold input stage. The ADC conversion is controlled by an internally generated signal, ADCLK (see Figure 10). The ADC tracks the output of the PGA while ADCLK is high and holds when ADCLK is low. This allows maximum time for the PGA output to settle to its final value before being sampled. The conversion is then performed and the parallel output is updated, after a 2.5 cycle pipeline delay, on the edge of ϕ2. The pipeline delay of the entire XRD98L59 is 4 clock cycles.

The ADC reference levels, VRT & VRB, are set by an internal resistor divider between VDD and GND. The divider provides VRB=VDD/10 and VRT=VDD/1.3. To maximize the performance of the XRD98L59, VRT & VRB should have high frequency by-pass capacitors to AGND. The value of these by-pass capacitors will affect the time required for the reference to charge up and settle after power down mode. Using 0.01uF capacitors will give about 40 µs settling time for full accuracy.

The ADC output bus is equipped with a high impedance capability which is controlled by OE bit in the serial interface control register. The outputs are enabled when the OE bit is high, and go into high impedance mode when the OE bit is low.

The ADC input node can be accesed for test purposes using the ADCIN mode (SDI address 0100). Use the following procedure to enable the ADCIN mode:

1) In the Serial interface Clock register, set the Clamp Opt bit low (D4).

2) In the Serial interface Control register, set the ADCIN bit high (D2).

3) Clock SBLK & SPIX to generate internal ADC_CLK signal.

4) Apply ADC input signal to CCDin.

In this test mode the analog signal, Vin, applied to CCDin pin will be converted by the ADC. The ADC output code is related to Vin by the following rules:

1) For Vin < VRB, ADC output code = 0,
2) For Vin > VRT, ADC output code = 1023,
3) For VRB < Vin < VRT, ADC output code = 1024 x (Vin - VRB) / (VRT - VRB)

CONTROL & RESET REGISTERS

ADCIN Bit

This bit activates a switch that connects CCDin directly to the ADC input. In this mode, the PGA output is disabled. See the ADC section for details.

PD Bit (Power Down)

This bit is used to put the chip in the Power Down mode. It has the same effect as the PD pin. When the PD bit is high the chip will go into the power down mode, all conversions stop. When the PD bit is low the chip is in its normal active mode. In the Power Down mode the digital output pins are forced to the high impedance mode and the ADC reference is disconnected. The serial interface pins remain active in the Power Down mode.

OE Bit (Output Enable)

The ADC digital output bus is equipped with a high impedance capability. When the OE bit is high the digital outputs are enabled (active). When the OE bit is low the digital outputs are in the high impedance mode (not active). The OE bit only controls the digital output drivers, all other circuits on the chip will remain active.

RESET Bit

This bit is used to reset all internal registers to default values. This includes all the serial interface registers as well as the registers in the calibration logic. To reset the chip write a “1” to the reset bit. The reset bit will clear itself after an internal delay, so there is no need to write a “0” to the reset bit. The chip also has a Power-On-Reset function (POR) so it will always power up with default values in all registers. It is recommended that the XRD98L59 be reset after power is cycled to avoid loading potentially incorrect serial port data from other ASICs in the system.

BLACK LEVEL OFFSET CALIBRATION

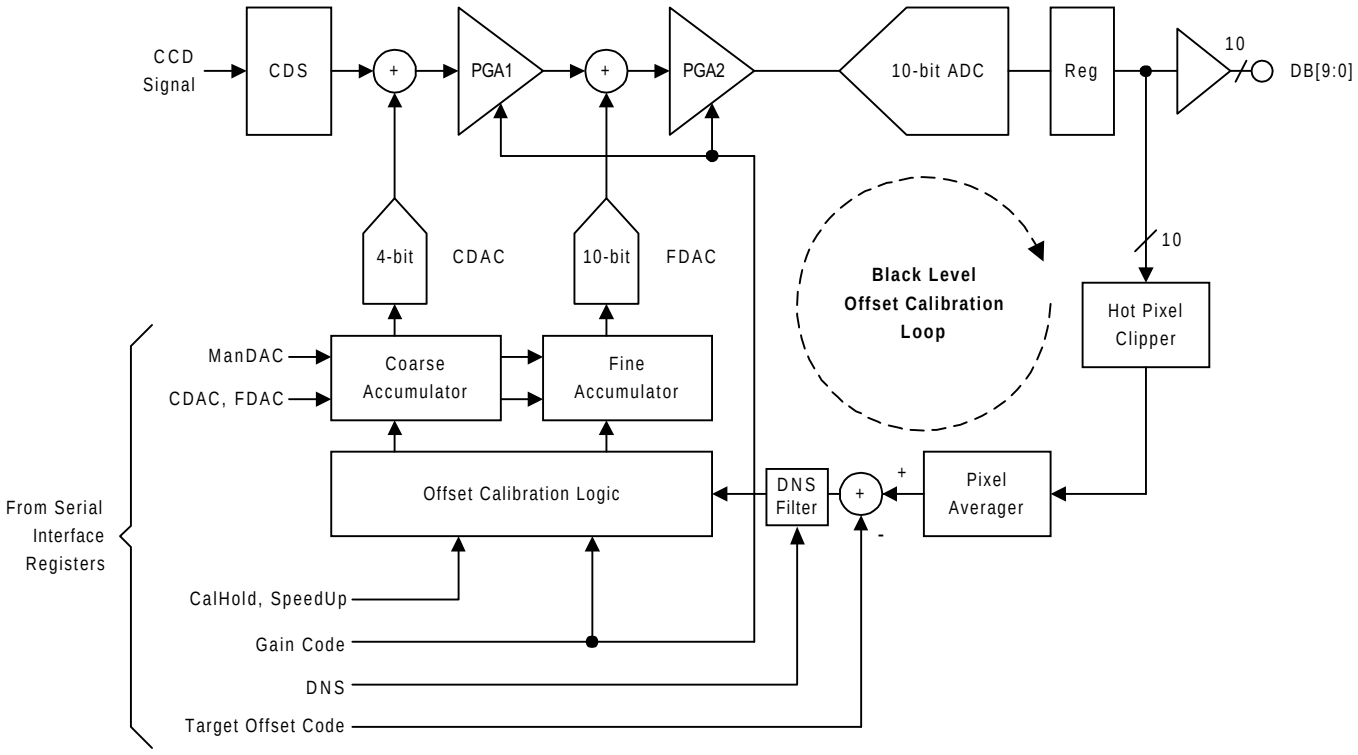


Figure 15. Black Level Offset Calibration Block Diagram

To get the maximum color resolution and dynamic range, the XRD98L59 uses a digitally controlled feedback circuit to correct for offset in the CCD signal as well as offset in the CDS, PGA & ADC signal path. This calibration is done while the CCD outputs Optical Black (OB) pixels. The CAL input signal is used to define when the CCD output contains OB pixels. The calibration logic will take into account the internal pipeline delay.

Hot Pixel Clipper

CCD's occasionally have hot pixels. These are defective pixels which always output a bright level. To ensure the Black Level is not significantly affected by hot pixels in the OB area, the Hot Pixel Clipper limits pixel data from the ADC to a maximum value of 127 (7Fh). The Hot Pixel Clipper is only active when CAL is active. This clipping only affects the data used by the internal calibration logic. Data on the digital output bus DB[9:0] is not clipped.

Pixel Averager

After the clipper, the logic takes the average of the Optical Black pixels defined by CAL. This averaging function filters noise.

Offset Difference Using the Target Offset Register

The Target Offset register (Address 0001) value (6 lsb's) is subtracted from the OB pixel average. If the difference is positive, the offset DACs are decremented to reduce the effective ADC output code. If the difference is negative, the offset DACs are adjusted to increase the effective ADC output code. The amount of adjustment is shown in Figure 16.

Set the Target Offset Register value equal to the desired black level output code. For example: Set Target Offset Register to code 32 and black CCD outputs are nominally output as 32. Default is code 32 decimal.

Coarse & Fine Accumulators

The Coarse and Fine Accumulators are the registers which hold the digital codes for the Coarse and Fine Offset DACs. The Offset DAC adjustments are made by adding or subtracting to the value in the Fine Accumulator. If there is an overflow or underflow in the Fine Accumulator, the Fine Accumulator is reset to it's mid-scale value, and the Coarse Accumulator is incremented or decremented accordingly.

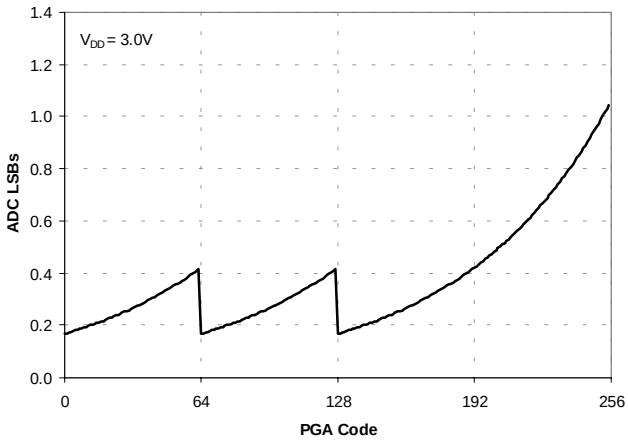


Figure 16. XRD98L59 Offset DAC Step Size in ADC Output LSBs

CALIBRATION OPTIONS

Speed Up Mode

The purpose of this option is to reduce the amount of time required for initial convergence of the calibration feedback system. The feedback system is designed to have a slow response time to avoid introducing image artifacts. The slow response time is achieved by limiting the Fine accumulator changes to ± 1 count at a time. The Speed Up option maintains this slow response while the difference between the averaged ADC data and the Target Offset Code is small. But when the difference is larger than ± 32 lsb's the Fine accumulator takes large steps. The actual step size depends on the Gain code, and is set such that the step will cause no more than a 32 LSB change in the ADC output.

To activate the Speed Up mode write a 1 to the SpeedUp bit in the Calibration register (bit D3 of Serial Interface Register #5). By default the SpeedUp mode is active.

Digital Noise Supression (DNS Filter)

To activate the DNS mode, a "1" is written to DNS1 bit in the Calibration register (bit D2 of Serial Interface Register #5). By default the DNS mode is active.

In DNS mode, the user has the option to select narrow band or wide band Noise Suppression Filters by setting DNS0 bit to a "1" (narrow) or "0" (wide) respectively. Best performance is achieved by setting DNS1 = "1" and DNS0 = "0".

Hold Mode

The purpose of this mode is to prevent any changes in the Fine or Coarse accumulators. The idea is to first run the calibration normaly so the Fine and Coarse accumulators converge on the programmed Target Offset Code. Then, just before acquiring the final image data, activate the Hold mode. This will ensure the black level offset of the CDS/PGA does not change while the final image is being transferred out of the CCD. Once the image has been acquired from the CCD, turn off the Hold mode so the chip can continue to compensate for any changes in offset due to temperature drift or other effects.

To activate the Hold mode write a 1 to the CAL Hold bit in the Calibration register (bit D4 of Serial Interface Register #5). By default the Hold mode is not active.

Manual Mode

The purpose of this mode is to disable the automatic calibration feature. In the Manual mode, the Coarse accumulator is programmed by writing to the CDAC register, the Fine accumulator is programmed by writing to the FDAC register. The Fine accumulator is a 10 bit register, but the Serial interface registers are only 8 bits wide. As shown in the Serial Interface Register Address Map, two serial interface registers are concatenated to provide 10 bits to the Fine accumulator.

To activate the Manual mode write a 1 to the ManDAC bit in the Calibration register (bit D0 of Serial Interface Register #5). By default the Manual mode is not active.

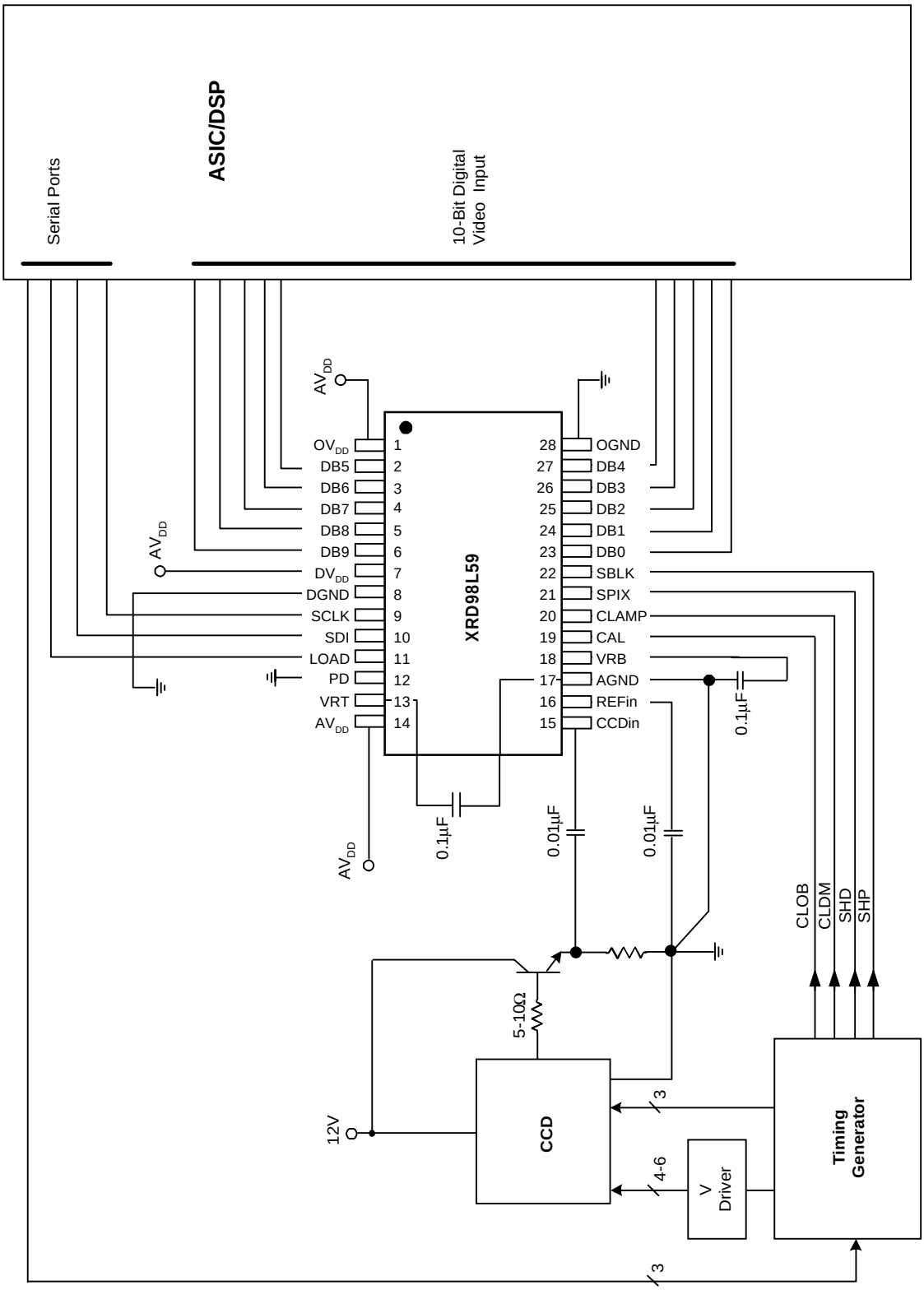


Figure 17. Application Diagram; ASIC with External Timing Generator

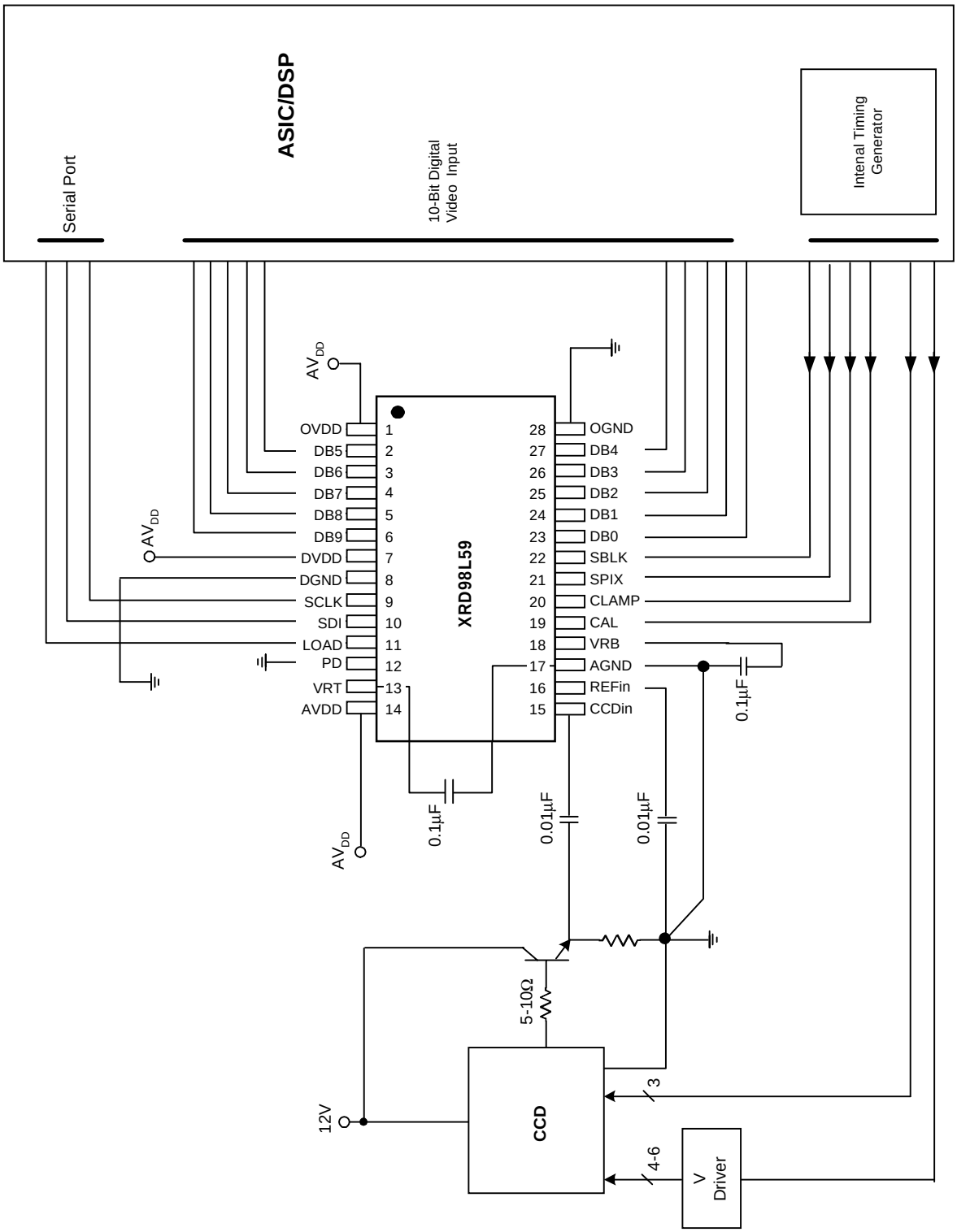


Figure 18. Application Diagram; ASIC with Internal Timing Generator

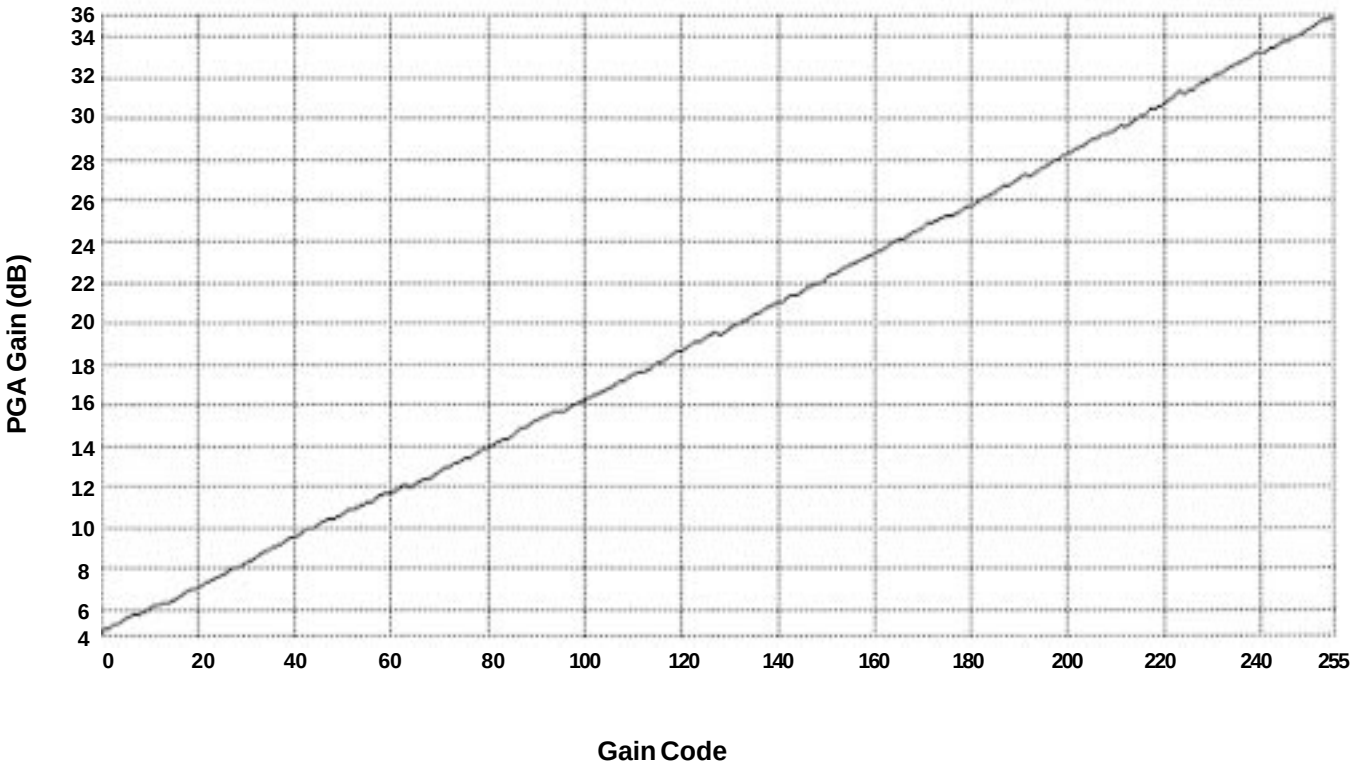


Figure 19. PGA Gain vs. Gain Code

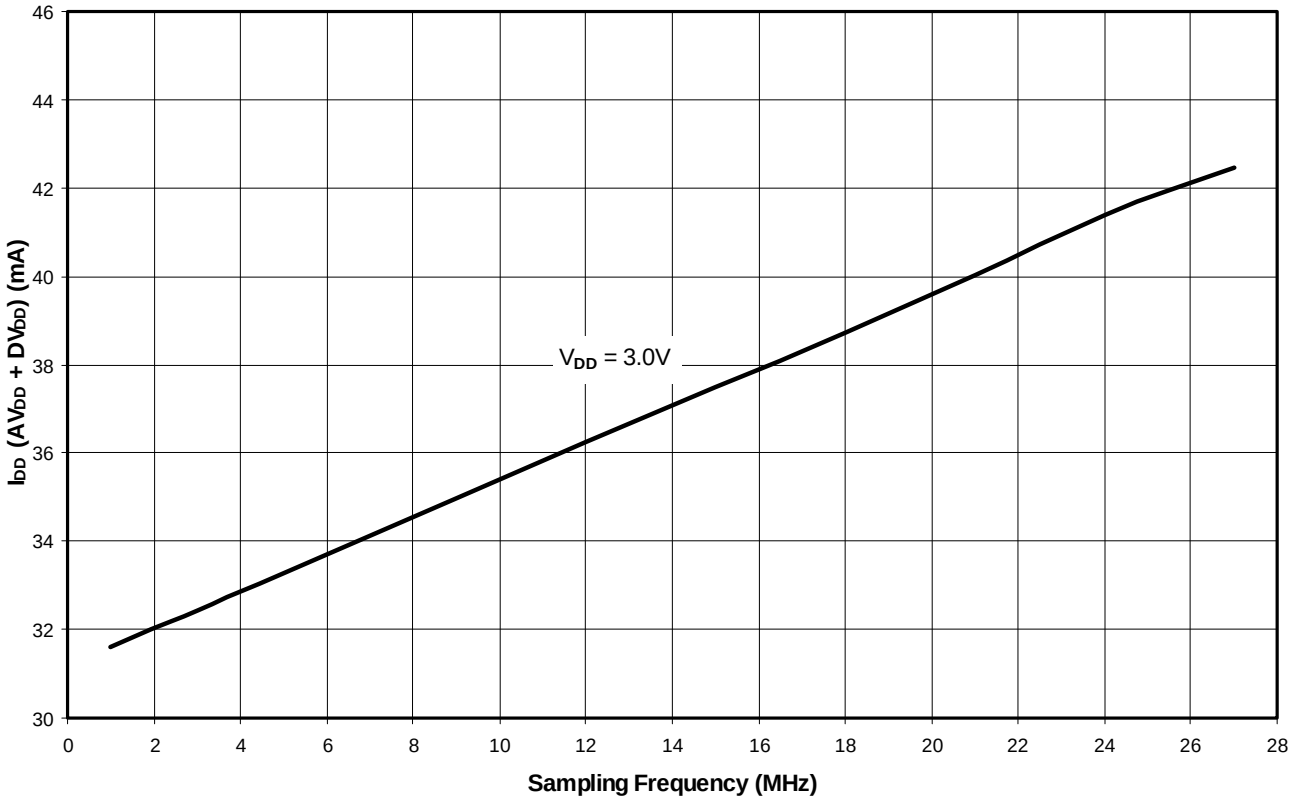


Figure 20. IDD vs Sample Rate

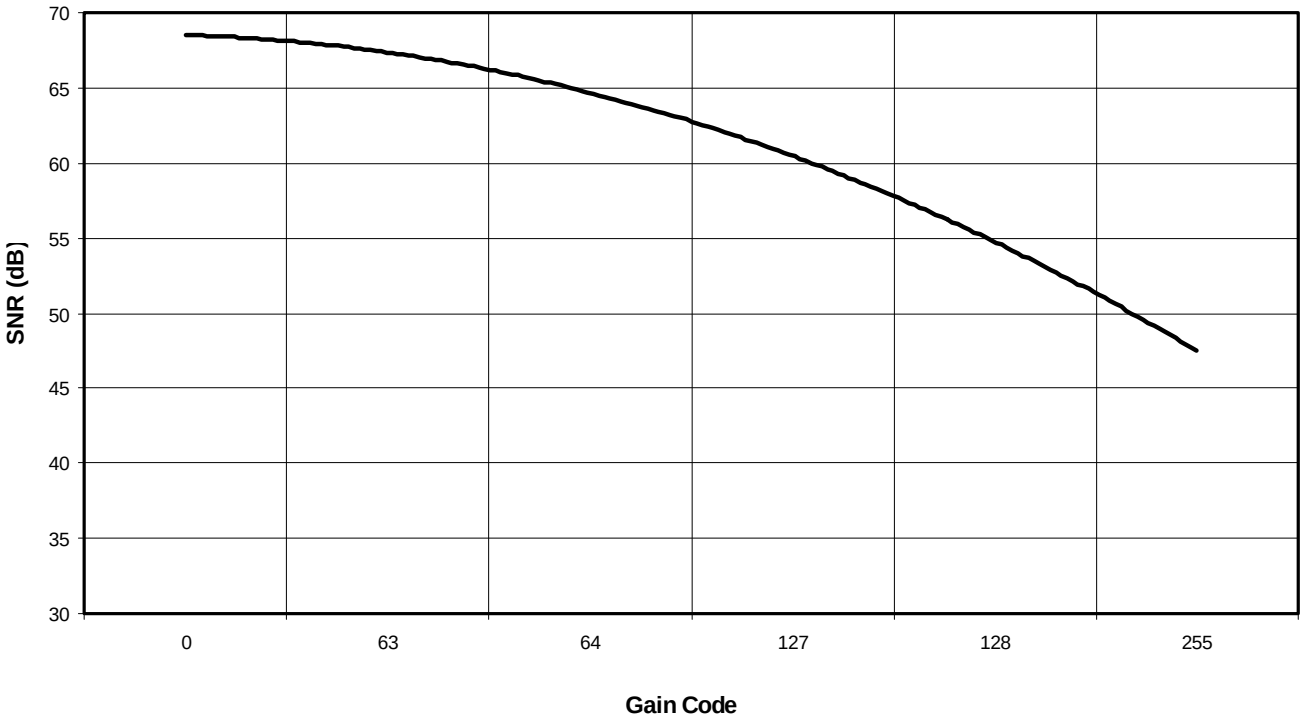


Figure 21. Typical SNR vs Gain at 20MHz Sample Rate
SNR = 20 log (Full scale voltage/rms noise)

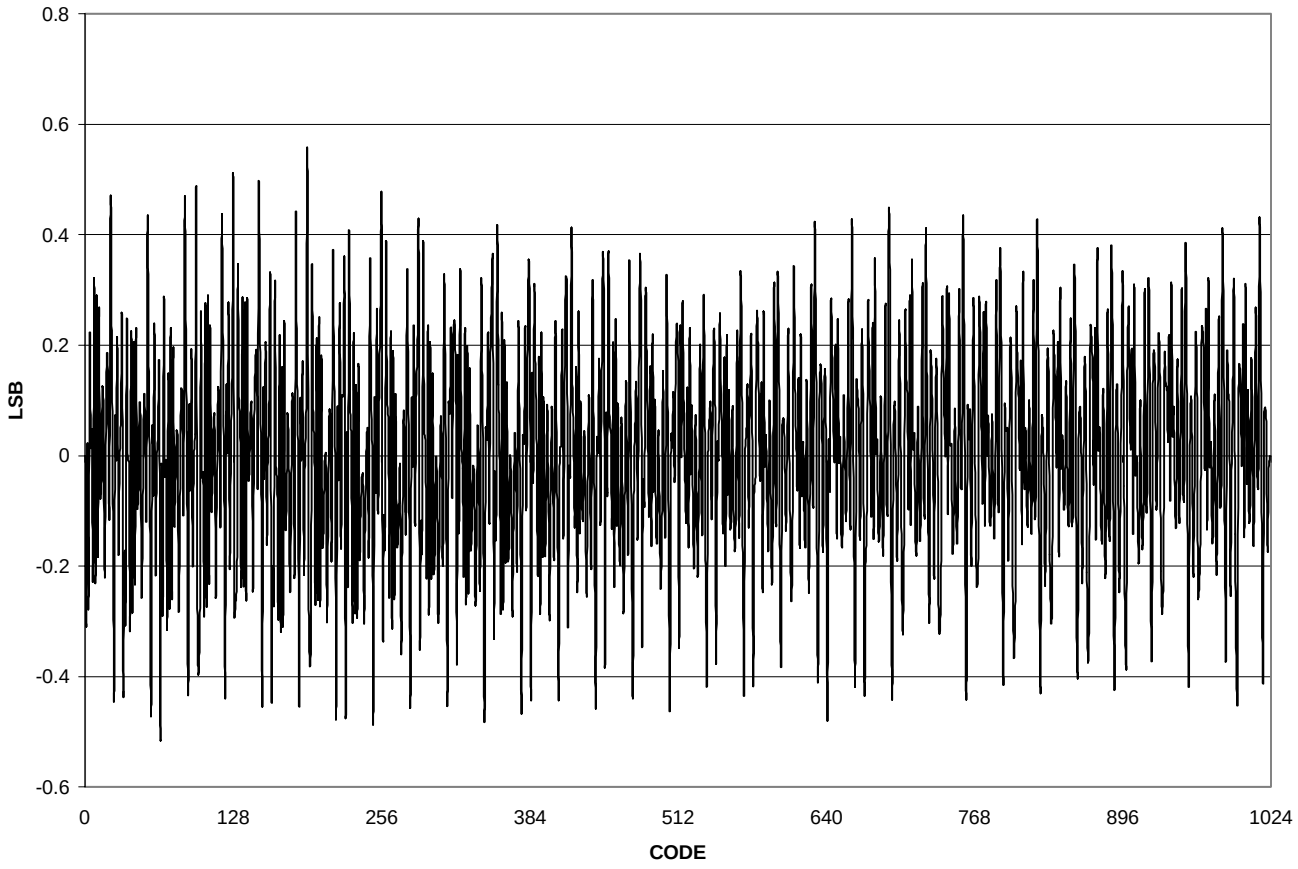


Figure 22. ADC Only DNL

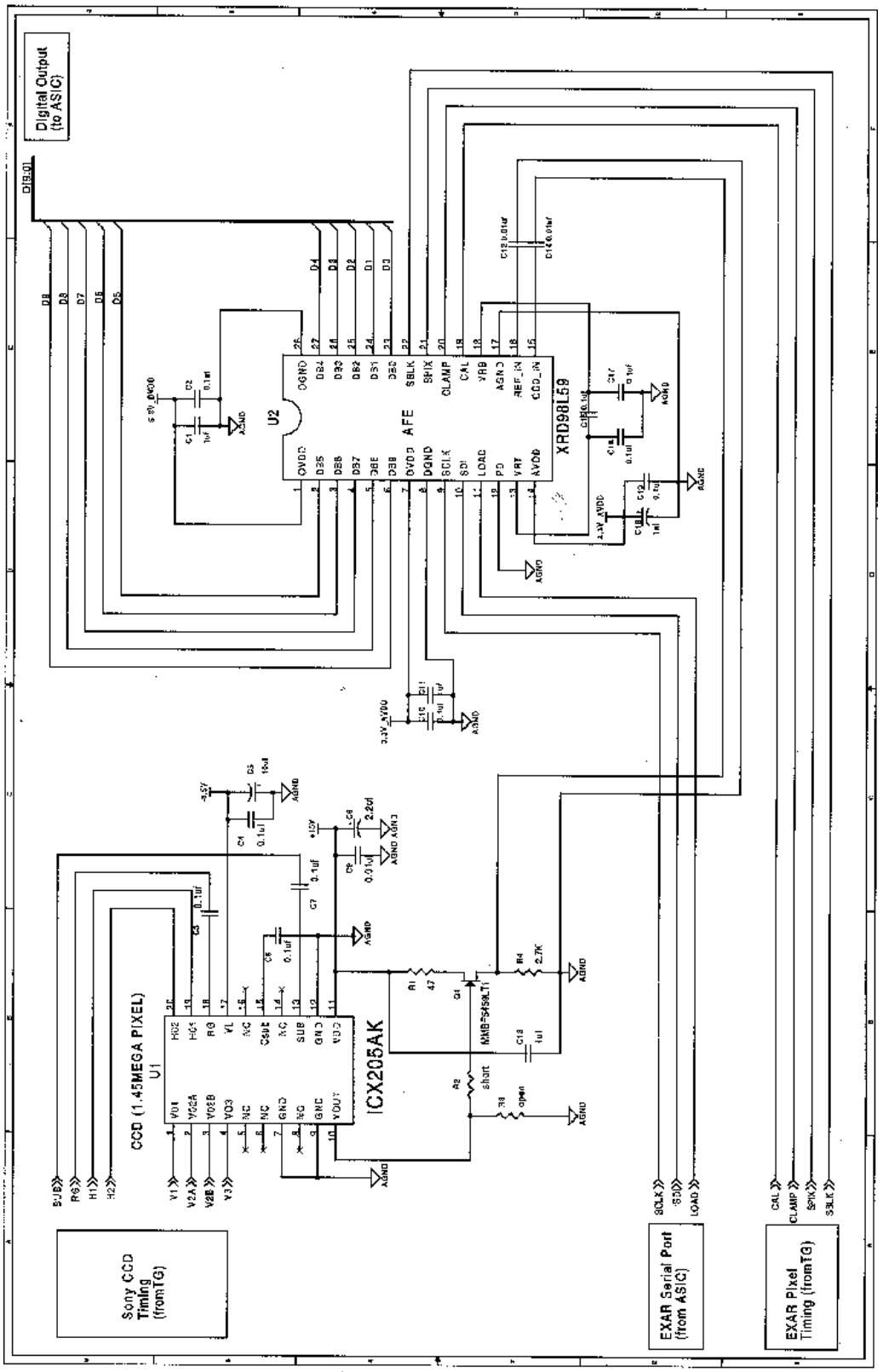


Figure 23. XRD98L59 1.45 Mpixel Camera Reference Schematic (Sheet 1)

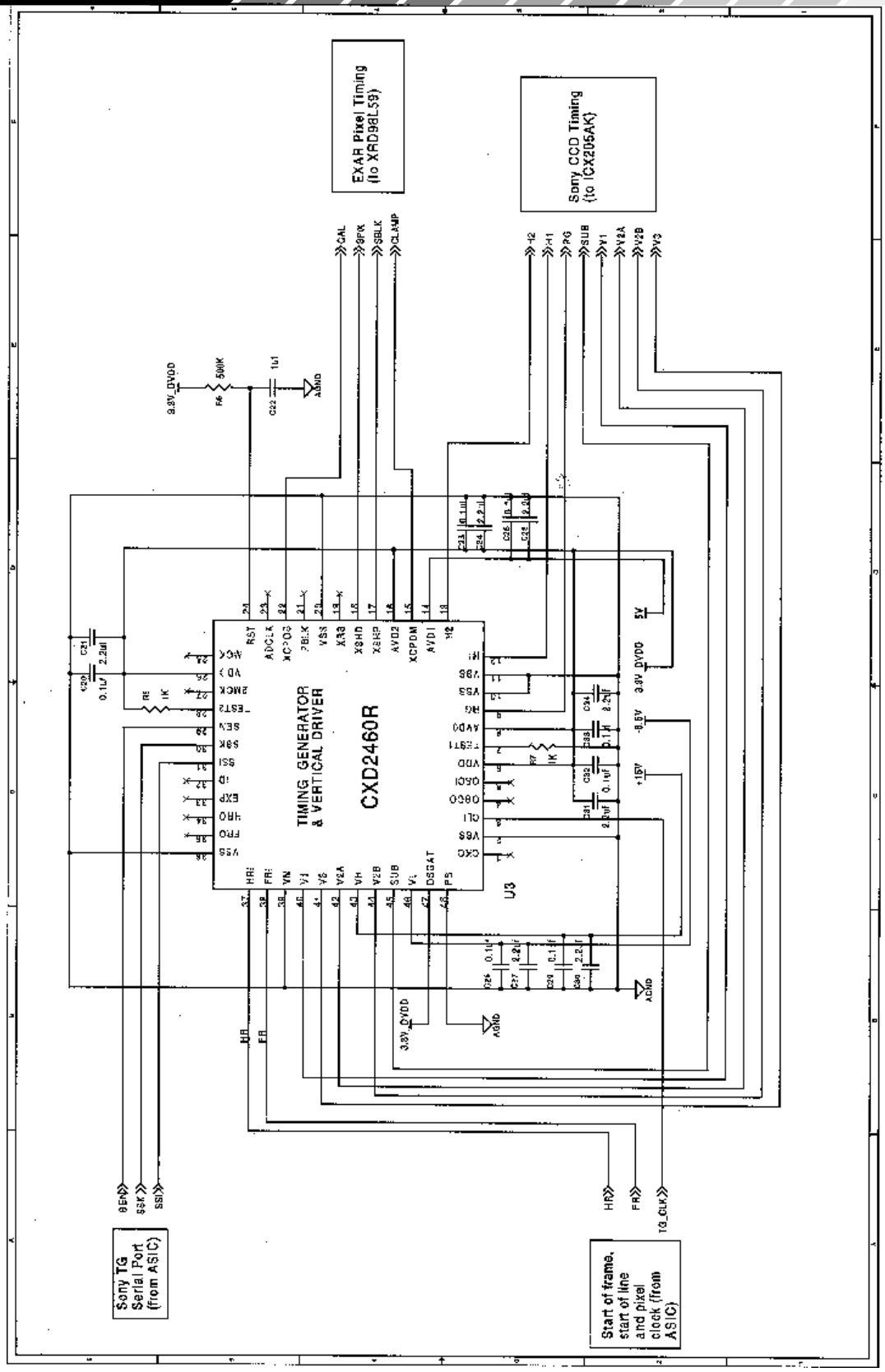


Figure 24. XRD98L59 1.45 Mpixel Camera Reference Schematic (Sheet 2)

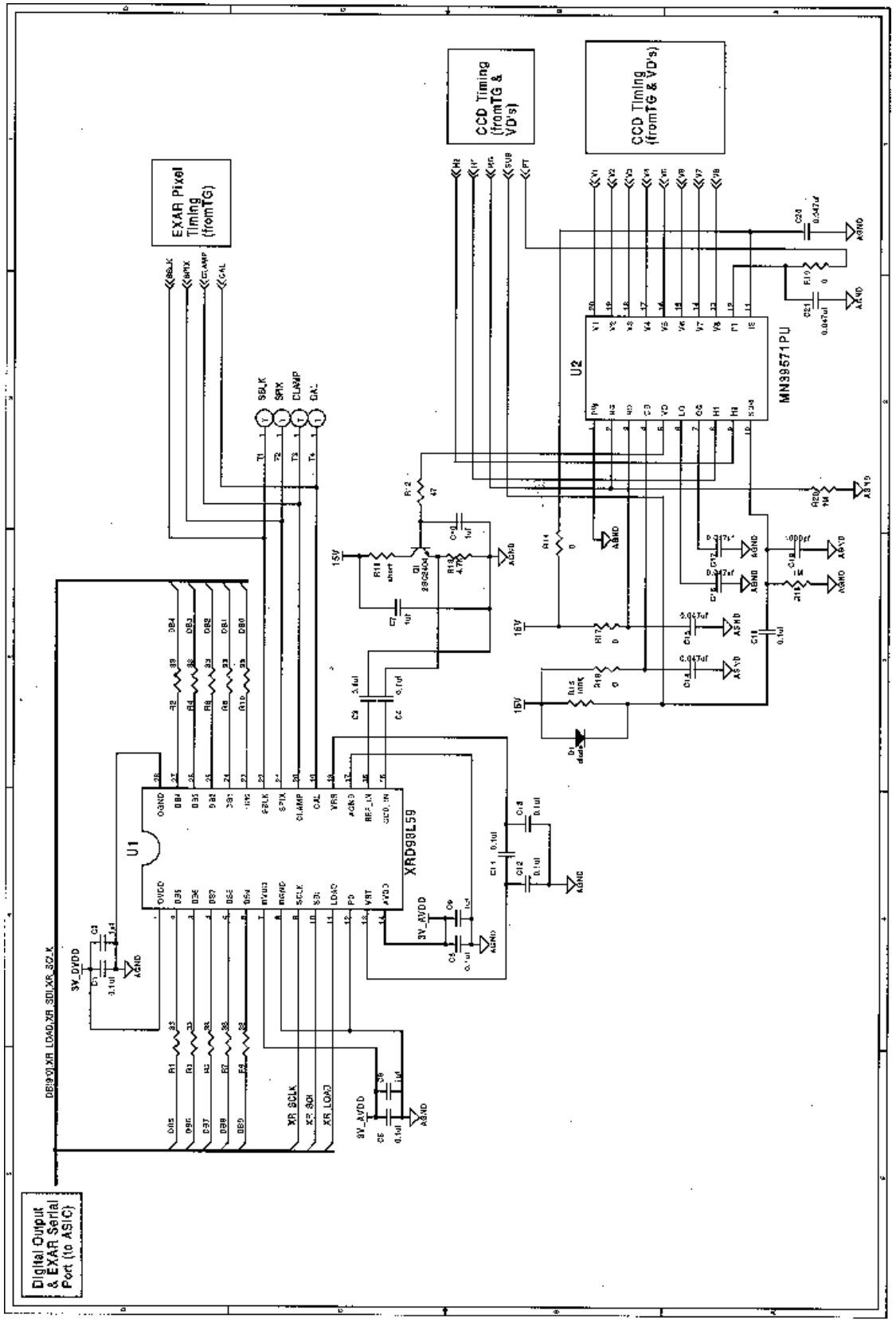


Figure 25. XRD98L59 2.31 Mpixel Camera Reference Schematic (Sheet 1)

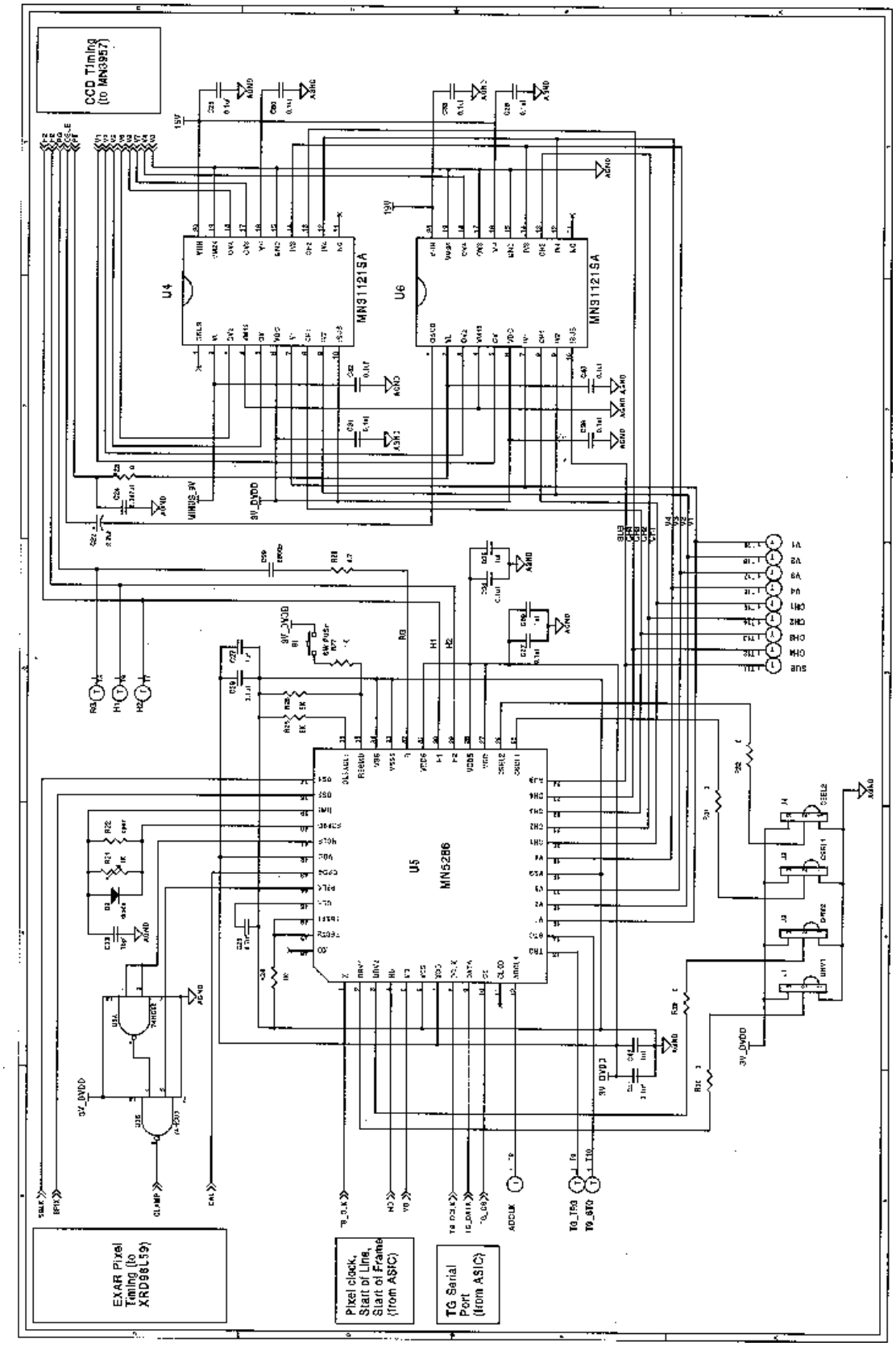
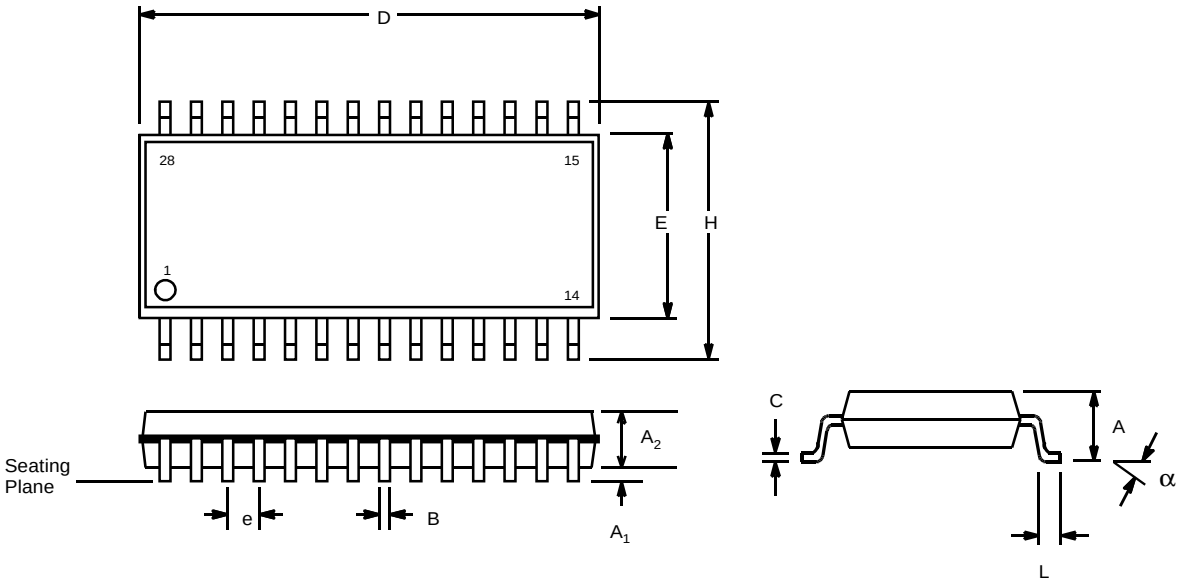


Figure 26. XRD98L59 2.31 Mpixel Camera Reference Schematic (Sheet 2)

28 LEAD THIN SHRINK SMALL OUTLINE

(4.4mm TSSOP)

Rev. 2.00



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.033	0.047	0.85	1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.378	0.386	9.60	9.80
E	0.169	0.177	4.30	4.50
e	0.0256 BSC		0.65 BSC	
H	0.248	0.256	6.30	6.50
L	0.018	0.030	0.45	0.75
α	0°	8°	0°	8°

Note: *The control dimension is in millimeter column*

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