



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
OUTPUT				
High peak output current ⁽²⁾		$I_{OH(PEAK)}$	0.6	A
Low peak output current ⁽²⁾		$I_{OL(PEAK)}$	0.6	A
Supply voltage		$(V_{CC} - V_{EE})$	0 to + 35	V
Output voltage		$V_{O(PEAK)}$	0 to + V_{CC}	V
Output power dissipation		P_{diss}	250	mW
OPTOCOUPLER				
Isolation test voltage between emitter and detector, climate per DIN 500414, part 2, Nov. 74	$t = 1.0 \text{ min}$	V_{ISO}	5300	V_{RMS}
Storage temperature range		T_S	- 55 to + 125	°C
Ambient operating temperature range		T_A	- 40 to + 110	°C
Total power dissipation		P_{tot}	285	mW
Lead solder temperature ⁽³⁾	for 10 s, 1.6 mm below seating plane		260	°C

Notes

⁽¹⁾ $T_{amb} = 25 \text{ °C}$, unless otherwise specified.

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.

⁽²⁾ Maximum pulse width = 10 μs , maximum duty cycle = 0.2 %. This value is intended to allow for component tolerances for designs with I_O peak minimum = 2.5 A. See applications section for additional details on limiting I_{OH} peak.

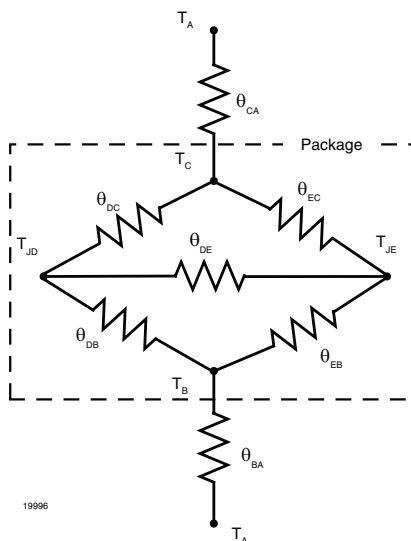
⁽³⁾ Refer to reflow profile for soldering conditions for surface mounted devices (SMD). Refer to wave profile for soldering conditions for through hole devices (DIP).

RECOMMENDED OPERATING CONDITION				
PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Power supply voltage	$V_{CC} - V_{EE}$	15	30	V
Input LED current (ON)	I_F	7	16	mA
Input voltage (OFF)	$V_{F(OFF)}$	- 3	0.8	V
Operating temperature	T_{amb}	- 40	+ 110	°C

THERMAL CHARACTERISTICS					
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT	
LED power dissipation	at 25 °C	P_{diss}	35	mW	
Output power dissipation	at 25 °C	P_{diss}	250	mW	
Total power dissipation	at 25 °C	P_{tot}	285	mW	
Maximum LED junction temperature	at 25 °C	T_{jmax}	125	°C	
Maximum output die junction temperature	at 25 °C	T_{jmax}	125	°C	
Thermal resistance, junction emitter to board	at 25 °C	θ_{JEB}	169	°C/W	
Thermal resistance, junction emitter to case	at 25 °C	θ_{JEC}	192	°C/W	
Thermal resistance, junction detector to board	at 25 °C	θ_{JDB}	82	°C/W	
Thermal resistance, junction detector to case	at 25 °C	θ_{JDC}	80	°C/W	
Thermal resistance, junction emitter to junction detector	at 25 °C	θ_{JED}	200	°C/W	
Thermal resistance, case to ambient	at 25 °C	θ_{CA}	2645	°C/W	

Note

The thermal model is represented in the thermal network below. Each resistance value given in this model can be used to calculate the temperatures at each node for a given operating condition. The thermal resistance from board to ambient will be dependent on the type of PCB, layout and thickness of copper traces. For a detailed explanation of the thermal model, please reference Vishay's thermal characteristics of optocouplers application note.



ELECTRICAL CHARACTERISTICS ⁽¹⁾						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
High level output current	$R_g = 2.3 \, \Omega, C_g = 22 \, \text{nF}$	$I_{OH}^{(2)}$	0.1	0.4		A
	$R_g = 2.3 \, \Omega, C_g = 22 \, \text{nF}$	$I_{OH}^{(3)}$	0.5			A
Low level output current	$R_g = 2.3 \, \Omega, C_g = 22 \, \text{nF}$	$I_{OL}^{(2)}$	0.1	0.6		A
	$R_g = 2.3 \, \Omega, C_g = 22 \, \text{nF}$	$I_{OL}^{(3)}$	0.5			A
High level output voltage	$I_O = -100 \, \text{mA}$	$V_{OH}^{(4)}$	$V_{CC} - 1.5$	$V_{CC} - 0.6$		V
Low level output voltage	$I_O = 100 \, \text{mA}$	V_{OL}		0.3	1.0	V
High level supply current	Output open, $I_F = 8$ to $16 \, \text{mA}$	I_{CCH}		4.2	7.0	mA
Low level supply current	Output open, $V_F = -3.0$ to $+0.8 \, \text{V}$	I_{CCL}		3.7	7.0	mA
Threshold input current low to high	$I_O = 0 \, \text{mA}, V_O > 5 \, \text{V}$	I_{FLH}		1.1	5.0	mA
Threshold input voltage high to low		V_{FHL}	0.8			V
Input forward voltage	$I_F = 10 \, \text{mA}$	V_F	1.0	1.3	1.6	V
Temperature coefficient of forward voltage	$I_F = 10 \, \text{mA}$	$\Delta V_F / \Delta T_A$		-1.4		mV/°C
Input reverse breakdown voltage	$I_R = 10 \, \mu\text{A}$	BV_R	5			V
Input capacitance	$f = 1 \, \text{MHz}, V_F = 0 \, \text{V}$	C_{IN}		60		pF
UVLO threshold	$V_O \geq 5 \, \text{V}$	V_{UVLO+}	11.0	12.2	13.5	V
	$I_F = 10 \, \text{mA}$	V_{UVLO-}	9.5	10.7	12.0	V
UVLO hysteresis		$UVLO_{HYS}$		1.5		V

Notes

⁽¹⁾ Minimum and maximum values were tested over recommended operating conditions ($T_A = -40 \, ^\circ\text{C}$ to $110 \, ^\circ\text{C}$, $I_{F(ON)} = 7 \, \text{mA}$ to $16 \, \text{mA}$, $V_{F(OFF)} = -3.0 \, \text{V}$ to $0.8 \, \text{V}$, $V_{CC} = 15 \, \text{V}$ to $30 \, \text{V}$, $V_{EE} = \text{ground}$) unless otherwise specified. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information only and are not part of the testing requirements. All typical values were measured at $T_{amb} = 25 \, ^\circ\text{C}$ and with $V_{CC} - V_{EE} = 30 \, \text{V}$.

⁽²⁾ Maximum pulse width = $50 \, \mu\text{s}$, maximum duty cycle = 0.5 %.

⁽³⁾ Maximum pulse width = $10 \, \mu\text{s}$, maximum duty cycle = 0.2 %. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.5 A.

⁽⁴⁾ In this test V_{OH} is measured with a dc load current. When driving capacitive loads V_{OH} will approach V_{CC} as I_{OH} approaches zero amps. Maximum pulse width = 1 ms, maximum duty cycle = 20 %.

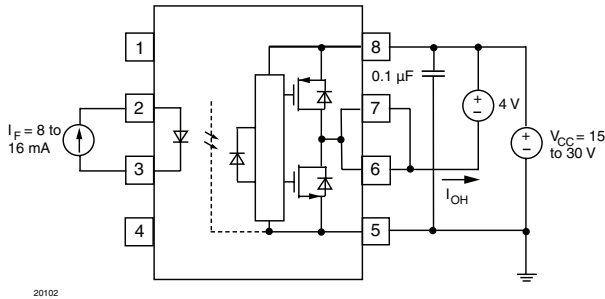
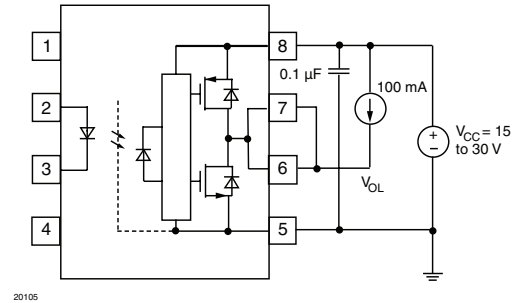
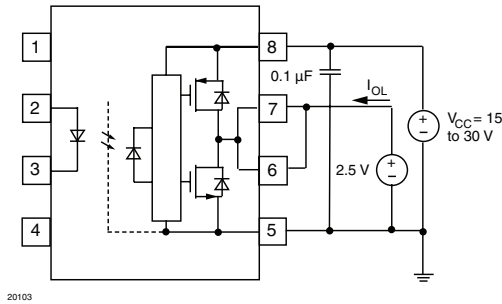
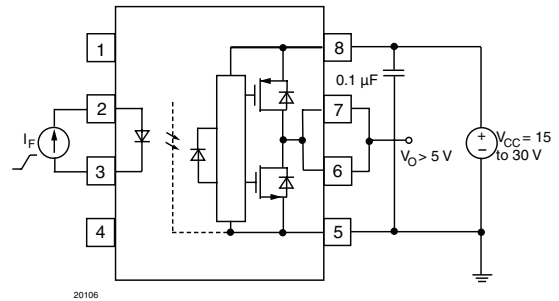
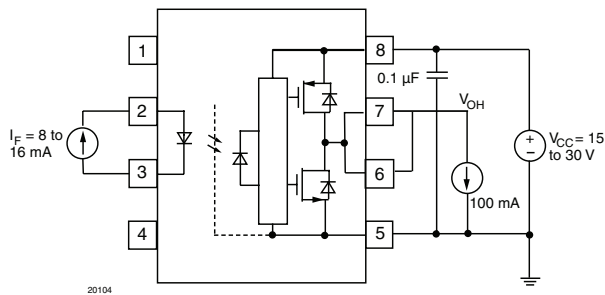
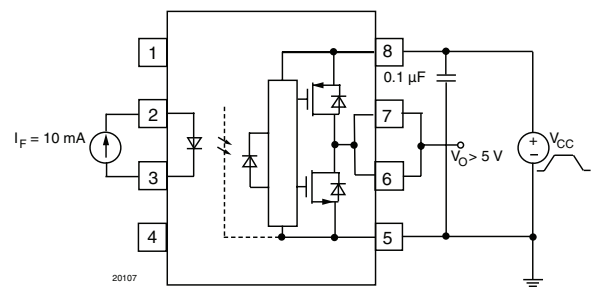
TEST CIRCUITS

Fig. 1 - I_{OH} Test Circuit

Fig. 4 - V_{OL} Test Circuit

Fig. 2 - I_{OL} Test Circuit

Fig. 5 - I_{FLH} Test Circuit

Fig. 3 - V_{OH} Test Circuit


Fig. 6 - UVLO Test Circuit

SWITCHING CHARACTERISTICS (1)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Propagation delay time to logic low output (1)	$R_g = 47 \Omega$, $C_g = 3 \text{ nF}$, $f = 10 \text{ kHz}$, duty cycle = 50 %	t_{PHL}	0.2		0.4	μs
Propagation delay time to logic high output (1)	$R_g = 47 \Omega$, $C_g = 3 \text{ nF}$, $f = 10 \text{ kHz}$, duty cycle = 50 %	t_{PLH}	0.2		0.4	μs
Pulse width distortion (2)	$R_g = 47 \Omega$, $C_g = 3 \text{ nF}$, $f = 10 \text{ kHz}$, duty cycle = 50 %	PWD			0.2	μs
Propagation delay difference between any two parts (3)	$R_g = 47 \Omega$, $C_g = 3 \text{ nF}$, $f = 10 \text{ kHz}$, duty cycle = 50 %	PDD ($t_{\text{PHL}} - t_{\text{PLH}}$)	- 0.35		0.35	μs
Rise time	$R_g = 47 \Omega$, $C_g = 3 \text{ nF}$, $f = 10 \text{ kHz}$, duty cycle = 50 %	t_r		0.1		μs
Fall time	$R_g = 47 \Omega$, $C_g = 3 \text{ nF}$, $f = 10 \text{ kHz}$, duty cycle = 50 %	t_f		0.01		μs
UVLO turn on delay	$V_O > 5 \text{ V}$, $I_F = 10 \text{ mA}$	$T_{\text{UVLO-ON}}$		1.1		μs
UVLO turn off delay	$V_O > 5 \text{ V}$, $I_F = 10 \text{ mA}$	$T_{\text{UVLO-OFF}}$		1.1		μs

Notes

(1) This load condition approximates the gate load of a 1200 V/25 A IGBT.

(2) Pulse Width Distortion (PWD) is defined as $|t_{\text{PHL}} - t_{\text{PLH}}|$ for any given device.

(3) The difference between t_{PHL} and t_{PLH} between any two VO3150 parts under the same test condition.

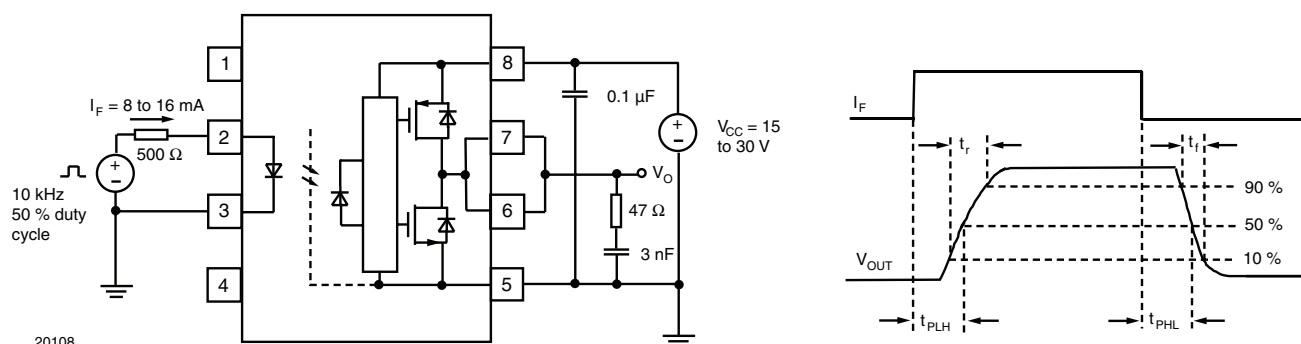


Fig. 7 - t_{PLH} , t_{PHL} , t_r and t_f Test Circuit and Waveforms

COMMON MODE TRANSIENT IMMUNITY

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Common mode transient immunity at logic high output (1, 2)	$T_A = 25^\circ\text{C}$, $I_F = 10 \text{ to } 16 \text{ mA}$, $V_{\text{CM}} = 1500 \text{ V}$, $V_{\text{CC}} = 30 \text{ V}$	$ \text{CM}_\text{H} $	15	30		$\text{kV}/\mu\text{s}$
Common mode transient immunity at logic low output (1, 3)	$T_A = 25^\circ\text{C}$, $V_{\text{CM}} = 1500 \text{ V}$, $V_{\text{CC}} = 30 \text{ V}$, $V_F = 0 \text{ V}$	$ \text{CM}_\text{L} $	15	30		$\text{kV}/\mu\text{s}$

Notes

(1) Pins 1 and 4 need to be connected to LED common.

(2) Common mode transient immunity in the high state is the maximum tolerable $|dV_{\text{CM}}/dt|$ of the common mode pulse, V_{CM} , to assure that the output will remain in the high state (i.e., $V_O > 15 \text{ V}$).

(3) Common mode transient immunity in a low state is the maximum tolerable $|dV_{\text{CM}}/dt|$ of the common mode pulse, V_{CM} , to assure that the output will remain in a low state (i.e., $V_O < 1 \text{ V}$).

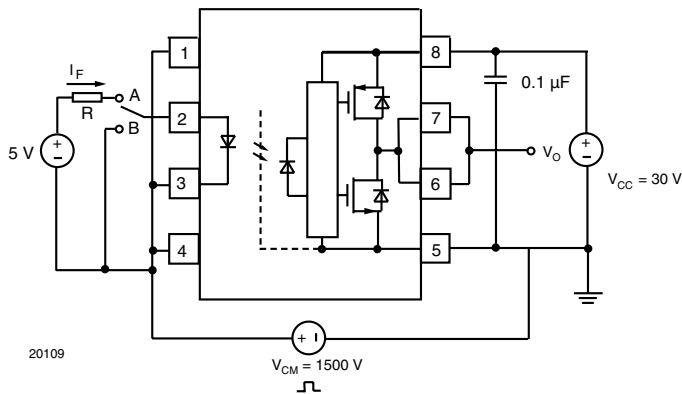


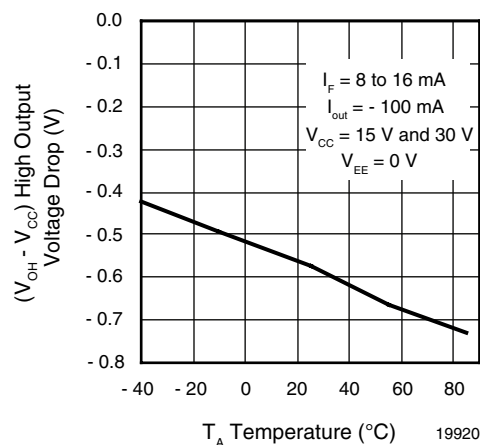
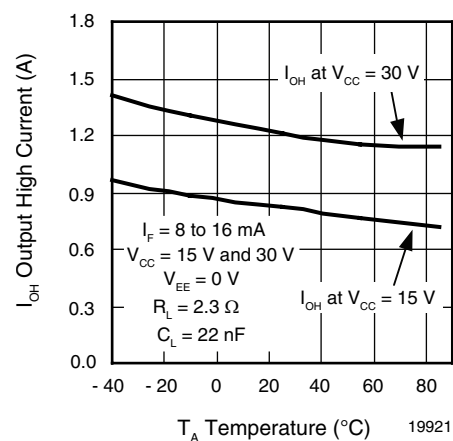
Fig. 8 - CMR Test Circuit and Waveforms

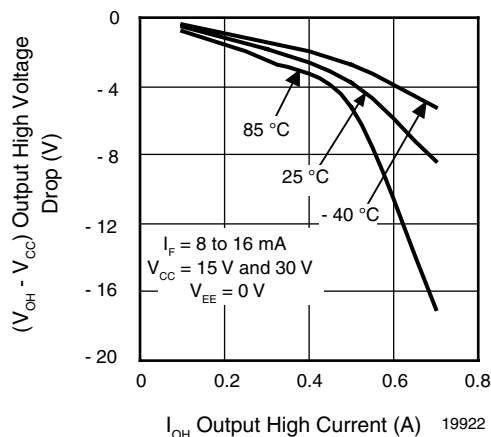
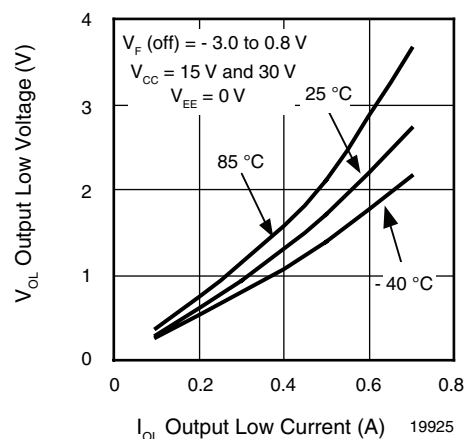
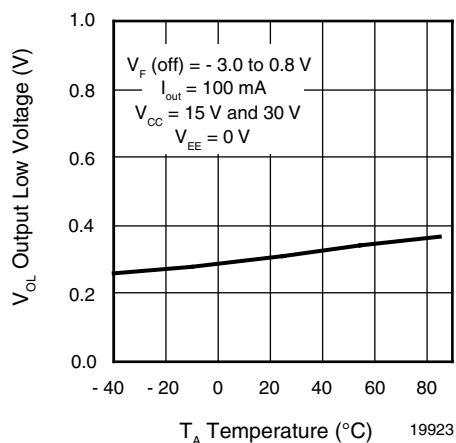
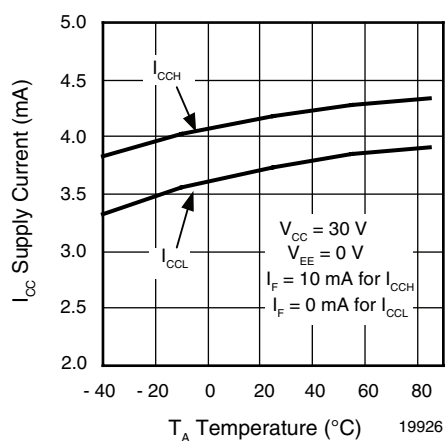
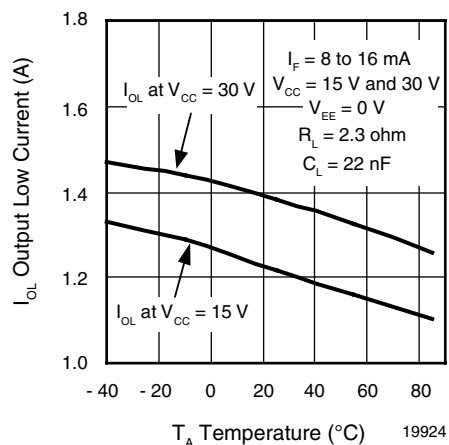
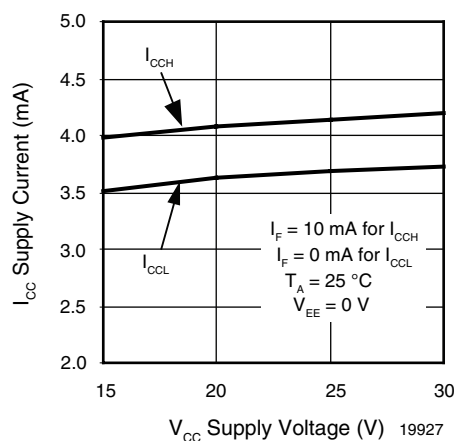
SAFETY AND INSULATION RATINGS

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Climatic classification (according to IEC68 part 1)				55/110/21		
Comparative tracking index		CTI	175		399	
Peak transient overvoltage		V_{IOTM}	8000			V
Peak insulation voltage		V_{IORM}	630			V
Safety rating - power output		P_{SO}			500	mW
Safety rating - input current		I_{SI}			300	mA
Safety rating - temperature		T_{SI}			175	°C
Creepage distance	standard DIP-8		7			mm
Clearance distance	standard DIP-8		7			mm
Creepage distance	400 mil DIP-8		8			mm
Clearance distance	400 mil DIP-8		8			mm

Note

As per IEC 60747-5-2, § 7.4.3.8.1, this optocoupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of protective circuits.


 Fig. 9 - V_{OH} vs. Temperature

 Fig. 10 - I_{OH} vs. Temperature

Fig. 11 - V_{OH} vs. I_{OH} Fig. 14 - V_{OL} vs. I_{OL} Fig. 12 - V_{OL} vs. TemperatureFig. 15 - I_{CC} vs. TemperatureFig. 13 - I_{OL} vs. TemperatureFig. 16 - I_{CC} vs. V_{CC}

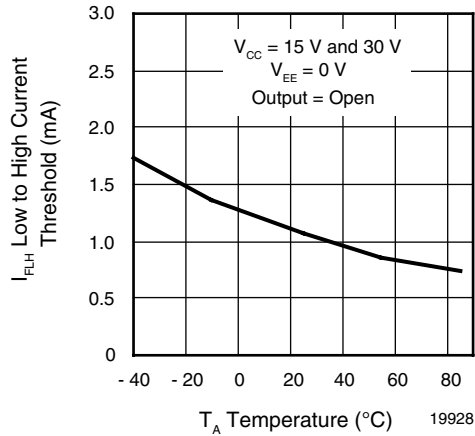
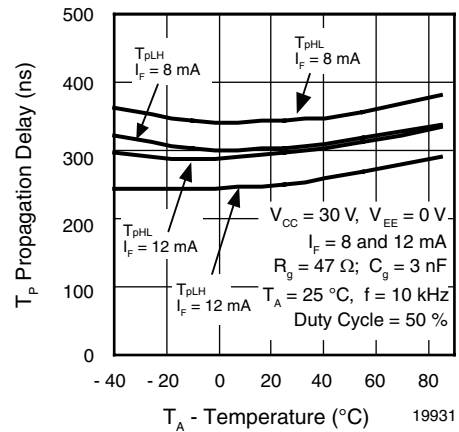
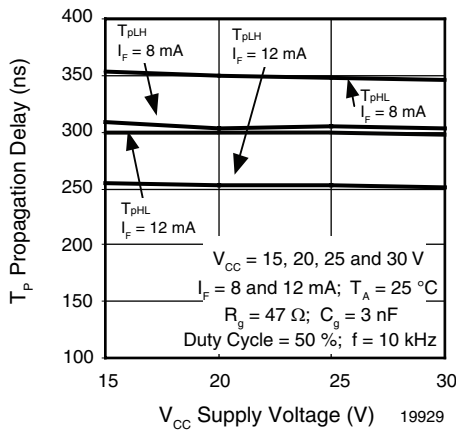
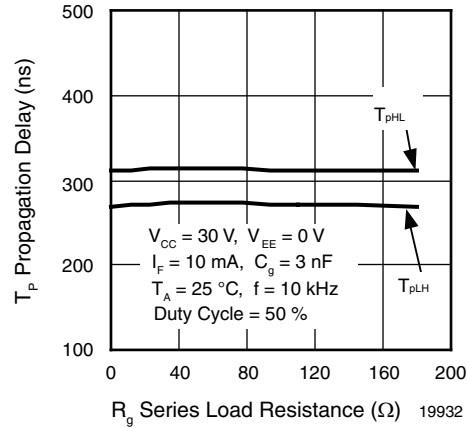
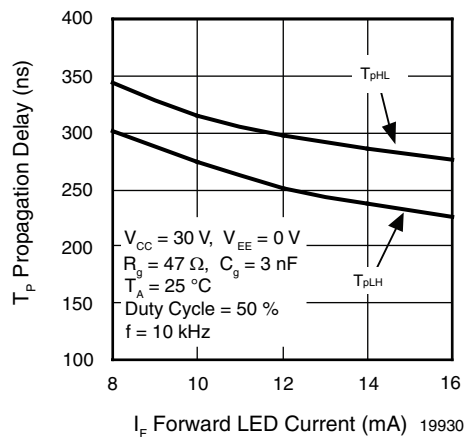
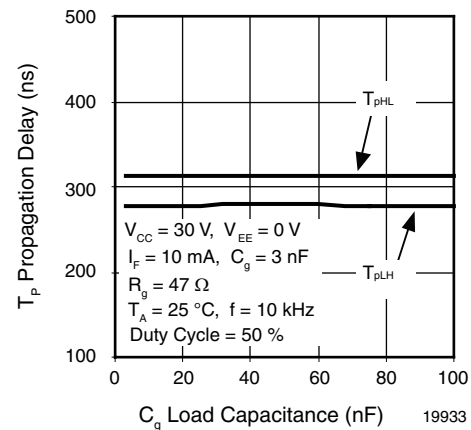

 Fig. 17 - I_{FLH} vs. Temperature


Fig. 20 - Propagation Delay vs. Temperature


 Fig. 18 - Propagation Delay vs. V_{CC}

 Fig. 21 - Propagation Delay vs. R_g

 Fig. 19 - Propagation Delay vs. I_F

 Fig. 22 - Propagation Delay vs. C_g

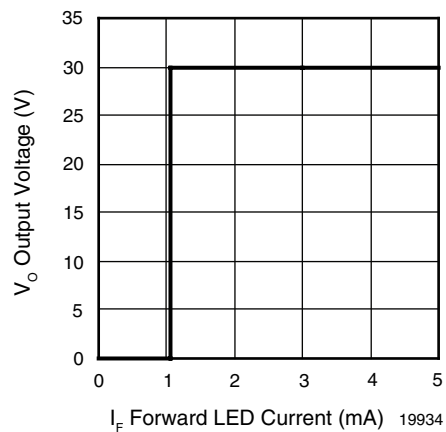


Fig. 23 - Transfer Characteristics

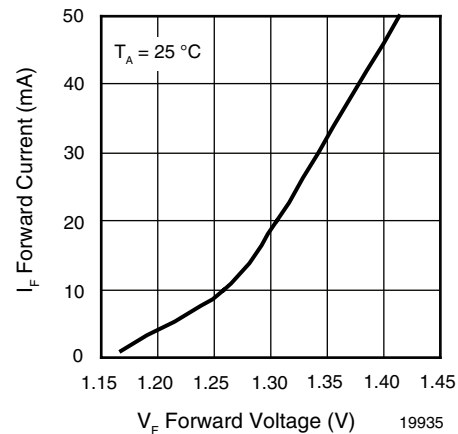
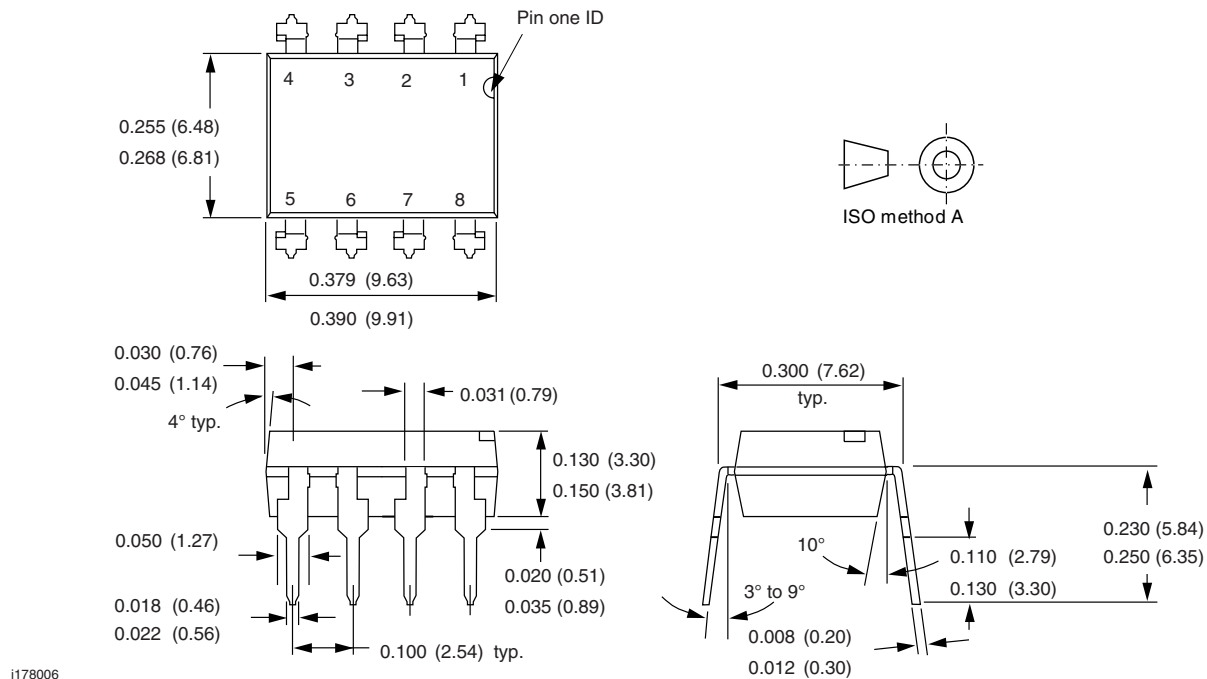


Fig. 24 - Input Current vs. Forward Voltage

PACKAGE DIMENSIONS in inches (millimeters)

**OZONE DEPLETING SUBSTANCES POLICY STATEMENT**

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively.
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design
and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Vishay Semiconductors products for any unintended or unauthorized application, the buyer shall indemnify Vishay Semiconductors against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany



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