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1 Block diagrams and pins descriptions

Figure 1. Block diagram

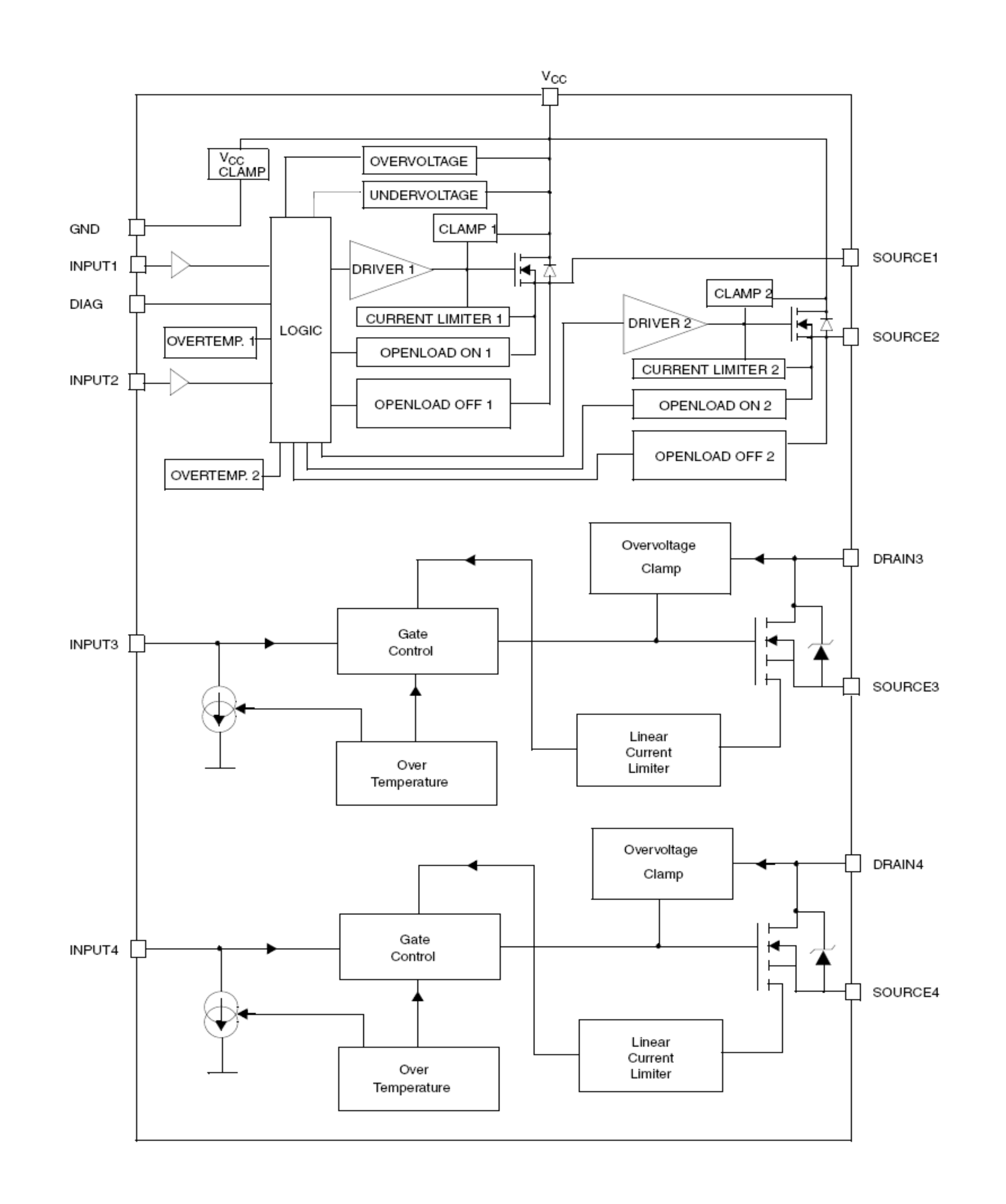
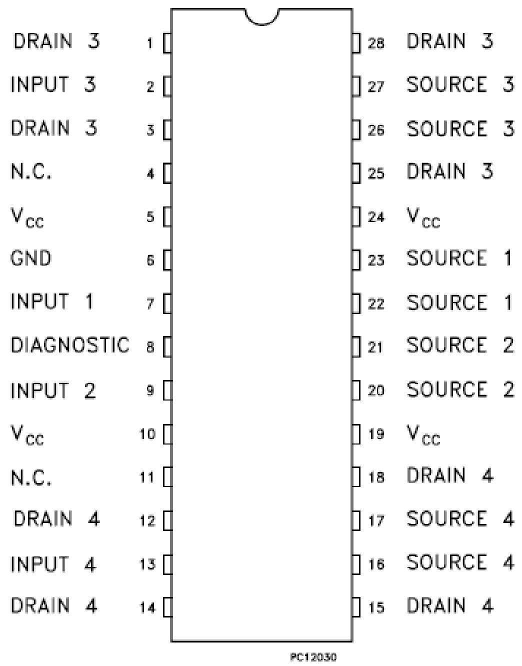


Table 2. Pin definition and function

No	Name	Function
1, 3, 25, 28	DRAIN 3	Drain of switch 3 (low-side switch)
2	INPUT 3	Input of switch 3 (low-side switch)
4, 11	N.C.	Not connected
5, 10, 19, 24	V_{CC}	Drain of switches 1 and 2 (high-side switches) and power supply voltage
6	GND	Ground of switches 1 and 2 (high-side switches)
7	INPUT 1	Input of switch 1 (high-side switches)
8	DIAGNOSTIC	Diagnostic of switches 1 and 2 (high-side switches)
9	INPUT 2	Input of switch 2 (high-side switch)
12, 14, 15, 18	DRAIN 4	Drain of switch 4 (low-side switch)
13	INPUT 4	Input of switch 4 (low-side switch)
16, 17	SOURCE 4	Source of switch 4 (low-side switch)
20, 21	SOURCE 2	Source of switch 2 (high-side switch)
22, 23	SOURCE 1	Source of switch 1 (high-side switch)
26, 27	SOURCE 3	Source of switch 3 (low-side switch)

Figure 2. Connection diagram



2 Electrical specifications

2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value Max (°C/W)
$R_{thj\text{-}case}$	Thermal resistance junction-case (high side switch)	20
$R_{thj\text{-}case}$	Thermal resistance junction-case (low side switch)	20
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (with 6 cm^2 of Cu heat sink)	See *Figure 49*

2.2 Absolute maximum ratings

Table 4. Dual high side switch

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-6	A
I_{IN}	DC input current	±10	mA
I_{STAT}	DC status current	±10	mA
V_{ESD}	Electrostatic discharge (human body model: R = 1.5KΩ; C = 100pF) – Input – Status – Output – Vcc	 4000 4000 5000 5000	 V V V V
P_{tot}	Power dissipation (T_C =25°C)	6	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

Table 5. Low side switch

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage (V_{IN} = 0V)	Internally clamped	V
V_{IN}	Input voltage	Internally clamped	V
I_{IN}	Input current	±20	mA

Table 5. Low side switch (continued)

Symbol	Parameter	Value	Unit
$R_{IN\ MIN}$	Minimum input series impedance	10	Ω
I_D	Drain current	Internally limited	A
I_R	Reverse DC output current	-15	A
V_{ESD1}	Electrostatic discharge (R = 1.5KΩ, C = 100pF)	4000	V
V_{ESD2}	Electrostatic discharge on output pin only (human body model: R = 330Ω, C = 150pF)	5000	V
P_{tot}	Power dissipation (T_C = 25°C)	6	W
T^j	Operating junction temperature	Internally limited	°C
T_c	Case operating temperature	Internally limited	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.3 Electrical characteristics for dual high side switch

8V < V_{CC}< 36V; -40°C < T_j < 150°C, unless otherwise specified.

Table 6. Power outputs (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}(1)	Operating supply voltage		5.5	13	36	V
V_{USD}(1)	Undervoltage shutdown		3	4	5.5	V
V_{OV}(1)	Overvoltage shutdown		36	-	-	V
R_{ON}	On-state resistance	I_{OUT} =2A; T_j =25°C I_{OUT} =2A; V_{CC} >8V	-	-	60 120	mΩ mΩ
I_S(1)	Supply current	Off-state; V_{CC} = 13V; V_{IN} =V_{OUT} =0V Off-state; V_{CC} = 13V; V_{IN} =V_{OUT} =0V; T_j =25°C On-state; V_{CC} = 13V;	-	12 12 5	40 25 7	µA µA mA
$I_{L(off1)}$	Off-state output current	V_{IN} =V_{OUT} =0V; V_{CC} =36V; T_j = 125°C	0	-	50	µA
$I_{L(off2)}$	Off-state output current	V_{IN} =0V; V_{OUT} =3.5V	-75	-	0	µA
$I_{L(off3)}$	Off-state output current	V_{IN} =V_{OUT} =0V; V_{CC} = 13V; T_j = 125°C	-	-	5	µA
$I_{L(off4)}$	Off-state output current	V_{IN} =V_{OUT} =0V; V_{CC} = 13V; T_j = 25°C	-	-	3	µA

1. Per device.

Table 7. Switching (per each channel) (V_{CC}= 13V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	R_L =6.5Ω from V_{IN} rising edge to V_{OUT} =1.3V	-	30	-	μs
$t_{d(off)}$	Turn-off delay time	R_L =6.5Ω from V_{IN} falling edge to V_{OUT} = 11.7V	-	30	-	μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L =6.5Ω from V_{OUT} = 1.3V to V_{OUT} = 10.4V	-	See relative diagram	-	V/μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L =6.5Ω from V_{OUT} = 11.7V to V_{OUT} =1.3V	-	See relative diagram	-	V/μs

Table 8. Logic input (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Input low level		-	-	1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25V	1	-	-	μA
V_{IH}	Input high level		3.25	-	-	V
I_{IH}	High level input current	V_{IN} = 3.25V	-	-	10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.5	-	-	V
V_{ICL}	Input clamp voltage	I_{IN} = 1mA I_{IN} = -1mA	6	6.8 -0.7	8	V V

Table 9. Status pin (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1.6 mA	-	-	0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT} = 5V	-	-	10	μA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT} = 5V	-	-	100	pF
V_{SCL}	Status clamp voltage	I_{STAT} = 1mA I_{STAT} = -1mA	6	6.8 -0.7	8	V V

Table 10. Protections (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135	-	-	°C
T_{hyst}	Thermal hysteresis		7	15	-	°C

Table 10. **Protections (per each channel) (continued)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{SDL}	Status delay in overload conditions	$T_j > T_{TSD}$	-	-	20	µs
I_{lim}	Current limitation	 T_j = 125°C 5.5V < V_{CC} <36V	6 8.5	9	15 15 15	A A A
V_{demag}	Turn-off output clamp voltage	I_{OUT} =2A; L=6mH	VCC-41	VCC-48	VCC-55	V

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 11. **Openload detection (per each channel)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{OL}	Openload on-state detection threshold	V_{IN} = 5V	50	100	200	mA
$t_{DOL(on)}$	Openload on-state detection delay	I_{OUT} = 0A	-	-	200	µs
V_{OL}	Openload off-state voltage detection threshold	V_{IN} = 0V	1.5	2.5	3.5	V
$t_{DOL(off)}$	Openload detection delay at turn-off		-	-	1000	µs

2.4 Electrical characteristics for low side switches

-40°C < T_j < 150°C, unless otherwise specified.

Table 12. **Off-state**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CLAMP}	Drain source clamp voltage	V_{IN} =0V; I_D = 7A	40	45	55	V
V_{CLTH}	Drain source clamp threshold voltage	V_{IN} =0V; I_D =2mA	36	-	-	V
V_{INTH}	Input threshold voltage	V_{DS} =V_{IN}; I_D =1mA	0.5	-	2.5	V
I_{ISS}	Supply current from input pin	V_{DS} =0V; V_{IN} = 5V	-	100	150	µA

Table 12. Off-state (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{INCL}	Input-source clamp voltage	I_{IN} =1mA I_{IN} =-1mA	6 -1.0	6.8	8 -0.3	V
I_{DSS}	Zero input voltage drain current (V_{IN} =0V)	V_{DS} = 13V; V_{IN} =0V; T_j =25°C V_{DS} = 25V; V_{IN} =0V	-	-	30 75	µA

Table 13. On-state

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$R_{DS(on)}$	Static drain source on resistance	V_{IN} =5V; I_D =7A; T_j = 25°C V_{IN} =5V; I_D =7A	-	-	35 70	mΩ

T_j = 25°C, unless otherwise specified.

Table 14. Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
g_{fs}(1)	Forward trans conductance	V_{DD} =13V; I_D =7A	-	18	-	S
C_{OSS}	Output capacitance	V_{DS} = 13V; f = 1 MHz; V_{IN} = 0V	-	400	-	pF

1. Pulsed: Pulse duration = 300µs, duty cycle 1.5%

Table 15. Switching

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} =15V; I_D =7A V_{gen} =5V; R_{gen} = $R_{IN\ MIN}$ =10Ω	-	80	250	ns
t_r	Rise time		-	350	1000	ns
$t_{d(off)}$	Turn-off delay time		-	450	1350	ns
t_f	Fall time		-	150	500	ns
$t_{d(on)}$	Turn-on delay time	V_{DD} =15V; I_D =7A V_{gen} =5V; R_{gen} =2.2KΩ	-	1.5	4.5	µs
t_r	Rise time		-	9.7	30	µs
$t_{d(off)}$	Turn-off delay time		-	9	25	µs
t_f	Fall time		-	10.2	30	µs
$(dI/dt)_{on}$	Turn-on current slope	V_{DD} =15V; I_D =7A V_{gen} =5V; R_{gen} = $R_{IN\ MIN}$ =10Ω	-	16	-	A/µs
Q_i	Total input charge	V_{DD} =12V; I_D =7A; V_{IN} =5V I_{gen} = 2.13mA	-	36.8	-	nC

Table 16. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{SD} [(1)]	Forward on voltage	I_{SD} =7A; V_{IN} =0V	-	0.8	-	V
t_{rr}	Reverse recovery time	I_{SD} = 7A; dI/dt = 40A/µs V_{DD} = 30V; L = 200µH	-	300	-	ns
Q_{rr}	Reverse recovery charge		-	0.80	-	µC
I_{RRM}	Reverse recovery current		-	5	-	A

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

-40°C < Tj < 150°C, unless otherwise specified.

Table 17. Protections

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{lim}	Drain current limit	V_{IN} =5V; V_{DS} =13V V_{IN} =5V; V_{DS} =13V; T_j =125°C	12 15	18	24 24	A A
t_{dlim}	Step response current limit	V_{IN} =5V; V_{DS} = 13V	-	45	-	µs
T_{jsh}	Over temperature shutdown		150	175	-	°C
T_{jrs}	Over temperature reset		135	-	-	°C
I_{gf}	Fault sink current	V_{IN} = 5V; V_{DS} =13V; T_j =T_{jsh}	10	15	20	mA
E_{as}	Single pulse avalanche energy	starting T_j =25°C; V_{DD} = 24V V_{IN} =5V; R_{gen} = $R_{IN\ MIN}$ =10Ω; L=24mH	400	-	-	mJ

2.5 Dual high-side switch timing data

Figure 3. Switching time waveforms

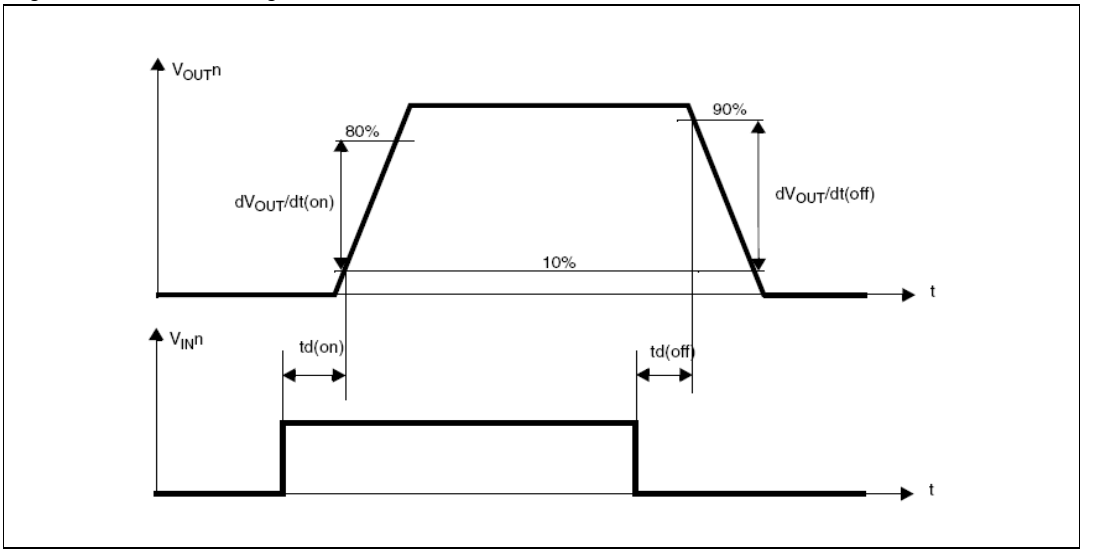


Table 18. Truth table

Conditions	Input	Output	Status
Normal operation	L H	L H	H H
Current limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Over temperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output voltage > V_{OL}	L H	H H	L H
Output current < I_{OL}	L H	L H	H L

Figure 4. Open-load status timing (with external pull-up)

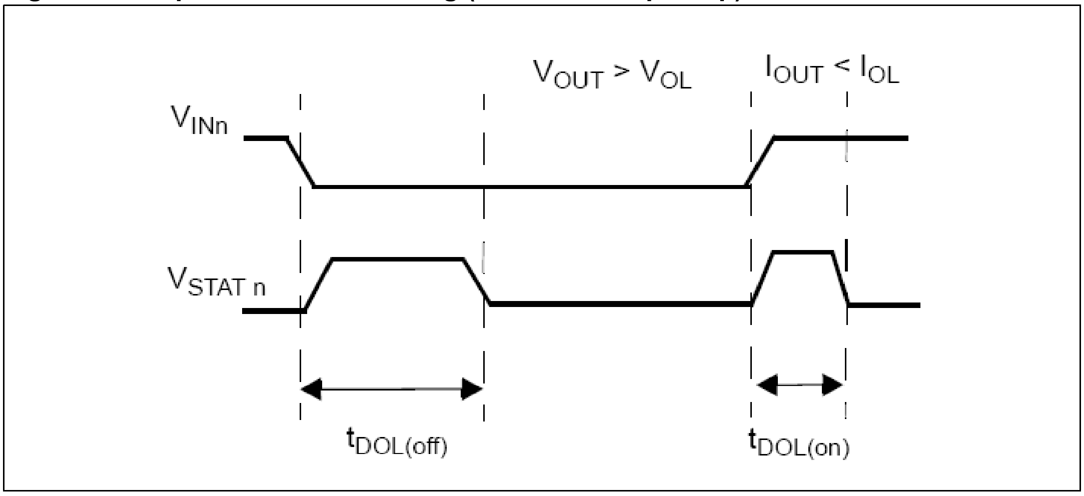
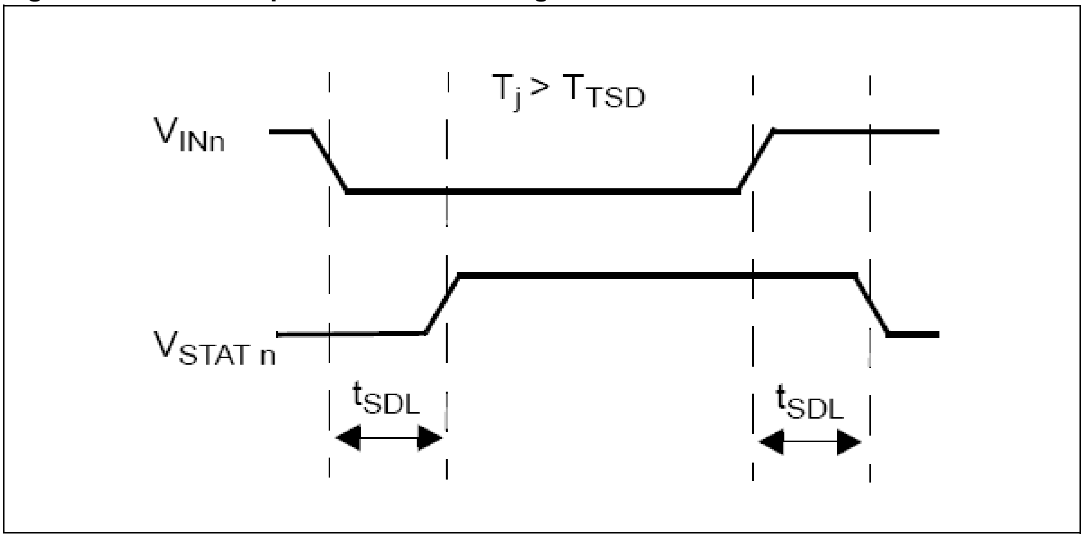


Figure 5. Over temperature status timing



2.6 Electrical characterization for dual high side switch

Figure 6. Off-state output current

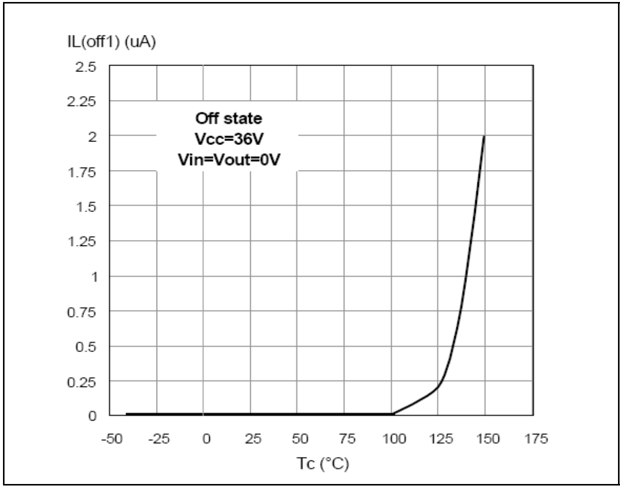


Figure 7. Input clamp voltage

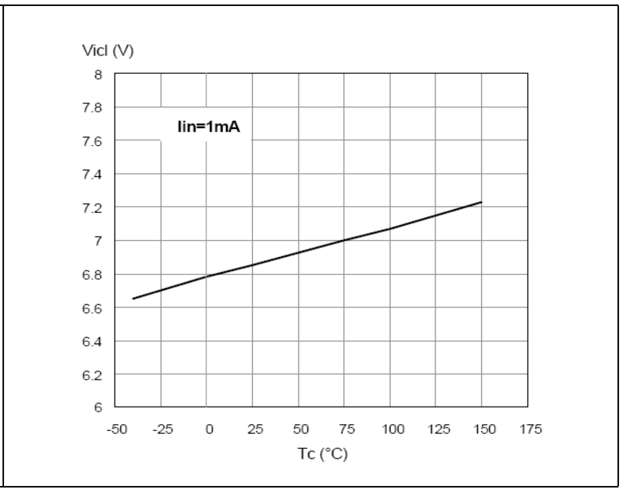


Figure 8. High level input current

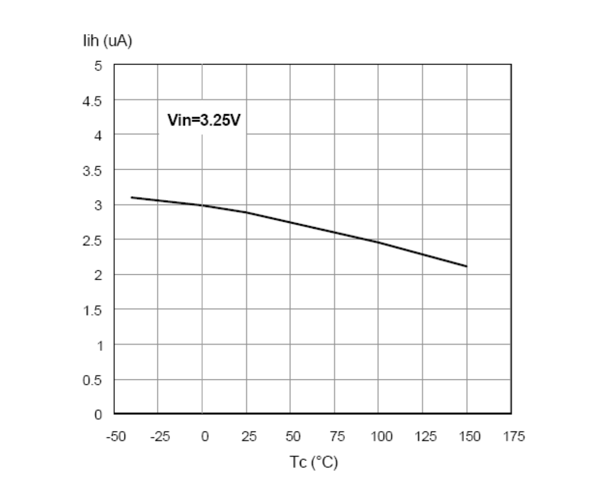


Figure 9. Input high level voltage

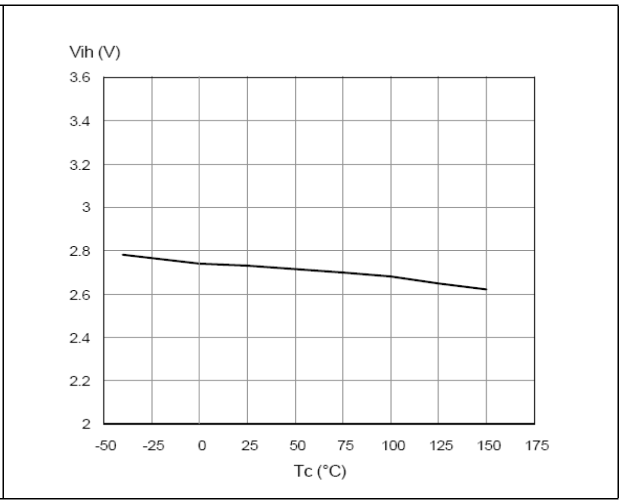


Figure 10. Input low level voltage

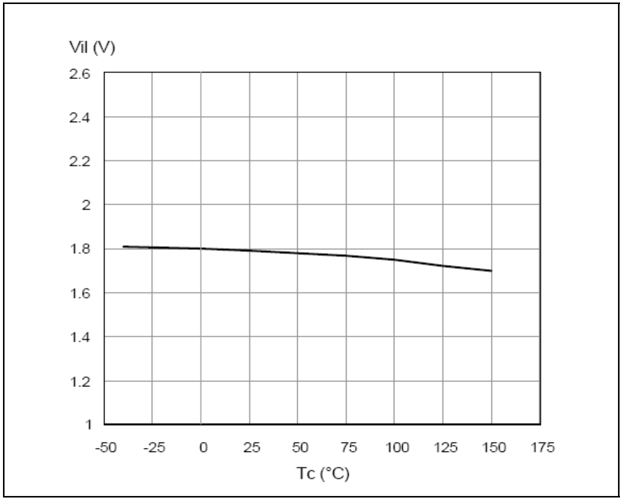


Figure 11. Input hysteresis voltage

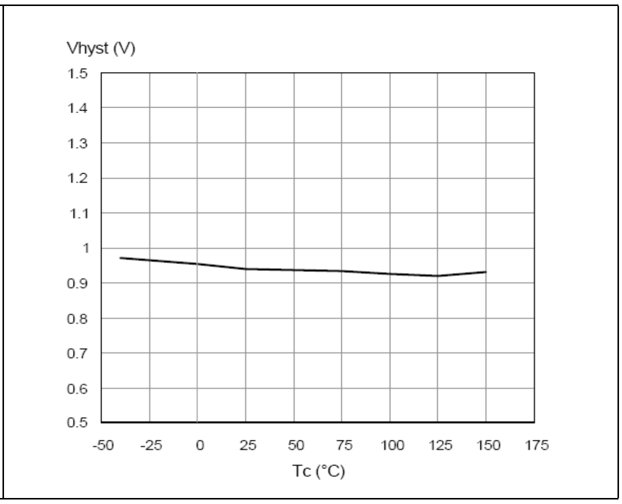


Figure 12. Overvoltage shutdown

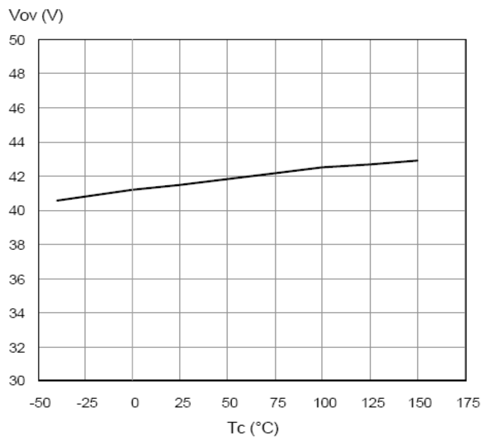


Figure 13. I_{LIM} vs T_{case}

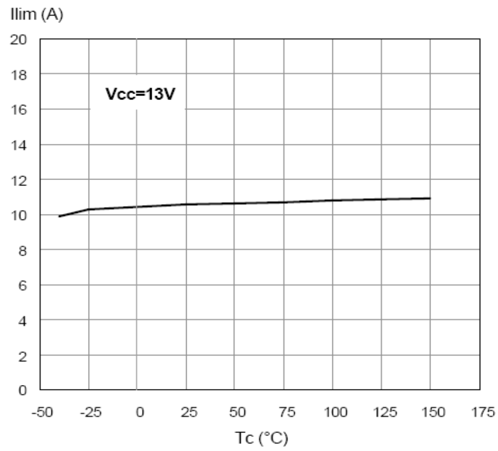


Figure 14. Turn-on voltage slope

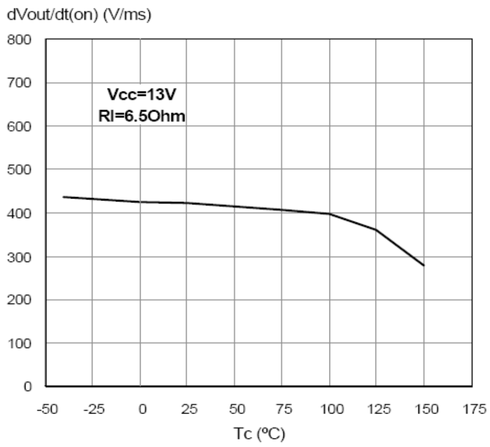


Figure 15. Turn-off voltage slope

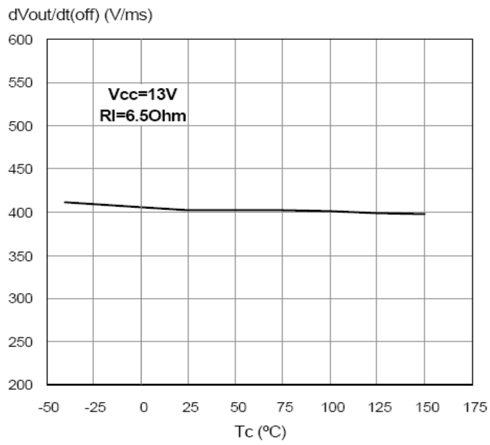


Figure 16. On-state resistance vs T_{case}

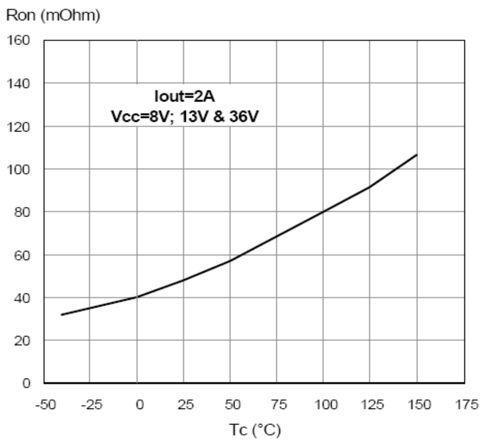


Figure 17. On-state resistance vs V_{CC}

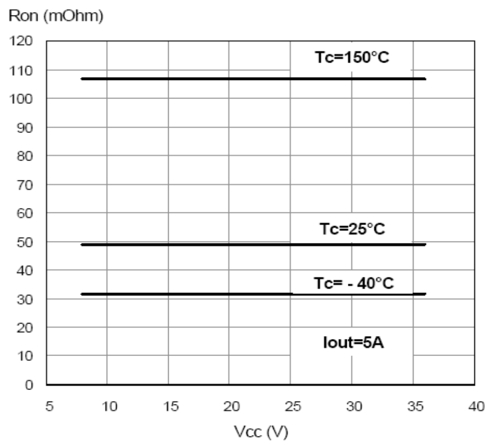


Figure 18. Status leakage current

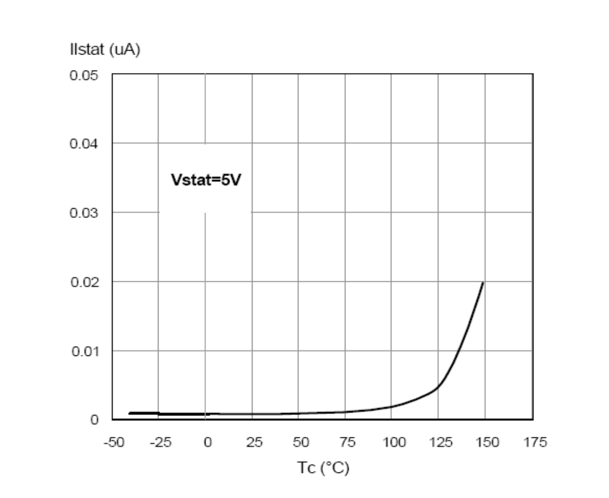


Figure 19. Status low output voltage

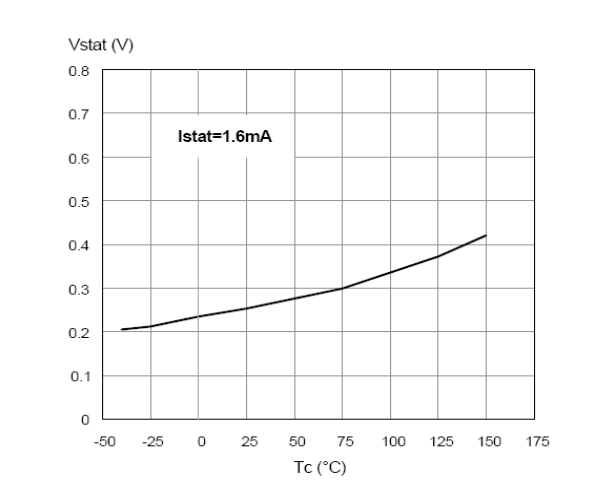


Figure 20. Openload on-state detection threshold

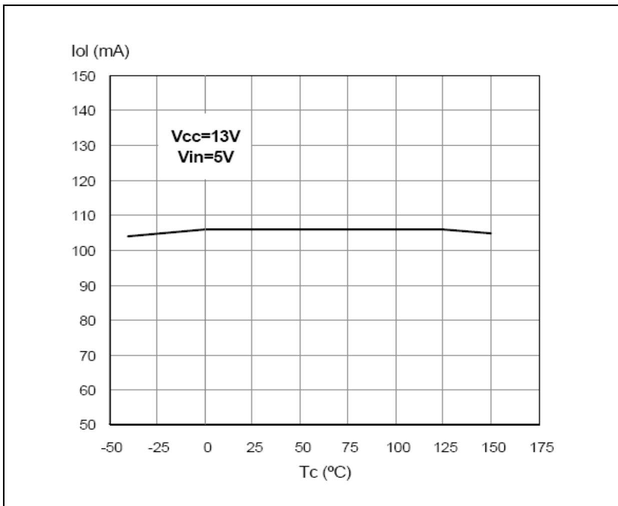


Figure 21. Openload off-state voltage detection threshold

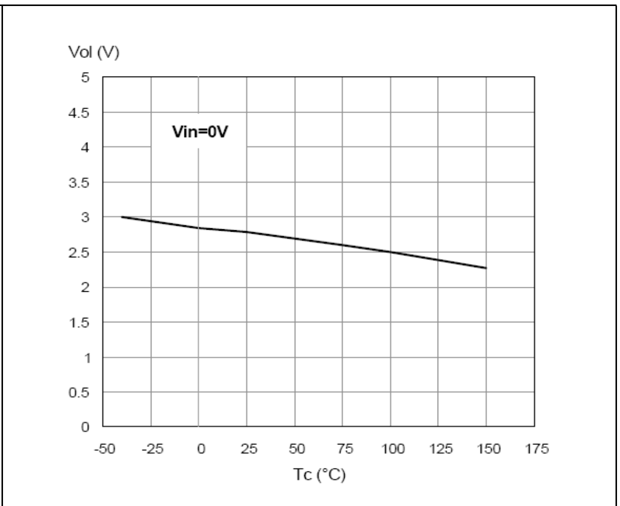
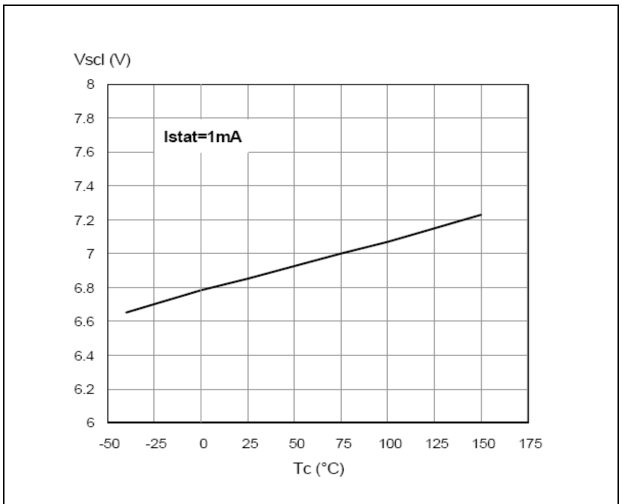


Figure 22. Status clamp voltage



2.7 Electrical characterization for low side switches

Figure 23. Static drain source on resistance

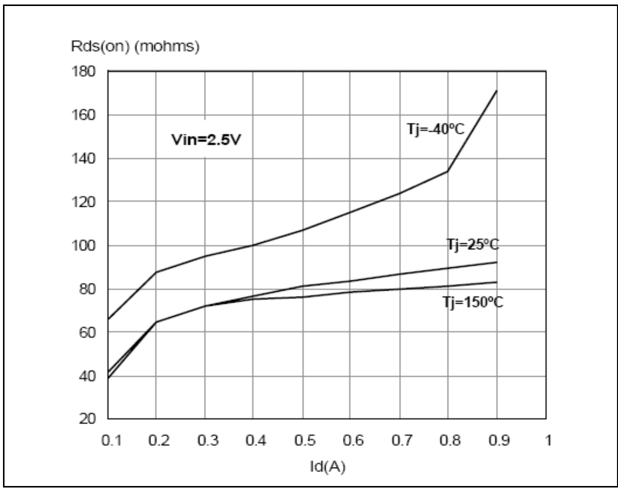


Figure 24. Derating curve

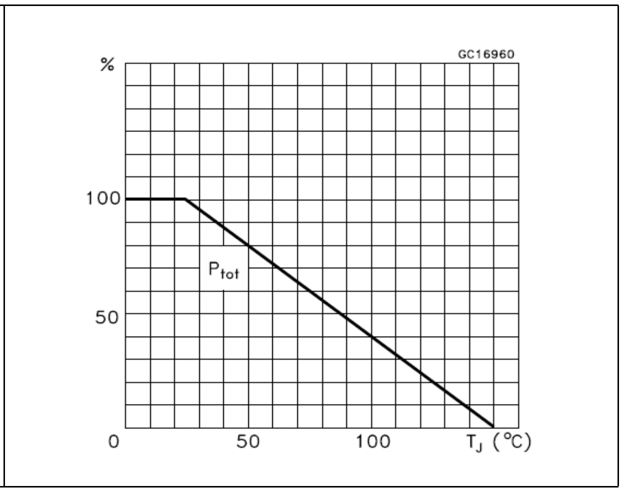


Figure 25. Transconductance

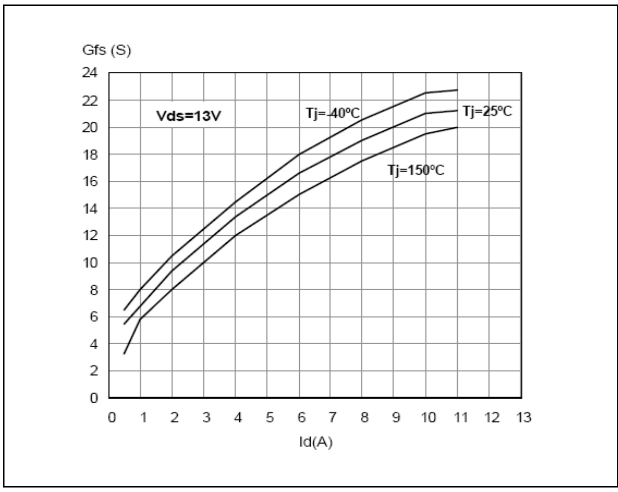


Figure 26. Transfer characteristics

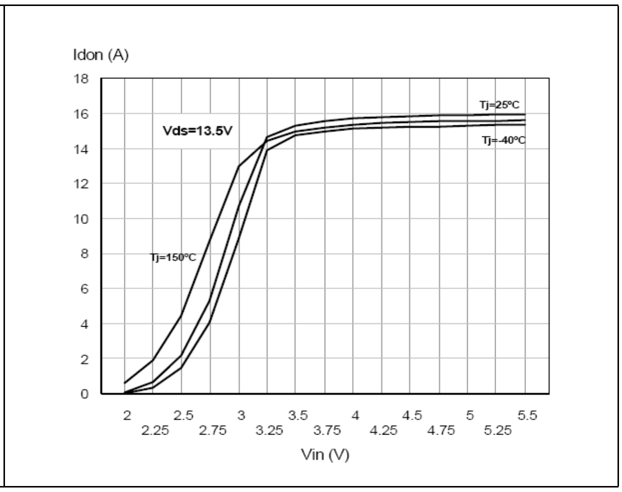


Figure 27. Turn-on current slope (V_{in}=5V)

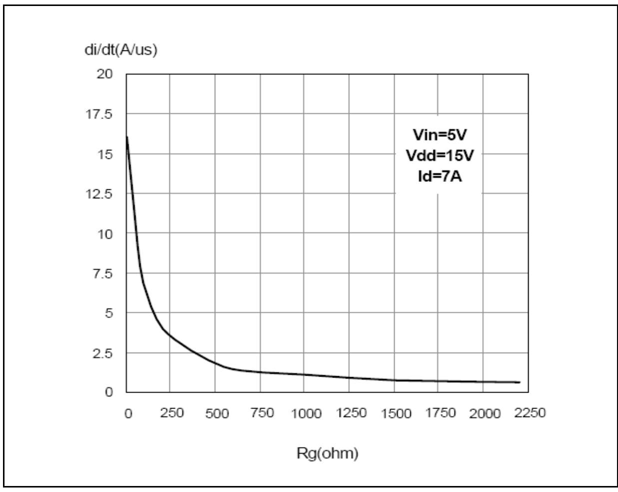


Figure 28. Turn-on current slope (V_{in}=3.5V)

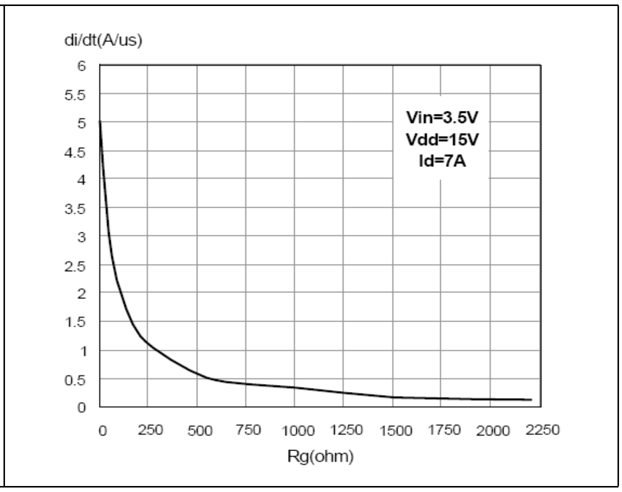


Figure 29. Input voltage vs input charge

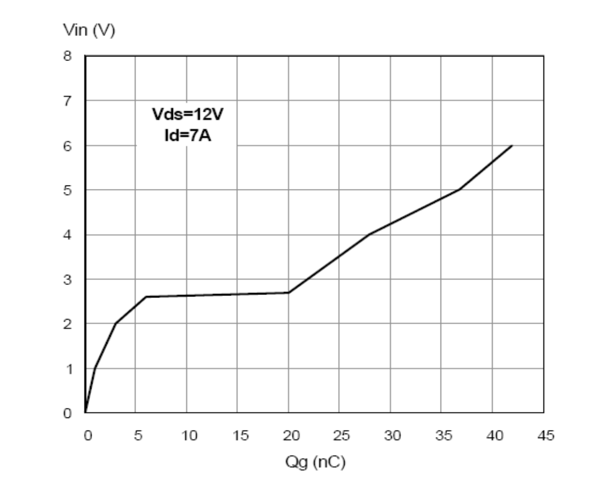


Figure 30. Capacitance variations

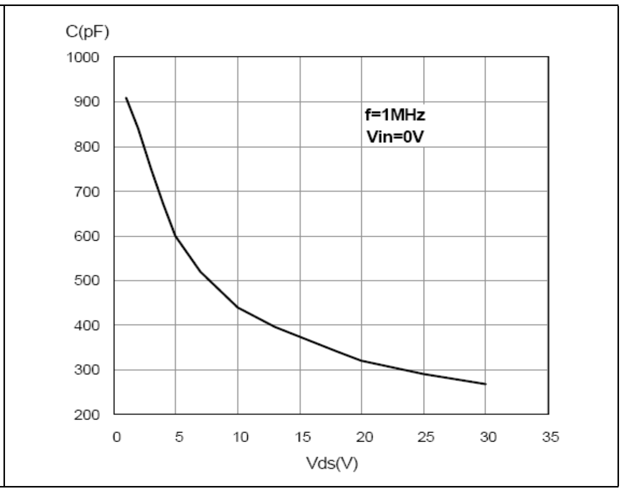


Figure 31. Switching time resistive load (V_{in}=5V)

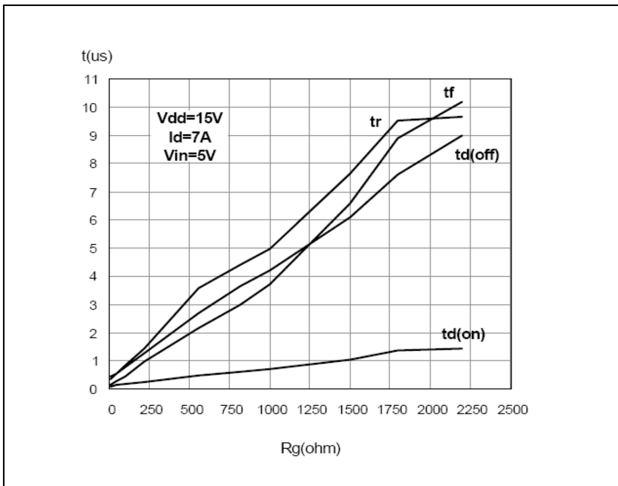


Figure 32. Switching time resistive load (R_g=10Ohm)

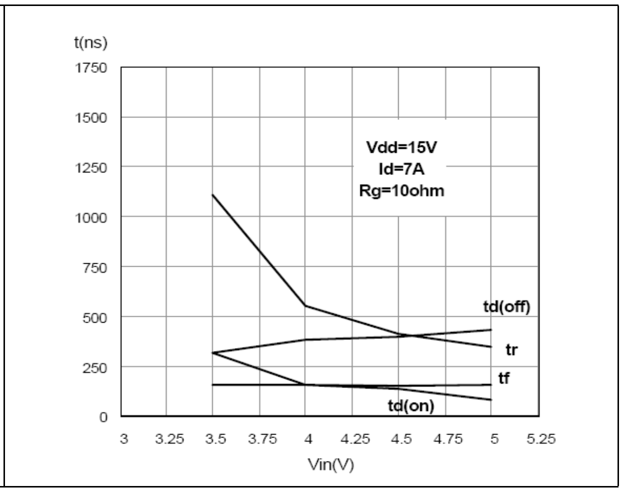


Figure 33. Output characteristics

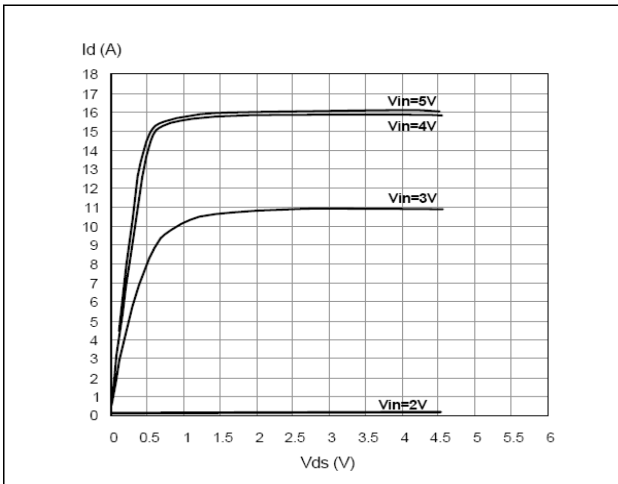


Figure 34. Step response current limit

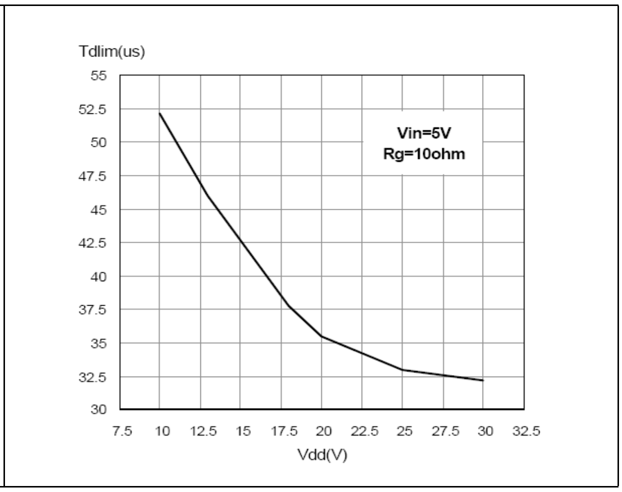


Figure 35. Source drain diode forward characteristics

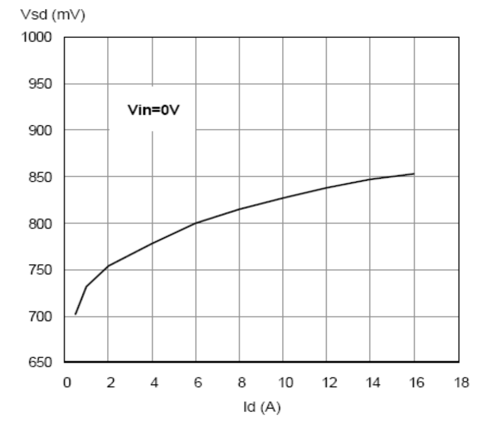


Figure 36. Static drian source on resistance vs I_d

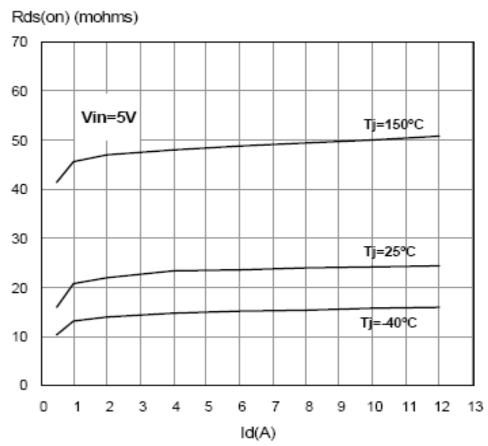


Figure 37. Static drain source on resistance vs input voltage (I_d=7A)

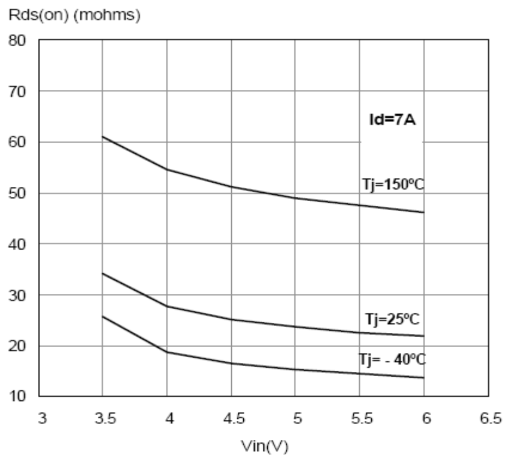


Figure 38. Static drain source on resistance vs input voltage

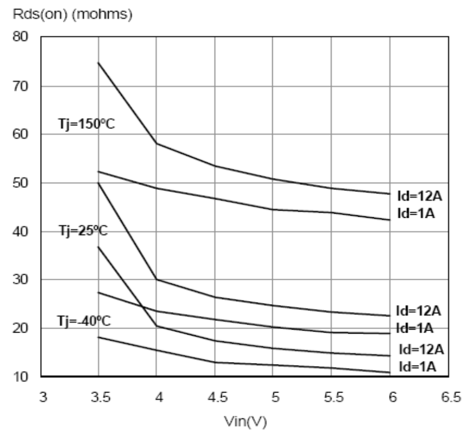


Figure 39. Normalized input threshold voltage vs temperature

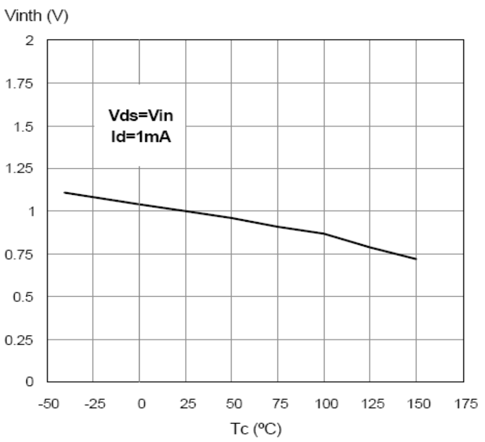


Figure 40. Normalized on resistance vs temperature

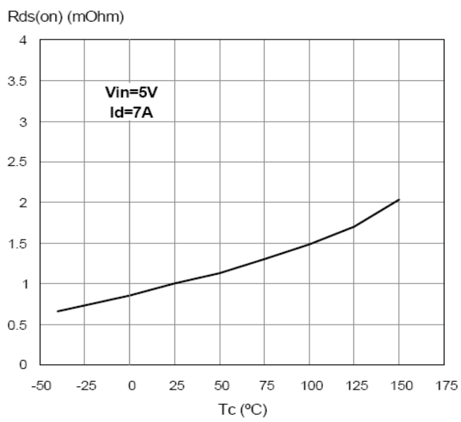


Figure 41. Turn-off drain source voltage slope (V_{in}=3.5V)

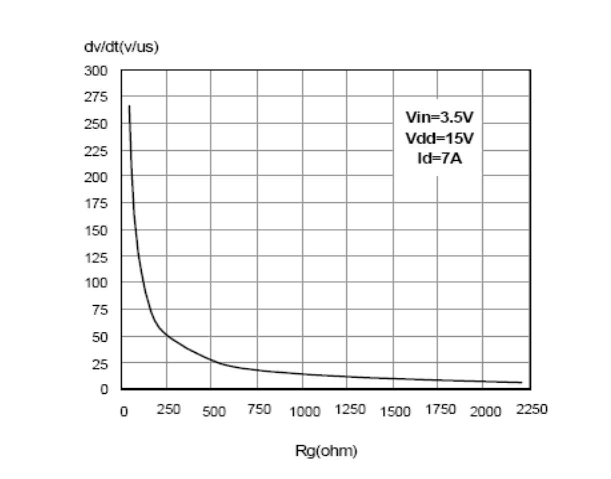


Figure 42. Turn-off drain source voltage slope (V_{in}=5V)

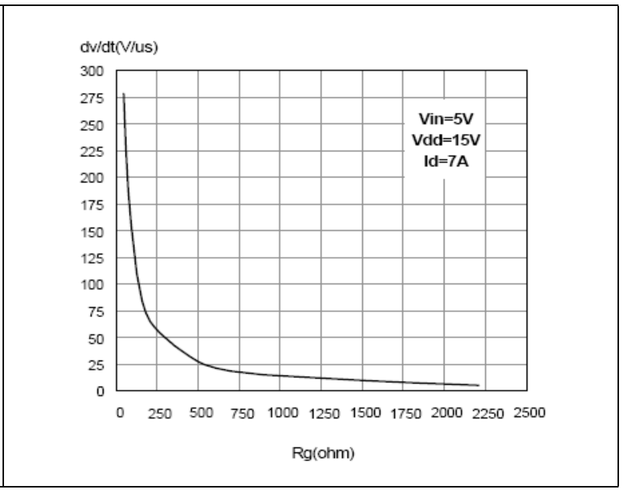
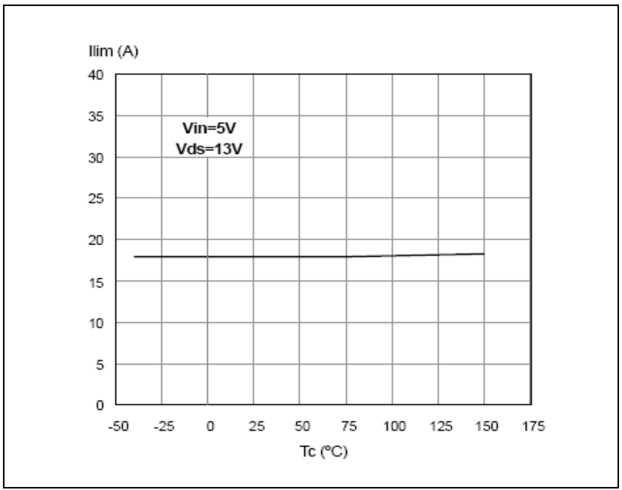
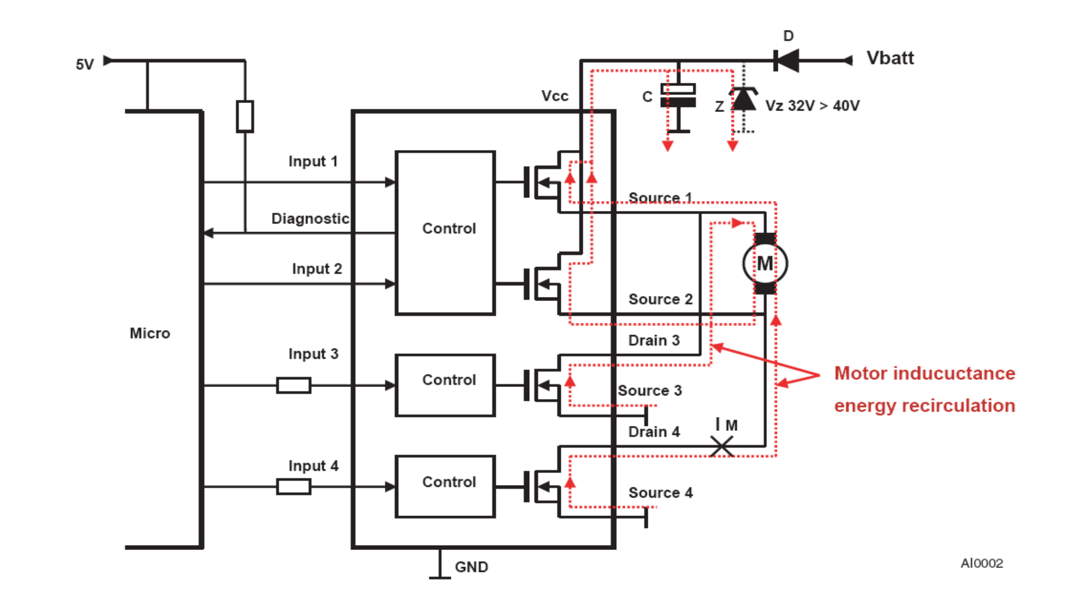


Figure 43. Current limit vs junction temperature



3 Application recommendations

Figure 44. Application diagram bridge drivers



Most motor bridge drivers use a reverse battery protection diode (D) inside the supply rail. This diode prevents a reverse current flow back to V_{BATT} in case the bridge becomes disabled via the logic inputs while motor inductance still carries energy. In order to prevent a hazardous overvoltage at circuit supply terminal (V_{CC}), a blocking capacitor (C) is needed to limit the voltage overshoot. As basic orientation, 50µF per 1A load current is recommended. As an alternative, a Zener protection (Z) is also suitable.

Even if a reverse polarity diode is not present, it is recommended to use a capacitor or Zener at V_{CC} because a similar problem appears in case the supply terminal of the module has intermittent electrical contact to the battery or gets disconnected while the motor is operating.

Figure 45. Recommended motor operation

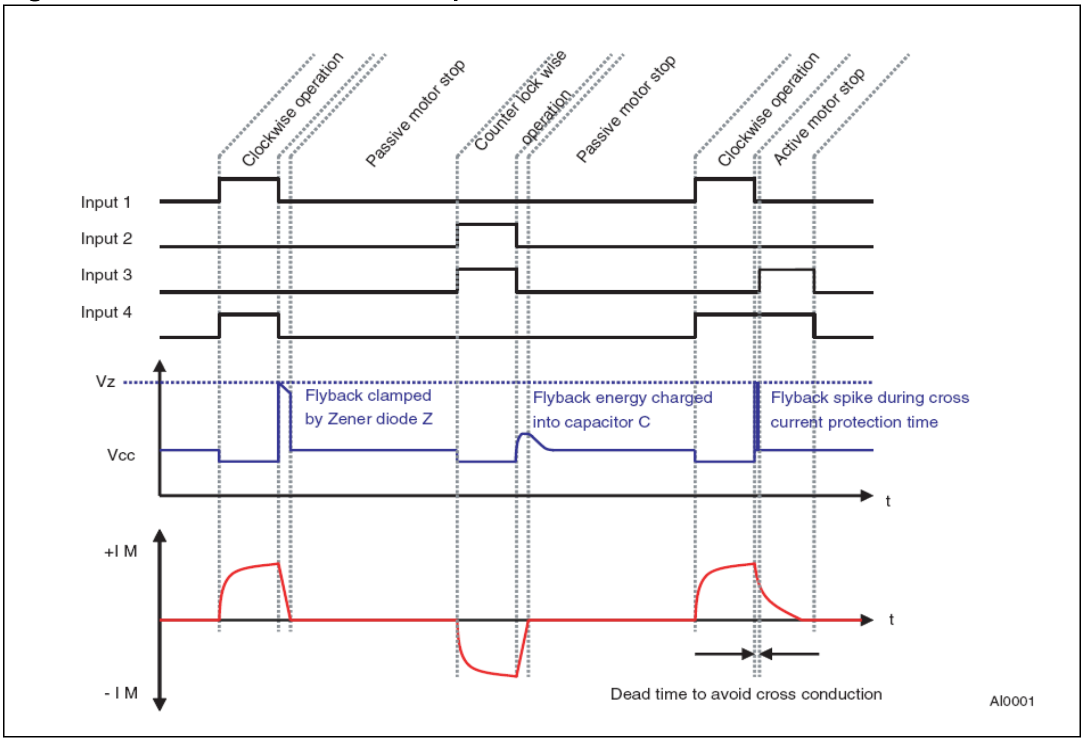
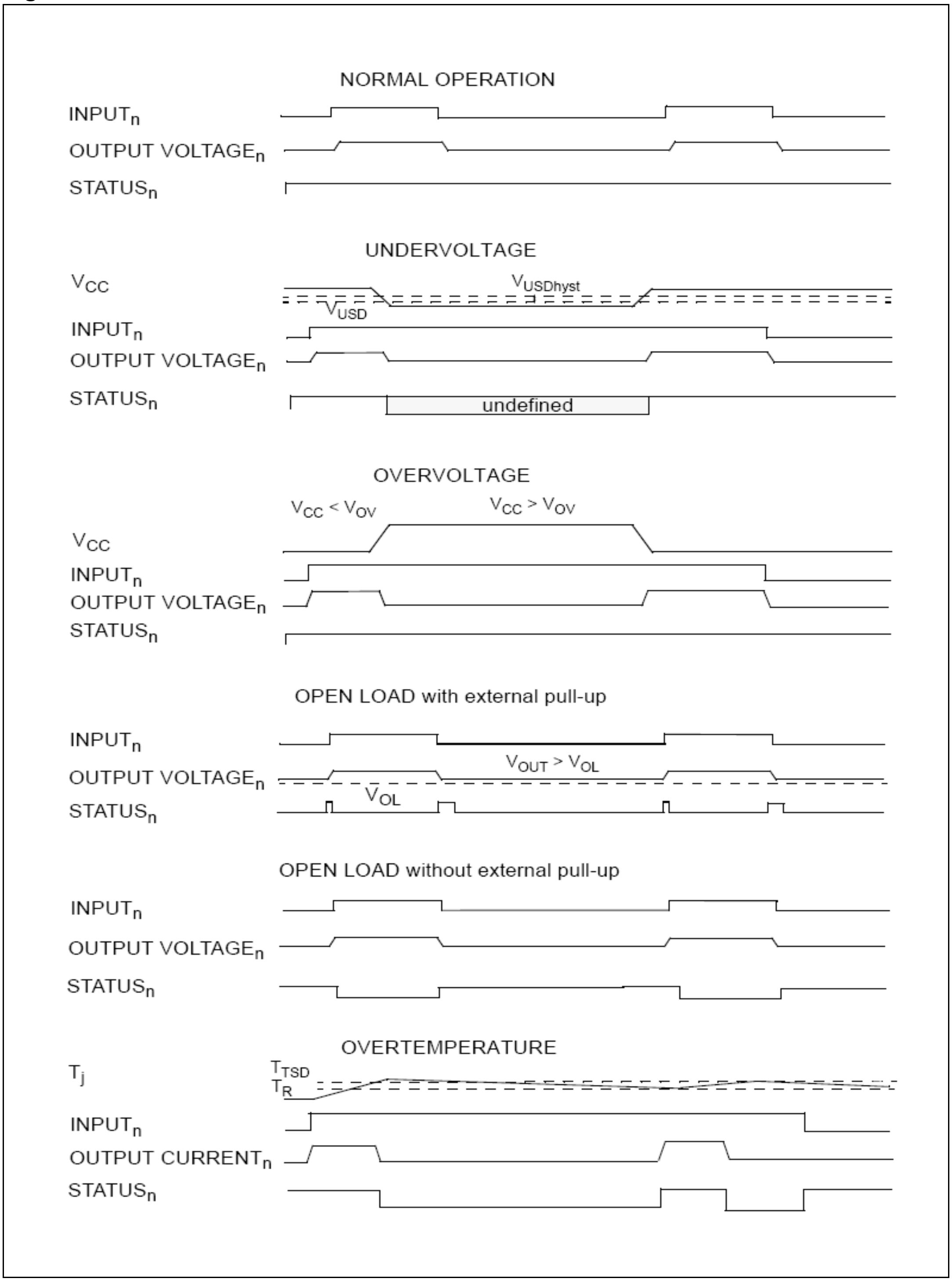


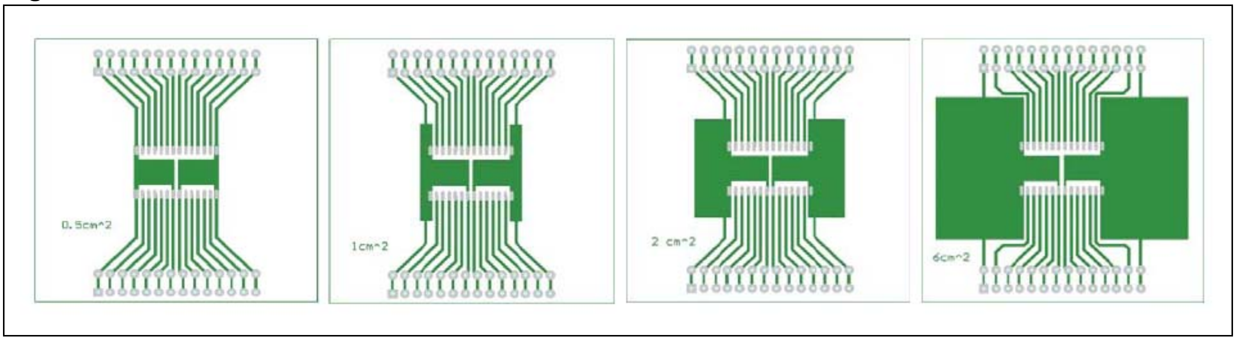
Figure 46. Waveforms



4 Thermal data

4.1 SO-28 thermal data

Figure 47. SO-28 PC board



Note: Layout condition of Rth and Zth measurements (PCB FR4 area = 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35µm, Copper areas: from minimum pad layout to 6cm^2).

Figure 48. Chipset configuration

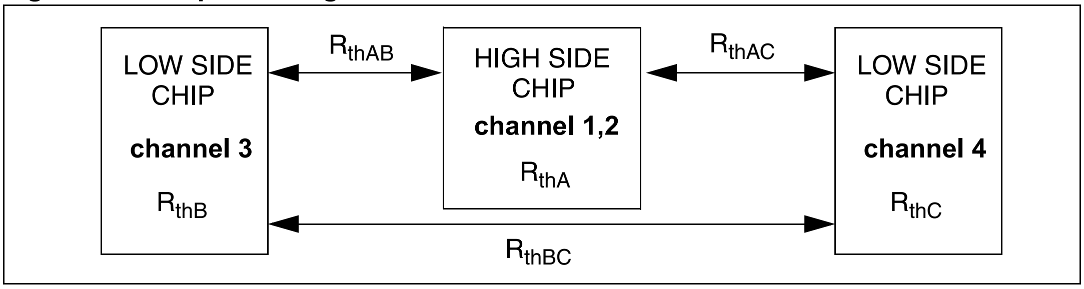
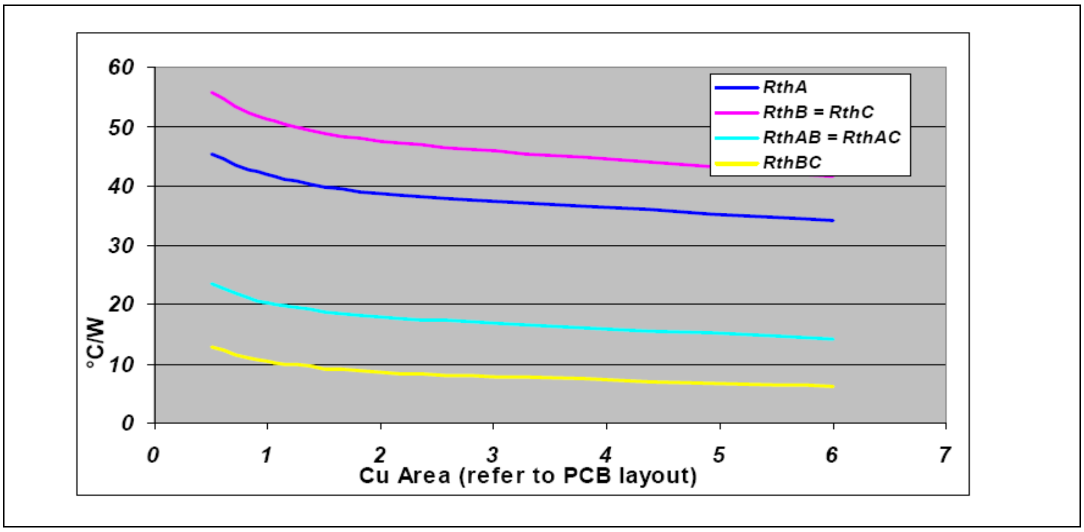


Figure 49. Auto and mutual Rthj-amb vs PCB copper area in open box free air condition[(a)]



a. see definitions in *Section 5.2 on page 31*

4.2 Thermal calculation in clockwise and anti-clockwise operation in steady state mode

Table 19. Thermal calculation in clockwise and anti-clockwise operation in steady state mode

HS_1	HS_2	LS_3	LS_4	T_{jHS12}	T_{jLS3}	T_{jLS4}
On	Off	Off	On	$P_{dHS1} \times R_{thHS} + P_{dLS4} \times R_{thHSLS} + T_{amb}$	$P_{dHS1} \times R_{thHSLS} + P_{dLS4} \times R_{thLSLS} + T_{amb}$	$P_{dHS1} \times R_{thHSLS} + P_{dLS4} \times R_{thLS} + T_{amb}$
Off	On	On	Off	$P_{dHS2} \times R_{thHS} + P_{dLS3} \times R_{thHSLS} + T_{amb}$	$P_{dHS2} \times R_{thHSLS} + P_{dLS3} \times R_{thLS} + T_{amb}$	$P_{dHS2} \times R_{thHSLS} + P_{dLS3} \times R_{thLSLS} + T_{amb}$

4.2.1 Thermal resistances definition

Values according to the PCB heatsink area.

$R_{thHS} = R_{thHS1} = R_{thHS2}$ = high side chip thermal resistance junction to ambient (HS_1 or HS_2 in on-state)

$R_{thLS} = R_{thLS3} = R_{thLS4}$ = low side chip thermal resistance junction to ambient

$R_{thHSLS} = R_{thHS1LS4} = R_{thHS2LS3}$ = mutual thermal resistance junction to ambient between high side and low side chips

$R_{thLSLS} = R_{thLS3LS4}$ = mutual thermal resistance junction to ambient between low side chips

4.2.2 Thermal calculation in transient mode[b]

$T_{jHS12} = Z_{thHS} \times P_{dHS12} + Z_{thHSLS} \times (P_{dLS3} + P_{dLS4}) + T_{amb}$

$T_{jLS3} = Z_{thHSLS} \times P_{dHS12} + Z_{thLS} \times P_{dLS3} + Z_{thLSLS} \times P_{dLS4} + T_{amb}$

$T_{jLS4} = Z_{thHSLS} \times P_{dHS12} + Z_{thLSLS} \times P_{dLS3} + Z_{thLS} \times P_{dLS4} + T_{amb}$

4.2.3 Single pulse thermal impedance definition

Values according to the PCB heatsink area.

Z_{thHS} = high side chip thermal impedance junction to ambient

$Z_{thLS} = Z_{thLS3} = Z_{thLS4}$ = low side chip thermal impedance junction to ambient

$Z_{thHSLS} = Z_{thHS12LS3} = Z_{thHS12LS4}$ = mutual thermal impedance junction to ambient between high side and low side chips

$Z_{thLSLS} = Z_{thLS3LS4}$ = mutual thermal impedance junction to ambient between low side chips

4.2.4 Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

b. Calculation is valid in any dynamic operating condition. Pd values set by user.

Figure 50. SO-28 HSD thermal impedance junction ambient single pulse

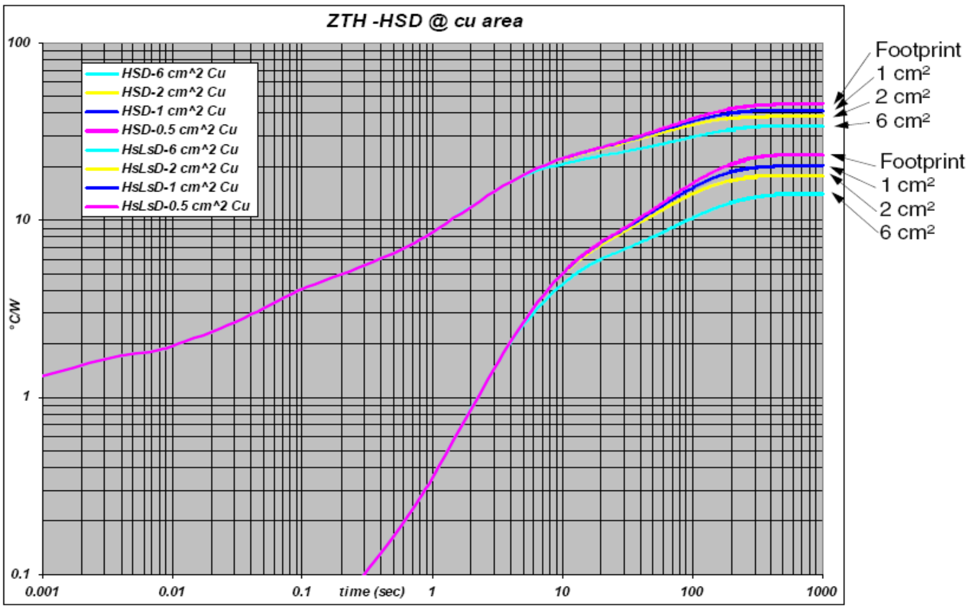


Figure 51. SO-28 LSD thermal impedance junction ambient single pulse

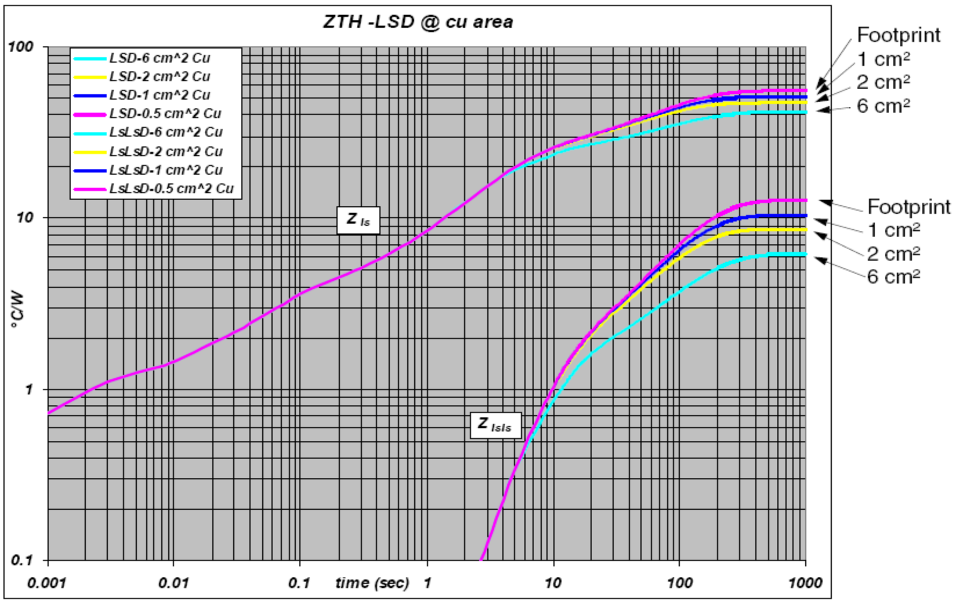


Figure 52. Thermal fitting model of an H-bridge in SO-28

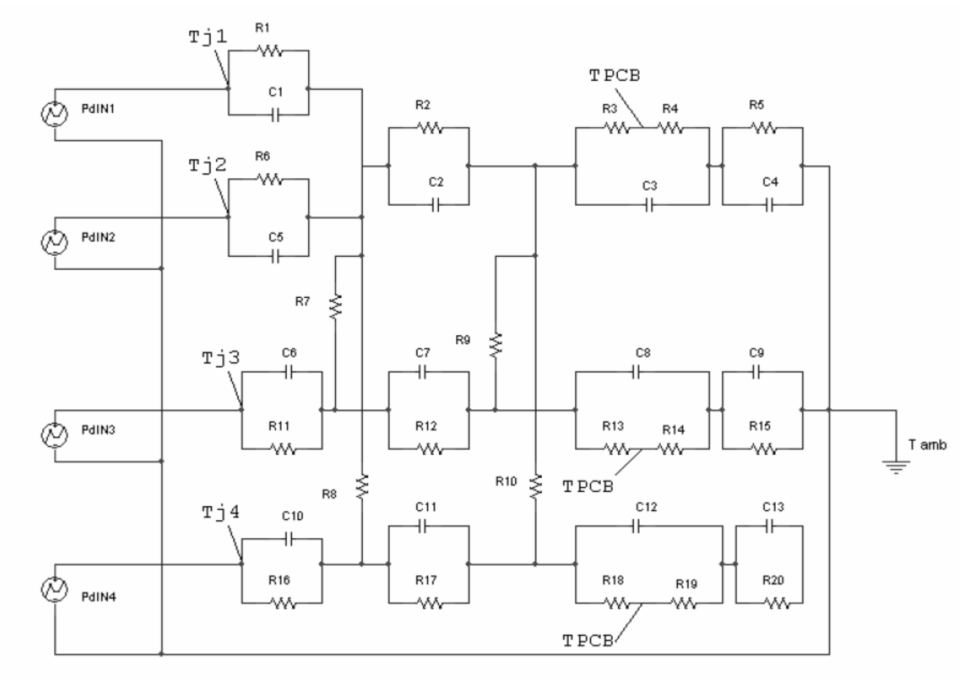


Table 20. Thermal parameters(1)

Area/island (cm2)	Footprint	1	2	6
R1 = R6 (°C/W)	1.5			
R2 (°C/W)	2.6			
R12 = R17 (°C/W)	2.6			
R3 = R13 = R 18 (°C/W)	15.5			
R4 = R14 = R19 (°C/W)	10.5			
R5 = R15 = R20 (°C/W)	62.28	52.28	44.28	32.28
R7 = R8 = R9 = R10 (°C/W)	150			
R11 = R16 (°C/W)	1			
C1 = C5 (W.s/°C)	0.00035			
C2 = C7 = C11 (W.s/°C)	0.024			
C3 = C8 =C 12 (W.s/°C)	0.2			
C4 = C9 = C13 (W.s/°C)	1.6	1.61	1.7	3.25
C6 = C10 (W.s/°C)	0.0009			

1. The blank space means that the value is the same as the previous one.

5 Package mechanical data

5.1 SO-28 mechanical data

Figure 53. SO-28 package outline

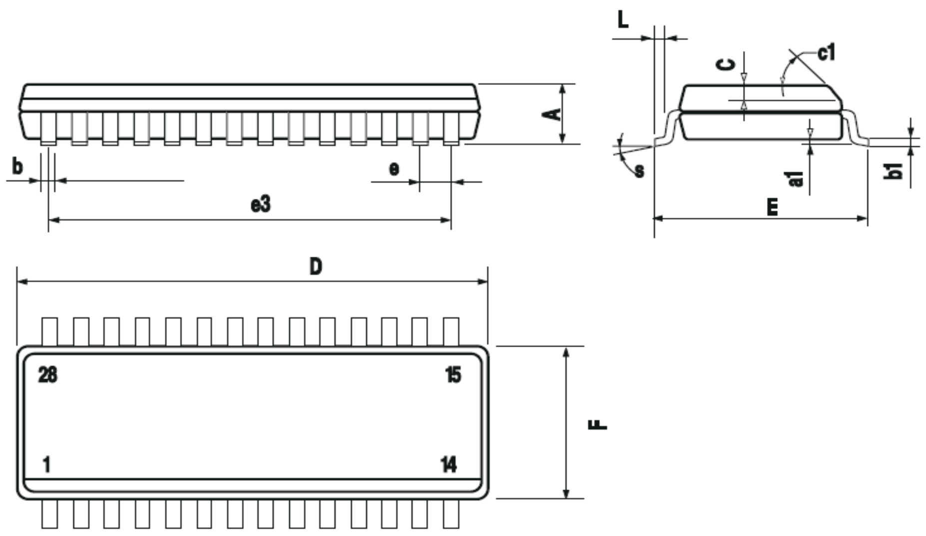
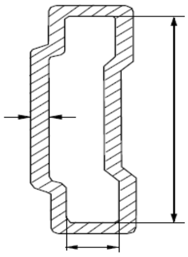


Table 21. SO-28 mechanical data

DIM	mm			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.393		0.419
e		1.27			0.050	
e3		16.51			0.650	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					

5.2 SO-28 tube shipment

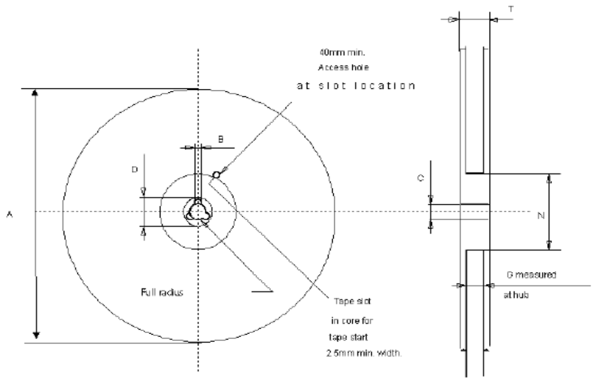
Figure 54. Tube dimensions (no suffix)



Dimension	mm
Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

5.3 Tape and reel shipment

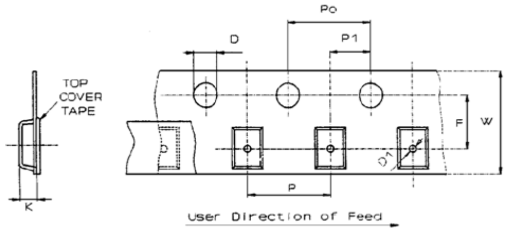
Figure 55. Tape and reel dimensions (suffix "13TR")



Reel dimensions

SO-28 tube shipment (no suffix)

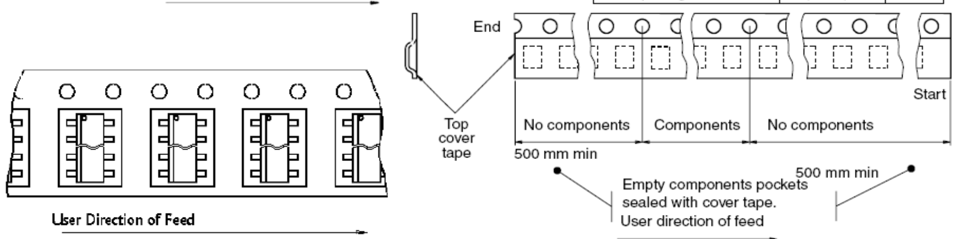
Dimension	mm
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
D (min)	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4



Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Description	Dimension	mm
Tape width	W (± 0.3)	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	16
Hole Diameter	D (+ 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2



6 Revision history

Table 22. Document revision history

Date	Revision	Changes
01-Sep-2004	1	Initial release.
31-Aug-2006	2	Document formatted into new ST template Dimensions updated, see *Figure 55: Tape and reel dimensions (suffix “13TR”) on page 31* Application diagram updated, see *Figure 44: Application diagram bridge drivers on page 23*
30-Jun-2009	3	Updated *Table 3: Thermal data*
10-Jul-2009	4	Updated note of *Figure 47: SO-28 PC board*. Updated *Figure 48: Chipset configuration*.