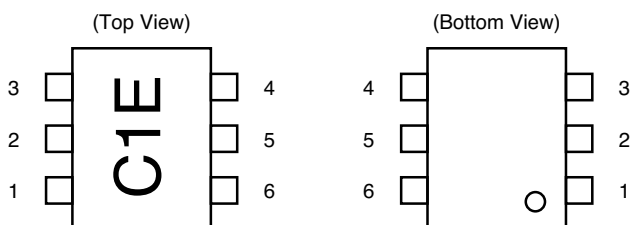


PIN CONNECTIONS

Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	OUTPUT
5	GND
6	V _{CC}

★ PRODUCT LINE-UP OF 5 V-BIAS SILICON MMIC MEDIUM OUTPUT POWER AMPLIFIER

(T_A = +25°C, V_{CC} = V_{out} = 5.0 V, Z_S = Z_L = 50 Ω)

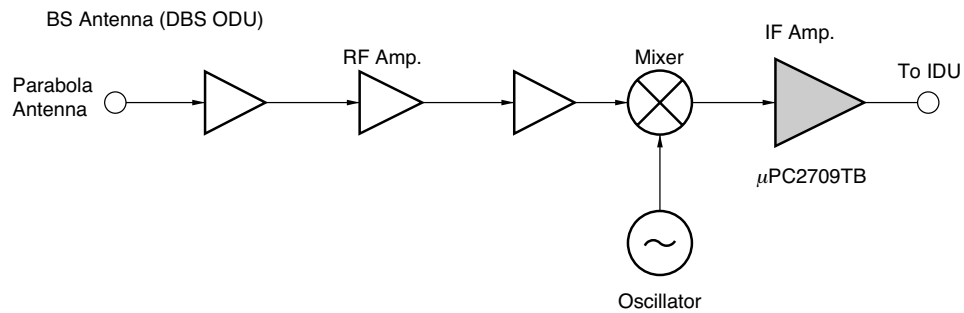
Part No.	f _u (GHz)	P _{O (sat)} (dBm)	G _P (dB)	NF (dB)	I _{cc} (mA)	Package	Marking
μ PC2708T	2.9	+10.0	15	6.5 @f = 1 GHz	26	6-pin minimold	C1D
μ PC2708TB						6-pin super minimold	
μ PC2709T	2.3	+11.5	23	5 @f = 1 GHz	25	6-pin minimold	C1E
μ PC2709TB						6-pin super minimold	
μ PC2710T	1.0	+13.5	33	3.5 @f = 0.5 GHz	22	6-pin minimold	C1F
μ PC2710TB						6-pin super minimold	
μ PC2776T	2.7	+8.5	23	6.0 @f = 1 GHz	25	6-pin minimold	C2L
μ PC2776TB						6-pin super minimold	

Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

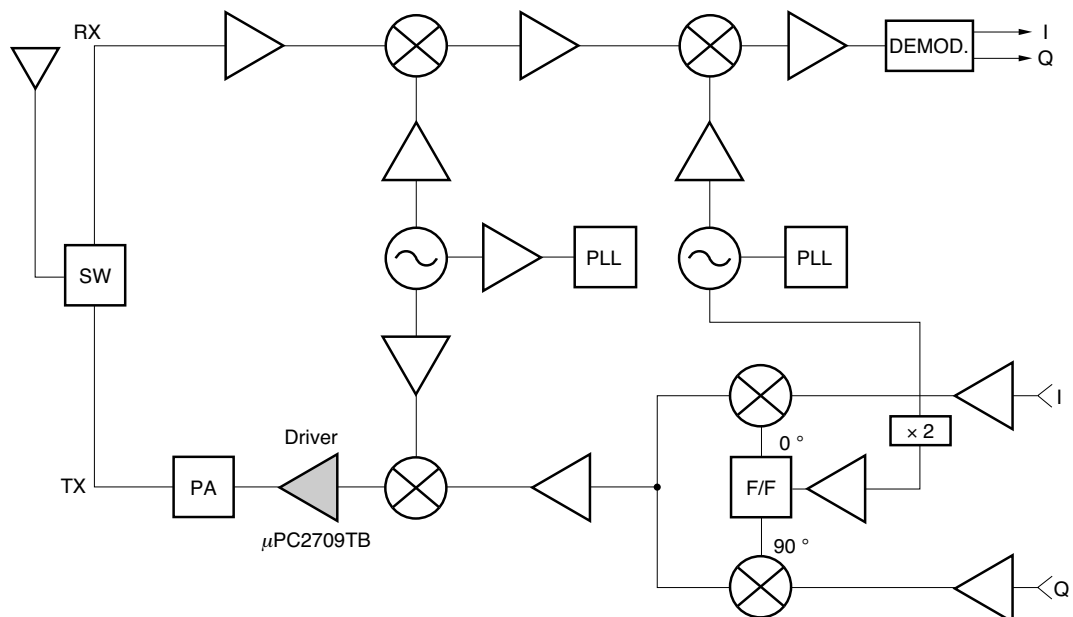
Caution The package size distinguishes between minimold and super minimold.

SYSTEM APPLICATION EXAMPLE

EXAMPLE OF DBS CONVERTERS



EXAMPLE OF 900 MHz BAND, 1.5 GHz BAND DIGITAL CELLULAR TELEPHONE



PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V) ^{Note}	Function and Applications	Internal Equivalent Circuit
1	INPUT	–	1.05	Signal input pin. A internal matching circuit, configured with resistors, enables 50 Ω connection over a wide band. A multi-feedback circuit is designed to cancel the deviations of h_{FE} and resistance. This pin must be coupled to signal source with capacitor for DC cut.	
4	OUTPUT	Voltage as same as V_{CC} through external inductor	–	Signal output pin. The inductor must be attached between V_{CC} and output pins to supply current to the internal output transistors.	
6	V_{CC}	4.5 to 5.5	–	Power supply pin, which biases the internal input transistor. This pin should be externally equipped with bypass capacitor to minimize its impedance.	
2 3 5	GND	0	–	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance defference.	

Note Pin voltage is measured at $V_{CC} = 5.0$ V

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{CC}	$T_A = +25^\circ\text{C}$, Pin 4 and 6	6	V
Total Circuit Current	I_{CC}	$T_A = +25^\circ\text{C}$	60	mA
Power Dissipation	P_D	Mounted on double copper clad $50 \times 50 \times 1.6$ mm epoxy glass PWB ($T_A = +85^\circ\text{C}$)	270	mW
Operating Ambient Temperature	T_A		-40 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^\circ\text{C}$
Input Power	P_{in}	$T_A = +25^\circ\text{C}$	+10	dBm

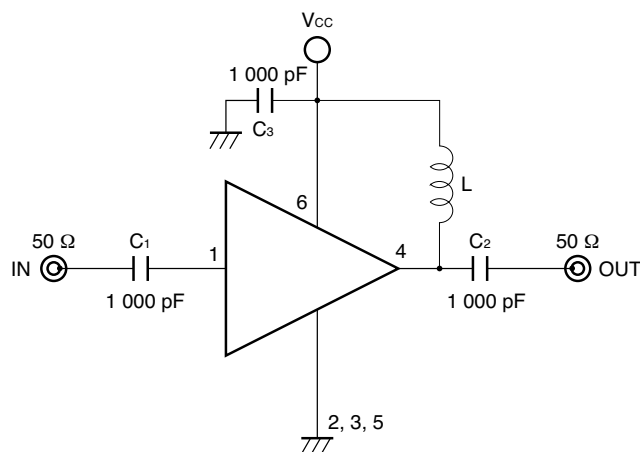
RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	The same voltage should be applied to pin 4 and 6.
Operating Ambient Temperature	T_A	-40	+25	+85	$^\circ\text{C}$	

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = V_{out} = 5.0$ V, $Z_s = Z_L = 50 \Omega$)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No input signal	19	25	32	mA
Power Gain	G_P	$f = 1$ GHz	21.0	23.0	26.5	dB
Saturated Output Power	$P_{O(sat)}$	$f = 1$ GHz, $P_{in} = 0$ dBm	+9.0	+11.5	–	dBm
Noise Figure	NF	$f = 1$ GHz	–	5.0	6.5	dB
Upper Limit Operating Frequency	f_u	3 dB down below flat gain at $f = 0.1$ GHz	2.0	2.3	–	GHz
Isolation	ISL	$f = 1$ GHz	26	31	–	dB
Input Return Loss	RL_{in}	$f = 1$ GHz	7	10	–	dB
Output Return Loss	RL_{out}	$f = 1$ GHz	7	10	–	dB
Gain Flatness	ΔG_P	$f = 0.1$ to 1.8 GHz	–	± 1.0	–	dB

TEST CIRCUIT



COMPONENTS OF TEST CIRCUIT FOR MEASURING ELECTRICAL CHARACTERISTICS EXAMPLE OF ACTUAL APPLICATION COMPONENTS

	Type	Value
C ₁ to C ₂	Bias Tee	1 000 pF
C ₃	Capacitor	1 000 pF
L	Bias Tee	1 000 nH

	Type	Value	Operating Frequency
C ₁ to C ₃	Chip capacitor	1 000 pF	100 MHz or higher
L	Chip inductor	300 nH	10 MHz or higher
		100 nH	100 MHz or higher
		10 nH	1.0 GHz or higher

INDUCTOR FOR THE OUTPUT PIN

The internal output transistor of this IC consumes 20 mA, to output medium power. To supply current for output transistor, connect an inductor between the V_{CC} pin (pin 6) and output pin (pin 4). Select large value inductance, as listed above.

The inductor has both DC and AC effects. In terms of DC, the inductor biases the output transistor with minimum voltage drop to output enable high level. In terms of AC, the inductor make output-port impedance higher to get enough gain. In this case, large inductance and Q is suitable.

CAPACITORS FOR THE V_{CC}, INPUT, AND OUTPUT PINS

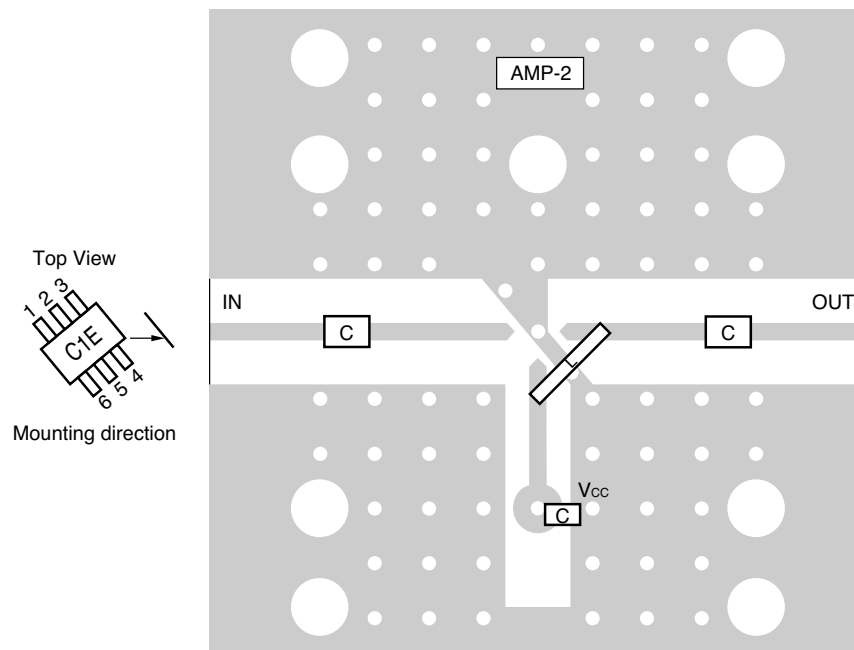
Capacitors of 1 000 pF are recommendable as the bypass capacitor for the V_{CC} pin and the coupling capacitors for the input and output pins.

The bypass capacitor connected to the V_{CC} pin is used to minimize ground impedance of V_{CC} pin. So, stable bias can be supplied against V_{CC} fluctuation.

The coupling capacitors, connected to the input and output pins, are used to cut the DC and minimize RF serial impedance. Their capacitance are therefore selected as lower impedance against a 50 Ω load. The capacitors thus perform as high pass filters, suppressing low frequencies to DC.

To obtain a flat gain from 100 MHz upwards, 1 000 pF capacitors are used in the test circuit. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 10 000 pF. Because the coupling capacitors are determined by equation, $C = 1/(2 \pi R f_c)$.

ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

	Value
C	1 000 pF
L	300 nH

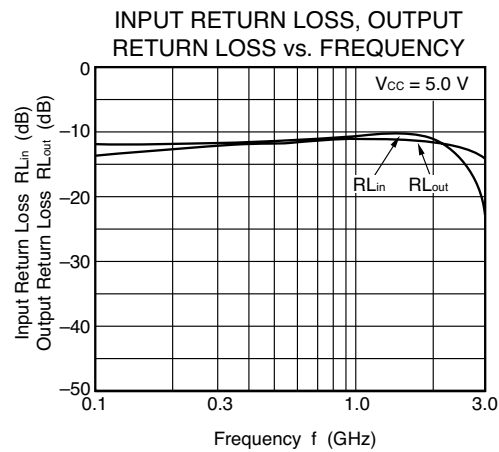
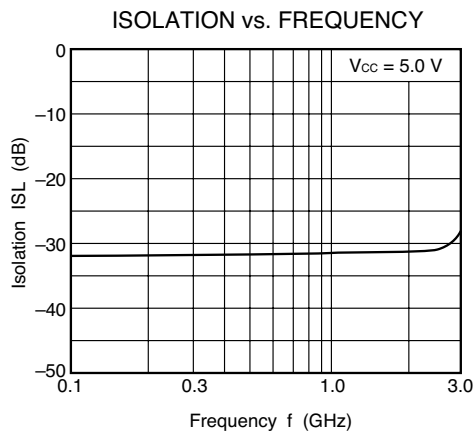
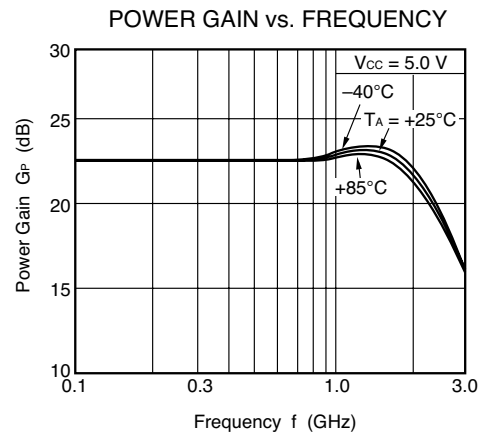
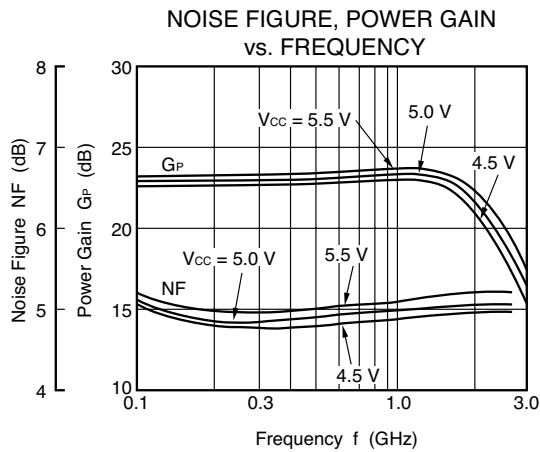
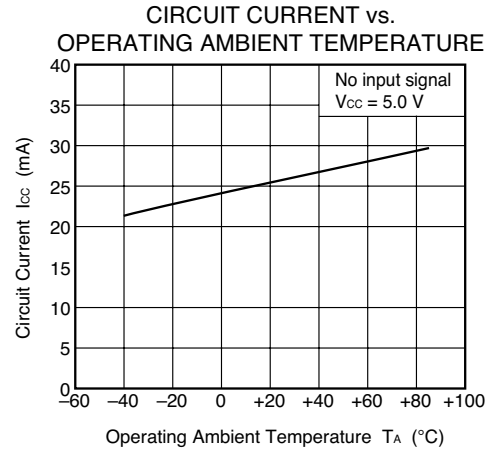
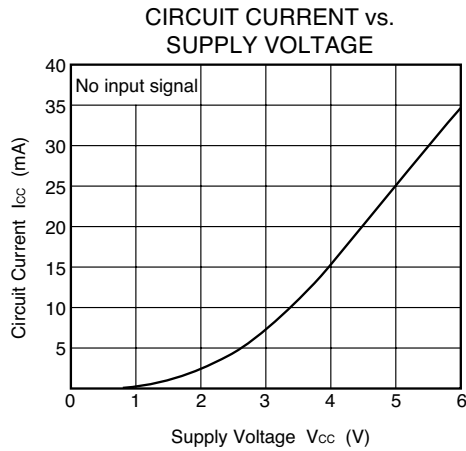
Notes

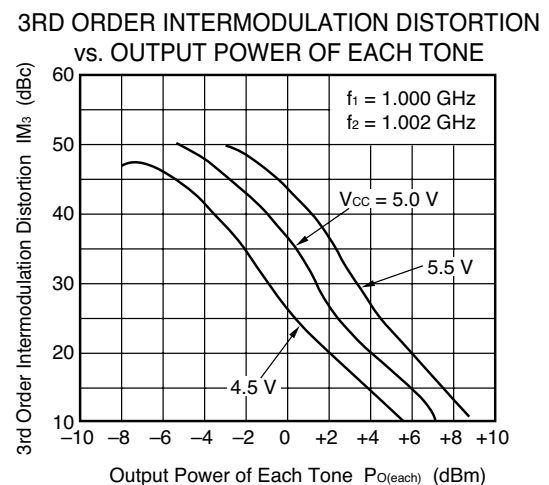
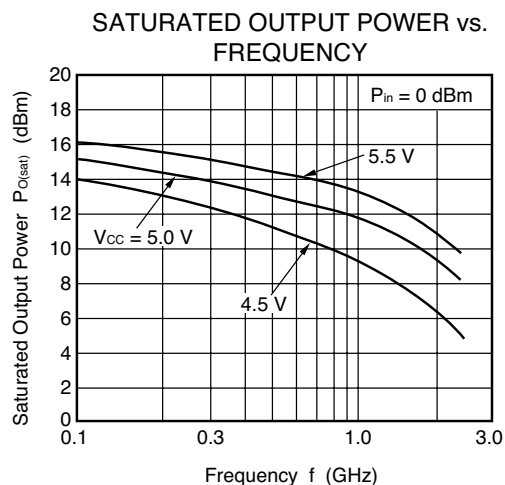
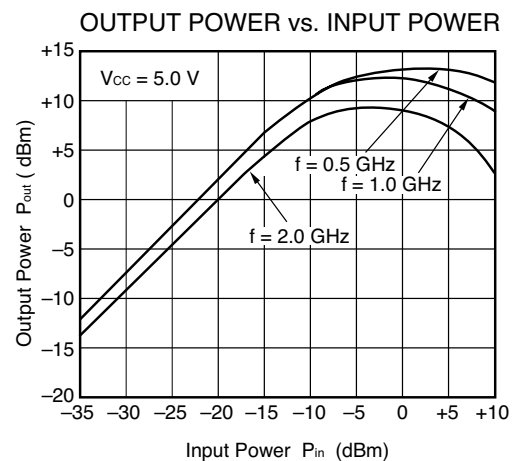
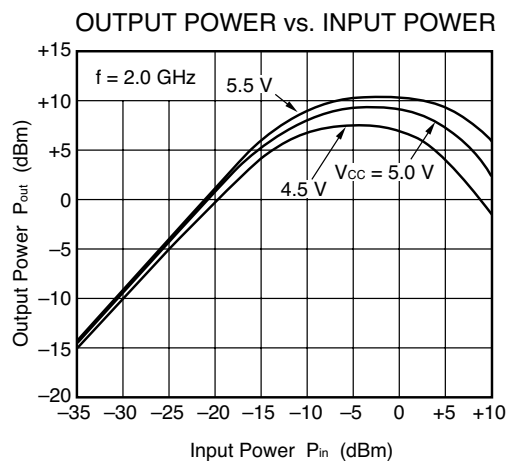
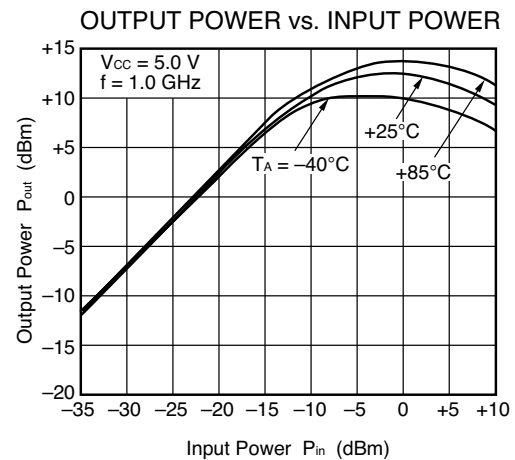
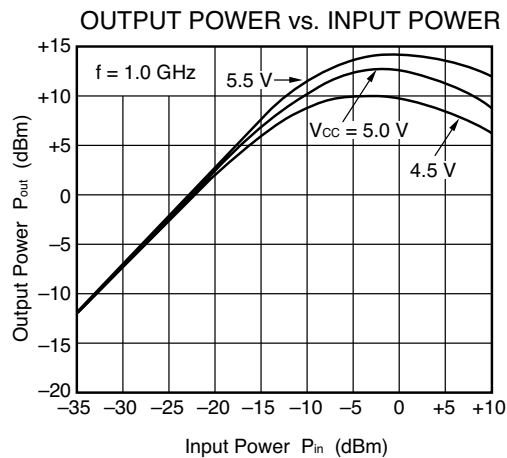
1. 30 × 30 × 0.4 mm double sided copper clad polyimide board.
2. Back side: GND pattern
3. Solder plated on pattern
4. ○ ○: Through holes

For more information on the use of this IC, refer to the following application note:

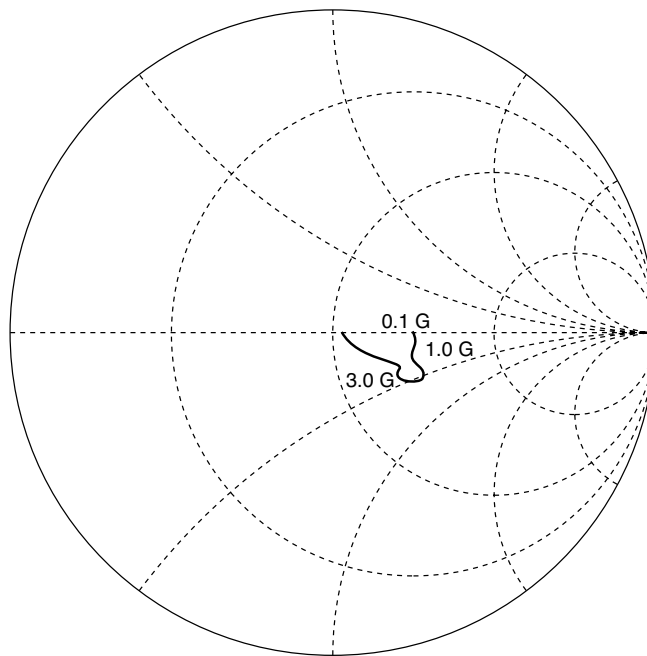
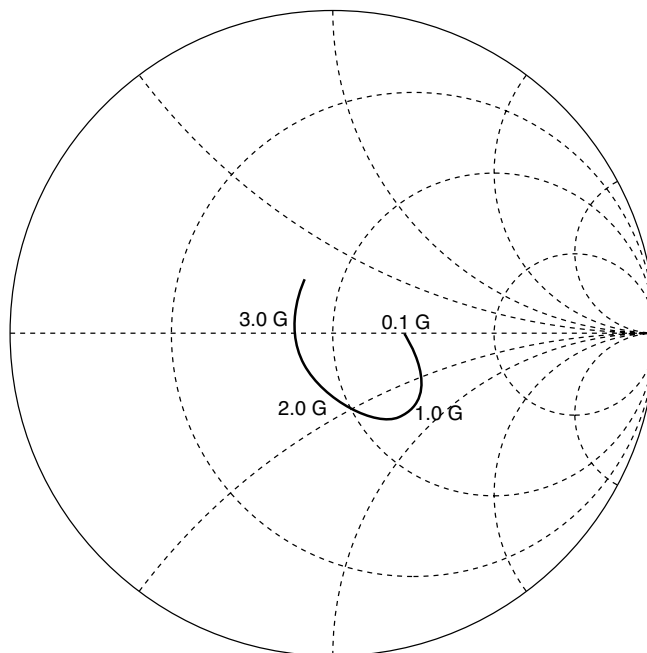
USAGE AND APPLICATION OF SILICON MEDIUM-POWER HIGH-FREQUENCY AMPLIFIER MMIC (P12152E).

TYPICAL CHARACTERISTICS (Unless otherwise specified, $T_A = +25^\circ\text{C}$)





Remark The graphs indicate nominal characteristics.

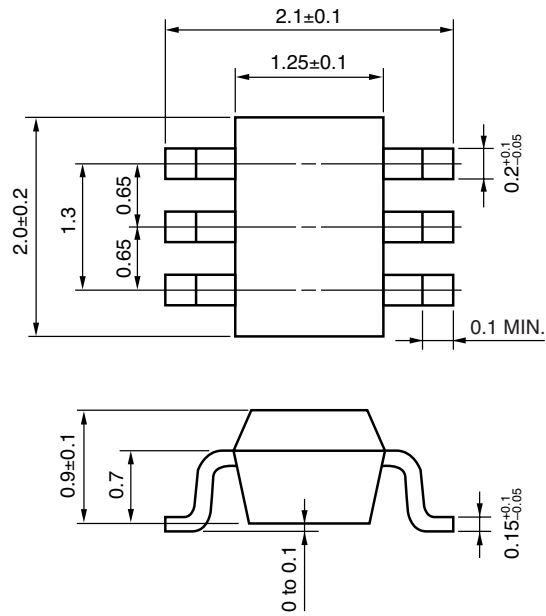
S-PARAMETERS ($T_A = +25^\circ\text{C}$, $V_{CC} = V_{out} = 5.0\text{ V}$)**S₁₁-FREQUENCY****S₂₂-FREQUENCY**

TYPICAL S-PARAMETER VALUES ($T_A = +25^\circ\text{C}$) $V_{CC} = V_{out} = 5.0\text{ V}$, $I_{CC} = 26\text{ mA}$

Frequency MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂		K
	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	
100.0000	0.227	0.2	13.698	-4.5	0.027	-1.0	0.196	0.9	1.37
200.0000	0.239	1.0	13.724	-9.6	0.027	3.1	0.207	2.2	1.36
300.0000	0.245	2.9	13.830	-14.5	0.026	4.7	0.212	4.1	1.38
400.0000	0.244	2.5	13.998	-19.9	0.027	7.8	0.223	3.4	1.32
500.0000	0.243	1.5	14.109	-25.0	0.026	9.8	0.234	2.1	1.33
600.0000	0.247	-1.5	14.246	-30.4	0.027	11.9	0.252	-0.4	1.26
700.0000	0.265	-3.2	14.538	-35.5	0.028	13.6	0.270	-2.3	1.20
800.0000	0.284	-3.6	14.703	-41.3	0.028	14.9	0.287	-4.6	1.15
900.0000	0.301	-3.3	15.051	-47.0	0.028	17.2	0.298	-7.4	1.10
1000.0000	0.305	-2.4	15.331	-53.5	0.029	18.8	0.309	-11.9	1.05
1100.0000	0.299	-3.2	15.605	-60.0	0.029	20.9	0.322	-17.1	1.04
1200.0000	0.300	-6.3	15.773	-66.7	0.029	22.5	0.336	-21.5	1.01
1300.0000	0.314	-10.3	16.152	-74.0	0.030	23.8	0.353	-24.8	0.95
1400.0000	0.328	-14.4	16.282	-81.0	0.030	26.1	0.353	-28.8	0.93
1500.0000	0.354	-17.3	16.337	-89.3	0.032	25.6	0.368	-35.5	0.86
1600.0000	0.359	-19.5	16.370	-96.5	0.031	26.8	0.370	-41.8	0.86
1700.0000	0.373	-22.1	16.256	-104.5	0.033	28.0	0.382	-46.9	0.81
1800.0000	0.371	-26.8	15.977	-112.7	0.032	29.3	0.381	-52.8	0.83
1900.0000	0.379	-31.1	15.529	-120.5	0.033	31.3	0.378	-57.8	0.83
2000.0000	0.386	-36.0	15.307	-128.1	0.034	31.0	0.373	-64.1	0.82
2100.0000	0.387	-39.5	14.745	-135.9	0.033	32.2	0.366	-70.8	0.85
2200.0000	0.374	-43.8	14.212	-143.7	0.033	30.5	0.363	-78.1	0.90
2300.0000	0.360	-48.7	13.633	-151.3	0.033	33.9	0.353	-83.0	0.94
2400.0000	0.339	-55.4	12.846	-158.7	0.032	35.5	0.331	-90.0	1.06
2500.0000	0.338	-62.0	11.990	-165.5	0.033	38.0	0.318	-95.6	1.11
2600.0000	0.334	-66.0	11.265	-172.1	0.033	39.1	0.304	-102.5	1.20
2700.0000	0.330	-69.0	10.560	-177.8	0.033	40.8	0.295	-108.3	1.25
2800.0000	0.311	-69.9	9.942	176.2	0.033	43.5	0.282	-113.7	1.36
2900.0000	0.291	-72.5	9.432	171.3	0.035	44.9	0.267	-118.6	1.40
3000.0000	0.258	-76.5	8.818	166.5	0.035	47.4	0.246	-125.1	1.55
3100.0000	0.240	-80.6	8.353	161.9	0.035	53.4	0.225	-131.2	1.64

★ PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)



NOTES ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).
All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
- (3) The bypass capacitor should be attached to the V_{cc} pin.
- (4) The inductor (L) must be attached between V_{cc} and output pins. The inductance value should be determined in accordance with desired frequency.
- (5) The DC cut capacitor must be attached to input and output pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None ^{Note}	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None ^{Note}	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None ^{Note}	WS60-00-1
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit: None ^{Note}	—

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

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